Design of High-Frequency GaN HEMT-Based DC–DC Converter

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***Abstract*—Switch-mode power converters commonly operate at switching frequencies from kilohertz to a few megahertz, traditionally relying on silicon-based transistors and control circuitry. However, parasitic limitations in silicon devices constrain further frequency scaling. This article presents a fully gallium nitride (GaN)-based dc–dc converter designed for high-frequency operation. The proposed architecture employs a GaN-based ring oscillator for on-chip pulsewidth modulation generation and includes all converter modules operating within the 8–43 MHz range. Experimental results validate the proposed design, demonstrating its feasibility and performance in high-frequency power conversion. The findings support the development of integrated GaN-based power conversion systems for advanced system-on-chip applications.**

***Index Terms*—Gallium nitride, power converter, pulsed width modulator, ring oscillator (RO).**

I. INTRODUCTION

POWER conversion plays a pivotal role in enabling sustainable energy solutions and ensuring the operational viability of modern electronic systems. Presently, the majority of electrical energy conversion systems are implemented using switch-mode power converters, which rely on externally applied periodic control signals to transfer energy from sources to loads via passive elements such as capacitors and inductors, as well as active semiconductor switches. Conventionally, these converters are built upon silicon-based transistors actuated by binary (ON/OFF) control schemes. Among the most widely adopted control techniques is pulsewidth modulation (PWM) [1], which regulates switching behavior to achieve desired output characteristics. Numerous methodologies for PWM control in dc–dc converter topologies have been extensively investigated and reported in the literature [2], [3], [4], [5], [6]. Designers typically realize these control strategies using PWM circuits composed of silicon transistors, bipolar junction transistors, comparators, and operational amplifiers.

In modern implementations, field-effect transistors (FETs) are prevalently used in control circuits. However, these devices inherently exhibit parasitic components, including gate resistance (r_G), input capacitance (C_{ISS}), channel resistance (R_{DS}), and output capacitance (C_{OSS}). These parasitics impose practical limits on the achievable switching frequency, thereby constraining the performance of silicon-based control circuitry. Even advanced silicon metal–oxide–semiconductor (MOS)-based PWM controllers encounter frequency limitations due to the latency and constraints associated with analog and digital feedback sensing circuits that determine the PWM signals.

To overcome these frequency limitations inherent in silicon, recent advancements in power electronics have focused on improving converter efficiency, power density, and reliability. Notably, GaN has emerged as a compelling wide-bandgap (WBG) semiconductor material for high-performance power electronic devices [7], [8], [9]. The full exploitation of GaN high electron mobility transistors (HEMTs) is facilitated by monolithic integration with peripheral circuits, including gate drivers, protection modules, and sensing/control interfaces [10], [11].

GaN possesses several favorable material properties—such as high electron mobility, wide bandgap, and superior thermal conductivity—that enable it to outperform traditional silicon devices in high-frequency applications. Specifically, GaN HEMTs exhibit significantly reduced input capacitance, on-state resistance, and output capacitance, allowing for operation at substantially higher switching frequencies. For instance, conventional silicon-based power transistors are typically limited to switching frequencies in the range of 1–3 MHz due to input capacitances exceeding 1000 pF and relatively slower transition dynamics. In contrast, GaN HEMTs offer subnanosecond switching transitions, with rise and fall times below 1 ns, thereby supporting reliable operation beyond 30 MHz [12]. As demonstrated in recent studies [13], [14], GaN devices achieve lower conduction losses and enable oscillator circuits operating in the 100 MHz to 1 GHz range, illustrating their distinct advantages in high-frequency power conversion. GaN-based circuits have been shown to attain gigahertz-level switching frequencies [15]. However, the transition to GaN technology introduces new engineering challenges. These include the need for specialized gate drivers, advanced ferrite materials, and digital processing systems—such as high-speed microcontrollers and digital signal processors—that can support the control and protection requirements of ultrahigh-frequency operation. Notably, traditional analog and digital PWM generation circuits based on silicon

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technology are insufficient to support such elevated switching frequencies, necessitating the development of novel control architectures compatible with GaN's performance envelope.

The implications of GaN's advantages extend to overall converter design. Modern power converters commonly operate within frequency ranges spanning tens of kilohertz to several megahertz. The adoption of GaN technology substantially enhances the performance of contemporary power converter designs by enabling higher efficiency and operation at frequencies extending into the tens of megahertz. This elevated switching frequency reduces the overall size of passive components, such as inductors and capacitors, thereby promoting compact converter architectures. Furthermore, the realization of GaN-based converters in monolithic form factors can significantly mitigate parasitic elements and electromagnetic ringing while simultaneously increasing switching speed and reducing energy losses.

GaN transistors are available in both depletion-mode (D-mode) and enhancement-mode (E-mode) variants. Among these, E-mode GaN devices have gained broader acceptance due to their operational similarity to conventional N-type silicon MOSFETs and their simplified gate drive requirements. As such, the design and analysis of converter topologies optimized exclusively for E-mode GaN transistors are imperative for advancing the integration of WBG technologies into power electronics.

To enable high-frequency operation in dc–dc converters, the availability of fast and controllable PWM signal sources is essential. A critical component in the generation of PWM signals is the ring oscillator (RO), which is widely employed in silicon-based integrated circuit designs for self-oscillating signal generation [17]. Several studies have proposed RO implementations utilizing GaN transistors [10], [18], [19], [20]. In [10], a GaN-based RO employs complementary logic inverters on a monolithic chip from both E-mode and D-mode GaN HEMTs, yielding an oscillation frequency of 1.087 MHz with a 5 V supply and nine inverter stages. The primary goal in [10] was to validate CMOS-style integration in GaN platforms, not to enable dynamic waveform control. Similarly, Zhang et al. [18] presented a p-GaN-based RO operating between 1.5 and 2 MHz, with a focus on a wide temperature range (25 °C–400 °C), but they offered no method for active duty cycle or frequency control. In [19], an RO utilizing 501 stages of direct-coupled GaN FET logic with 20 nm gate lengths achieved an oscillation frequency of 0.133 GHz at 2.5 V. However, the oscillation frequency was entirely fixed by device and layout characteristics. Until now, no mechanism has been proposed for dynamically modulating the duty cycle and frequency in an integrated solution. None of the previously proposed RO designs were integrated into or evaluated for switching power converter applications. Our proposed circuit incorporates the full converter on a chip and allows much higher frequency operation with both frequency and accurate duty cycle control.

Moreover, while these RO architectures exhibit promising oscillatory behavior, their applicability in high-speed dc–dc converter switching remains largely unverified. Current RO implementations leveraging D-mode GaN transistors have demonstrated only marginal performance improvements over their silicon counterparts in high-frequency contexts. To address this gap, the present work proposes the development of a GaN HEMT-based RO with explicit fully analog duty cycle and frequency control, tailored for PWM generation in dc–dc converters. This architecture is intended to overcome the switching frequency limitations of conventional silicon-based systems and facilitate the design of highly efficient, high-frequency power converters.

While ROs are essential, high-frequency operation mandates full monolithic integration of the power converter. Despite notable progress in GaN-based converter designs, monolithic integration of a complete GaN dc–dc converter operating in the megahertz range remains an open challenge. In [21], a GaN integration platform was introduced using normally-OFF AlGaN/GaN metal–insulator–semiconductor (MIS) HEMTs, demonstrating a buck converter operating at 10 kHz with a 15–30 V input range and integrated feedback and PWM modules. A subsequent study [22] presented a monolithic GaN voltage converter based on MIS HEMTs, incorporating control and drive circuitry with a PWM generator operating at 500 kHz and supporting duty cycles between 30% and 70%. Another implementation [23] demonstrated a GaN E-mode-based dc–dc buck converter with PWM control at 250 kHz, 48 V input, and peak load current of 5 A, achieving 84.3% efficiency.

These efforts underscore the potential of GaN technology for power conversion applications; however, significant advancements are still required to realize monolithic converters optimized for operation in the tens of megahertz. Accordingly, further investigation into the device physics of GaN transistors and their integration into circuit-level topologies is essential to fully exploit their advantages over silicon in high-frequency domains. A key aspect of this research is the feasibility analysis of RO-based PWM generation within a GaN-based converter architecture, which may serve as a foundational step toward monolithic "converter-on-chip" implementations.

Traditional approaches to PWM generation at high frequencies often rely on digital controllers. However, their integration into monolithic GaN-based power converters presents several technical challenges. Parasitic effects, along with electromagnetic interference (EMI), can deteriorate switching performance, exacerbate power losses, and constrain the achievable operating speed. Furthermore, intrinsic differences between silicon and GaN device structures complicate the seamless integration of digital control elements within GaN-based systems.

To mitigate these limitations, this study proposes an entirely analog approach that capitalizes on the intrinsic high-speed and low-parasitic advantages of GaN HEMTs. By eliminating the reliance on silicon-based digital components, the proposed methodology aims to reduce signal distortion and energy dissipation, thereby improving system efficiency and operational robustness. Specifically, a novel topology for a fully GaN-based power converter is introduced, targeting monolithic integration and operation at frequencies in the tens of megahertz. This includes the design of a PWM generator utilizing an RO constructed from E-mode GaN HEMTs, along with feedback control circuitry for regulating the output signal of the power converter.

Key design challenges such as dead time generation, signal synchronization, and thermal management are also addressed

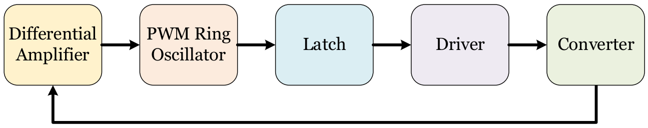


Fig. 1. Circuit block diagram.

within the proposed architecture. The converter topology will initially be realized on a printed circuit board (PCB) using discrete GaN components to evaluate its functionality and to validate its suitability for future monolithic integration. Experimental results will provide critical insights into the feasibility and performance advantages of GaN HEMTs in integrated high-frequency power conversion systems.

This work aims to provide a comprehensive and contemporary perspective on the development of fully GaN-based power converters. Both simulation and experimental results are presented to validate the proposed converter's performance and efficiency, representing a significant advancement toward realizing compact, high-frequency, and high-efficiency power systems. The proposed converter architecture comprises the following five principal subcircuits:

1) the power stage;
2) the gate driver circuitry for the power switches;
3) a dead time generation circuit;
4) a PWM signal generation circuit; and
5) a differential amplifier-based control circuit.

The exclusive use of GaN devices across all subcircuits underscores the feasibility of a monolithically integrated GaN power converter, eliminating the dependence on silicon-based components. This unified GaN implementation not only simplifies the integration process but also ensures material uniformity and compatibility throughout the chip, thereby enhancing reliability and manufacturability.

The remainder of this article is organized as follows: Section II details the circuit topology and provides analytical insights into its operation. Section III presents simulation and experimental results to validate the functionality and performance of the fabricated prototype. Section IV concludes this article and outlines directions for future research.

II. CIRCUIT TOPOLOGY AND ANALYSIS

The proposed fully GaN-based power converter architecture comprises five primary subcircuits: the power stage (of any selected topology), the gate driver for the power switches, a latch-based dead time generation circuit, the PWM generator, and a differential amplifier, as shown in Fig. 1. The differential amplifier continuously compares the regulated output signal (e.g., output voltage) against a reference value and delivers the resulting error signal to the RO-based PWM generator. This closed-loop feedback mechanism facilitates dynamic stability by enabling real-time adjustment of the duty cycle in response to fluctuations in both load and input voltage conditions.

The fully analog implementation inherently eliminates response latency and quantization noise often associated with digital controllers, thereby enhancing transient response and improving regulation under high-frequency operation. In contrast to digital control architectures, which may suffer from jitter and stringent timing constraints, the analog GaN-based configuration reduces parasitic-induced instabilities and supports reliable operation at elevated switching frequencies.

The PWM block interprets the error signal to synthesize an appropriate duty cycle (or switching frequency), which is subsequently processed by the latch circuitry to generate both the PWM and its complementary $\overline{\text{PWM}}$ signals. These signals incorporate an adjustable dead time interval to prevent shoot-through in the power stage. Finally, the gate driver circuit amplifies the control signals to appropriate levels for driving the power switch gates, ensuring efficient and robust switching within the chosen converter topology.

A. *Differential Amplifier*

The proposed fully GaN-integrated system includes the differential amplifier completely within the operational loop. This is crucial for minimizing parasitic elements inherent in otherwise hybrid designs. This approach ensures seamless compatibility for monolithic integration and fully exploits GaN's superior properties to deliver the rapid stability required at megahertz switching frequencies.

The differential amplifier serves as the core feedback control element within the proposed converter architecture, regulating the PWM signal in accordance with the error signal derived from the output voltage and its reference. In power converters operating at switching frequencies in the tens of megahertz, the amplifier must exhibit both a high bandwidth and a high slew rate to ensure accurate, fast-responding control. Conventional silicon-based operational amplifiers are widely available; however, their performance typically degrades at high frequencies due to inherent material limitations and parasitic effects. In contrast, GaN offers superior electron mobility and lower intrinsic parasitics, making it a suitable candidate for high-frequency analog circuit implementations. Recent research has demonstrated the viability of GaN for realizing fundamental analog building blocks, including comparators [21], [24], differential amplifiers [25], [26], reference voltage generators [27], and current sensors [26], [28]. Notably, the differential amplifier presented in [25] employs MIS-HEMT technology to achieve high gain and an extended unity-gain bandwidth. Building upon this foundation, a fully GaN-based differential amplifier was developed, as shown in Fig. 2. This design enhances noise rejection and stability of the PWM signal, which is critical for ensuring robust switching in high-frequency converter operation.

The amplifier generates a pair of complementary outputs that vary symmetrically in response to the differential input voltage. One output transitions high while the other remains low, facilitating differential PWM signal control. The operation of the amplifier can be quantitatively analyzed as follows. The current mirror is formed using transistor Q_9 with transistor Q_{10} configured by shorting its gate and drain to maintain a fixed current mirror reference. A variable resistor R_D modulates the current mirror behavior by altering the gate voltage of Q_{10},

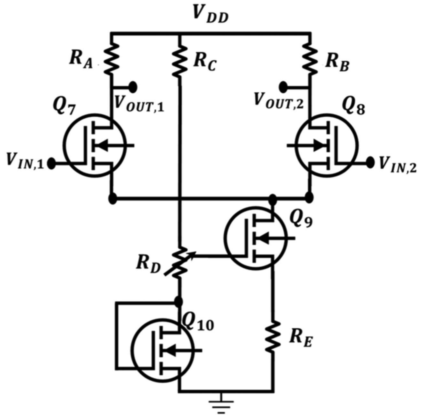


Fig. 2. Differential amplifier circuit.

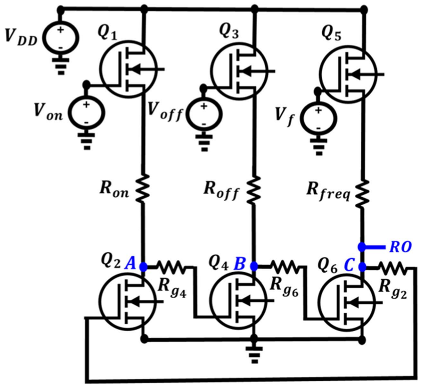


Fig. 3. GaN-based RO circuit.

described by

$$V_{G(Q_{10})} = V_{\mathrm{TH}} + (V_{\mathrm{DD}} - V_{\mathrm{TH}}) \cdot k \cdot R_D / (R_D + R_C) \tag{1}$$

where $k \cdot R_D$ denotes the adjustable component of the variable resistor R_D, and V_{TH} is the threshold voltage of the transistor. The source current through Q_9 is given by

$$I_{S(Q_9)} = I_{D(Q_8)} + I_{D(Q_7)}. \tag{2}$$

The output voltages of the amplifier are defined as

$$V_{\mathrm{OUT},1} = V_{\mathrm{DD}} - I_{D(Q_7)} \cdot R_A \tag{3}$$

$$V_{\mathrm{OUT},2} = V_{\mathrm{DD}} - I_{D(Q_8)} \cdot R_B. \tag{4}$$

Assuming a symmetrical design where $R_A = R_B = R_M$, the differential output voltage becomes

$$\Delta\, V_{\mathrm{OUT}} = V_{\mathrm{OUT},1} - V_{\mathrm{OUT},2} = R_M \; \left(I_{D(Q_8)} - I_{D(Q_7)}\right). \tag{5}$$

This differential output is subsequently used to modulate the PWM signal, enabling real-time adjustment to maintain output voltage regulation under dynamic load and input conditions. Specifically, the differential output voltage drives the gate control nodes of the PWM generator (denoted as V_{ON} and V_{OFF}, corresponding to transistors Q_1 and Q_3, respectively, as shown in Fig. 3). This architecture provides the basis for high-frequency analog regulation, with the RO acting as a voltage-controlled duty cycle modulator.

The circuit reaches equilibrium when the input voltages to the differential amplifier are equal, resulting in a balanced output. At startup, with both differential inputs at 0 V, transistors Q_7 and Q_8 remain in the cutoff region, and consequently, the output nodes settle at the supply voltage V_{DD}. As the input voltage increases beyond a threshold determined by the sum of gate-source voltages, the output begins to decrease. Specifically, the output voltage transitions occur once the input exceeds the threshold voltage determined by: $V_{\mathrm{IN}} > V_{\mathrm{GS}(Q_7)} + V_{\mathrm{GS}(Q_9)} - V_{\mathrm{TH}}$. At this point, Q_7 and Q_8 transition from the cutoff region into the saturation region. As the input voltage further increases, these transistors shift into the ohmic region once the input surpasses the condition: $V_{\mathrm{IN}} > V_{\mathrm{DD}} - I_{S(Q_9)} \cdot R_M/2 + V_{\mathrm{TH}}$. Accordingly, the valid common-mode voltage range for proper amplifier operation can be expressed as

$$\begin{aligned} V_{\mathrm{GS}(Q_7)} + V_{\mathrm{GS}(Q_9)} - V_{\mathrm{TH}} < V_{\mathrm{IN}} < \min \{ (V_{\mathrm{DD}} - I_{S(Q_9)} \\ \cdot\ R_M/2 + V_{\mathrm{TH}}), (V_{\mathrm{DD}}) \}. \end{aligned} \tag{6}$$

To facilitate measurement of the current flowing through the current mirror, a resistor R_E is inserted into the mirror branch. The voltage drop across this resistor provides a direct means of calculating the mirror current, which can be obtained by dividing the measured voltage by the resistance value of R_E. This enables real-time current monitoring and validation of current mirror performance under varying load and biasing conditions.

B. PWM Ring Oscillator

ROs are self-sustaining oscillatory circuits that initiate oscillations when a sufficient voltage is applied across an odd-numbered chain of logic inverters. The regenerative instability inherent to this configuration leads to periodic signal generation. For the proposed megahertz, fully GaN-based dc–dc converter, the implementation of the PWM generator with a GaN-based RO is essential to fully exploit the high-speed switching capabilities of GaN devices in a dynamically controllable manner. Recent research has introduced innovative topologies for GaN-based PWM generators leveraging RO circuits to exploit the high-speed switching capabilities of GaN devices [20], [29], [30]. The oscillation frequency and duty cycle of the PWM output are primarily determined by the supply voltage, as well as the intrinsic resistance and capacitance of each inverter stage.

Fig. 3 shows the proposed GaN-based RO circuit. Due to the unipolar nature of GaN technology, where only N-type devices are commercially available, the design deviates from conventional silicon-based implementations. Specifically, the typical RO configuration integrates D-mode transistors for the pull-up network and E-mode transistors for the pull-down network. In this circuit, the upper transistors Q_1, Q_3, and Q_5 are driven by an external gate voltage, whereas the lower transistors Q_2, Q_4, and Q_6 are sequentially driven by the output of the preceding inverter stage.

To analyze the RO operation, we initially assume that the upper transistors are always conducting. The oscillation begins as the drain voltage of Q_2 increases, initiating the charging of the gate capacitance of Q_4 through the *RC* network formed by the ON-state resistance R_{ON}, gate resistor R_{G4}, and the input

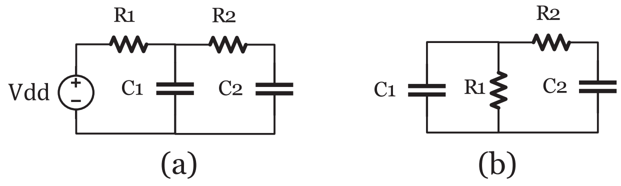


Fig. 4. Timing circuit (a) charge and (b) discharge.

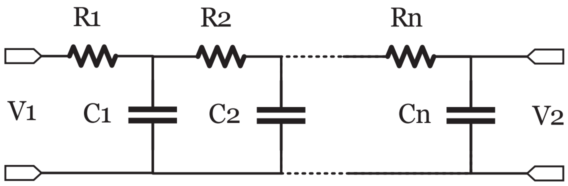


Fig. 5. *RC* ladder.

capacitance C_{IN} of Q_4. When the gate voltage $V_{G,4}$ exceeds the threshold voltage V_T, Q_4 begins to conduct, pulling down the gate voltage of Q_6. During this discharge phase, the gate of Q_6 discharges through the path comprising C_{IN}, R_{G6}, the internal gate resistance r_{Gate} and the channel resistance R_{DS} of Q_4. The discharge path is faster than the charge path due to the relatively low resistance of the conducting transistor and series gate resistor, enabling rapid state transitions.

Subsequently, the drain voltage of Q_6 rises, causing the gate voltage of Q_2 to increase. Once V_{G2} crosses the threshold, Q_2 conducts, pulling down its drain voltage and ceasing conduction in Q_4. The oscillation process continues as dictated by the *RC* time constants during both charge and discharge phases.

Fig. 4(a) and (b) shows the equivalent *RC* models for the charge and discharge cycles, respectively. In Fig. 4(a), R_1 represents the resistor connected to the drain of the transistor and C_1 corresponds to the transistor's output capacitance C_{OSS}. C_2 and R_2 represent the input capacitance C_{ISS} and gate resistance r_G of the following stage. In Fig. 4(b), the discharge path is modeled with R_1 representing the conducting transistor's channel resistance R_{DS}, and C_1 representing its output capacitance C_{OSS}. C_2 and R_2 retain the same interpretation as in the charge phase.

The gate voltage of Q_6 in the RO circuit can be described by a second-order linear differential equation, as given in the following equation:

$$\ddot{V}_{C_{\text{GS}}} + \frac{\text{R}_1 (C_2 + \text{C}_1) + \text{R}_2 C_2}{\text{R}_1 C_2 \text{R}_2 \text{C}_1} \dot{V}_{C_{\text{GS}}} + \frac{1}{\text{R}_1 C_2 \text{R}_2 \text{C}_1} V_{C_{\text{GS}}} = \frac{1}{\text{R}_1 C_2 \text{R}_2 \text{C}_1} V_{S.} \quad (7)$$

The derived expression reveals that the system exhibits an exponential damping ratio ξ >1, indicating an overdamped response, as formulated in the following equation:

$$\xi_{\text{charge}} = (\text{R}_1 (C_2 + \text{C}_1) + \text{R}_2 C_2) / 2\sqrt{\text{R}_1 \cdot C_2 \cdot \text{R}_2 \cdot \text{C}_1}. \quad (8)$$

The solution to the differential equation in (7) for the gate-source voltage $V_{C_{\text{GS},C}}(t)$ is expressed in (9). It demonstrates the overdamped system's behavior as the superposition of two decaying exponentials as follows:

$$V_{C_{\text{GS},C}}(t) \cong V + C_1 e^{-\xi\omega_0 \left(1 - \sqrt{1 - \frac{1}{\xi^2}}\right) t} + C_2 e^{-\xi\omega_0 \left(1 - \sqrt{1 - 1/\xi^2}\right) t}. \quad (9)$$

The timing circuits associated with the charging and discharging phases are shown in Fig. 4(a) and (b), respectively. Due to the complexity of solving (9) analytically, numerical methods are employed. However, to simplify the estimation of the delay introduced by the *RC* ladder network, the Elmore delay (ED) model offers an efficient approximation [31]. ED is defined as the first moment of the impulse response and represents the center of mass of the signal in the time domain as follows:

$$\text{ED} \equiv \int_0^{\infty} t \cdot V(t)\, d. \quad (10)$$

For the charging delay of an *RC* ladder network, such as the one shown in Fig. 5 [32], the ED can be computed by the summation of products of resistances and downstream capacitances as follows:

$$\text{ED} = R_1 \ (C_1 + .. + C_n) + R_2 (C_2 + .. + C_n) + .. + R_n C_n. \quad (11)$$

This expression allows for efficient estimation of propagation delays in complex *RC* structures and serves as a practical tool for high-frequency circuit analysis, particularly in GaN-based timing circuits. Applying the ED model to the charging circuit, the charging time can be approximated as

$$\tau_C \cong R_1 (C_1 + C_2) + R_2 C_2. \quad (12)$$

Assuming a first-order *RC* charging behavior, the gate voltage during the charging phase follows:

$$V_{C_{\text{GS},C}} \ (t) = V(\infty) \left(1 - e^{-(t/\tau_C)}\right). \quad (13)$$

The discharge path is shown in Fig. 4(b). Here, the gate of transistor Q_6 and the output capacitance of Q_4 discharge through the gate resistance R_G, the internal gate resistance r_{Gate} and the channel resistance R_{DS} of Q_4. As the resistances and capacitances associated with this path are significantly smaller, the discharge is modeled as a first-order system with a time constant given as

$$\tau_D \cong C_2 (r + R_2). \quad (14)$$

Accordingly, the gate voltage during discharging is given by

$$V_{C_{\text{GS},C}} \ (t) = V_{\text{GS,MAX}} \cdot e^{-t/\tau_{d.}} \quad (15)$$

The operation of the RO, as shown in Fig. 4, is governed by sequential charging and discharging of gate voltages through a chain of transistors. Each leg undergoes a gate voltage rise to the threshold V_{TH} during charging, followed by a fall to V_{TH} during discharging. The operational sequence begins with the drain terminal of Q_2 ceasing conduction, initiating gate charging of Q_4 Once the gate voltage of Q_4 reaches V_{TH}, it conducts and triggers the discharge of the gate of Q_6. When Q_6 gate voltage drops to V_{TH}, it ceases conduction, and Q_2's gate begins charging, repeating the cycle. This process completes one full oscillation period.

The timing for each charging phase is computed as

$$t_C = -\tau_C \cdot \ln\left(1 - V_{\mathrm{TH}}/V(\infty)\right) \tag{16}$$

and for the discharging phase

$$t_D = -\tau_D \cdot \ln\left(V_{\mathrm{TH}}/V(\infty)\right). \tag{17}$$

Considering the component relationships $R_1 \gg R_2$ and $C_1 < C_2$, the charging time significantly exceeds the discharging time. The ratio of the time constants is given by

$$\tau_C/\,\tau_D = \left(R_1\left(C_1 + C_2\right) + R_2C_2\right)/\left(C_2\left(r + R_2\right)\right). \tag{18}$$

In the RO circuit of Fig. 3, each full cycle includes three charging and three discharging intervals of the gate voltage transitioning to and from V_{TH}. Given the topology, the maximum gate voltage swing reaches approximately $2 \cdot \mathrm{V_{TH}}$, and therefore

$$V_{\mathrm{TH}} \leq V_{\mathrm{GS,MAX}}(\infty) \leq 2 \cdot \mathrm{V_{TH}}. \tag{19}$$

Substituting this bound into (17), the upper limit of the discharge time becomes

$$t_D \leq -\tau_D \cdot \ln\left(V_{\mathrm{TH}}/2 \cdot \mathrm{V_{TH}}\right). \tag{20}$$

Combining (16), (18), and (20), the oscillation frequency f_{RO} of the RO can be derived. While this analysis uses first-order approximations via the ED model and simple *RC* behavior, it neglects certain parasitic effects. Nevertheless, the model provides an effective estimation method for the timing behavior and frequency of GaN-based ROs.

$$f_{\mathrm{SW}} = \left(t_{C,A} + t_{C,B} + t_{C,C} + t_{D,A} + t_{D,B} + t_{D,C}\right)^{-1}. \tag{21}$$

Analysis of (21) reveals the upper-frequency boundary for a given RO hardware configuration. The upper transistors Q_1, Q_3, and Q_5 govern the charging paths by selectively enabling or interrupting the supply current. In conjunction, the middle resistors and the external gate voltage sources establish additional constraints on RO operation. These upper transistors remain conductive under appropriate gate bias conditions.

If the drain voltage of Q_6, i.e., $V_{D,6}$, is considered the output PWM signal, then the circuit elements R_{ON}, R_{OFF}, and R_{freq} determine the on-time t_{ON}, off-time R_{OFF}, and switching frequency f_{SW}, respectively. The analysis demonstrates that dynamically controlling the gate voltages of the upper transistors provides the ability to simultaneously tune all PWM parameters (t_{ON}, t_{OFF}, and the total period T).

To ensure the proper charging behavior, the new supply voltage to the *RC* network must satisfy

$$V_{\mathrm{GS}} + V_{R2} + V_{R1} \leq V_{G,N} - V_{\mathrm{TH}}. \tag{22}$$

Consequently, the maximum gate-source voltage during charging is bounded as

$$V_{\mathrm{TH}} \leq V_{\mathrm{GS,MAX}} \leq \min\left\{\left(2 \cdot V_{\mathrm{TH}}\right), \left(V_{G,N} - V_{\mathrm{TH}}\right)\right\}. \tag{23}$$

The gate voltage at the end of the charge–discharge sequence in leg *N* denoted by $V_{\mathrm{GS},N,MAX}$ is determined by

$$V_{\mathrm{GS},N,\mathrm{MAX}} = \left(V_{G,N} - V_{\mathrm{TH}}\right)\left(1 - e^{-\frac{t_{C,N} + t_{D,N+1} + t_{C,N+2}}{\tau_{C,N}}}\right). \tag{24}$$

The PWM control mechanism is realized by adjusting the gate voltages V_{ON}, V_{OFF}, and V_{ON} as well as the associated resistances R_{ON}, R_{OFF}, and R_{freq} as shown in Fig. 3. Specifically

1) V_{ON} (applied to the gate of Q_1): Initiates the charging phase, thereby controlling the output on-time.
2) V_{OFF} (applied to the gate of Q_2): Triggers the discharging phase, setting the off-time.
3) V_{freq} (applied to the gate of Q_3): Modulates the overall switching frequency by affecting both charging and discharging dynamics.

The drain of Q_6 (leg C) serves as the PWM output. The middle resistor in leg A (R_{ON}) and the upper gate voltage $V_{G,A}$ significantly influence the on-time. A decrease in R_{ON} accelerates the charging of the gate in leg B, prompting a faster discharge in leg C. This extended low-state in leg C results in an increased on-time at the output. Similarly, increasing $V_{G,A}$ raises the final gate voltage [per (13)], further accelerating the charging process and prolonging the on-time. Conversely, lowering $V_{G,A}$ reduces the on-time.

Leg B modulates the off-time. Reducing R_{off} expedites the gate charging in leg C, thus extending its conduction duration and increasing the off-time. Lowering $V_{G,B}$ similarly lengthens the off-time, while increasing it shortens the off-time. Leg C primarily determines the switching frequency and indirectly influences the on-time. A decrease in R_{freq} leads to a higher switching frequency and increased on-time. Likewise, raising $V_{G,C}$ increases both the frequency and on-time, whereas a reduction in $V_{G,C}$ has the opposite effect. This design strategy enables precise control over the PWM waveform by tuning both analog voltages and resistances, offering a compact and flexible method for frequency and duty cycle regulation in GaN-based RO circuits. The modulation of the PWM duty cycle is particularly effective at high switching frequencies due to the intrinsic fast response and low parasitic characteristics of GaN HEMTs. The analog adjustment of gate voltages and resistances directly controls the charge and discharge time constants, facilitating continuous and accurate duty cycle and frequency adjustment even in the tens of megahertz range.

C. Latch Circuit

PWM signals incorporating dead time between transitions are essential for the high-side (HS) and low-side (LS) transistors in gate driver circuits. The inclusion of dead time is critical to prevent shoot-through conditions, which arise when both HS and LS transistors conduct simultaneously, resulting in a short circuit across the power supply terminals. The proper implementation of dead time significantly enhances the reliability and efficiency of switching operations. In recent years, the generation of dead time in gate driver architectures has attracted considerable attention from researchers [33], [34], [35], [36], [37]. Two straightforward techniques are commonly employed to introduce dead

TABLE I
COMPARATIVE ANALYSIS OF LATCH NOR AND LATCH NAND

Feature	**Latch NOR**	**Latch NAND**
Speed	Low	High
Dead Time Generation	Easy	Complex
Static Power Consumption	High	High
Dynamic Power Consumption	Low	Moderate
Noise Immunity	Low	High
Design Complexity	Low	High

time between complementary PWM signals. The first technique utilizes a latch-based circuit comprising NOR gates. The second technique employs a similar latch configuration using NAND gates.

The implementation of dead time using GaN-based latch circuits introduces unique design challenges, primarily due to the unavailability of complementary GaN devices analogous to P-channel MOSFETs (p-MOS). This limitation precludes the use of standard CMOS technology and necessitates alternative design strategies. Specifically, the pull-up operation in the latch circuit is achieved using resistive elements, whereas pull-down functionality is provided by E-mode GaN transistors. As a result, GaN-based latch implementations may exhibit increased static and dynamic power consumption, reduced noise margins, and more complex layout constraints compared to their CMOS counterparts.

A comparative evaluation of latch circuit types is required to identify the most suitable architecture for generating dead time. Table I presents a detailed comparison between NOR and NAND latch configurations. Implementing dead time with the NAND-based latch is more complex due to the inherent characteristics of NAND gate logic, which necessitates additional circuitry to ensure nonoverlapping output transitions. From a speed perspective, the NOR latch is typically slower, attributable to the larger transistor dimensions used in NOR gates, which increase input capacitance. Furthermore, the *RC* time constant formed by the pull-up resistor and parasitic capacitance further delays signal transitions. However, the NOR latch exhibits lower dynamic power consumption, as it experiences less frequent switching activity. NAND gates, in contrast, offer superior noise immunity and faster switching speeds due to their low-resistance paths and compact design. Despite these advantages, the NOR latch was selected in this work owing to its robustness in enforcing critical dead time in gate drive applications. To enhance control precision, the value of the pull-up resistor in the NOR configuration must be appropriately selected to match the desired timing characteristics. Lastly, an inverting stage is required at the output of the NOR latch to produce the correct logic levels for subsequent stages.

Fig. 6 shows the proposed technique for generating dead time between complementary PWM signals. Initially, two PWM inputs are processed through NOT gates to obtain their respective inverted signals. These inverted signals are then applied to the inputs of a NOR-based latch circuit. The dead time intervals are governed by the pull-up resistors, denoted as $R_{\text{PULL}-\text{UP}(n)}$, which control the timing of the latch transitions. The outputs of the NOR latch are subsequently fed into two logic inverters to produce the final PWM outputs. Specifically, the dead time between the original PWM signal and its complement $\overline{\text{PWM}}$ is determined by $R_{\text{PULL}-\text{UP}(2)}$, whereas the dead time between $\overline{\text{PWM}}$ and PWM is controlled by $R_{\text{PULL}-\text{UP}(1)}$.

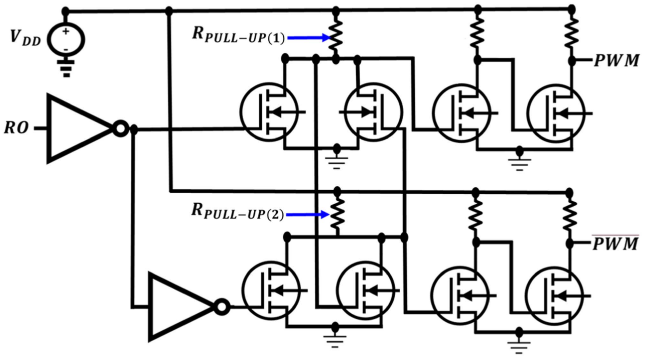


Fig. 6. Topology for the latch NOR design.

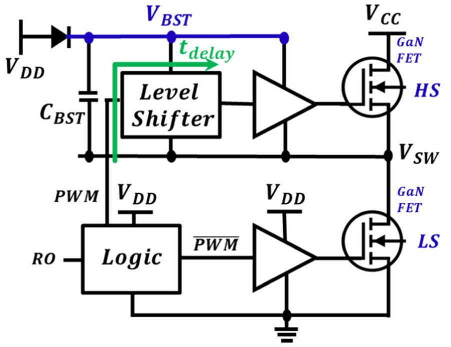


Fig. 7. Gate driver.

D. Gate Driver

Two primary techniques are employed to control power supply switching elements. The first involves the use of a dedicated discrete switch, whereas the second adopts a half-bridge configuration. In the half-bridge arrangement, a gate driver is required to independently control the HS and LS switches. Currently, two widely adopted methods exist for driving the HS switch. The first method is the bootstrap technique [38], [39], [40], in which the HS switch is implemented using an N-channel MOSFET (n-MOS), as shown in Fig. 7.

The second method employs a p-MOS for the HS switch and necessitates a dedicated floating supply generator to establish a suitable low-side reference for the driver [41]. Among these methods, the bootstrap technique is generally preferred due to the smaller silicon footprint of n-MOS devices relative to p-MOS transistors [42]. In this approach, the HS gate drive voltage is generated using a bootstrap capacitor and a diode. When the LS switch is turned ON, the bootstrap capacitor C_{BST} is charged to the supply voltage V_{DD} via the diode. During the dead time, when both switches are turned OFF, C_{BST} retains its charge, maintaining a voltage of approximately V_{DD}. To enable proper switching of the HS device, a level shifter is required to translate the PWM control signal from a ground-referenced range (0 to V_{DD}) to a high-side referenced range (V_{DD} to $V_{\mathrm{DD}}+V_{\mathrm{CC}}$) [43]. Here, V_{CC} represents the positive supply voltage of the half-bridge GaN FET power stage. This ensures that the gate-to-source voltage V_{GS} of the HS device remains within safe operating limits during switching transitions.

E. Converter

Transistors in power converters operate in one of two primary switching modes: hard switching or soft switching. In a hard-switching operation, current flows through the inductor during both the turn-ON and turn-OFF transitions of the transistor. During these transitions, the simultaneous presence of voltage and current across the drain-source terminals results in significant commutation losses due to overlap. These losses become more pronounced at higher switching frequencies. Additionally, hard switching often produces excessive voltage ringing and EMI, which can degrade reliability and potentially damage the switching devices. To mitigate false triggering and device overstress, the switching speed must be intentionally reduced—typically by increasing the value of the series gate resistor. However, hard-switching converters inherently suffer from higher switching losses and elevated EMI levels.

Critical-conduction-mode (CRCM) is among the simplest and most effective techniques to realize zero-voltage switching (ZVS). While soft switching reduces switching losses and EMI, it may introduce higher conduction losses, particularly due to increased peak inductor currents that elevate harmonic content and consequently the RMS current. In CRCM-based PWM converters, particularly with freewheeling switches, zero-current switching (ZCS) can be achieved at turn-OFF, and ZVS at turn-ON. Under these conditions, switching losses are nearly eliminated. However, conduction losses may rise by approximately 33% compared to continuous conduction mode (CCM) operation [15]. Therefore, CRCM is more suitable for applications where switching losses dominate over conduction losses, as is the case in the proposed converter.

The three fundamental nonisolated dc–dc converter topologies are the buck, boost, and buck–boost converters. A synchronous buck converter requires a high-side driver due to the shared ground reference between the control circuitry and the power stage. The boost converter, commonly used for voltage step-up in rectifier applications, can operate in CCM with hard switching, or in CRCM or discontinuous conduction mode under soft-switching conditions such as ZVS or ZCS. Buck and boost converters exhibit topological symmetry and are often conceptualized as a half-bridge leg. The buck–boost converter supports both voltage step-up and step-down operations.

F. Analysis of Power Losses in Subcircuits

The schematic of the all-GaN-based converter is shown in Fig. 8. The power losses associated with the proposed circuit were systematically classified and quantified using established analytical models, as summarized in Table II. Dynamic losses, primarily attributed to the charging and discharging of gate capacitances, were estimated using

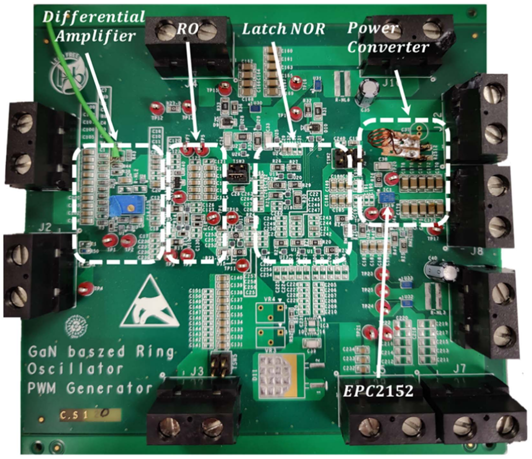


Fig. 8. Photograph of the all-GaN-based converter prototype.

$$P_{\mathrm{DYN}} \cong {V_{\mathrm{DRV}}}^2 \cdot f_{\mathrm{SW}} \cdot C_{\mathrm{ISS}} \tag{25}$$

where V_{DRV} denotes the driving voltage, f_{SW} the switching frequency, and C_{ISS} the input capacitance of the GaN device. The static losses arising from conduction were evaluated as

$$P_{\mathrm{STAT}} \cong R_{\mathrm{DS}} \cdot {I_{\mathrm{RMS}}}^2. \tag{26}$$

Resistive pull-up losses were modeled as $P_{\mathrm{PULL-UP}} = {V_{\mathrm{DRV}}}^2/R$, whereas pull-down resistive losses were expressed as $P_{\mathrm{PULL-DOWN}} = R_{\mathrm{DS}} \cdot {I_{\mathrm{LOAD}}}^2$. In the differential amplifier stage, power dissipation was attributed to several mechanisms: dynamic gate capacitance charging of transistors Q_7, Q_8, and Q_9; load capacitance discharging with the subsequent RO stage transistors Q_3 and Q_1; static current sourced drawn by $I_{S(Q_9)}$; and resistive losses components R_A, R_B, R_C, R_D, and the drain source resistance R_{DS} of transistor Q_{10}. These losses were evaluated with respect to the supply voltage V_{DD}.

For the RO stage, dynamic losses originated from charging and discharging the gate capacitances of transistors Q_1 through Q_6, and the load capacitances associated with Q_2, Q_4, and Q_6. Static losses included contributions from the on-resistance of transistors $Q_1 - Q_6$ and additional resistive elements R_{ON}, R_{OFF}, and R_{freq}.

Within the Latch NOR circuit, supplied by the voltage $V_{\mathrm{LATCH\_NOR}}$ derived from the source terminal of transistor Q_5, power losses were evaluated in two parts. First, in the latch body (transistors $Q_{14} - Q_{17}$), dynamic losses due to gate capacitances charging were considered. Notably, gate capacitance losses were computed for each conducting transistor individually rather than cumulatively, as only a single pull-down path is active at any given logic state.

Static losses encompassed contributions from both the pull-up and pull-down networks. Within the pull-up network, either $R_{\mathrm{PULL-UP(1)}}$ or $R_{\mathrm{PULL-UP(2)}}$ remained active in any given logical state, ensuring continuous conduction. In contrast, the pull-down network featured a single active transistor at any time, resulting in losses calculated as $2 \cdot R_{\mathrm{DS(ON)}} \cdot {I_{\mathrm{LOAD}}}^2$, which accounts for their sequential switching behavior.

TABLE II
ANALYSIS OF POWER LOSSES IN SUBCIRCUITS PER CYCLE

Sub-circuit	Loss Type	Formula
Differential Amplifier	Dynamic Gate	$P_{GATE} = \sum_{i=7}^{9} C_{ISS} \cdot f_{SW} \cdot {V_{GS,Q(i)}}^2$
	Static Current	$P_{STAT} = V_{DD} \cdot I_{S(Q9)}$
	Resistive Losses	$P_R = (R_A + R_B) \cdot {I_{S(Q9)}}^2 + \frac{{V_{DD}}^2}{R_C + R_D + R_{DS}}$
	Total_{AMP}	$P_T = P_{GATE} + P_{STAT} + P_R$
RO	Dynamic Gate	$P_{GATE} = \sum_{i=1}^{6} C_{ISS} \cdot f_{SW} \cdot {V_{GS,Q(i)}}^2$
	Dynamic C_{OSS}	$P_{DYN} = \sum_{i=2,4,6} C_{OSS} \cdot f_{SW} \cdot {V_{DS,Q(i)}}^2$
	Static Losses	$P_{STAT} = R_{on} \cdot {I_{D,Q(1)}}^2 + R_{off} \cdot {I_{D,Q(3)}}^2$ $+ R_{freq} \cdot {I_{D,Q(5)}}^2 + \sum_{i=1,3,5} 2 \cdot {I_{D,Q(i)}}^2 \cdot R_{DS}$
	$\mathrm{Total}_{\mathrm{RO}}$	$P_T = P_{GATE} + P_{DYN} + P_{STAT}$
Latch NOR	Dynamic Gate	$P_{GATE} = 9 \cdot C_{ISS} \cdot f_{SW} \cdot {V_{LATCH\_NOR}}^2$
	Static Pull-Up	$P_{PULL-UP} = {V_{LATCH\_NOR}}^2 \cdot$ $\cdot \left(\left(1/R_{PULL-UP(1)} \right) + \left(1/R_{PULL-UP(2)} \right) \right)$
	Static Pull-Down	$P_{PULL-DOWN} = 9 \cdot R_{DS} \cdot {I_{LOAD}}^2$
	Resistive Losses	$P_R = 7 \cdot \left({V_{LATCH\_NOR}}^2 / R \right)$
	$\mathrm{Total}_{\mathrm{Latch\_NOR}}$	$P_T = P_{GATE} + P_R +$ $+ P_{PULL-UP} + P_{PULL-DOWN}$
Gate Driver	Level Shifter	$P_{LEVEL\_SHIFTER} = f(V_{BUS}, Q_{LS}, f_{SW})$
	GaN FETs	$P_{FETs} = f(V_{DD}, C_{ISS,FET}, f_{SW})$
	Bootstrap Diode	$P_{BOOTSTRAP} = f(C_{Diode}, Q_{RR}, f_{SW})$
	Gate-Loop	$P_{LOOP} = f(I_{OUT}, L_{CS}, f_{SW})$
	$\mathrm{Total}_{\mathrm{Gate\_Driver}}$	$P_T = P_{FETs} + P_{BOOTSTRAP} + P_{LOOP} +$ $+ P_{LEVEL\_SHIFTER}$

For the logic inverters embedded within the latch NOR circuit, seven identical inverter gates were employed, each utilizing the same pull-up resistance. Consequently, dynamic losses due to gate capacitance charging were aggregated as seven times the individual inverter loss. The static losses for the pull-up network were expressed as $7 \cdot ({V_{\mathrm{LATCH\_NOR}}}^2/R)$, whereas those for the pull-down network were modeled as $7 \cdot R_{\mathrm{DS}} \cdot {I_{\mathrm{LOAD}}}^2$.

Finally, in the gate driver stage, total power losses were predominantly attributed to multiple sources given as follows:

1) the level shifter, with losses dependent on the bus voltage V_{BUS}, switching frequency, and required gate charge;
2) the enhancement-mode GaN FETs operating in both the HS and LS positions of the half-bridge configuration, whose losses were influenced by the driving voltage V_{DRV}, switching frequency, and gate charge;
3) gate-loop parasitics, where losses scaled with the load current and switching transitions; and
4) the operation of the bootstrap diode.

Notably, substituting the bootstrap diode with a controlled FET presents a promising approach for mitigating losses associated with the diode's forward voltage drop and reverse recovery charge (Q_{RR}).

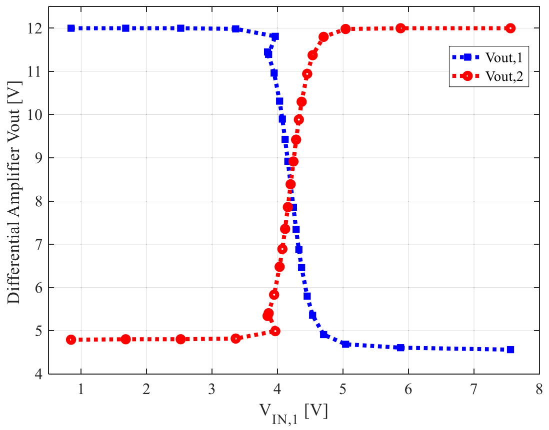


Fig. 9. Output voltage ranges of the differential amplifier.

TABLE III
KEY PARAMETERS OF THE GAN-BASED CONVERTER COMPONENTS

Parameter	EPC2038 (GaN FET)	EPC2152 (GaN Driver)
Technology	GaN HEMT	GaN HEMT
Maximum Voltage	$V_{DS} = 100\ V$	$V_{IN} = 80\ V$
Maximum Drain Current	$I_{D,MAX} = 0.5\ A$	$15\ A$
V_{TH} (typ./max.)	$1.7/2.5\ V$	N.A.
C_{GS}	$7\ pF$	N.A.
C_{DS}	$1.6\ pF$	N.A.
R_{DS}	$3300\ m\Omega$	$8.5\ m\Omega$
r_G	$4.8\ \Omega$	N.A.
Propagation Delay	N.A.	$20\ nS$

III. SIMULATION AND EXPERIMENTAL VALIDATION

The operational theory was experimentally validated using a converter constructed entirely from GaN-based components. The differential amplifier, PWM RO, and latch NOR circuits were implemented using EPC2038 GaN FETs, in conjunction with appropriately selected resistive elements. The generated PWM signal was used to drive the EPC2152 integrated system-on-chip, which incorporates an eGaN FET half-bridge power stage. The two eGaN FETs configured in the half-bridge topology possess identical drain-source on-resistances ($R_{\mathrm{DS(ON)}}$). The complete prototype, comprising the differential amplifier, PWM RO, latch NOR circuit, gate driver, and power conversion stage, is shown in Fig. 9.

The key parameters of the GaN-based converter components are listed in Table III. The experimental setup comprised a standard laboratory power supply and a Keysight EXR108A Infiniium EXR-Series real-time oscilloscope (1 GHz bandwidth, 16 GSa/s sampling rate). Signal probing was performed using a Keysight N2795A active probe, featuring a 100 MHz bandwidth, 1 pF input capacitance, and 1 MΩ input resistance. The ultralow input capacitance minimized parasitic loading on high-frequency GaN circuits, particularly in sensitive blocks such as the PWM RO and dead time latch. Frequency and duty cycle measurements were performed using the oscilloscope's automatic functions and verified manually by inspecting waveform transitions across multiple time scales. The circuit was

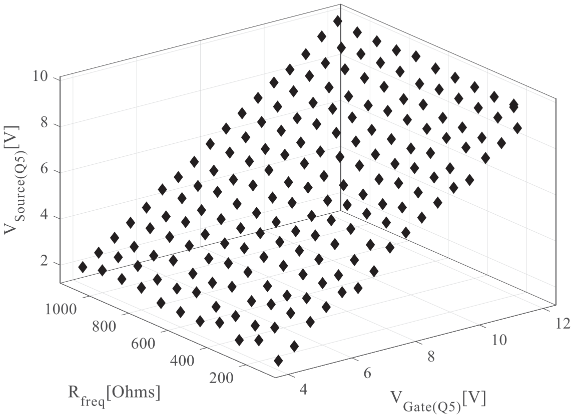


Fig. 10. Simulation-based determination of the supply voltage for the latch NOR circuit, ensuring safe operation within the maximum V_{GS} rating of the EPC2038 GaN transistors.

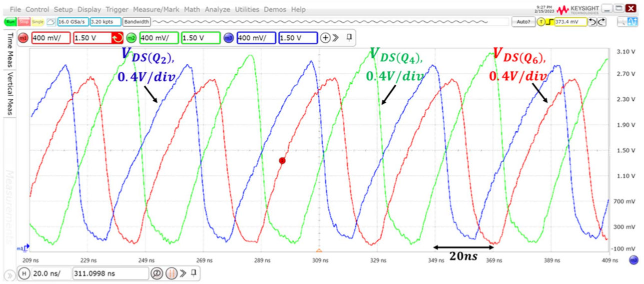


Fig. 11. Oscillation waveforms of the PWM generator, demonstrating stable ring oscillator operation at a frequency of approximately 23.88 MHz.

operated with a supply voltage of $V_{\text{DD}} = 12\,\text{V}$ throughout all measurements.

The first subcircuit analyzed is the differential amplifier. Fig. 10 shows the output voltage characteristics of the differential amplifier in response to variations in the gate voltage of transistor Q_1 while the gate voltage of transistor Q_2 is fixed at 4.2 V. In this experiment, the current mirror bias current is set to approximately $I_S(Q_9) \approx 0.7$ mA. The measured output voltage of the amplifier spans from 12 to 4.561 V. The measured output voltage of the amplifier spans from 12 to 4.561 V. These results confirm the expected operation of the differential pair: when the gate voltage of transistor Q_7 is lower than that of transistor Q_8, transistor Q_7 enters the cutoff region, whereas Q_8 operates in the active region, consistent with theoretical predictions.

The subsequent experiment focuses on the PWM RO subcircuit. Simulations were conducted using LTspice to determine appropriate values for the frequency-setting resistor R_{freq} and the gate voltage applied to transistor Q_6. These parameters directly influence the voltage at the source terminal of Q_6, which serves as the power supply voltage for the subsequent NOR latch stage. Next, the performance of the PWM RO subcircuit was investigated. The simulation results for the PWM RO are presented in Fig. 11. The EPC2038 GaN transistor has a maximum gate-source voltage (V_{GS}) rating of 6 V. To ensure safe operation and prevent device degradation in the latch NOR circuit, the supply voltage for this stage was limited to 4.8 V. This value was achieved by selecting a frequency-setting resistor $R_{\text{freq}} = 800\,\Omega$ and applying a gate voltage of 7.5 V to transistor Q_6.

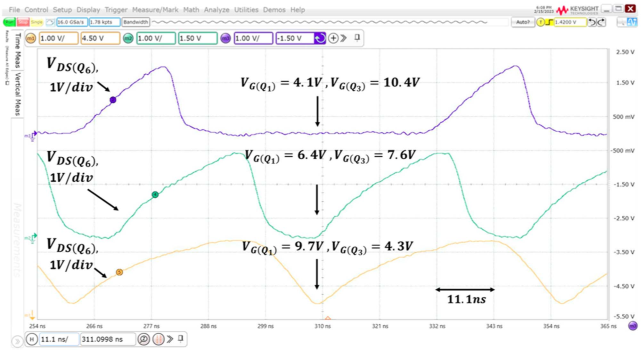


Fig. 12. RO-generated PWM signals demonstrating variation in duty cycle achieved through gate voltage modulation.

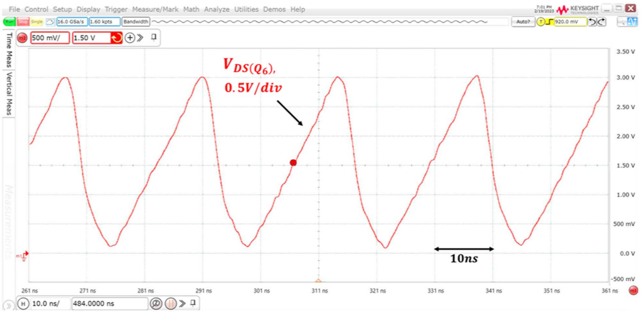


Fig. 13. Maximum RO output frequency measured at $f \cong 42.56\,\text{MHz}$ for $R_{\text{freq}} = 500\,\Omega$.

Fig. 12 shows the dynamic operation of the RO, in which each transistor sequentially activates the next stage in the ring. In this experiment, transistor Q_6 was designated as the output node, and the measured oscillation frequency was approximately $f \cong 23.88\,\text{MHz}$. The signals for Q_2, Q_4, and Q_6 exhibit variations due to differing *RC* time constants in each oscillator leg. These time constants govern the charging and discharging behavior of the gate and load capacitances, resulting in slight disparities in duty cycle and signal amplitude across the stages. The output signal observed at Q_6 reflects the cumulative propagation delay and timing interactions across the full oscillator loop, whereas signals at intermediate nodes, such as Q_2 and Q_4, primarily characterize internal oscillator dynamics.

Fig. 13 shows the controllability of the duty by varying the gate voltages, emphasizing the flexibility and tunability inherent in the RO topology.

To evaluate the controllability of the PWM duty cycle, three experimental measurements were conducted. In the first measurement, intended to validate shutdown control, gate voltages were set to $V_G\ (Q_1) = 4.1\,\text{V}$ and $V_G\ (Q_3) = 10.4\,\text{V}$, yielding a duty cycle of 18.2%. In the second measurement, the gate voltages were adjusted to $V_G\ (Q_1) = 6.4\,\text{V}$ and $V_G\ (Q_3) = 7.6\,\text{V}$, resulting in a duty cycle of 49.9%. The third measurement, focused on verifying time-domain control, employed $V_G\ (Q_1) = 9.7\,\text{V}$ and $V_G\ (Q_3) = 4.3\,\text{V}$, achieving a duty cycle of 68.8%. Additionally, the impact of the frequency-setting

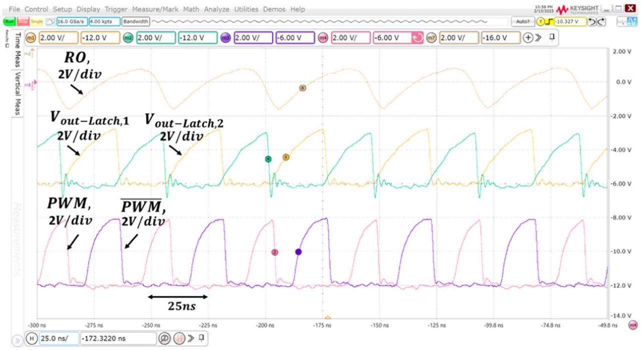


Fig. 14. Operation of the latch NOR signal generator at an input frequency of approximately 21.93 MHz, illustrating the generation of complementary PWM signals without initial dead time.

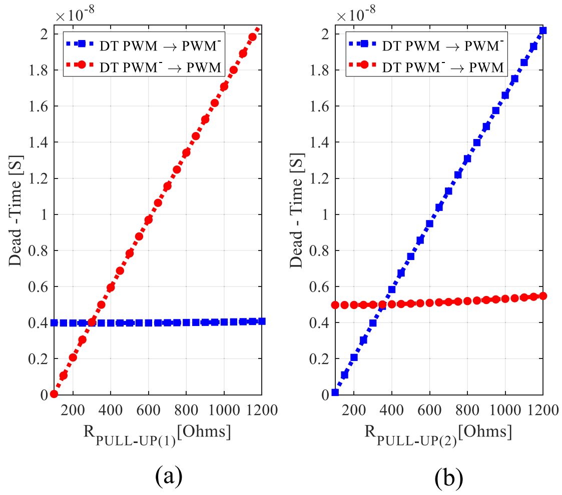
resistor R_{freq} on oscillator performance was characterized. When $R_{\text{freq}} = 800\,\Omega$, the maximum oscillation frequency was approximately $f \cong 25.79\,\text{MHz}$. Reducing R_{freq} to $500\,\Omega$, increased the maximum frequency to $f \cong 42.56\,\text{MHz}$. The $800\,\Omega$ configuration is presented in Fig. 14.

A performance benchmark was conducted to compare GaN and silicon transistors in the PWM RO circuit, focusing on their achievable frequency ranges under equivalent operating conditions. The silicon device selected for comparison was the BS170 N-channel small-signal MOSFET. Both implementations were supplied with an identical supply voltage of $V_{\text{DD}} = 12\,\text{V}$ and configured with the same frequency-setting resistor of $R_{\text{freq}} = 800\,\Omega$. Each devices were tested at a drain current of $I_D = 0.5\,\text{A}$. The EPC2038 GaN transistor supports a drain-source voltage of $V_{\text{DS}} = 100\,\text{V}$, whereas the BS170 operates up to $V_{\text{DS}} = 60\,\text{V}$. To ensure comparable layout and parasitic conditions, the silicon-based circuit was also implemented on a PCB, using an identical RO topology. The GaN-based RO demonstrated a frequency range of 8–27 MHz, significantly outperforming the silicon-based RO, which exhibited a frequency range of only 0.5–3.5 MHz.

The output of the RO is then processed by the latch NOR circuit to generate two complementary PWM signals with an adjustable dead time. The operation of the latch NOR circuit is shown in Fig. 15, demonstrating performance at an RO input frequency of 21.93 MHz. The input RO signal had a duty cycle of 64.7%.

The latch outputs produced two complementary signals, but initially without any inherent dead time between transitions. To introduce a controllable dead time, two stages of signal inversion were added, and appropriate values were selected for the pull-up resistors R_A and R_B. With this configuration, the latch outputs maintained the same frequency as the RO signal. The duty cycle of the first output signal was measured at 22%, whereas the complementary signal exhibited a duty cycle of 29.5%. Across multiple test conditions, the duty cycle of the gate-driving signals was observed to vary in the range of 17.4%–74.97%, confirming the circuit's tunability.

Further analysis was conducted to evaluate the influence of resistor values on dead time generation between the complementary signals. Fig. 16 shows the adjustable dead time between the two latch outputs, achieved by modifying the pull-up resistor values in LTspice simulations. The RO input frequency was 15.98 MHz with a duty cycle of 40.93%. In Fig. 16(a), with a pull-up resistor value of 300Ω, a shorter dead time was observed. In Fig. 16(b), increasing the pull-up resistor to 350Ω resulted in a longer dead time, demonstrating the effectiveness of resistor-based tuning for precise dead time control.



(a) (b)

Fig. 15. Dead time control between the PWM and $\overline{\text{PWM}}$ signals through variation of resistor $R_{\text{PULL-UP(1)}}$ (a) and $R_{\text{PULL-UP(2)}}$ (b) values.

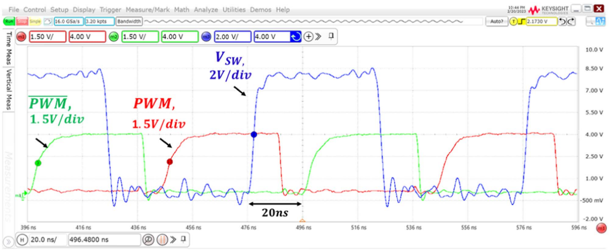


Fig. 16. Gate driver operation of the EPC2152 without a connected power converter, demonstrating independent switching performance.

This experiment validated the ability to adjust dead time between complementary PWM signals, with observed values ranging from 2 to 20 ns. Such tunability is critical in high-frequency switching applications, offering enhanced safety and performance—particularly in dc–dc converters, where precise timing directly influences power conversion efficiency and thermal management. Adjustable dead time minimizes switching overlap and shoot-through risk, allowing converters to adapt dynamically to varying load conditions while maintaining high efficiency and reliability across a broad operational envelope.

Subsequently, the functionality of the gate driver circuitry was evaluated. Both PWM and $\overline{\text{PWM}}$ signals were fed into the gate driver circuitry. The performance of the EPC2152 gate driver was evaluated without a load converter, operating at a switching frequency of 10.09 MHz. Fig. 17 shows the corresponding gate drive waveforms, with the duty cycle measured at 40.2% for the PWM signal and 38.8% for the $\overline{\text{PWM}}$ signal.

This test also enabled analysis of the gate drive propagation delay. To ensure symmetry between the HS and LS drivers, several design considerations were implemented. Both HS and

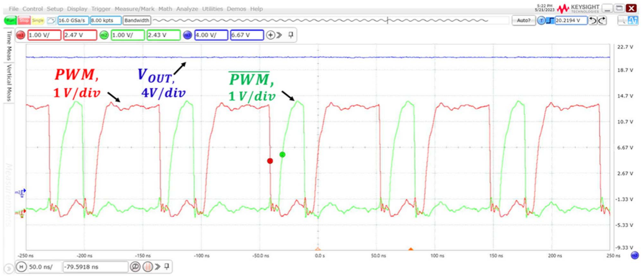


Fig. 17. Experimental operation of the GaN-based boost converter driven by the EPC2152 at a switching frequency of 10.61 MHz.

TABLE IV
EXPERIMENTAL LOSS OF THE SOLELY GAN DC–DC CONVERTER AT A FREQUENCY OF 10.61 MHZ

Sub-circuit	Parameter	Value	Units
Differential Amplifier	Supply Voltage (V_{DD})	12	V
	Average Current	2.421	mA
	Power Loss $P_{Differential\_Amplifier}$	29.05	*mW*
RO	Supply Voltage (V_{DD})	12	V
	Average Current	134	mA
	Upper GaN Losses	999.44	*mW*
	Lower GaN Losses	4.527	*mW*
	Resistor Losses	14.26	*mW*
	Power Loss P_{RO}	1.0276	*W*
Latch NOR	Resistor Losses	554.57	*mW*
	GaN Transistor Losses	29.829	*mW*
	Power Loss P_{Latch_NOR}	584.399	*mW*
Gate Driver	Supply Voltage (V_{DD})	12	V
	Power Loss P_{Gate_Driver}	2.568	*W*
Converter	Input Voltage (V_{IN})	12	V
	Load Resistor	10	Ω
	Output Voltage	20.613	V
	Output Power (P_{OUT})	42.49	*W*
Total Circuit	Total Power Loss (P_T)	$P_{Differential\_Amplifier} + P_{RO} + P_{Latch\_NOR} + P_{Gate\_Driver} + P_{OUT}$	*W*
	Efficiency	P_{OUT}/P_T	%

TABLE V
SUMMARY OF EXPERIMENTAL RESULTS FOR SUBCIRCUIT PERFORMANCE IN A SOLELY GAN DC–DC CONVERTER

Experiment	Parameter	Measured Results
Differential Amplifier	Output Voltage Range	$4.561 - 12\ V$
	Current Mirror	$I_{S(Q_9)} \approx 0.7\ mA$
PWM RO	Frequency Range (GaN EPC2038, $R_{freq} = 800\ \Omega$)	$8 - 27\ MHz$
	Frequency Range (Silicon BS170, $R_{freq} = 800\ \Omega$)	$0.5 - 3.5\ MHz$
	Maximum Frequency (GaN EPC2038, $R_{freq} = 800\ \Omega$)	$42.56\ MHz$
Latch NOR	Frequency	$21.93 MHz$
	Dead Time Control Range	$2\ n - 20\ n$
	Duty Cycle Range	$17.4\% - 74.97\%$
EPC2152 Gate Driver	Frequency Range	$0.5 - 14.5\ MHz$
	Power range	$0.465 - 3.72\ W$
Boost Converter	Input Voltage	$12\ V$
	Inductor value	$50\ nH$ (air inductor)
	Output voltage (Fig. 18)	$20.613\ V$
	Switching Frequency (Fig. 18)	$10.61\ MHz$
	PWM Duty Cycle (Fig. 18)	57.1%
	$\overline{PWM}$ Duty Cycle (Fig. 18)	19.8%
	Efficiency (Fig. 18)	90.98%
	Efficiency Range ($10\ MHz$, $20\ V$ output, load current: $1 - 10\ A$)	$84.29\% - 91.62\%$

LS drivers were triggered by the same PWM input to maintain synchronization. Matched components were used for both driver stages to achieve similar switching characteristics. A 1 μF bootstrap capacitor was employed on the high-side driver to ensure stable voltage levels during operation. Furthermore, careful routing of the gate drive traces was adopted to minimize parasitic inductance and capacitance, thereby improving switching speed and reducing delay mismatches.

An experimental evaluation was conducted to determine the standalone operational limits of the gate driver in the absence of a connected converter or reactive components. The EPC2152 gate driver demonstrated reliable switching operation across a frequency range of 0.5–14.5 MHz. Within this range, the associated power consumption varied from 0.465 W at the lower frequency limit to 3.72 W at the upper limit. These results confirm the gate driver's suitability for high-frequency applications and provide insight into its power demands under unloaded conditions.

Finally, the EPC2152 gate driver was integrated with a GaN-based boost converter to validate full system operation. Fig. 18 shows the boost converter behavior at a switching frequency of 10.61 MHz. To ensure consistent operation and avoid any bias between measurement stages, all subcircuits, including the EPC2152 gate driver and logic circuitry, were powered from a shared 12 V supply ($V_{DD} = 12$ V) during full system validation. The applied PWM signal had a duty cycle of 57.1%, whereas the complementary $\overline{\text{PWM}}$ signal exhibited a duty cycle of 19.8%. The converter supply voltage matched the system logic supply, $V_{DD} = 12$ V. A 50 nH air-core inductor and a 10 Ω resistive load were used in the test configuration, confirming successful power conversion at high frequency.

Table IV summarizes the power loss distribution across the major subcircuits of the fully GaN-based dc–dc converter under test conditions. The converter achieved an output voltage of 20.613 V at a switching frequency of 10.61 MHz. The experimental results demonstrate a high overall system efficiency of 90.98%, underscoring the effectiveness of GaN technology

TABLE VI
COMPARISON OF RECENTLY REPORTED GAN-BASED DC–DC CONVERTER TOPOLOGIES

Ref.	**Integration**	**Integration**	**Switching Frequency**	V_{OUT}/V_{IN}	**Maximum Efficiency**	**PWM Generator**	**Control Signal**	**Topology Converter**
[45] 2019	0.18 μm Si-BCD + Commercial GaN	Package Integrated	$50\ kHz$	$70\ V/3.3\ V$	70.3%	☑ Sawtooth	☒	Boost
[21] 2020	Au-free CMOS-Compatible, AlGaN/GaN MIS-HEMTs	Monolithic All-GaN	$10\ kHz$	$10\ V/16-29\ V$	N.A.	☑ Sawtooth	☑	Buck
[46] 2022	0.18 μm Si-CMOS + LV GaN	Package Integrated	$10\ MHz$	$1\ V/5\ V$	83.5%	☑ FPGA	☑	Buck
[47] 2022	GaN-on-SOI	Monolithic AHB	$0.5\ MHz$	$1\ V/36-48\ V$	83.4%	☑ RO	☒	Buck
[48] 2023	0.13μm CMOS-SOI + Commercial GaN HEMT	Fully Integrated	$500\ MHz$	$14-20\ V/6\ V$	58%	☒	☒	Boost
This Work	GaN HEMTs	Discrete PCB	$\geq 10\ MHz$	$20\ V/12\ V$	91.62%	☑ RO	☑	Buck, Boost, and Buck-Boost

BCD: Bipolar-CMOS-DMOS; LV: Low Voltage; FPGA: Field-Programmable Gate Array; AHB: Asymmetrical Half-Bridge; SOI: Silicon on Insulator.

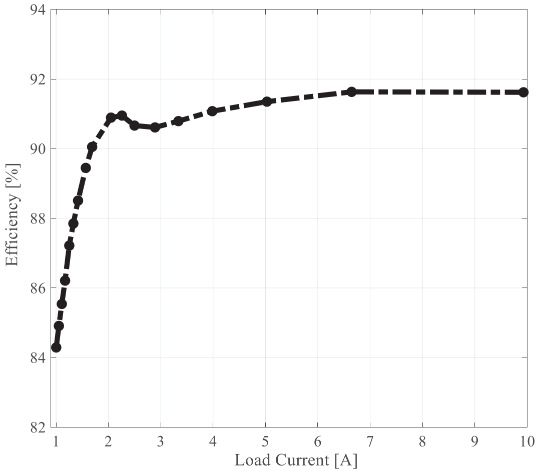


Fig. 18. Measured circuit efficiency as a function of load current for the GaN-based boost converter at an output voltage of 20 V and a switching frequency of 10 MHz.

for high-frequency power conversion and validating the performance of the proposed architecture.

Furthermore, Fig. 18 shows the measured efficiency of the boost converter as a function of load current, with an output voltage maintained at 20 V and a switching frequency of 10 MHz. Under these operating conditions, the converter exhibited an efficiency range from 84.29% to 91.62%, demonstrating stable and high-performance operation across varying load levels.

The efficiency profile of the proposed dc–dc converter exhibits deviations from the conventional smooth curve typically observed in power converters. This behavior is primarily attributed to the characteristics of the EPC2152 gate driver used in the design. As specified in the EPC2152 datasheet, the driver is optimized for operation up to 3 MHz; however, in this study, the converter was operated at 10 MHz. At such elevated frequencies, switching losses increase significantly, resulting in a sharp efficiency peak followed by a more rapid decline—unlike traditional designs where the efficiency degradation is more gradual and predictable.

The output power (P_{OUT}) was calculated by measuring the output voltage and current, whereas the input power was determined through measurements of the voltage and current supplied to the converter. Measurements were sampled to capture the converter's dynamic behavior at the 10 MHz switching frequency. Table V summarizes the key operating parameters and experimental results obtained from the main subcircuits.

A comparative analysis with recently reported GaN-based dc–dc converter topologies is provided in Table VI to contextualize the performance of the proposed architecture. The comparison encompasses several critical design parameters, including integration level, fabrication process, switching frequency, and converter topology. A distinguishing feature of the proposed design lies in its exclusive use of GaN HEMTs, thereby eliminating performance limitations typically encountered in hybrid silicon–GaN configurations. This all-GaN approach represents a step toward the realization of fully monolithic converter-on-chip solutions.

In our prior work [44], a GaN-based resonant gate driver topology was developed, employing GaN transistors as the gate driving stage for Silicon Carbide power switches. That design demonstrated a 26% reduction in gate losses at a switching frequency of 2.5 MHz by suppressing the Miller effect, thus enabling efficient high-voltage operation. These results further validate the potential of GaN technology in enhancing the performance and efficiency of WBG semiconductor systems.

IV. DISCUSSION

The proposed dc–dc converter architecture, based exclusively on GaN HEMT transistors, demonstrates the feasibility of achieving high-efficiency energy conversion while underscoring the advantages of GaN technology in high-frequency power applications. This work represents a significant step toward monolithic integration by investigating the essential building blocks required for a fully integrated GaN-based power system. The experimental results provide critical insights into circuit operation and switching behavior, which are vital considerations for future single-chip implementation.

The converter comprises five principal subcircuits: the power stage, gate driver, NOR latch for dead time generation, PWM RO, and differential amplifier. Each subcircuit was individually validated through experimental testing. The differential amplifier exhibited an output voltage range spanning from 4.561 V to the supply voltage of 12 V. For the GaN-based PWM RO, the proposed topology achieved a maximum oscillation frequency of 42.56 MHz with an R_{freq} of 0.5 kΩ. At $R_{\text{freq}} = 0.8\,\text{k}\Omega$, the RO frequency range using GaN EPC2038 transistors was measured between 8 and 27 MHz, whereas the same topology implemented with a silicon BS170 transistor yielded a range of 0.5–3.5 MHz. The NOR latch topology was employed to generate complementary PWM signals with an adjustable dead time. A controllable deadband range from 2 to 20 ns was achieved between the PWM and its complement, with the overall duty cycle adjustable between 17.4% and 74.97%. The performance of the EPC2152 gate driver was also characterized in an isolated configuration (i.e., without a connected power stage or reactive components), demonstrating operational capability from 0.5 to 14.5 MHz and a power dissipation in the range of 0.465–3.72 W.

Experimental validation of the proposed GaN-based boost converter at a switching frequency of 10.61 MHz demonstrates an efficiency of 90.98%. Achieving high efficiency at such frequencies required careful minimization of conduction and switching losses through the selection of GaN transistors with low $R_{\text{DS(on)}}$ optimization of gate drive conditions and meticulous PCB layout to reduce parasitic inductance and capacitance. Although a boost converter was used for demonstration, the modular nature of the RO-based PWM generator and the gate driver architecture allows seamless adaptation to other converter topologies, including buck and buck–boost configurations. This flexibility highlights the broader applicability of the proposed design for high-frequency, high-performance power conversion.

Importantly, the converter design outperforms silicon-based counterparts in terms of frequency scalability and dynamic control, made possible by a fully discrete GaN implementation. In contrast to fixed-specification Power Management ICs, which are constrained by limited configurability and often suffer from high parasitic elements, the proposed discrete GaN configuration provides enhanced control over critical parameters such as dead time, duty cycle, and switching frequency. Furthermore, the all-analog nature of the design avoids issues associated with digital control, including propagation delays, clock-related timing constraints, and EMI susceptibility. This enables more precise switching and improved efficiency at high frequencies.

Loss analysis indicates that, beyond the converter and gate driver stages, primary losses occur in the resistive elements of the latch NOR pull-up network and transistor Q_5 of the RO subcircuit. While these losses do not impede high-frequency operation, increasing pull-up resistance to reduce losses must be balanced against potential degradation in signal transition times and dead time precision. Despite its advantages, the proposed topology has several limitations. The use of discrete GaN HEMT transistors contributes to increased cost and board space. Operation at tens of megahertz introduces challenges such as ringing, EMI, and efficiency degradation, requiring stringent control of parasitics and signal integrity. PCB layout techniques such as minimizing trace lengths, placing decoupling capacitors close to power pins, and selecting low-parasitic passive components were employed to address these challenges. Resistor values were optimized to manage rise/fall times, mitigate voltage spikes, and reduce susceptibility to false triggering.

To further reduce the converter's physical footprint, future research may explore the monolithic integration of a GaN-based level shifter and control logic. While the current architecture already implements all major analog subcircuits using GaN HEMTs, the remaining off-chip interconnects between voltage domains impose layout complexity and parasitic overhead. Integrating the level shifter directly on the one GaN die eliminates cross-technology boundaries, reduces PCB area, and supports even higher switching frequencies. These improvements would in turn enable further reduction in passive component size and overall converter volume, marking a crucial step toward a fully integrated GaN-based converter-on-chip. Nevertheless, increased parasitic effects at very high frequencies remain a concern and may impact long-term reliability. Additionally, while GaN-on-Si offers integration potential, it presents fabrication challenges that may limit scalability. The reliability of the proposed circuit under extended operation remains an open question and will require further investigation to assess the viability of this topology in long-term, real-world applications.

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