Design and Implementation of Power Line Communication Among Distributed H-Bridges in a Cascaded Multilevel Converter

Linchong Xu, *Member, IEEE*, Xing Zhang, *Senior Member, IEEE*, Wei Zhao, Jun Xu, and Jiacai Zhuang

***Abstract*—In distributed cascaded multilevel converters, communication between converter modules is crucial for enabling distributed control. The most cost-effective approach for this communication is utilizing the series-connected power line. However, switching noise generated by the converter modules significantly disrupts the communication channel, posing challenges to achieving reliable transmission. This article proposes a power line communication (PLC) design method specifically tailored for converter modules operating in noisy environments. In each module, a differential balanced bridge (DBB) structure is implemented to suppress noise, thereby enhancing the signal-to-noise ratio (SNR) of the PLC and enabling fast, low-latency communication. A system channel model is developed to analyze the transmission gains of both noise and signal, facilitating a comprehensive SNR evaluation. Finally, a prototype system consisting of eight H-bridge converter modules is constructed to demonstrate the practicality and effectiveness of the proposed method.**

***Index Terms*—Cascaded multilevel topology, differential balanced bridge (DBB), impulse noise, low delay, photovoltaic (PV) generation system.**

I. Introduction

CASCADED multilevel converters have been widely used in power systems, particularly in applications such as STATCOM, solid-state transformers, photovoltaic (PV) generation systems, and transformerless energy storage systems. Compared to two-level converters, multilevel converters offer advantages such as modular expandability, reduced switching frequency, improved conversion efficiency, and decreased current harmonic content [1], [2], [3], [4], [5].

Cascaded multilevel converters can be controlled using either centralized or distributed control methods. However, in PV generation systems, particularly those requiring module-level maximum power point tracking (ML-MPPT), distributed control offers a more effective solution [6], [7], [8]. Distributed control depends on communication, where the primary controller sends control instructions to each converter unit [6], [7]. The communication system must be high-speed, low-latency, and highly reliable.

Traditionally, wired communication technologies such as fiber optics, CAN, RS-485, and Ethernet have been widely adopted in cascaded multilevel systems due to their proven reliability [9], [10], [11], [12]. For instance, [9] and [10] utilize the CAN protocol with fiber optics as the communication medium for distributed control, while [11] enhance the network topology while retaining fiber optics. Wu et al. [12] utilize ethernet control automation technology (EtherCAT) in cascaded H-bridge systems for high-speed control. However, the use of fiber optics or electrical cables increases installation costs and, more critically, compromises system reliability. This is especially concerning in harsh environments, where cables are vulnerable to damage and aging, posing significant risks to system reliability. Conversely, wireless communication methods such as Wi-Fi and Zigbee eliminate the need for cables but are often criticized for potential delays, reliability issues, and susceptibility to environmental interference, making them generally unsuitable for real-time control applications [13].

Power line communication (PLC) is widely used in power systems because it eliminates additional communication lines and is less susceptible to spatial interference. Recent research works have focused on integrating PLC with the monitoring and control of power electronic converters. In [14] and [15], a capacitively coupled PLC scheme is proposed to transmit carrier communication signals using coupling transformers. However, the transmission efficiency is limited by the high-frequency impedance of solar modules. To enhance dc PLC transmission efficiency, a parallel resonant coupling circuit was applied to PV module monitoring systems, achieving a data rate of 10 kbps [16]. Nevertheless, these PLC implementations are restricted to dc lines with high signal-to-noise ratios (SNRs), making them unsuitable for cascaded multilevel systems with low SNR.

A novel technique, known as talkative power conversion (TPC) or power and signal dual modulation (PSDM), has been proposed to integrate data modulation into power electronic converters [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. Wu et al. [17] present the communication model, modulation, and demodulation methods based on Buck topology,

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achieving a communication rate of 2 kbps. Zhu et al. [20] incorporate the data carrier into the power control loop, achieving a dc PLC with a bit rate of 2 kbps. Spread spectrum techniques can be applied in PSDM to enhance communication security and improve noise immunity [21], [22]. However, the typically low communication rate of TPC limits its practical applications.

Conventional PLC techniques use power transmission lines as the communication channel, with power signals and communication signals separated in the frequency domain. However, the internal series-connected power line in a cascaded multilevel converter is plagued with significant noise across a wide frequency range. This noise adversely affects the SNR of the communication signal, thereby limiting the communication rate [30].

To establish a data link within cascaded multilevel converters, [26] introduce a dedicated H-bridge module (HBM) for signal transmission within the cascaded H-bridge system, where FSK modulation was employed to achieve a communication rate of 600 bps. Furthermore, [27], [28] introduced power and data transmission modules into cascaded H-bridges using the time division multiple access (TDMA) method. To mitigate the impact of impulse noise, complex encoding and decoding algorithms are employed, but the communication rate is limited to less than 1 kbps. Gupta and Mazumder [29] proposed a sequential cotransmission scheme for power and data, transmitting them in different time periods. However, large duty cycles present challenges for transmitting larger data packets.

Orthogonal Frequency Division Multiplexing (OFDM), owing to its high spectral efficiency and strong resilience to interference [23], [24], has been widely adopted in standardized PLC solutions to support higher data rates. For example, G3-PLC achieves up to 33.4 kbps [35], PRIME up to 128 kbps [36], and IEEE 1901.2 up to 500 kbps [37]. This makes OFDM-based PLC a promising candidate for enabling high-speed data transmission in cascaded multilevel converter systems. However, the use of cyclic prefix, synchronization overhead, and the computational burden of fast Fourier transform (FFT)/inverse fast Fourier transform (IFFT) operations introduce significant latency, which is incompatible with the stringent low-latency requirements of distributed control systems.

This article presents a novel PLC approach designed for high-data-rate internal communication within a cascaded multilevel converter. The approach improves the system's SNR by implementing a differential balanced bridge (DBB) coupling scheme, incorporating ON-OFF keying (OOK) modulation, and employing precision analog demodulation for detection, thereby increasing the data rate and minimizing latency. The primary contributions of this article are as follows.

1) A PLC scheme for multilevel converters is proposed. This scheme utilizes a DBB coupling structure to suppress wideband noise in cascaded multilevel converters, significantly enhancing communication quality and enabling high-rate communication.
2) The communication model of the system is established, and the transfer functions of the signal and noise are analyzed. The efficiency and practicability of the proposed method are validated through the construction of an experimental system comprising of eight H-bridge converters.

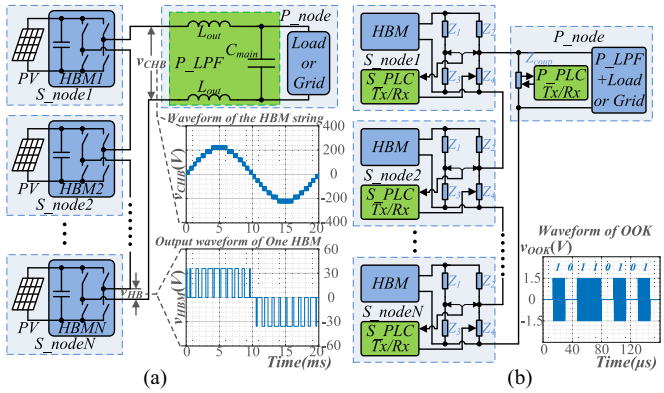

Fig. 1. Structure diagram. (a) Typical cascaded multilevel converter for PV power generation. (b) Proposed PLC scheme.

This article is organized as follows. Section II describes the system structure and analyzes the noise characteristics of PLC in cascaded multilevel converters. Section III discusses coupling methods and introduces the DBB coupling scheme. Section IV provides a detailed design of the communication system. Section V validates the prototype through experimental results. Finally, Section VI concludes this article.

II. PLC Principle in Cascaded Multilevel Converter

A. System Structure

Fig. 1(a) shows the structure of a cascaded multilevel converter for PV power generation, comprising N HBMs connected in series and powered by PV panels. Each HBM generates a low-frequency (500 Hz) pulsed voltage without filtering, as shown on the right side of Fig. 1(a). The combined output of all series-connected modules is then filtered by a centralized filter block, which consists of two separate inductors and a capacitor.

In the proposed system, each HBM is positioned close to its corresponding PV panel, resulting in several meters of separation between adjacent HBMs. Given this physical distribution, PLC is the most suitable method for data exchange. A primary-secondary control strategy is implemented, where all HBMs function as secondary nodes (S_nodes), while the centralized filter block serves as the primary node (P_node). Notably, a primary controller is integrated within the P_node to facilitate communication and compute the required power control reference.

To coordinate the output of HBMs, carrier phase-shifting sinusoidal pulse width modulation strategy is employed. Each HBM adopts SPWM technology individually, with a specific phase shift applied to the triangular carriers of different HBMs [6]. Consequently, during initialization, the P_node allocates the phase shift angle to each S_node according to its assigned address through broadcasting the startup frame. In operation, the P_node establishes synchronization with the grid and broadcasts downlink frames, which contain synchronization data, grid-side information, and control instructions to all S_nodes. Each S_node implements ML-MPPT, generates its own SPWM based on the received data, and transmits an uplink frame containing dc information to the P_node, when receives the downlink frame. The P_node processes the dc information from the uplink frame

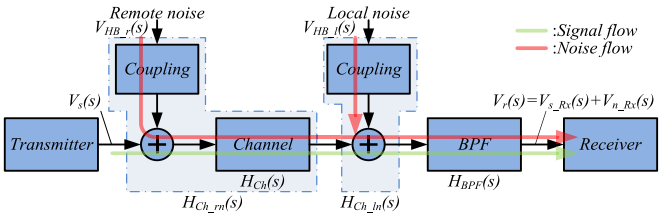

Fig. 2. Block diagram of the communication system.

to calculate the subsequent control instructions, which are then loaded into the next downlink frame. This process is repeated in a continuous cycle to ensure the proper operation of the system.

To implement the distributed control scheme in the cascaded multilevel converter, a reliable PLC link must be established between each HBM and the primary node. Signal couplers should be deliberately designed to facilitate PLC between the primary and secondary nodes. As shown in Fig. 1(b), Z_1, Z_2, Z_3, and Z_4 form the coupling circuit of the *S*_node, while Z_{coup} is the coupling circuit of the *P*_node. The PLC waveform is depicted on the right side of Fig. 1(b).

B. Communication Model

The block diagram of the PLC system is illustrated in Fig. 2. To eliminate noise, a BPF with an in-band gain of 1 is employed. Thus, the received data signal $V_{s\cdot Rx}$ can be expressed as

$$V_{s\_Rx}(s) = V_s(s) H_{\text{Ch}}(s) H_{\text{BPF}}(s) \approx V_s(s) H_{\text{ch}}(s). \quad (1)$$

Within this system, noise is divided into two distinct components: local noise and remote noise. The received noise signal $V_{n\cdot Rx}$ is

$$\begin{aligned} &V_{n\_Rx}(s) \\ &= [V_{\text{HB}\_r}(s) H_{\text{Ch\_rn}}(s) + V_{\text{HB}\_l}(s) H_{\text{Ch\_ln}}(s)] H_{\text{BPF}}(s) \\ &= [V_{\text{HB}\_r}(s) H_{\text{BPF}}(s)] H_{\text{Ch\_rn}}(s) \\ &\quad + [V_{\text{HB}\_l}(s) H_{\text{BPF}}(s)] H_{\text{Ch\_ln}}(s) \end{aligned} \quad (2)$$

where $V_s(s)$, $V_{\text{HB}\cdot r}(s)$, and $V_{\text{HB}\cdot l}(s)$ are the output signals of the transmitter, the remote HBM, and the local HBM, respectively. The transfer functions of data signal, remote noise, local noise, and BPF are denoted as $H_{\text{Ch}}(s)$, $H_{\text{Ch}\cdot\text{rn}}(s)$, $H_{\text{Ch}\cdot\text{ln}}(s)$, and $H_{\text{BPF}}(s)$ respectively. Minimizing noise is essential for optimal performance.

C. Noise Analysis

The proposed PLC system employs the power flow path of the cascaded multilevel converter as the communication channel. However, each HBM generates a PWM power waveform without filtering, which introducing significant interference, making the HBMs noise sources. In the system, most of the noise originates from the rising and falling edges of the HBM's PWM output. However, this noise is neither Gaussian noise nor stationary, so its impact cannot be assessed solely based on its high-frequency components. In the worst-case scenario, when the edge of the PWM wave coincides with a symbol period, it introduces a short-term interference to the data symbol, as shown in Fig. 3.

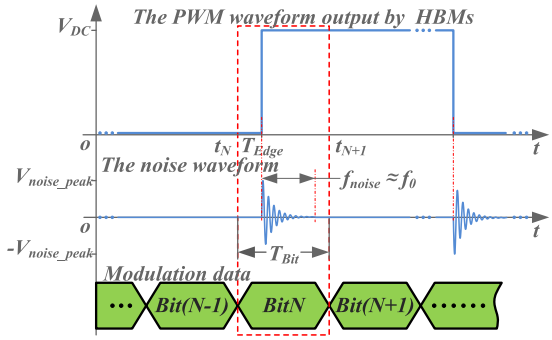

Fig. 3. Waveforms of a noise in a symbol period.

The input noise, i.e., the PWM waveform generated by an HBM over a short period, can be equivalent to

$$v_{\text{HB\_Bit}}(t) = \begin{cases} 0, & t < T_{\text{Edge}} \\ V_{\text{DC}}, & t \geq T_{\text{Edge}} \end{cases} \quad (3)$$

where V_{DC} is the amplitude of the PWM waveform. The transfer function of the BPF is denoted as

$$H_{\text{BPF}}(s) = \frac{\frac{\omega_0}{Q} s}{s^2 + \frac{\omega_0}{Q} s + \omega_0{}^2} \quad (4)$$

where ω_0 is the central angular frequency of BPF, with its relationship with the center frequency f_0 is $\omega_0 = 2\pi f_0$, and Q is the quality factor of the BPF. Thus, the noise passing through the BPF can be expressed as

$$\begin{aligned} V_{n\_\text{inB}}(s) &= V_{\text{HB\_Bit}}(s) H_{\text{BPF}}(s) \\ &= V_{DC} \frac{\frac{\omega_0}{Q}}{s^2 + \frac{\omega_0}{Q} s + \omega_0{}^2} e^{-sT_{\text{Edge}}}. \end{aligned} \quad (5)$$

Letting $T_{\text{Edge}} = 0$, the output noise in time domain is

$$v_{n\_\text{inB}}(t) = \mathcal{L}^{-1}[V_{n\_\text{inB}}(s)] = \frac{V_{\text{DC}}}{kQ} e^{-\frac{\omega_0}{2Q} t} \cdot \sin(k\omega_0 t) \quad (6)$$

where $k = \sqrt{1 - 1/4Q^2} \approx 1$.

From (6), it can be observed that the equivalent noise is a damped sine wave, with a frequency close to the central frequency of the passband. The peak of the equivalent noise is

$$V_{\text{np\_inB}} = A \cdot e^{-\frac{\pi}{4kQ}} \quad (7)$$

where

$$A = \frac{V_{\text{DC}}}{kQ} \approx \frac{V_{\text{DC}}}{Q}.$$

This means the converter will introduce impulse noise [30], [31] with peak values of approximately V_{DC}/Q, which critically affects communication. Consequently, it is crucial to eliminate this impulse noise. Given the high amplitude, short duration, and fast attenuation of impulse noise, it is meaningful to analyze SNR over a short period, such as one symbol period. Furthermore, the cascaded multilevel converter system ensures that the step waveforms generated by each HBM do not coincide in the time

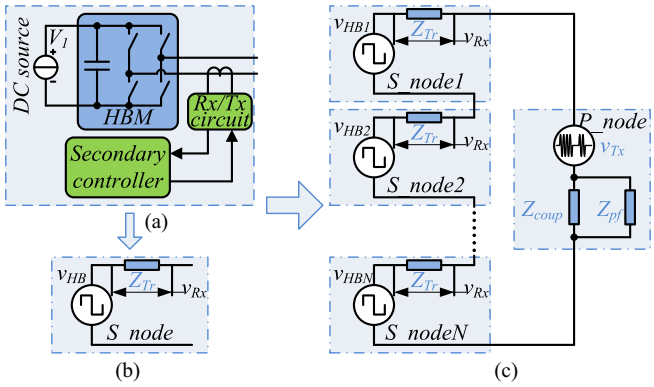

Fig. 4. Conventional inductive coupling circuit and its channel model. (a) HBM with inductive coupling circuit. (b) Equivalent model of the coupling circuit. (c) Simplified channel model.

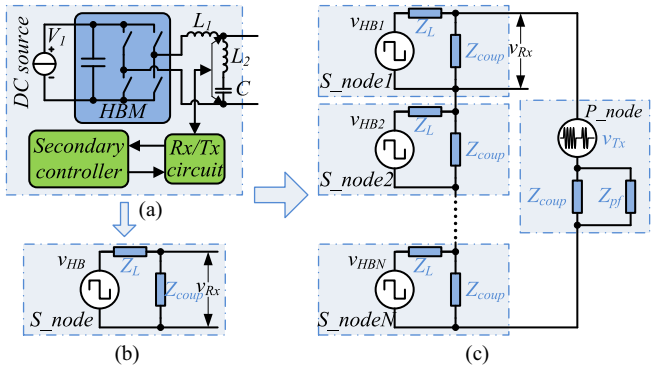

Fig. 5. Low-pass coupling circuit and its channel model. (a) HBM with low-pass coupling circuit. (b) Equivalent model of the low-pass coupling circuit. (c) Simplified channel model.

domain. Consequently, in (2), the total noise is the sum of local and remote noise at different times, which should have the same amplitude as the noise emitted by a single HBM. Local and remote noise should be analyzed separately.

III. Design of Coupling Circuit With Noise Reduction

The coupling circuit is indispensable for the PLC system and significantly influences communication performance. This section analyzes and evaluates various strategies to identify the optimal solution.

A. Conventional Unbalanced Coupling Circuit

Fig. 4(a) depicts a conventional inductive coupling circuit employing a magnetic core. Fig. 4(b) shows the equivalent model where the HBMs are treated as a noise source v_{HBi}. The simplified channel model of the PLC system is shown in Fig. 4(c). In this model, for the secondary node, the received noise during one symbol period can be approximately expressed as

$$V_{Tr\_n}\ (s) = \frac{Z_{Tr} V_{n\_\mathrm{inB}}\,(s)}{N Z_{Tr} + Z_{\mathrm{pri}}} \approx \frac{V_{n\_\mathrm{inB}}\,(s)}{N+1} \tag{8}$$

where Z_{pri} is the impedance of the *P*_node, Z_{Tr} is the impedance of the *S*_node, and $Z_{\mathrm{pri}} \approx Z_{\mathrm{Tr}}$.

The noise at the receiver is highly significant, as it reflects the output voltage of each HBM, making this coupling circuit unsuitable for environments with impulsive noise.

To suppress the impulse noise, a low-pass structure is introduced as depicted in Fig. 5(a). Fig. 5(b) presents the equivalent model. Z_L *and* Z_{coup} constitute a low-pass filter (LPF) structure to diminish the amplitude of the impulse noise, where Z_{coup} is an *LC* series resonant network with a resonant frequency equal to the communication frequency. In the passband, $Z_L >> Z_{\mathrm{coup}}$, leading to a simplified channel model of the PLC system, as shown in Fig. 5(c).

Within this system, the communication signal is obtained from Z_{coup}, the transfer function of the remote noise channel, $H_{\mathrm{LPF\_rn}}$ can be approximately expressed as

$$H_{\mathrm{LPF\_rn}}\,(s) = \frac{V_{\mathrm{Rx}}}{V_{\mathrm{HBi}}} = \frac{Z_{\mathrm{coup}}}{Z_L + Z_{\mathrm{coup}}} \frac{Z_{\mathrm{LPF}}}{(N-1)\,Z_{\mathrm{LPF}} + Z_{\mathrm{pri}}} \approx \frac{Z_{\mathrm{coup}}}{Z_L + Z_{\mathrm{coup}}} \frac{1}{N} \tag{9}$$

where Z_{LPF} is the impedance of the *S*_node, and in the passband, $Z_{\mathrm{LPF}} \approx Z_{\mathrm{pri}}$. The transfer function of the local noise channel, $H_{\mathrm{LPF\_ln}}$ can be approximately expressed as

$$H_{\mathrm{LPF\_ln}}\ (s) = \frac{V_{\mathrm{Rx}}}{V_{\mathrm{HBi}}} \approx \frac{Z_{\mathrm{coup}}}{Z_L + Z_{\mathrm{coup}}}. \tag{10}$$

According to the above-mentioned noise analysis, communication is primarily affected by PWM edges. Therefore, the noise received at the secondary node (e.g., *S*_node*j*) is the superposition of multiple noise sources v_{HBi} at different times in the time domain, rather than the superposition of amplitudes. When $N>>1$, the maximum noise in one symbol period can be approximately considered as

$$\begin{aligned} V_{\mathrm{LPF}\_nj}\ (s) &= \max\left[V_{n\_\mathrm{inB}}\,(s)\,H_{\mathrm{LPF}\_ln}\,(s), V_{n\_\mathrm{inB}}\,(s)\,H_{\mathrm{LPF\_rn}}\,(s)\right] \\ &= \frac{Z_{\mathrm{coup}}}{Z_L + Z_{\mathrm{coup}}} V_{n\_\mathrm{inB}}\,(s). \end{aligned} \tag{11}$$

It is clear that, although the low-pass structure effectively mitigates remote noise in the communication frequency spectrum, the local noise cannot be suppressed and would significantly impact communication.

B. Proposed Balanced Coupling Circuit

To attenuate the impact of local noise, a symmetrical leg is introduced based on the LPF structure, as shown in Fig. 6(a). Fig. 6(b) presents the equivalent model, where port CD is connected to the cascaded line, and port EF serves as the communication port. According to the principle of bridge balance [32], when $Z_1 = Z_2$, $Z_3 = Z_4$ with port CD open, the received signal v_{Rx} at EF is zero, effectively minimizing the received local noise. This structure is referred to as DBB. A simplified

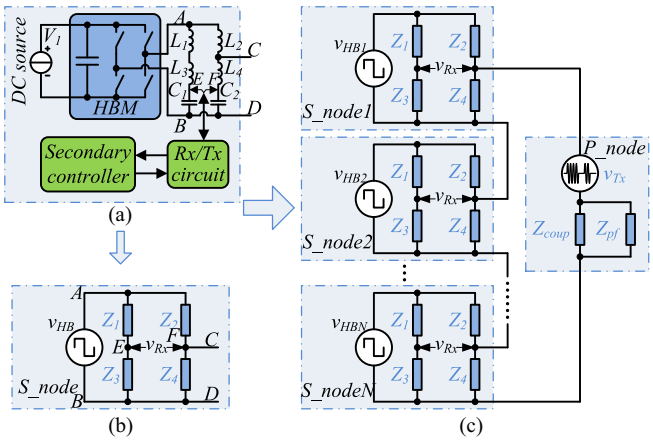

Fig. 6. DBB coupling circuit and its channel model. (a) HBM with DBB coupling circuit. (b) Equivalent model of the DBB coupling circuit. (c) Simplified channel model.

channel model of the PLC system based on the DBB structure is shown in Fig. 6(c).

The transfer function of the remote noise channel $H_{\mathrm{DBB\_rn}}$ is the same as $H_{\mathrm{LPF\_rn}}$, and can be approximately expressed as

$$H_{\mathrm{DBB\_rn}}(s) = \frac{Z_4}{Z_4 + Z_2}\frac{1}{N}. \tag{12}$$

The transfer function of the local noise channel $H_{\mathrm{DBB\_ln}}$ can be approximately expressed as

$$H_{\mathrm{DBB\_ln}}(s) = 0. \tag{13}$$

It is evident that the local noise is fully suppressed when port CD is disconnected from the system. Furthermore, even when port CD is connected, the local noise can still be effectively mitigated if the external impedance of this port is significantly greater than Z_4.

The suppression of local noise by the DBB is primarily influenced by the external impedance of port CD. A comprehensive analysis of this external impedance will be presented in Section IV.

The maximum noise received during one symbol period at the secondary node (*S*_node*j*) can be approximately considered as

$$\begin{aligned} V_{\mathrm{DBB}\_nj}(s) &= \max\left[V_{n\_\mathrm{inB}}(s) H_{\mathrm{DBB}\_ln}(s), V_{n\_\mathrm{inB}}(s) H_{\mathrm{DBB\_rn}}(s)\right] \\ &= \frac{Z_4}{N(Z_4 + Z_2)} V_{n\_\mathrm{inB}}(s) \end{aligned} \tag{14}$$

where $Z_4 = Z_{\mathrm{coup}}$, $Z_2 = Z_{\mathrm{L}}$, $Z_2 >> Z_4$. Consequently, in terms of impulse noise suppression, the DBB structure demonstrates significant advantages over the low-pass structure.

Given that $Z_1 >> Z_3$, $Z_2 >> Z_4$, and Z_{pf} is the impedance of the power filter, with $Z_{\mathrm{pf}} >> Z_{\mathrm{coup}}$ in the passband, the transfer function of the data signal can be approximately as

$$H_{\mathrm{DBB\_s}}(s) = \frac{Z_{\mathrm{DBB}}}{NZ_{\mathrm{DBB}} + Z_{\mathrm{pri}}} \approx \frac{1}{N+1}. \tag{15}$$

Based on the above-mentioned analysis, the signal attenuation of the DBB coupling circuit is comparable to that of the low-pass structure coupling circuit, with the added benefit of noise suppression. Therefore, this method is well-suited for the impulsive noise environment of the proposed system. The following section presents a more detailed analysis of the DBB coupling channel, with a particular focus on noise analysis.

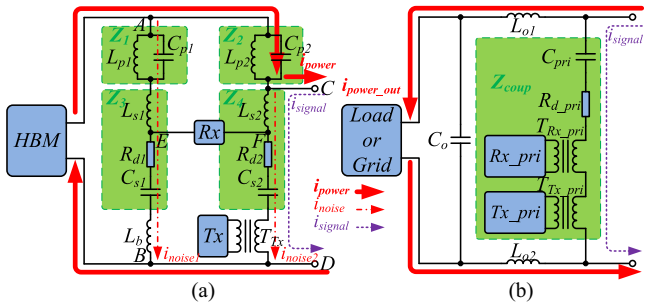

Fig. 7. Coupling scheme topology structure. (a) Secondary node (*S*_node *n; n* = *12,3,* . . . ,*N*) DBB coupling circuit. (b) Primary node (*P*_node) coupling circuit.

IV. Communication System Analysis and Implementation

The previous section compared balanced and unbalanced coupling methods, demonstrating that DBB coupling effectively suppresses noise as expected. In this section, a detailed analysis of the proposed system is conducted with respect to the channel, modulation and demodulation, and coupling loss.

The detailed design of the DBB coupling circuit is illustrated in Fig. 7(a). Based on the previous analysis of the DBB, the *LC* parallel resonant networks Z_1 and Z_2 are employed to enhance the amplitude of the received communication signal. In addition, the *LC* series resonant networks Z_3 and Z_4 are designed to have resonant points matching the communication frequency. The modulated data signal is coupled from the transmitter *Tx* through the coupling transformer T_{Tx} to the power line via the port CD. The communication signal is acquired on C_{s2}. To improve the integrity of the received signal *Rx*, damping resistors R_{d1} and R_{d2} are used to adjust the *Q* factor of the resonant network for bandwidth tuning.

The inductance L_b corresponds to the leakage inductance of the coupling transformer T_{Tx}, which helps maintain impedance balance. These two inductances should be designed to be sufficiently small to avoid affecting the resonant point of Z_4. Therefore, they are neglected in the following analysis for simplicity.

In the primary node, as shown in Fig. 7(b), the capacitor C_{pri}, the damping resistor R_{d_pri}, the receiving transformer T_{Rx_pri}, and the transmitting transformer T_{Tx_pri} are connected in series. L_{Rx_pri} is the magnetizing inductance of T_{Rx_pri}. Together, L_{Rx_pri}, R_{d_pri}, and C_{pri} form a series resonance network with its resonance point set at the communication frequency, creating a low impedance Z_{coup} for communication signals. The leakage inductance of T_{Tx_pri} should be designed to be minimal to prevent interference with the resonance of Z_{coup}, and is ignored in subsequent analysis. A symmetrical LPF comprising two inductors L_{o1}, L_{o2} ($L_{o1} = L_{\mathrm{o2}} = L_{\mathrm{o}}$) and a capacitor C_o is incorporated in the primary node to act as a power filter.

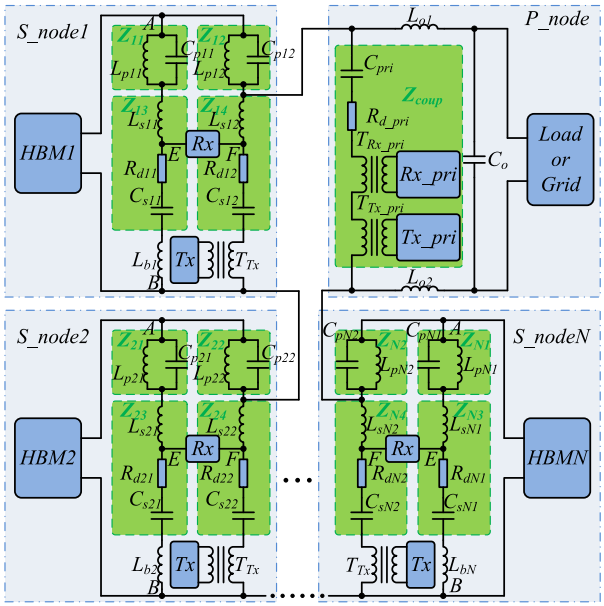

Fig. 8. Scheme structure of PLC system.

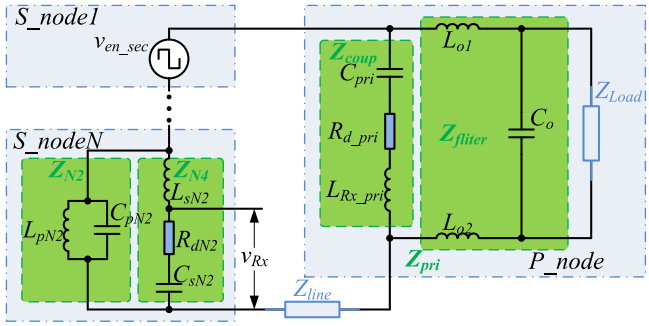

Fig. 9. Noise signal equivalent circuit based on DBB coupling scheme.

A complete PLC system with the DBB coupling structure is depicted in Fig. 8. This section aims to analyze the communication system and draw key conclusions at the system level.

A. Equivalent Circuit Analysis of Noise Channel

For noise analysis, the noise on the channel can be modeled as a centralized noise source $v_{\text{en·sec}}$, as shown in Fig. 9. The transfer function from the original noise source v_{HB1} to the equivalent noise source can be expressed as

$$H_{\text{en\_sec}}(s) = \frac{v_{\text{en\_sec}}}{v_{\text{HB1}}} = \frac{\frac{Z_4(s)Z_{\text{out}}(s)}{Z_4(s)+Z_{\text{out}}(s)}}{Z_2(s) + \frac{Z_4(s)Z_{\text{out}}(s)}{Z_4(s)+Z_{\text{out}}(s)}} \tag{16}$$

where Z_{out} is the external impedance, and can be expressed as

$$Z_{\text{out}}(s) = (N-1)\, Z_{\text{oth\_sec}}(s) + Z_{\text{pri}}(s) + Z_{\text{line}}(s). \tag{17}$$

The equivalent impedance of the cascaded line Z_{line} can be modeled using a short transmission line approximation [33], Z_{line} can be expressed as

$$Z_{\text{line}}(s) = N(R_{\text{line}} + sL_{\text{line}}) \tag{18}$$

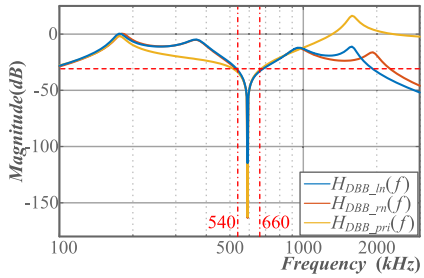

Fig. 10. Gain of the noise at the receiver of the primary node and secondary nodes.

where N is the number of secondary nodes.

The impedance of the other secondary nodes (S_node*n*; $n = 2,3,\ldots,N$), $Z_{\text{oth·sec}}$ can be expressed as

$$Z_{\text{oth\_sec}}(s) = \frac{Z_2(s)\, Z_4(s)}{Z_2(s) + Z_4(s)}. \tag{19}$$

The impedance of the primary node can be expressed as

$$Z_{\text{pri}}(s) = \frac{Z_{\text{coup}}(s)\, Z_{\text{pf}}(s)}{Z_{\text{coup}}(s) + Z_{\text{pf}}(s)}. \tag{20}$$

The transfer function of the local noise channel, $H_{\text{DBB·ln}}(s)$ is

$$H_{\text{DBB\_ln}}(s) = H_{\text{en\_sec}}(s)\frac{R_d + \frac{1}{sC_{s1}}}{Z_4(s)} - \frac{R_d + \frac{1}{sC_{s1}}}{Z_2(s) + Z_4(s)}. \tag{21}$$

The transfer function of the remote noise channel, $H_{\text{DBB·rn}}(s)$ is

$$H_{\text{DBB\_rn}}(s) = H_{\text{en\_sec}}(s)\frac{Z_{\text{oth\_s}}(s)}{Z_{\text{out}}(s)}. \tag{22}$$

The transfer function of the noise at the $P_$node, $H_{\text{DBB·pri}}(s)$ is

$$H_{\text{DBB\_pri}}(s) = H_{\text{en\_sec}}(s)\frac{Z_{\text{pri}}(s)}{Z_{\text{out}}(s)}. \tag{23}$$

Fig. 10 illustrates the amplitude-frequency characteristics of $H_{\text{DBB·ln}}(s)$, $H_{\text{DBB·rn}}(s)$, and $H_{\text{DBB·pri}}(s)$, all of which exhibit suppression of over 30 dB for in-band noise. When the data symbol aligns with either the rising or falling edge of the PWM wave produced by the local HBM, the local noise power can be expressed as

$$\begin{aligned} P_{\text{ln\_imp}} &= \frac{1}{T_{\text{Bit}}}\int_0^{\infty} |V_{\text{HB\_}l}(s)\, H_{\text{BPF}}(s)\, H_{\text{DBB\_ln}}(s)|^2 ds \\ &= \frac{1}{T_{\text{Bit}}}\int_0^{T_{\text{Bit}}} \left|\mathcal{L}^{-1}\left[V_{\text{HB\_Bit}}(s)\, H_{\text{BPF}}(s)\right] * H_{\text{DBB\_ln}}(f_0)\right|^2 dt \\ &= \frac{1}{T_{\text{Bit}}}\int_0^{T_{\text{Bit}}} \left|A\cdot e^{-\frac{\omega_0}{2Q}t}\cdot\sin(k\omega_0 t)\right|^2 * |H_{\text{DBB\_ln}}(f_0)|^2 dt \end{aligned} \tag{24}$$

where T_{Bit} is the period of one bit. Similarly, the remote noise power can be expressed as

$$P_{\text{rn\_imp}} = \frac{1}{T_{\text{Bit}}}\int_0^{T_{\text{Bit}}} \left|A\cdot e^{-\frac{\omega_0}{2Q}t}\cdot\sin(k\omega_0 t)\right|^2$$

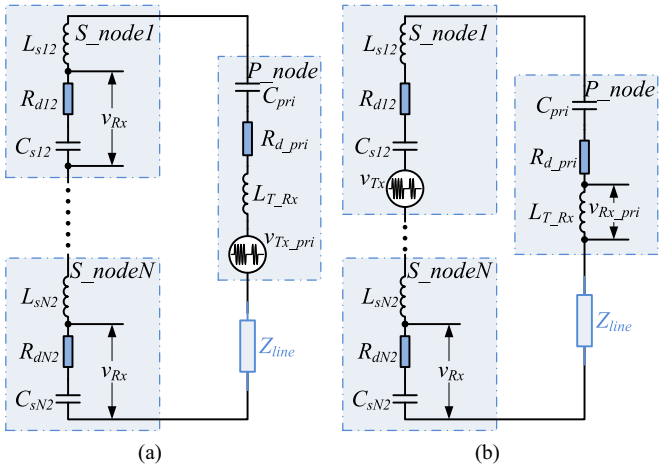

Fig. 11. Equivalent circuit of communication signal based on DBB coupling scheme. (a) Primary node as the transmitter. (b) One of the secondary nodes as the transmitter.

$$* \left|H_{\mathrm{DBB\_rn}}\left(f_0\right)\right|^2 dt. \tag{25}$$

The data symbol is modulated using OOK, resulting in a signal power denoted as

$$P_s = \frac{1}{2T_{\mathrm{Bit}}} \int_0^{T_{\mathrm{Bit}}} \left|A_s \cdot \sin\left(\omega_0 t\right)\right|^2 dt \tag{26}$$

where A_s is the amplitude of the signal. Considering the worst-case scenario where both local and remote noise occur simultaneously within a single symbol period, the worst SNR can be represented as

$$\mathrm{SNR}_{\mathrm{DBB}} = 10\log\left[\frac{P_s}{P_{\mathrm{rn\_imp}} + P_{\mathrm{ln\_imp}}}\right]. \tag{27}$$

The parameters associated with the communication system are listed in Table II. In the proposed system, $\mathrm{SNR}_{\mathrm{DBB}} = 22.19$ dB. Similarly, the SNR under conventional unbalanced coupling can be calculated as $\mathrm{SNR}_{\mathrm{unbal}}$ 5.24 dB. A comparison reveals a significant improvement in the SNR. This high value indicates that the PWM noise generated by HBMs will not substantially affect communication. As a result, conventional modulation and demodulation strategies can be applied.

B. Equivalent Circuit Analysis of Data Communication

In the PLC system, a series-connected RLC circuit is employed for signal decoupling. When the primary node transmits data signal to secondary nodes, the communication system is modeled as shown in Fig. 11(a). The transfer function from the primary node to the receivers at the secondary nodes can be expressed as

$$H_{\mathrm{DBB\_ps}}\left(s\right) = \frac{v_{\mathrm{Rx}}\left(s\right)}{v_{\mathrm{Tx\_pri}}\left(s\right)} = \frac{b_0 s + b_1}{a_0 s^2 + a_1 s + a_2} \tag{28}$$

where

$$a_0 = \mathrm{NC}_{\mathrm{pri}} C_{s2}\left(L_{s2} + L_{\mathrm{line}} + \frac{L_{\mathrm{Rx\_pri}}}{N}\right)$$

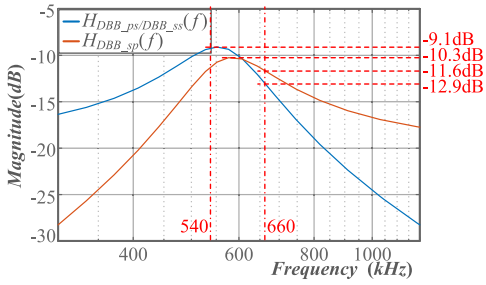

Fig. 12. Gain curves of signals at primary and secondary nodes.

$$a_1 = \mathrm{NC}_{\mathrm{pri}} C_{s2}\left(R_{\mathrm{line}} + R_{d2} + \frac{R_{d\_\mathrm{pri}}}{N}\right)$$

$$a_2 = \mathrm{NC}_{\mathrm{pri}} + C_{s2}$$

$$b_0 = R_d C_{\mathrm{pri}} C_{s2}$$

$$b_1 = C_{\mathrm{pri}}.$$

When a secondary node (*S*_node1) transmits data signals, while both the primary and the other secondary nodes (*S*_node*n; n* = *2,3,* . . . ,*N*) receive these signals. The system channel model is shown in Fig. 11(b). The transfer function from one secondary node to another, $H_{\mathrm{DBB\_ss}}(s) = H_{\mathrm{DBB\_ps}}(s)$. The transfer function from a secondary node to the primary node $H_{\mathrm{DBB\_sp}}(s)$ can be expressed as

$$H_{\mathrm{DBB\_sp}}\left(s\right) = \frac{d_0 s^2}{c_0 s^2 + c_1 s + c_2} \tag{29}$$

where

$$c_0 = \mathrm{NC}_{\mathrm{pri}} C_{s2}\left(L_{s2} + L_{\mathrm{line}} + \frac{L_{\mathrm{Rx\_pri}}}{N}\right)$$

$$c_1 = \mathrm{NC}_{\mathrm{pri}} C_{s2}\left(R_{\mathrm{line}} + R_{d2} + \frac{R_{d\_\mathrm{pri}}}{N}\right)$$

$$c_2 = \mathrm{NC}_{\mathrm{pri}} + C_{s2}$$

$$d_0 = L_{\mathrm{Rx\_pri}}\, C_{\mathrm{pri}} C_{s2}.$$

The amplitude-frequency characteristics of transfer functions $H_{\mathrm{DBB\_ps}}(s)$, $H_{\mathrm{DBB\_ss}}(s)$, and $H_{\mathrm{DBB\_sp}}(s)$ are shown in Fig. 12. Since the channel passband is typically defined as the range where the gain drops by 3 dB from its peak value [34]. Fig. 12 shows that $H_{\mathrm{DBB\_ps}}(s)$ and $H_{\mathrm{DBB\_ss}}(s)$ reach a peak of -9.1 dB and fall to -12.9 dB at 660 kHz. Similarly, $H_{\mathrm{DBB\_sp}}(s)$ peaks at -10.3 dB and drops to -11.6 dB at 660 kHz. Therefore, both can be considered to fall within this passband range. The bandwidth of the overall channel (from transmitter to receiver) satisfies the requirements for data recognition.

C. Design of PLC Transmitter and Receiver

In the proposed system, ensuring reliable, high-data-rate, and low-latency communication is essential. Moreover, since the PLC communication program is integrated with power control and implemented by a microcontroller unit (MCU), a simple modulation method is preferred. Hence, OOK, the simplest

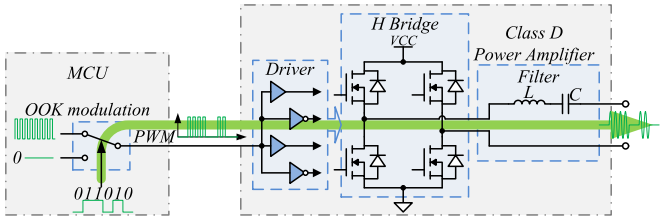

Fig. 13. Signal modulation control block diagram.

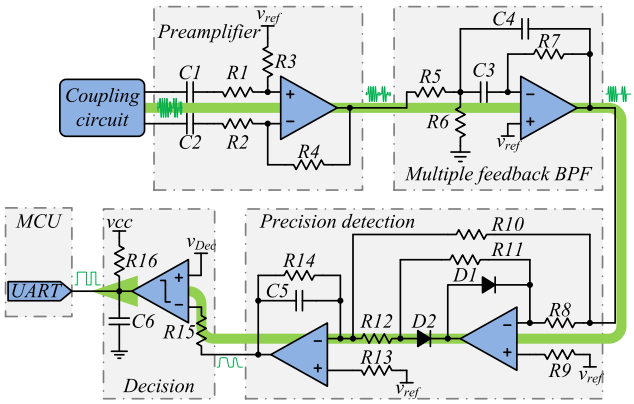

Fig. 14. Signal demodulation structure diagram.

ASK method, is chosen for its straightforward modulation and demodulation implementation.

On the transmitter side, data is modulated onto a square wave carrier, with control provided by software. As shown in Fig. 13, the MCU's PWM module generates a square wave with frequency f_0 and a duty cycle of 0.5, which is switched ON and OFF by software based on the transmitted data bits. The modulated square wave is then fed into a Class D power amplifier, which injects the modulated signal into the cable through a coupling circuit.

On the receiver side, an envelope detection circuit with a filter is employed, as shown in Fig. 14. The filter adopts the multiple feedback (MFB) band-pass topology. The received signal is first filtered to remove noise outside the frequency band. The filtered signal is subsequently rectified into a dc level to recover the baseband data. To facilitate data processing, the data frame is designed to be compatible with the universal asynchronous receiver/transmitter (UART), with each byte containing a start bit and a stop bit, enabling the data to be received directly by the UART.

D. PLC-Based Control Architecture and Power Loss Analysis

The system control is implemented through PLC, as shown in Fig. 15. The controller of the primary node performs phase-locked loop synchronization with the grid voltage $v_{g\cdot Sa}$ and transmits the results, including grid frequency f_g, grid voltage amplitude V_{gM}, and zero-crossing points (ZCPs), to all secondary nodes via the downlink frame. The controller in each secondary node performs dc voltage control and grid current control for the HBM, and generates the corresponding switching

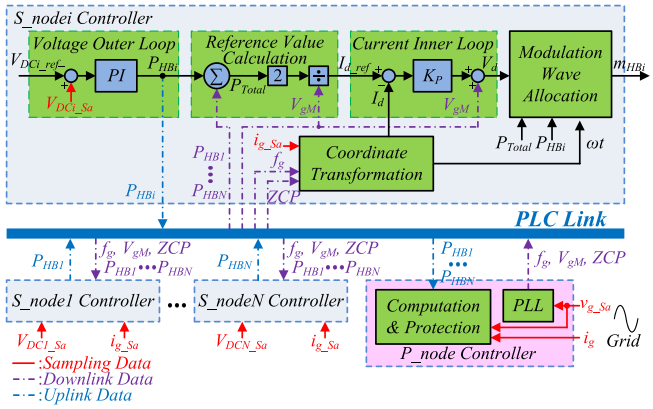

Fig. 15. Control block diagram of system.

drive signals. Meanwhile, it sends the power of each HBM P_{HBi} to the PLC link via the uplink frame.

As an example, the controller of the ith HBM S_node$i$, regulates the dc-side voltage $V_{\mathrm{DC}\,i}$ through a voltage outer loop based on the dc reference $V_{\mathrm{DC}\,i\cdot\mathrm{ref}}$ and calculates the actual power of the corresponding HBM $P_{\mathrm{HB}\,i}$. The S_node$i$ controller also receives the power of the remaining HBMs $P_{\mathrm{HB}\,j}$ ($j = 1,2,\ldots,N; j{\neq}i$), grid frequency f_g, grid voltage amplitude V_{gM}, and ZCPs from other controllers via communication.

Based on the grid frequency f_g, ZCP and the sampled grid current $i_{g\cdot Sa}$, the grid angle ωt is reconstructed, and the corresponding active feedback current I_d, reactive feedback current I_q are calculated. The active feedback current I_d is used for the current inner loop control. The active current reference $I_{d\cdot\mathrm{ref}}$ is generated by the reference calculation module, which computes $I_{d\cdot\mathrm{ref}}$ based on the sum of the power from all HBMs $P_{\mathrm{HB}j}$ ($j = 1,2,\ldots,N; j{\neq}i$), together with the grid voltage magnitude V_{gM}.

Since the system is designed to achieve unity power factor control, the reference value of the reactive current $I_{q\cdot\mathrm{ref}}$ is set to zero, i.e., $I_{q\cdot\mathrm{ref}} = 0$. The current inner loop employs a proportional controller, with the controller output being the active reference voltage amplitude V_d, from which the total modulation voltage amplitude can be further calculated. Finally, according to the proportional relationship between the ac-side output voltage amplitude of the HBM and the transmitted power, the modulation wave of the ith HBM $m_{\mathrm{HB}\,i}$ is calculated.

Compared to the traditional cascaded multilevel system, the proposed system introduces a DBB coupling scheme. Therefore, it is essential to analyze the impact of DBB integration on the overall system efficiency. Loss analysis generally focuses on the power frequency, the DBB coupling circuit can be equivalently simplified to the circuit shown in Fig. 16. Based on the power frequency characteristics of each component in Fig. 16, the impedance of L_{p2} is significantly smaller than the impedance of C_{p2} and Z_4. Consequently, only the loss on L_{p2} needs to be considered in the loss analysis introduced by DBB, as the losses from other components are negligible. In addition, the power frequency current flowing through L_{p2} can be equivalently represented by the power frequency current i_{power} in the cascaded loop to simplify the calculation.

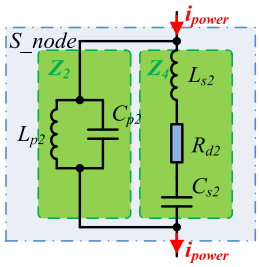

Fig. 16. Equivalent simplified circuit of *S*_node based on power frequency.

TABLE I
PARAMETERS OF PRIMARY AND SECONDARY NODE COUPLING CIRCUIT

Symbol	Parameter	value
L_{p1}, L_{p2}	Inductance in networks Z_1 and Z_2	$3.3\,\mu H$
L_{s1}, L_{s2}	Inductance in networks Z_3 and Z_4	$3.3\,\mu H$
L_{Rx_pri}	The magnetizing inductance of the primary node receiving transformer T_{Rx_pri}	$3.3\,\mu H$
L_{o1}, L_{o2}	Power circuit output filter inductance	$650\,\mu H$
L_{line}	Equivalent inductance per unit length of line	$300\,nH$
C_{p1}, C_{p2}	Capacitance in networks Z_1 and Z_2	$22\,nF$
C_{s1}, C_{s2}	Capacitance in networks Z_3 and Z_4	$22\,nF$
C_{pri}	Primary node coupling capacitance	$22\,nF$
C_o	Power circuit output filter Capacitance	$55\,\mu F$
R_{d1}, R_{d2}	Damping resistor of the secondary node	$4.3\,\Omega$
R_{d_pri}	Damping resistor of the primary node	$4.3\,\Omega$
R_{line}	Equivalent resistance per unit length of line	$10\,m\Omega$
R_{Lp2}	The resistance of the inductor L_{p2}	$2\,m\Omega$
N	Number of nodes	8

To ensure the balance of the DBB, the inductor L_{p2} is designed to be nonsaturable. As a result, the magnetic losses can be neglected, and only the copper losses are considered. Therefore, the loss of the DBB can be expressed as

$$\text{Loss}_{\text{DBB}} = {i_{\text{power}}}^2 R_{Lp2} \tag{30}$$

where R_{Lp2} represents the resistance of the inductor L_{p2}. The loss introduced by DBB can be calculated as $\text{Loss}_{\text{DBB}} = 193$ mW. Compared to the total system power of 1.6 kW, the losses introduced by all DBBs account for only 0.096%.

V. EXPERIMENTAL VERIFICATION

A. Experimental Setup

A prototype system consisting of a primary node and eight secondary nodes was designed to validate the proposed method. The circuit configuration of the system is depicted in Fig. 8, with a total power capacity of 1.6 kW. Additional system parameters are provided in Table I. The photographs of the system and the secondary node PCB board are presented in Fig. 17(a) and (b).

B. Communication Performance and Process

Compared to traditional inductive coupling and DBB coupling, the pure noise output of BPF in PLC receiver is shown in Fig. 18. From Fig. 18(b), the peak-to-peak noise value under DBB coupling is only 390 $\text{mV}_{P\text{-}P}$, which is significantly lower compared to the traditional inductive coupling value of more

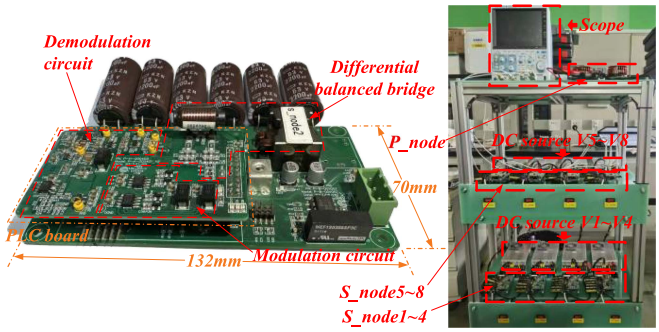

Fig. 17. Photographs of the experimental system. (a) Secondary node PCB board. (b) Prototype system.

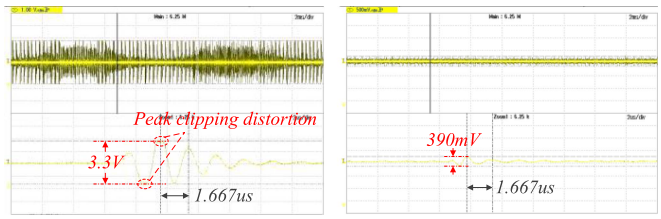

Fig. 18. Comparison of receiver noise between traditional inductive coupling and DBB coupling. (a) Receiver noise under traditional inductive coupling. (b) Receiver noise under DBB coupling.

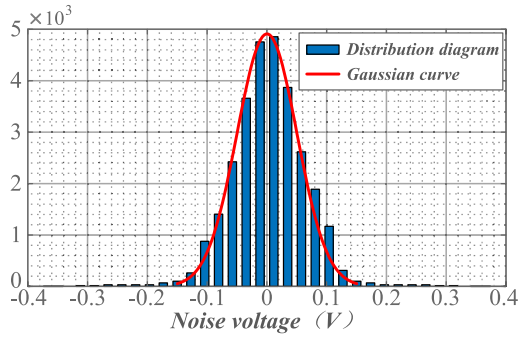

Fig. 19. Noise distribution diagram and Gaussian density function curve.

than 3.3 $\text{V}_{P\text{-}P}$ in Fig. 18(a). Impulse noise has been substantially reduced, and the total noise exhibits the characteristics of Gaussian noise. The probability distribution of noise, shown in Fig. 19, follows a Gaussian distribution, with the density function:

$$f_N(n) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(n-\mu)^2}{2\sigma^2}} \tag{31}$$

where N is a random variable, n represents the possible value of N, μ is the mean, and σ^2 is the variance of the sample, which can be regarded as the average power of noise. Therefore, the SNR at the EF differential point can be expressed as [21]

$$\text{SNR} = 10lg\left(\frac{{A_s}^2}{2\sigma^2}\right) \tag{32}$$

where A_s is the signal amplitude after passing through the BPF. The system's bit error rate (BER) for the envelope demodulation

TABLE II
PARAMETERS OF COMMUNICATION SYSTEM FOR SIMULATION

Symbol	Parameter	Value
f_0	Frequency of carrier wave	*600 kHz*
T_{bit}	Period of 1 bit	*16.67 μs*
R_{bit}	Baud rate	*60 kbps*
BW	Bandwidth	*120 kHz*
σ^2	Average noise power	*0.002 W*
A_s	Amplitude of signal after BPF	*1.65 V*
SNR	Signal-to-Noise Ratio	*26.391 dB*
BER	Bit Error Rate	2.52×10^{-48}

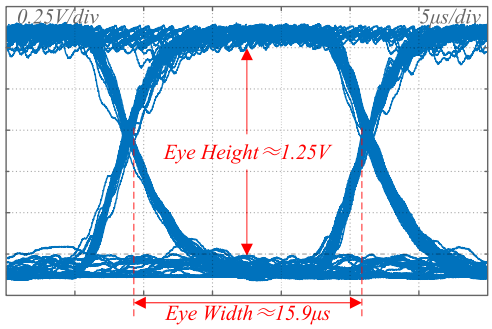

Fig. 20. Eye diagram of the prototype system.

method can be expressed as

$$\mathrm{BER} = \frac{1}{2} e^{-\frac{A_s^2}{8\sigma^2}}. \tag{33}$$

The parameters associated with the communication system are listed in Table II. From the results, it can be observed that the SNR meets the requirements for OOK usage, and the BER is also very low, fully satisfying the system's performance requirements.

On the other hand, the eye diagram is shown in Fig. 20. It is clear that the eye opening is wide and distinct, the transitions between symbols are smooth, with no visible inter-symbol interference. This pattern typically suggests that the signal has not been severely distorted or interfered with during transmission. The crossing points are close to the zero-voltage level, which is ideal for accurate symbol decision-making. The receiver can clearly distinguish the symbol states, where eye height is approximately 1.25 V, and eye width is about 15.9 μs. Compared to the envelope amplitude and symbol period, this indicates that the system has a higher noise margin and greater timing tolerance. As a result, this eye diagram indicates that the signal quality is good, with the system showing strong tolerance to noise, interference, and timing errors. The error rate is low, and the communication performance is stable.

The OOK signal pair and communication delay are depicted in Fig. 21. In Fig. 21(a), Channel 1 (CH1) represents the restored OOK baseband signal at the UART port of the receiver MCU; Channel 2 (CH2) outputs the driving signal of the modulated wave from the PWM port of the transmitter MCU. The upper part of Fig. 21(a) provides a macroscopic comparison between the transmitted OOK signal and the restored OOK bit signal, it

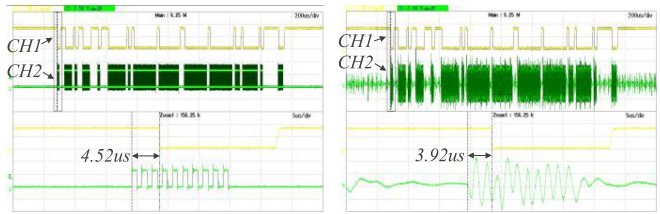

Fig. 21. OOK signal pair and communication delay. (a) OOK signal pair and total communication delay. (b) Demodulation delay.

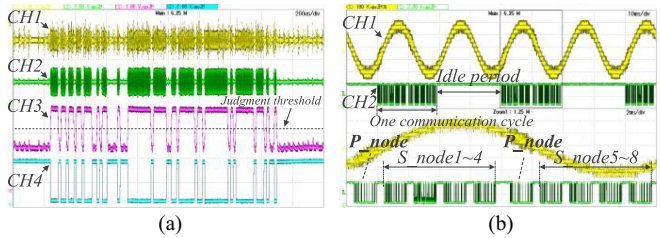

Fig. 22. Process of communication. (a) Demodulation process of one data packet. (b) Communication sequential logic.

can be seen that the received OOK signal exhibits minimal distortion, and the bit signal is restored accurately, confirming the robustness of our proposed system. The lower part of Fig. 21(a) presents a detailed comparison of these two waveforms at the starting point, where the total communication delay is observed to be 4.52 μs. In Fig. 21(b), CH1 again displays the restored baseband signal, CH2 represents the waveform output by the receiver DBB. The results confirm that demodulation is performed effectively and remains completely immune to noise, with a measured demodulation delay of 3.92 μs. This delay is very small and constant, as demodulation is implemented by a precision detection circuit rather than digital demodulation.

Fig. 22(a) illustrates the complete demodulation process of a data packet, with CH1 to CH4 representing the DBB output of the receiver, the BPF output of the receiver, the precision detection circuit output of the receiver, and the UART port waveform of the receiver MCU, respectively. Comparing CH1 and CH2, the out-of-band noise is significantly attenuated. CH3 represents the waveform after precise detection. A substantial margin exists between the noise and the decision threshold (gray dotted line in the figure). Consequently, the noise does not affect the demodulation process. Finally, CH4 confirms that the data demodulation is correct.

Fig. 22(b) reflects the communication cycle of the system, with the lower part providing a detailed view of a single communication cycle from the upper part. Here, CH1 represents the waveform output by the cascade connection of eight H-bridges, and CH2 shows the waveform of the UART port at the receiver of the secondary node. As evident from the lower part of Fig. 22(b), the waveform of eight H-bridge cascaded outputs is decent, and the system still has room for expansion of at least eight nodes while maintaining the same communication rate. The expansion space of the system will be larger when the communication rate of the system is increased.

TABLE III
COMPARISON OF PERFORMANCE WITH EXISTING METHODS

Technique	Application scenario	Environment noise	Data-Rate	Interference immunity	Latency	Frequency band
single-carrier TPC [20]	*Communication between Series-connected PV modules*	*Low, dominated by Gaussian noise*	*2 kbps*	*Low, without additional processing*	*High, ms-level latency (estimated from experimental waveforms)*	*8 kHz–12 kHz*
Spread Spectrum TPC [21], [22]	*Communication between Parallel-configured power supply*	*Moderate, background and impulse noise*	*6.67 kbps* [21]	*Moderate, due to signal power spreading*	*Moderate, hundreds-μs-level, due to spreading /de-spreading* [21]	*0 Hz–200 kHz* [21]
OFDM TPC [23], [24]	*Communication between parallel-configured power supply*	*Moderate, background and impulse noise*	*9.6 kbps* [23]	*Moderate, due to orthogonal multicarrier modulation and cyclic prefix*	*High, due to Synchronization, and FFT/IFFT process*	*2.18–8.83 kHz* [23]
Standardized PLC schemes [35], [36], [37]	*Communication between the devices connected to the main AC grid*	*High, non-stationary power-line noise*	*≤33.4 kbps* [35] *≤128 kbps* [36] *≤500 kbps* [37]	*High, due to robust MAC hierarchy and routing protocol*	*High, ms-level latency (caused by complex MAC and routing)*	*10–450 kHz* [35] *42–89 kHz+154–404 kHz* [36] *≤500 kHz* [37]
PLC in PV Monitoring [16]	*Communication between Series-connected PV modules*	*Low, minimal background noise*	*10 kbps*	*Low, without additional processing*	*Likely low, enabled by envelope detection-based demodulation*	*190 kHz–210 kHz*
TPC in CHB [26],[27], [28]	*Communication between series-connected power modules in a cascaded multilevel converter*	*High, substantial impulse noise*	*<1 kbps*	*Moderate, with complex encoding schemes*	*Likely Moderate, due to complex encoding/decoding algorithms*	*39 kHz–41 kHz*
The proposed method	*Communication between series-connected power modules in a cascaded multilevel converter*	*High, substantial impulse noise*	***60 kbps***	***High**, with DBB coupling circuit*	***Low, μs-level latency** (enabled by envelope detection-based demodulation)*	*540 kHz–660 kHz*

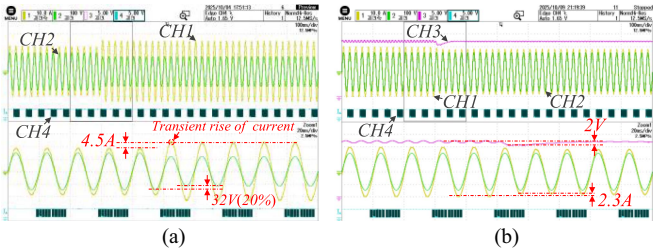

Fig. 23. System stability under PLC communication. (a) Grid voltage sag. (b) DC-side voltage fluctuation.

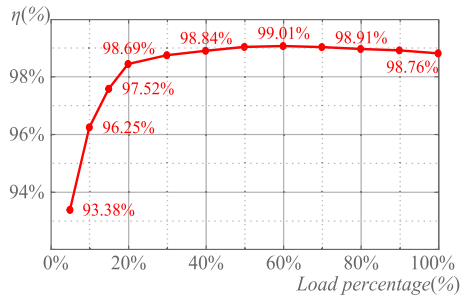

Fig. 24. Efficiency-load curve.

C. System Stability and Efficiency

System stability under PLC communication is illustrated in Fig. 23. In Fig. 23(a), CH1, CH2, and CH4 represent the grid-connected current, grid voltage, and the UART port waveform at the receiver of the secondary node, respectively. Upon a 20% grid voltage sag, the grid-connected current exhibits an instantaneous increase and stabilizes after one fundamental cycle, with the steady-state amplitude 4.5 A higher than pre-sag conditions. This response confirms the system's robustness to grid disturbances. The waveforms of CH1, CH2, and CH4 in Fig. 23(b) are identical to those in Fig. 23(a), with CH3 additionally depicting the dc-side voltage of the HBM. Under a 2V drop in the dc-side voltage, the grid-connected current undergoes one-cycle adjustment before stabilizing, resulting in a steady-state amplitude 2.3 A lower than pre-drop conditions. This demonstrates the system's resilience to dc-side disturbances.

The efficiency of the system's power conversion is calculated by multiplying the efficiencies of the *P*_node and a *S*_node, which are simultaneously measured by the power analyzer. The efficiency versus load curve is depicted in Fig. 24, from which it can be observed that the converter achieves a peak efficiency of 99.01% at 60% load conditions. For the majority of the load range (20% –100%), the efficiency remains above 98%. The efficiency of this experimental prototype is largely in line with that of the single-phase cascaded H-bridge, and the impact of the DBB on efficiency can be considered negligible.

D. Comparison With Existing Methods

As summarized in Table III, single-carrier without additional signal processing solution offers low implementation complexity but exhibits limited immunity to interference. Spread spectrum and OFDM TPC approaches enhance noise tolerance but suffer from low throughput and latency constraints. Standardized PLC schemes (G3-PLC, PRIME, IEEE 1901.2) achieve improved robustness against nonstationary power line noise, yet their reliance on synchronization, FFT/IFFT operations, and hierarchical MAC protocols leads to considerable latency.

In cascaded multilevel topologies, the power distribution paths aggravate impulsive noise, further restricting the achievable data rates and increasing latency when conventional TPC methods or standardized PLC schemes are employed. By contrast, the proposed scheme exploits a DBB coupling circuit in combination with envelope-detection demodulation, which enables a substantially higher data rate (60 kbps), ultralow latency (<5 μs), and strong interference resilience within the 540–660 kHz band. These attributes highlight its suitability for distributed control applications in high-performance power electronic systems.

VI. Conclusion

This article proposes a novel PLC scheme applied to cascaded multilevel topology, leveraging the balanced characteristics and LPF behavior of DBB bridge legs to suppress both local and remote high-frequency noise. A comprehensive system-level communication model is developed, incorporating OOK modulation, Class D amplification, and envelope-detection-based UART reception to achieve streamlined, low-latency communication. Experimental results on eight cascaded HBMs demonstrate 60 kbps transmission with less than 5 μs latency, validating the scalability of the system in terms of both module count and data rate.

This work presents a high-data-rate PLC technique with robust anti-interference capability for cascaded multilevel topologies and demonstrates its effectiveness in controlling CHB systems. This advancement addresses critical challenges in communication within power electronic equipment, offering significant potential to reduce the cost and enhance the reliability of CHB-based systems in renewable energy applications. Future research will focus on the mathematical stability analysis of distributed control achieved through communication, in order to assess the impact of data rate and latency on the implementation of distributed control in CHB systems, and to determine the optimal ranges of both factors.

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