Design Methodology of Sizing Power MOSFETs and Optimizing Phase Counts in Multiphase DC–DC Converter for Maximizing Power Efficiency

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***Abstract*—This article presents a design methodology of sizing power MOSFET switches with optimized phase counts to enhance the efficiency profile over a wide load range in multiphase dc–dc converters. In the conventional approach, identical sizes of all phases exhibit a large variation in power efficiency, especially over a wide load range. In the proposed method, power efficiency is improved in the entire load range by adopting appropriate sizing of the power MOSFETs in each phase. It also precisely determines the number of active phases and partitions the entire load range into sub-ranges. To further reduce the design effort, a discriminant-assisted process is introduced to quickly verify the feasibility of input specifications by evaluating the sign (positive or negative) of the discriminant. This confines the search space for the minimum effective equivalent resistance of the active phases while significantly reducing the design iteration time as required in the conventional trial-and-error approach. Various design scenarios are considered to determine the power MOSFET sizing using the proposed methodology. Among them, a variable baseline in different load sub-ranges maximizes the power efficiency with an appropriate number of phase counts. To experimentally validate the proposed methodology, a 3-phase current-mode dc–dc converter is implemented in a standard 180 nm CMOS technology with optimized power MOSFET switches. The converter operates at a switching frequency of 20 MHz, an input voltage V_{IN} of 2.7–3.3 V, and an output voltage V_O of 1.2 V. The measured result shows a flat efficiency profile with $\sim$1% variation in the full load current range of 200 mA to 1.4 A.**

***Index Terms*—Efficiency optimization, multiphase dc–dc converters, phase count optimization, power efficiency, power MOSFET sizing.**

NOMENCLATURE

List of variables used:

$$\alpha_{\text{PC}(i)} = \frac{\left[Q_{\text{PC}(i)} \cdot R_{N,\text{PC}(i)} + \frac{S_{\text{PC}(i)}}{R_{N,\text{PC}(i)} - R_{\text{INT},N,\text{PC}(i)}} + T_{\text{PC}(i)} - R_{\text{INT},P,\text{PC}(i)} \cdot P_{\text{PC}(i)}\right]}{P_{\text{PC}(i)}}$$

$$\alpha_{1,\text{PC}(i)} = \frac{T_{\text{PC}(i)}}{P_{\text{PC}(i)}} - R_{\text{INT},P,\text{PC}(i)}$$

$$\beta_{\text{PC}(i)} = \frac{R_{\text{PC}(i)} - Q_{\text{PC}(i)} \cdot R_{\text{INT},P,\text{PC}(i)} \cdot R_{N,\text{PC}(i)}}{P_{\text{PC}(i)}} - \frac{\frac{S_{\text{PC}(i)} \cdot R_{\text{INT},P,\text{PC}(i)}}{R_{N,\text{PC}(i)} - R_{\text{INT},N,\text{PC}(i)}}}{P_{\text{PC}(i)}} - \frac{R_{\text{INT},P,\text{PC}(i)} \cdot T_{\text{PC}(i)}}{P_{\text{PC}(i)}}$$

$$\beta_{1,\text{PC}(i)} = \frac{R_{\text{PC}(i)} - R_{\text{INT},P,\text{PC}(i)} \cdot T_{\text{PC}(i)}}{P_{\text{PC}(i)}}$$

$$\gamma_{\text{PC}(i)} = \left[Q_{\text{PC}(i)} \cdot R_{N,\text{PC}(i)} + \frac{S_{\text{PC}(i)}}{R_{N,\text{PC}(i)} - R_{\text{INT},N,\text{PC}(i)}}\right] \cdot \frac{1}{P_{\text{PC}(i)}}$$

$\Delta I_O = \frac{D \cdot (V_{\text{IN}} - V_{\text{OUT}})}{L \cdot f_{\text{SW}}}$: Peak-to-peak inductor ripple current.

η_{MIN}: Minimum baseline efficiency.

$\eta_{\text{MIN,PC}(i)}$: Minimum baseline efficiency for phase count $= i$, where $(i \in \mathbb{Z}^+)$.

$\lambda_{P,\text{PC}(i)} = \left(\frac{\frac{1}{\mu_P \cdot C_{\text{ox}} \cdot (V_{\text{IN}} - |V_{\text{th},P}|)}}{L_{P,\text{MIN}}}\right)$; $\lambda_{N,\text{PC}(i)} = \left(\frac{\frac{1}{\mu_N \cdot C_{\text{ox}} \cdot (V_{\text{IN}} - |V_{\text{th},N}|)}}{L_{N,\text{MIN}}}\right)$

μ_P and μ_N: mobility of holes and electrons, respectively.

τ : The tapering ratio inside the driver chain.

$A_{\text{PC}(i)} = T_F(\tau) \cdot V_{\text{IN}}^2 \cdot f_{\text{SW}}$

$b_{\text{PC}(i)} = \frac{V_O \cdot \{\eta_{\text{MIN,PC}(i)} - 1\} + \eta_{\text{MIN,PC}(i)} \cdot K \cdot f_{\text{SW}}}{\eta_{\text{MIN,PC}(i)}}$

$B_{\text{PC}(i)} = D \cdot \frac{\Delta I_O^2}{12}$

C_O & R_{ESR}: Output capacitor and its equivalent series resistance.

$C_{G,P,\text{PC}(i)}$ & $C_{G,N,\text{PC}(i)}$: Gate capacitance of power PMOS and NMOS switches, respectively, for phase count $= i$.

C_{ox}: Oxide gate capacitance per unit area.

$C_{\text{PC}(i)} = (1 - D) \cdot \frac{\Delta I_O^2}{12}$

D: Duty ratio.

$E_{\text{PC}(i)} = \frac{\Delta I_O^2}{12} \cdot (R_{\text{ESR}}) + V_{\text{IN}} \cdot I_Q$

f_{SW}: Switching frequency.

I_O: Load current.

$I_{O,\text{MIN}}$: Minimum load current.

$I_{O,\text{MAX}}$: Maximum load current.

$I_{O,\text{MIN,PC}(i)}$: Minimum load current for phase count $= i$.

$I_{O,\text{MAX,PC}(i)}$: Maximum load current for phase count $= i$.

I_Q: Controller quiescent current.

$K = (2.V_{\text{DI}}.t_{\text{DB}} + V_{\text{IN}}.t_{R/F})$

L & R_{DC}: Inductor and its direct current resistance.

PC(i): Phase count $= i$.

$P_{\text{PC}(i)} = D \cdot I_{O,\text{MIN,PC}(i)}^2 + B_{\text{PC}(i)}$

$P_{G,L,\text{PC}(i)}$: Total gate driving loss of a power MOSFET switch for phase count $= i$.

$P_{\text{DR},L,\text{PC}(i)}$: Total gate driver circuit loss to drive power MOSFET switches for phase count $= i$.

$P_{\text{TR},L,\text{PC}(i)}$: Total power MOSFET switching transition loss for phase count $= i$.

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$P_{\mathrm{DI},L,\mathrm{PC}(i)}$: Total power loss across diode for phase count $= i$.
$P_{\mathrm{CT},L,\mathrm{PC}(i)}$: Total power loss in the controller for phase count $= i$.
$Q_{\mathrm{PC}(i)} = (1-D)\cdot I^2_{O,\mathrm{MIN},\mathrm{PC}(i)} + C_{\mathrm{PC}(i)}$
$R_{\mathrm{PC}(i)} = A_{\mathrm{PC}(i)}\cdot\lambda_{P,\mathrm{PC}(i)}\cdot C_{\mathrm{ox}}\cdot L_{P,\mathrm{PC}(i)}$
$R_{N,\mathrm{OPT},\mathrm{PC}(i)}$: Optimized power NMOS switch resistance for phase count $= i$.
$R_{P,\mathrm{OPT},\mathrm{PC}(i)}$: Optimized power PMOS switch resistance for phase count $= i$.
$R_{\mathrm{CH},P,\mathrm{PC}(i)}$ & $R_{\mathrm{CH},N,\mathrm{PC}(i)}$ of power PMOS and NMOS switches channel resistance, respectively, for phase count $= i$.
$R_{\mathrm{INT},P(S),\mathrm{PC}(i)}$ & $R_{\mathrm{INT},P(D),\mathrm{PC}(i)}$: Power PMOS switch interconnect resistances on source and drain, respectively, for phase count $= i$.
$R_{\mathrm{INT},P,\mathrm{PC}(i)} = R_{\mathrm{INT},P(S),\mathrm{PC}(i)} + R_{\mathrm{INT},P(D),\mathrm{PC}(i)}$: Total interconnect resistances of the power PMOS switch for phase count $= i$.
$R_{P,\mathrm{PC}(i)} = R_{\mathrm{CH},P,\mathrm{PC}(i)} + R_{\mathrm{INT},P,\mathrm{PC}(i)}$: Total resistances of the PMOS side switch for phase count $= i$.
$R_{\mathrm{INT},N(S),\mathrm{PC}(i)}$ & $R_{\mathrm{INT},N(D),\mathrm{PC}(i)}$: Power NMOS switch interconnect resistances on source and drain, respectively, for phase count $= i$.
$R_{\mathrm{INT},N,\mathrm{PC}(i)} = R_{\mathrm{INT},N(S),\mathrm{PC}(i)} + R_{\mathrm{INT},N(D),\mathrm{PC}(i)}$: Total interconnect resistances of the power NMOS switch for phase count $= i$.
$R_{N,\mathrm{PC}(i)} = R_{\mathrm{CH},N,\mathrm{PC}(i)} + R_{\mathrm{INT},N,\mathrm{PC}(i)}$: Total resistances on the NMOS side switch for phase count $= i$.
$S_{\mathrm{PC}(i)} = A_{\mathrm{PC}(i)}\cdot\lambda_{N,\mathrm{PC}(i)}\cdot C_{\mathrm{ox}}\cdot L_{N,\mathrm{PC}(i)}$
t_{DB}: Dead band time.
$t_{R/F}$: Rise or fall time of the switch node V_{SW}.
$T_{\mathrm{PC}(i)} = E_{\mathrm{PC}(i)} + b_{\mathrm{PC}(i)}\cdot I_{O,\mathrm{MIN},\mathrm{PC}(i)} + I^2_{O,\mathrm{MIN},\mathrm{PC}(i)}\cdot R_{\mathrm{DC}}/\mathrm{PC}(i)$
$T_F(\tau) = \frac{\tau}{\tau-1}$
V_{IN} : Input supply voltage.
V_O: Output voltage.
V_{DI}: Potential drop across diode in dead-band.
$W_{P,\mathrm{PC}(i)}$ and $L_{P,\mathrm{PC}(i)}$: Width and length of power PMOS switch, respectively, for phase count $= i$.
$W_{N,PC(i)}$ and $L_{N,PC(i)}$: Width and length of power NMOS switch, respectively, for phase count $= i$.

I. Introduction

MULTIPHASE dc–dc converters are widely used as power management ICs in data centers, modern SoCs, and high-performance computing systems due to their ability to deliver high load currents and provide improved thermal management [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]. These application platforms operate in multiple power states, such as deep sleep, sleep, and active modes, frequently transitioning between them to optimize power consumption. Therefore, power converters must efficiently support wide load current ranges and quickly respond to mode changes, often operating at multi-MHz switching frequencies [11]. However, dynamic load conditions make it challenging to achieve consistently high and flat efficiency, as conduction losses dominate at high loads and switching losses become significant at lighter loads. Thus, power converters must be designed to maintain high and flat efficiency across the entire load range.

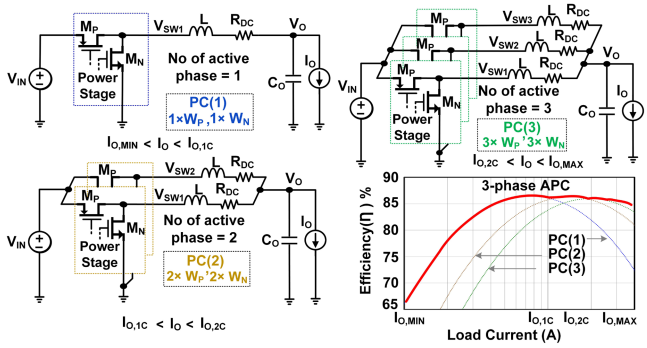


Fig. 1. Conventional equal-sized three-phase APC and its configuration in different load range with its typical efficiency plot.

Several state-of-the-art works aim to achieve a flat efficiency profile. For example, Dias and Santos [12] focussed on optimiming the switching frequency, while [13] and [14] target the driver stage and gate-voltage swing optimization of the power MOSFETs. However, these works are limited to single-phase buck converters. Some other works adopt a multiphase structure simply by increasing the number of phases to meet high load current demand [15], [16]. In these designs, all phases remain active across the entire load range. Efficiency degrades at low load due to excessive switching loss at high frequency. At high load, efficiency also drops because of large conduction loss. As a result, the overall flatness of the efficiency profile is reduced. On the other hand, works such as [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30] aim to improve efficiency flatness in multiphase dc–dc converters using conventional active phase count (APC) techniques. As shown in Fig. 1, these converters use multiple phases. Each phase has power stages of equal MOSFET switch size. Multiple phases are dynamically enabled or disabled based on the load current demand. However, this causes higher switching losses at low and intermediate loads as the switch size is not properly optimized. As a result, the efficiency still varies significantly across the entire load range. Moreover, in these approaches, the total switch size is optimised only for the maximum load current. This helps to achieve the desired silicon area and the targeted efficiency at full load. After fixing the total switch size, the number of phases is then selected to improve the flatness of the efficiency curve. Adding more phases does help flatten the curve; however, it also creates significant area overhead. A tradeoff therefore exists between efficiency flatness, phase count, and silicon area. Thus, conventional methods do not provide a systematic way to optimize these tradeoffs, especially in the low and intermediate load ranges. This often leads to suboptimal designs. Hence, an analytically guided methodology is required to determine both the optimal MOSFET switch sizes and the phase count.

To address these limitations, this work proposes an analytically guided and discriminant-aided design methodology. This methodology helps to obtain both power MOSFET switch sizes and phase count in multiphase dc–dc converters. Unlike the prior

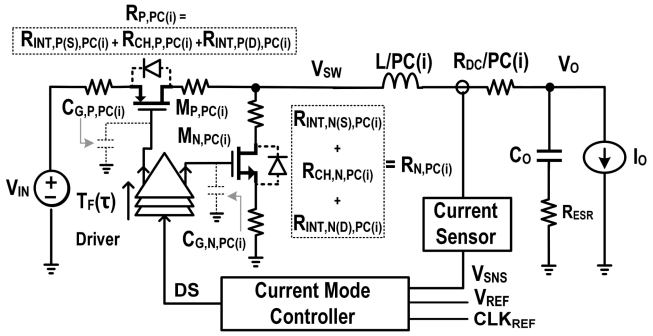


Fig. 2. Equivalent DC–DC buck converter with phase count = i (PC(i)).

approaches, our method systematically identifies the minimum effective equivalent resistance ($R_{\text{EFF,PC}(i)}$) required to maximize efficiency in the full load range. This provides a structured way to determine both the optimal MOSFET switch sizes and APCs for different load sub-ranges. To further reduce the design effort, a discriminant-aided process is introduced to quickly verify the feasibility of input specifications by evaluating the sign (positive or negative) of the discriminant. This confines the search space for the minimum $R_{\text{EFF,PC}(i)}$, significantly lowering computational complexity and design iteration time compared to conventional approaches. The effectiveness of the methodology is validated through multiple efficiency-driven case studies. These case studies demonstrate its adaptability to different scenarios. Among them, the best case is selected for implementation and fabrication. This prototype is then tested and verified experimentally. The rest of this article is organized as follows. Section II details the proposed methodology for single-phase and extends it to multiphase architectures, including the overall flow. Section III presents different case studies for efficiency-driven multiphase converter design. Section IV presents experimental results. Finally, Section V concludes this article.

II. Proposed Design Methodology

A. Analytical Breakdown of the Converter Power Losses

To facilitate loss analysis, Fig. 2 illustrates the equivalent dc–dc buck converter with a phase count = i (PC(i)). The terms $L/\text{PC}(i)$ and $R_{\text{DC}}/\text{PC}(i)$ represent the equivalent inductance and its corresponding dc resistance for PC(i), respectively. The power stage consists of the total PMOS switch size ($M_{P,\text{PC}(i)}$), total NMOS switch size ($M_{N,\text{PC}(i)}$), and their associated driver. The resistances of the metal interconnects are modeled at the source and drain terminals of the total PMOS switch, denoted by $R_{\text{INT},P(S),\text{PC}(i)}$ and $R_{\text{INT},P(D),\text{PC}(i)}$, respectively. Similarly, the interconnect resistances at the drain and source terminals of the total NMOS switch are indicated by $R_{\text{INT},N(D),\text{PC}(i)}$ and $R_{\text{INT},N(S),\text{PC}(i)}$. The power stage, together with the inductor and output capacitor, connects the input voltage (V_{IN}) to the output voltage (V_O). The current sensor senses the inductor current and feeds the corresponding V_{SNS} signal to the current-mode controller, where the same is compared with the reference voltage V_{REF} to produce the duty signal (DS) for regulating V_O close to V_{REF} [31].

The different power losses in the dc–dc converter are formulated in the Appendix. Considering all these contributions, the total power loss in the buck converter is given as follows:

$$P_{T,L,\text{PC}(i)} = P_{G,L,\text{PC}(i)} + P_{\text{DR},L,\text{PC}(i)} + P_{\text{TR},L,\text{PC}(i)} + P_{\text{DI},L,\text{PC}(i)} + P_{\text{CT},L,\text{PC}(i)} + P_{\text{CD},L,\text{PC}(i)}. \quad (1)$$

To simplify the analytical derivation, the losses in (1) have been reconstructed in (2) based on their dependence on I_O and f_{SW}. The losses directly related with only I_O are classified as $P_{I_O,L,\text{PC}(i)}$, those purely dependent on f_{SW} only as $P_{f_{\text{SW}},L,\text{PC}(i)}$ and those proportional to the product of I_O and f_{SW} as $P_{I_O\cdot f_{\text{SW}},\text{PC}(i)}$

$$P_{T,L,\text{PC}(i)} = P_{I_O,L,\text{PC}(i)} + P_{f_{\text{SW}},L,\text{PC}(i)} + P_{I_O\cdot f_{\text{SW}},L,\text{PC}(i)}. \quad (2)$$

Here, losses, which are proportional to I_O, are expressed as follows:

$$\begin{aligned} P_{I_O,L,\text{PC}(i)} &= I_O^2 \cdot \{D \cdot R_{P,\text{PC}(i)} + (1-D) \cdot R_{N,\text{PC}(i)} + R_{\text{DC}}/\text{PC}(i)\} \\ &= I_O^2 \cdot R_{\text{EFF,PC}(i)}. \end{aligned} \quad (3)$$

The losses that depend solely on switching frequency include gate driver loss and ripple-related conduction loss. To simplify the analysis, $P_{\text{CT},L,\text{PC}(i)}$ is included as part of $P_{f_{\text{SW}},L,\text{PC}(i)}$, although it is constant and independent of f_{SW}.

$$\begin{aligned} P_{f_{\text{SW}},L,\text{PC}(i)} &= T_F(\tau)\cdot V_{\text{IN}}^2 \cdot f_{\text{SW}} \cdot (C_{G,P,\text{PC}(i)} + C_{G,N,\text{PC}(i)}) \\ &\quad + \left(D \cdot \frac{\Delta I_O^2}{12}\right) \cdot R_{P,\text{PC}(i)} + \left\{(1-D) \cdot \frac{\Delta I_O^2}{12}\right\} \cdot R_{N,\text{PC}(i)} + \frac{\Delta I_O^2}{12} \cdot R_{ESR} + V_{IN} \cdot I_Q \\ &= A_{\text{PC}(i)} \cdot (C_{G,P,\text{PC}(i)} + C_{G,N,\text{PC}(i)}) \\ &\quad + B_{\text{PC}(i)} \cdot R_{P,\text{PC}(i)} \\ &\quad + C_{\text{PC}(i)} \cdot R_{N,\text{PC}(i)} + E_{\text{PC}(i)}. \end{aligned} \quad (4)$$

Finally, losses that are proportional to both I_O and f_{SW} arise from dead-time conduction and switching transitions as expressed follows:

$$\begin{aligned} P_{I_O\cdot f_{\text{SW}},\text{PC}(i)} &= \left(2 \cdot V_{\text{DI}} \cdot t_{\text{DB}} + V_{\text{IN}} \cdot t_{R/F}\right) \cdot I_O \cdot f_{\text{SW}} \\ &= K \cdot I_O \cdot f_{\text{SW}}. \end{aligned} \quad (5)$$

For optimization, it is useful to express $C_{G,P,\text{PC}(i)}$ and $C_{G,N,\text{PC}(i)}$ in terms of switch sizes. The gate capacitance of the power MOSFET switches can be written as $C_{G,P,\text{PC}(i)} = W_{P,\text{PC}(i)} \cdot L_{P,\text{MIN}} \cdot C_{\text{ox}}$ and $C_{G,N,\text{PC}(i)} = W_{N,\text{PC}(i)} \cdot L_{N,\text{MIN}} \cdot C_{\text{ox}}$. The value of $W_{P,\text{PC}(i)}$ and $W_{L,\text{PC}(i)}$ can be expressed as follows:

$$W_{P,\text{PC}(i)} = \left\{\frac{1}{\frac{\mu_P \cdot C_{\text{ox}} \cdot (V_{\text{IN}} - |V_{\text{th},P}|)}{L_{P,\text{MIN}}}}\right\} \frac{1}{R_{\text{CH},P,\text{PC}(i)}} = \frac{\lambda_{P,\text{PC}(i)}}{R_{\text{CH},P,\text{PC}(i)}} \quad (6)$$

$$W_{N,\mathrm{PC}(i)} = \left\{ \frac{1}{\frac{\mu_N \cdot C_{\mathrm{ox}} \cdot (V_{\mathrm{IN}} - |V_{\mathrm{th},N}|)}{L_{N,\mathrm{MIN}}}} \right\} \frac{1}{R_{\mathrm{CH},N,\mathrm{PC}(i)}} = \frac{\lambda_{N,\mathrm{PC}(i)}}{R_{\mathrm{CH},N,\mathrm{PC}(i)}}. \tag{7}$$

Typically, the lengths utilized for both PMOS and NMOS ($L_{P,\mathrm{MIN}}$ and $L_{N,\mathrm{MIN}}$) are set as minimum as supported by the technology. Hence,

$$\begin{aligned} C_{G,P,\mathrm{PC}(i)} &= W_{P,\mathrm{PC}(i)} \cdot L_{P,\mathrm{MIN}} \cdot C_{\mathrm{ox}} \\ &= \frac{\lambda_{P,\mathrm{PC}(i)} \cdot L_{P,\mathrm{MIN}} \cdot C_{\mathrm{ox}}}{R_{P,\mathrm{PC}(i)} - R_{\mathrm{INT},P,\mathrm{PC}(i)}} \end{aligned} \tag{8}$$

$$\begin{aligned} C_{G,N,\mathrm{PC}(i)} &= W_{N,\mathrm{PC}(i)} \cdot L_{N,\mathrm{MIN}} \cdot C_{\mathrm{ox}} \\ &= \frac{\lambda_{N,\mathrm{PC}(i)} \cdot L_{N,\mathrm{MIN}} \cdot C_{\mathrm{ox}}}{R_{N,\mathrm{PC}(i)} - R_{\mathrm{INT},N,\mathrm{PC}(i)}}. \end{aligned} \tag{9}$$

Substituting these values of $C_{G,P,\mathrm{PC}(i)}$ and $C_{G,N,\mathrm{PC}(i)}$, the total power loss in the buck converter ($P_{T,L,\mathrm{PC}(i)}$) can now be expressed as (10). The total loss in (10) has the scope for optimization as it contains terms that are directly or inversely related to $R_{P,\mathrm{PC}(i)}$, and $R_{N,\mathrm{PC}(i)}$

$$\begin{aligned} P_{\mathrm{T,L,PC(i)}} = I_O^2 \cdot \{ & D \cdot R_{P,\mathrm{PC}(i)} + (1-D) \\ & \cdot R_{N,\mathrm{PC}(i)} + R_{\mathrm{DC}}/\mathrm{PC}(i) \} \\ & + \frac{A_{\mathrm{PC}(i)} \cdot \lambda_{P,\mathrm{PC}(i)} \cdot C_{\mathrm{ox}} \cdot L_{P,\mathrm{MIN}}}{R_{P,\mathrm{PC}(i)} - R_{\mathrm{INT,P,PC(i)}}} \\ & + \frac{A_{\mathrm{PC}(i)} \cdot \lambda_{N,\mathrm{PC}(i)} \cdot C_{\mathrm{ox}} \cdot L_{N,\mathrm{MIN}}}{R_{N,\mathrm{PC}(i)} - R_{\mathrm{INT,N,PC(i)}}} \\ & + B_{\mathrm{PC}(i)} \cdot R_{P,\mathrm{PC}(i)} + C_{\mathrm{PC}(i)} \cdot R_{N,\mathrm{PC}(i)} \\ & + E_{\mathrm{PC}(i)} + K \cdot I_O \cdot f_{\mathrm{SW}}. \end{aligned} \tag{10}$$

B. Proposed Analytically Guided Efficiency Optimization in a Single Phase DC–DC Buck Converter {i.e., PC(1)}

This subsection presents an optimization method to determine optimum values of power MOSFET switches ($W_{P,\mathrm{PC}(i)}$ and $W_{N,\mathrm{PC}(i)}$), which maintain a minimum required efficiency (η_{MIN}) over the maximum load range. For the single-phase dc–dc buck converter, phase count = 1 {i.e., PC(1)}, the total resistances of the high-side and low-side power MOSFETs are denoted as $R_{P,\mathrm{PC(1)}}$ and $R_{N,\mathrm{PC(1)}}$, respectively. The minimum efficiency constraint is denoted as $\eta_{\mathrm{MIN,PC(1)}}$. The power conversion efficiency ($\eta_{\mathrm{PC(1)}}$) of a dc–dc buck converter with phase count = 1 {i.e., PC(1)} is defined as the ratio of output power to total input power, given by the following [32]:

$$\begin{aligned} \eta_{\mathrm{PC(1)}} &= \frac{V_{\mathrm{O}} \cdot I_O}{V_{\mathrm{O}} \cdot I_O + P_{T,L,\mathrm{PC(1)}}} \\ &= \frac{V_{\mathrm{O}} \cdot I_O}{V_{\mathrm{O}} \cdot I_O + K \cdot I_O \cdot f_{\mathrm{SW}} + P_{f_{\mathrm{SW}},L,\mathrm{PC(1)}} + I_O^2 \cdot R_{\mathrm{EFF,PC1}}}. \end{aligned} \tag{11}$$

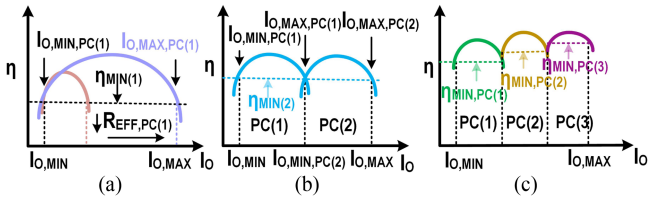


Fig. 3. Visualization of the proposed approach. (a) Lower fixed baseline efficiency ($\eta_{\mathrm{MIN(1)}}$) requiring phase count = 1. (b) Increased fixed baseline efficiency ($\eta_{\mathrm{MIN(2)}}$) requiring phase count = 2. (c) Variable baseline efficiency ($\eta_{\mathrm{MIN,PC(1)}}$, $\eta_{\mathrm{MIN,PC(2)}}$ and $\eta_{\mathrm{MIN,PC(3)}}$) requiring phase count = 3.

Substituting the required minimum efficiency $\eta_{\mathrm{MIN,PC(1)}}$ into (11) results in a quadratic equation in terms of the load current I_O

$$I_O^2 + \left\{ \frac{b_{\mathrm{PC(1)}}}{R_{\mathrm{EFF,PC(1)}}} \right\} \cdot I_O + \frac{P_{f_{\mathrm{SW}},L,\mathrm{PC(1)}}}{R_{\mathrm{EFF,PC1}}} = 0. \tag{12}$$

This quadratic expression characterises the relationship between the converter's losses and its efficiency constraint. For different combinations of high-side and low-side switch resistances ($R_{P,\mathrm{PC(1)}}$, $R_{N,\mathrm{PC(1)}}$), the effective resistance $R_{\mathrm{EFF,PC(1)}}$ and switching losses vary, yielding different root pairs of (12). These roots are defined as $I_{O,\mathrm{MIN,PC(1)}}$ and $I_{O,\mathrm{MAX,PC(1)}}$, representing the minimum and maximum load currents, respectively, over which the converter maintains the efficiency constraint. The proposed optimization method is visualized in Fig. 3(a), which plots the quadratic expression in (12) for a fixed efficiency target ($\eta_{\mathrm{MIN,PC(1)}}$). One root is fixed at the minimum required load current, $I_{O,\mathrm{MIN,PC(1)}} = I_{O,\mathrm{MIN}}$, to ensure that the efficiency constraint is satisfied at the low end. The goal of the optimization is to maximize the separation between the two roots, i.e., extend $I_{O,\mathrm{MAX,PC(1)}}$ as far as possible, which corresponds to maximising the usable load range. The second root is derived from the known relationship between the roots and coefficients of a quadratic

$$I_{O,\mathrm{MAX,PC(1)}} - I_{O,\mathrm{MIN,PC(1)}} = -\frac{b_{\mathrm{PC(1)}}}{R_{\mathrm{EFF,PC(1)}}} - 2 \cdot I_{O,\mathrm{MIN,PC(1)}}. \tag{13}$$

Equation (13) shows that increasing the load range depends on the effective resistance. To maintain the baseline efficiency $\eta_{\mathrm{MIN,PC(1)}}$, the effective resistance $R_{\mathrm{EFF,PC(1)}}$ must be minimized. Since $R_{\mathrm{EFF,PC(1)}}$ is a function of both $R_{P,\mathrm{PC(1)}}$ and $R_{N,\mathrm{PC(1)}}$, it should be reduced to a single variable by fixing $I_{O,\mathrm{MIN,PC(1)}}$. Expressing (13) in terms of $I_{O,\mathrm{MAX,PC(1)}}$ and substituting it into (12), yields

$$I_{O,\mathrm{MIN,PC(1)}}^2 + \left(\frac{b_{\mathrm{PC(1)}}}{R_{\mathrm{EFF,PC(1)}}} \right) I_{O,\mathrm{MIN,PC(1)}} + \frac{P_{f_{\mathrm{SW}},L,\mathrm{PC(1)}}}{R_{\mathrm{EFF,PC(1)}}} = 0. \tag{14}$$

By expressing $R_{\mathrm{EFF,PC(1)}}$ as a function of $R_{P,\mathrm{PC(1)}}$ and $R_{N,\mathrm{PC(1)}}$, and rewriting the above expression into a quadratic form in terms of $R_{P,\mathrm{PC(1)}}$, we get

$$R_{P,\mathrm{PC(1)}}^2 + \alpha_{\mathrm{PC(1)}} \cdot R_{P,\mathrm{PC(1)}} + \beta_{\mathrm{PC(1)}} = 0. \tag{15}$$

The two real and unequal roots of this equation represent valid values of $R_{P,\mathrm{PC(1)}}$ that satisfy the efficiency constraint at

$I_{O,\mathrm{MIN,PC(1)}}$

$$R_{P1/2,\mathrm{PC(1)}} = \frac{-\alpha_{\mathrm{PC(1)}} \mp \sqrt{\alpha^2_{\mathrm{PC(1)}} - 4 \cdot \beta_{\mathrm{PC(1)}}}}{2}. \tag{16}$$

Equation (16) represents $R_{P,\mathrm{PC(1)}}$ in terms of $R_{N,\mathrm{PC(1)}}$. Using (16), $R_{\mathrm{EFF,PC(1)}}$ can be expressed completely in terms of $R_{N,\mathrm{PC(1)}}$. This transformation enables a one-dimensional search for an optimum value of $R_{N,\mathrm{PC(1)}}$ at a minimum value of $R_{\mathrm{EFF,PC(1)}}$. Consequently, the corresponding optimum value of $R_{P,\mathrm{PC(1)}}$ can be obtained using (16). The optimal resistance values $R_{P,\mathrm{PC(1)}}$ (as $R_{P,\mathrm{OPT,PC(1)}}$) and $R_{N,\mathrm{PC(1)}}$ (as $R_{N,\mathrm{OPT,PC(1)}}$) can then be substituted into sizing expressions [e.g., (8) and (9)] to obtain the corresponding optimal switch widths $W_{P,\mathrm{OPT,PC(1)}}$ and $W_{N,\mathrm{OPT,PC(1)}}$. This single-phase optimization framework serves as the foundation for the subsequent extension to the multiphase converter architecture discussed next.

C. Extension to Multiphase Operation

As illustrated in Fig. 3(a), a relatively low baseline efficiency of $\eta_{\mathrm{MIN(1)}}$ can cover the entire load range ($I_{O,\mathrm{MIN}}$-$I_{O,\mathrm{MAX}}$) but with a significant efficiency variation across the range. This motivates the need for a multiphase approach in achieving a flatter efficiency profile.

To enable this, the baseline efficiency target is increased to $\eta_{\mathrm{MIN(2)}} (> \eta_{\mathrm{MIN(1)}})$ while maintaining the same load range, as shown in Fig. 3(b). The proposed method from the previous section is first applied to PC(1). The lower current of PC(1) is fixed to lower limit of the load current range ($I_{O,\mathrm{MIN,PC(1)}} = I_{O,\mathrm{MIN}}$), and the corresponding upper load current ($I_{O,\mathrm{MAX,PC(1)}}$) is optimized such that the minimum efficiency constraint $\eta_{\mathrm{MIN(2)}}$ is satisfied by minimising $R_{\mathrm{EFF,PC(1)}}$. This defines the maximum load current that can be supported using PC(1) while maintaining at least $\eta_{\mathrm{MIN(2)}}$. Since the target load range is not fully covered, an additional phase is introduced with PC(2). The upper load current limit from the previous phase count, $I_{O,\mathrm{MAX,PC(1)}}$, becomes the starting point for the next phase count, i.e., $I_{O,\mathrm{MIN,PC(2)}} = I_{O,\mathrm{MAX,PC(1)}}$. The same optimization process is repeated to determine $I_{O,\mathrm{MAX,PC(2)}}$, again targeting the efficiency constraint $\eta_{\mathrm{MIN(2)}}$ and minimizing $R_{\mathrm{EFF,PC(2)}}$. Although this fixed-baseline approach segments the load range across multiple phases and flattens the efficiency curve to some extent, further improvement is possible by changing the baseline efficiency per phase count, denoted as $\eta_{\mathrm{MIN,PC(i)}}$. This reduces both the efficiency profile variation and optimizes the total number of active phases required. For example, as shown in Fig. 3(c), the efficiency constraint for PC(1) is initially raised to $\eta_{\mathrm{MIN,PC(1)}}$ by optimizing switching losses at a fixed switching frequency. Then, for PC(2) and PC(3), the baseline efficiency targets are increased to $\eta_{\mathrm{MIN,PC(2)}}$ and $\eta_{\mathrm{MIN,PC(3)}}$, respectively. This adaptive baseline efficiency strategy ensures that each phase operates in its most efficient region, resulting in improved overall efficiency and an optimized number of active phases. At each step, the same analytical method is applied to maximise the load range that can be supported at the given baseline efficiency, starting from the previously computed $I_{O,\mathrm{MAX,PC(i-1)}}$ as the new $I_{O,\mathrm{MIN,PC(i)}}$ and minimizing $R_{\mathrm{EFF,PC(i)}}$ to determine $I_{O,\mathrm{MAX,PC(i)}}$. This proposed strategy ensures efficient load distribution across phases, the optimum number of active phases needed to meet efficiency targets and minimizes the variation across the entire operating range. Fig. 3(c) illustrates that this method achieves a high peak efficiency, yet has less variation throughout the load range with optimized phase count, compared to the fixed-baseline approach as shown in Fig. 3(b).

D. Proposed Discriminant-Aided $R_{N,PC(i)}$ Range Selection

Equations (13), (15), and (16) reduce the optimization to one variable, $R_{N,\mathrm{PC}(i)}$. However, the expressions for $\alpha_{\mathrm{PC}(i)}$ and $\beta_{\mathrm{PC}(i)}$ are still too complex for a closed-form solution. Thus, entire $R_{N,\mathrm{PC}(i)}$ values are scanned using (16) to identify the minimum $R_{\mathrm{EFF,PC}(i)}$ that maximises the separation between $I_{O,\mathrm{MAX,PC(i)}}$ and $I_{O,\mathrm{MIN,PC(i)}}$. To reduce computational time, an algorithm is proposed that bounds the search region of $R_{N,\mathrm{PC}(i)}$ to a finite region instead of scanning the entire values.

For physical realisation of the power PMOS switch size ($R_{P,\mathrm{PC}(i)}$), discriminant of the quadratic in (15) is a positive quantity expressed as follows:

$$\alpha^2_{\mathrm{PC}(i)} - 4 \cdot \beta_{\mathrm{PC}(i)} \geq 0. \tag{17}$$

$\alpha_{\mathrm{PC}(i)}$ and $\beta_{\mathrm{PC}(i)}$ is decomposed as shown follows:

$$\alpha_{\mathrm{PC}(i)} = \alpha_{1,\mathrm{PC}(i)} + \gamma_{\mathrm{PC}(i)} \tag{18}$$

$$\beta_{\mathrm{PC}(i)} = \beta_{1,\mathrm{PC}(i)} - R_{\mathrm{INT},P,\mathrm{PC}(i)} \cdot \gamma_{\mathrm{PC}(i)}. \tag{19}$$

Substituting (18) and (19) into (17) yields

$$\gamma^2_{\mathrm{PC}(i)} + (2 \cdot \alpha_{1,\mathrm{PC}(i)} + 4 \cdot R_{\mathrm{INT},P,\mathrm{PC}(i)}) \cdot \gamma_{\mathrm{PC}(i)} + \alpha^2_{1,\mathrm{PC}(i)} - 4 \cdot \beta_{1,\mathrm{PC}(i)} > 0. \tag{20}$$

Quadratic inequality (20) in terms of $\gamma_{\mathrm{PC}(i)}$ defines the range of values for which a real and positive $R_{P,\mathrm{PC}(i)}$ exists. The discriminant of (20), denoted as $\Delta'_{\mathrm{PC}(i)}$, is

$$\Delta'_{\mathrm{PC}(i)} = \left\{2 \cdot \alpha_{1,\mathrm{PC}(i)} + 4 \cdot R_{\mathrm{INT},P,\mathrm{PC}(i)}\right\}^2 - 4 \cdot \left\{\alpha^2_{1,\mathrm{PC}(i)} - 4 \cdot \beta_{1,\mathrm{PC}(i)}\right\}. \tag{21}$$

Two conditions are possible. For $\Delta'_{\mathrm{PC}(i)} < 0$, the quadratic equation in (20) remains positive for all values of $\gamma_{\mathrm{PC}(i)}$, implying that real solutions exist for all $\gamma_{\mathrm{PC}(i)}$ and, therefore, entire $R_{N,\mathrm{PC}(i)}$ region is valid. For $\Delta'_{\mathrm{PC}(i)} > 0$, the quadratic equation has two distinct real roots $\gamma_{1,\mathrm{PC}(i)}$ and $\gamma_{2,\mathrm{PC}(i)}$ with $\gamma_{1,\mathrm{PC}(i)} < \gamma_{2,\mathrm{PC}(i)}$. In this condition, the inequality (20) holds only for $\gamma_{\mathrm{PC}(i)} \leq \gamma_{1,\mathrm{PC}(i)}$ or $\gamma_{\mathrm{PC}(i)} \geq \gamma_{2,\mathrm{PC}(i)}$. This leads to the next step: expressing $\gamma_{\mathrm{PC}(i)}$ in terms of $R_{N,\mathrm{PC}(i)}$. The first inequality condition is expressed as follows:

$$\frac{1}{P_{\mathrm{PC}(i)}} \cdot \left\{Q_{\mathrm{PC}(i)} \cdot R_{N,\mathrm{PC}(i)} + \frac{S_{\mathrm{PC}(i)}}{R_{N,\mathrm{PC}(i)} - R_{\mathrm{INT},N,\mathrm{PC}(i)}}\right\} < \gamma_{1,\mathrm{PC}(i)} \tag{22}$$

$$R^2_{N,\mathrm{PC}(i)} - \left\{R_{\mathrm{INT},N,\mathrm{PC}(i)} + \frac{P_{\mathrm{PC}(i)} \cdot \gamma_{1,\mathrm{PC}(i)}}{Q_{\mathrm{PC}(i)}}\right\} \cdot R_{N,\mathrm{PC}(i)}$$

$$+\left\{\frac{S_{\mathrm{PC}(i)}+P_{\mathrm{PC}(i)}\cdot R_{\mathrm{INT},N,\mathrm{PC}(i)}\cdot\gamma_{1,\mathrm{PC}(i)}}{Q_{\mathrm{PC}(i)}}\right\}\leq 0. \quad (23)$$

Similarly, the second condition yields

$$R_{N,\mathrm{PC}(i)}^2-\left\{R_{\mathrm{INT},N,\mathrm{PC}(i)}+\frac{P_{\mathrm{PC}(i)}\cdot\gamma_{2,\mathrm{PC}(i)}}{Q_{\mathrm{PC}(i)}}\right\}\cdot R_{N,\mathrm{PC}(i)} + \left\{\frac{S_{\mathrm{PC}(i)}+P_{\mathrm{PC}(i)}\cdot R_{\mathrm{INT},N,\mathrm{PC}(i)}\cdot\gamma_{2,\mathrm{PC}(i)}}{Q_{\mathrm{PC}(i)}}\right\}\geq 0. \quad (24)$$

$\Delta'_{1,\mathrm{PC}(i)}$ and $\Delta'_{2,\mathrm{PC}(i)}$ are the discriminants of the quadratic equation in (23) and (24) and can be expressed as follows:

$$\Delta'_{1,\mathrm{PC}(i)}=\left\{R_{\mathrm{INT},N,\mathrm{PC}(i)}+\frac{P_{\mathrm{PC}(i)}\cdot\gamma_{1,\mathrm{PC}(i)}}{Q_{\mathrm{PC}(i)}}\right\}^2 - 4\cdot\left\{\frac{S_{\mathrm{PC}(i)}+P_{\mathrm{PC}(i)}\cdot R_{\mathrm{INT},N,\mathrm{PC}(i)}\cdot\gamma_{1,\mathrm{PC}(i)}}{Q_{\mathrm{PC}(i)}}\right\}. \quad (25)$$

For $\Delta'_{1,\mathrm{PC}(i)}$, two conditions may arise. If $\Delta'_{1,\mathrm{PC}(i)}<0$, then inequality in (23) has no real solutions for any value of $R_{N,\mathrm{PC}(i)}$. On the other hand, if $\Delta'_{1,\mathrm{PC}(i)}>0$, the quadratic in (23) has two distinct real roots, denoted as $R_{N,1a,\mathrm{PC}(i)}$ and $R_{N,1b,\mathrm{PC}(i)}$, with $R_{N,1a,\mathrm{PC}(i)}<R_{N,1b,\mathrm{PC}(i)}$. In this case, inequality (23) holds true only within the interval defined by these two roots, i.e., when $R_{N,1a,\mathrm{PC}(i)}<R_{N,\mathrm{PC}(i)}<R_{N,1b,\mathrm{PC}(i)}$

$$\Delta'_{2,\mathrm{PC}(i)}=\left\{R_{\mathrm{INT},N,\mathrm{PC}(i)}+\frac{P_{\mathrm{PC}(i)}\cdot\gamma_{2,\mathrm{PC}(i)}}{Q_{\mathrm{PC}(i)}}\right\}^2 - 4\cdot\left\{\frac{S_{\mathrm{PC}(i)}+P_{\mathrm{PC}(i)}\cdot R_{\mathrm{INT},N,\mathrm{PC}(i)}\cdot\gamma_{2,\mathrm{PC}(i)}}{Q_{\mathrm{PC}(i)}}\right\}. \quad (26)$$

Similarly, for $\Delta'_{2,\mathrm{PC}(i)}$, two conditions can arise. If $\Delta'_{2,\mathrm{PC}(i)}<0$, the inequality in (24) holds for all values of $R_{N,\mathrm{PC}(i)}$. In contrast, if $\Delta'_{2,\mathrm{PC}(i)}>0$, the quadratic equation in (24) has two distinct real roots, denoted as $R_{N,2a,\mathrm{PC}(i)}$ and $R_{N,2b,\mathrm{PC}(i)}$, with $R_{N,2a,\mathrm{PC}(i)}<R_{N,2b,\mathrm{PC}(i)}$. In this case, the inequality (24) is satisfied only in the regions outside these two roots, expressed as $R_{\mathrm{INT},N,\mathrm{PC}(i)}<R_{N,\mathrm{PC}(i)}<R_{N,2a,\mathrm{PC}(i)}$ and $R_{N,2b,\mathrm{PC}(i)}<R_{N,\mathrm{PC}(i)}<\infty$.

The flow chart of the proposed methodology to obtain the finite solution region of $R_{N,\mathrm{PC}(i)}$ is shown in Fig. 4. It begins with evaluating the sign of $\Delta'_{\mathrm{PC}(i)}$. If $\Delta'_{\mathrm{PC}(i)}<0$, a valid solution region exists for all $R_{N,\mathrm{PC}(i)}>R_{\mathrm{INT},N,\mathrm{PC}(i)}$. Otherwise, the values of $\Delta'_{2,\mathrm{PC}(i)}$ and $\Delta'_{1,\mathrm{PC}(i)}$ are checked sequentially. If $\Delta'_{2,\mathrm{PC}(i)}<0$, the solution region exists for all $R_{N,\mathrm{PC}(i)}>R_{\mathrm{INT},N,\mathrm{PC}(i)}$. If not, the valid range depends on the sign of $\Delta'_{1,\mathrm{PC}(i)}$. If $\Delta'_{1,\mathrm{PC}(i)}<0$ the solution region corresponds to $R_{N,\mathrm{PC}(i)}<R_{N,2a,\mathrm{PC}(i)}$ or $R_{N,\mathrm{PC}(i)}>R_{N,2b,\mathrm{PC}(i)}$. If both $\Delta'_{1,\mathrm{PC}(i)}>0$ and $\Delta'_{2,\mathrm{PC}(i)}>0$, the valid regions become $R_{N,\mathrm{PC}(i)}<R_{N,2a,\mathrm{PC}(i)}$, $R_{N,\mathrm{PC}(i)}>R_{N,2b,\mathrm{PC}(i)}$ or $R_{N,1a,\mathrm{PC}(i)}<R_{N,\mathrm{PC}(i)}<R_{N,2b,\mathrm{PC}(i)}$. This flowchart serves as a quick reference to confine the search region for fixing an optimal value of $R_{N,\mathrm{PC}(i)}$.

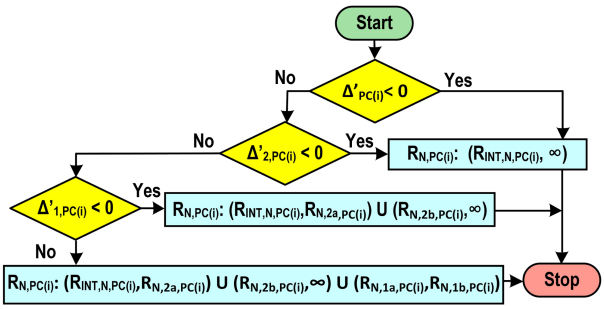


Fig. 4. Flowchart of the proposed methodology to confine the valid search region of $R_{N,\mathrm{PC}(i)}$.

E. Overall Design Methodology

In this subsection, the overall design methodology is presented. The process aims to obtain the optimised size of the power switches for the converter to flatten the power efficiency across the load range. As shown in Fig. 5, it begins with the designer's specifications, which include the input voltage (V_{IN}), output voltage (V_O), inductor value (L), inductor dc resistance (R_{DC}), output capacitor ESR (R_{ESR}), switching frequency (f_{SW}), minimum required efficiency (η_{MIN}), and the output load current range defined by $I_{O,\mathrm{MIN}}$ and $I_{O,\mathrm{MAX}}$. The process flow starts with a single phase by initialising the phase count (PC(i)) variable to $i=1$, and setting the minimum efficiency and load current for corresponding phase count as $\eta_{\mathrm{MIN},\mathrm{PC}(i)}=\eta_{\mathrm{MIN}}$ and $I_{O,\mathrm{MIN},\mathrm{PC}(i)}=I_{O,\mathrm{MIN}}$, respectively. The next step involves computing the coefficients of the PC(i) [$A_{\mathrm{PC}(i)}$, $B_{\mathrm{PC}(i)}$, $C_{\mathrm{PC}(i)}$, $E_{\mathrm{PC}(i)}$, $P_{\mathrm{PC}(i)}$, $Q_{\mathrm{PC}(i)}$, $R_{\mathrm{PC}(i)}$, $S_{\mathrm{PC}(i)}$, $T_{\mathrm{PC}(i)}$] required to identify a valid $R_{N,\mathrm{PC}(i)}$ solution region, as guided by the supporting sub-flowchart in Fig. 4. If a valid solution region is not found, the flow loops back by relaxing $\eta_{\mathrm{MIN},\mathrm{PC}(i)}$ and/or $I_{O,\mathrm{MIN},\mathrm{PC}(i)}$, or by returning L and/or f_{SW} to obtain a valid solution region. Once a valid region is identified, $R_{P,\mathrm{PC}(i)}$ and $R_{\mathrm{EFF},\mathrm{PC}(i)}$ are plotted across the $R_{N,\mathrm{PC}(i)}$ range, and the optimal resistances $R_{N,\mathrm{OPT},\mathrm{PC}(i)}$ and $R_{P,\mathrm{OPT},\mathrm{PC}(i)}$ are extracted at the point of minimum $R_{\mathrm{EFF},\mathrm{PC}(i)}$. The maximum load current for this phase that satisfies the required efficiency, $I_{O,\mathrm{MAX},\mathrm{PC}(i)}$, is then computed, defining a phase count specific load range from $I_{O,\mathrm{MIN},\mathrm{PC}(i)}$ to $I_{O,\mathrm{MAX},\mathrm{PC}(i)}$. If this phase-specific load range is not sufficient to meet the designer's requirements, the process loops back to adjust $\eta_{\mathrm{MIN},\mathrm{PC}(i)}$ and/or $I_{O,\mathrm{MIN},\mathrm{PC}(i)}$, or to retune L and/or f_{SW} in order to obtain an acceptable load range for the current phase count. If the phase-specific load range is found sufficient, the optimal PMOS and NMOS switch sizes ($W_{P,\mathrm{PC}(i)}$ and $W_{N,\mathrm{PC}(i)}$) are then determined using (8) and (9), followed by generation of the corresponding efficiency plot. A subsequent check is performed to verify whether the load range satisfies the overall load current range specified by the designer. If not, another phase is added with the minimum efficiency $\eta_{\mathrm{MIN},\mathrm{PC}(i+1)}$ and load current $I_{O,\mathrm{MIN},\mathrm{PC}(i+1)}$ getting initialized using the final values of $\eta_{\mathrm{MIN},\mathrm{PC}(i)}$ and $I_{O,\mathrm{MIN},\mathrm{PC}(i)}$ from the previous phase count, and phase counter is incremented ($i\rightarrow i+1$), after which the loop continues to finally cover the total load range. If the full load range is covered, a final check ensures that the resulting efficiency plot is acceptably flat; if not, the process restarts with

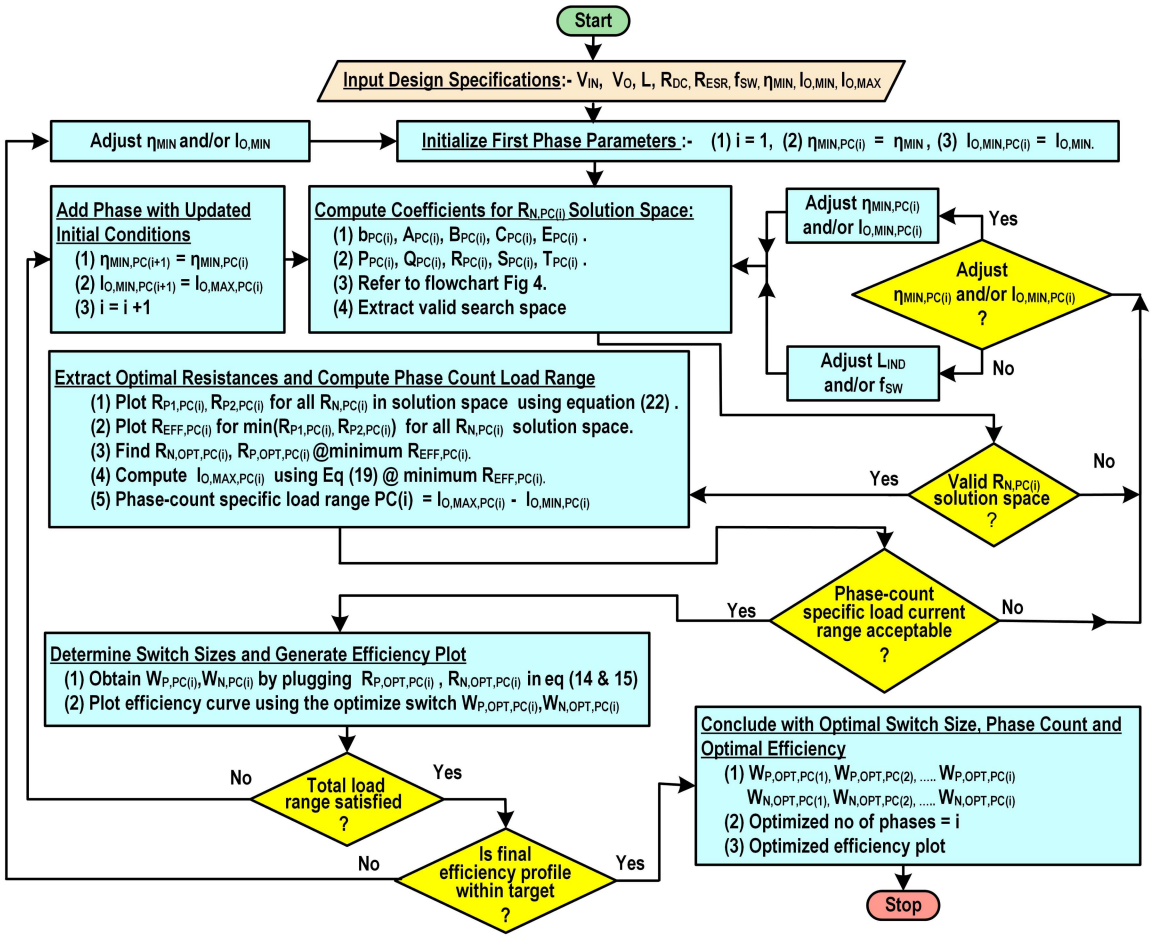


Fig. 5. Flow chart of the proposed design methodology.

revised values of η_{MIN} and/or $I_{O,\text{MIN}}$. Once the designer's specifications are met, the procedure concludes with the optimised efficiency profile and the corresponding final phase count.

III. Case Studies for Efficiency Driven Multiphase Converter Design

To validate the proposed methodology for efficiency-driven optimisation of power MOSFET sizing and phase count in a multiphase dc–dc buck converter, three case studies are conducted, each targeting a different baseline efficiency constraint to demonstrate its practical applicability. The converter operates with an input voltage $V_{\text{IN}} = 3.3\,\text{V}$, an output voltage $V_O = 1.2\,\text{V}$, and a switching frequency of 20 MHz. The inductor value is equal to 100 nH with a series resistance $R_{\text{DC}} = 20\,\text{m}\,\Omega$, and the output capacitor is 4.7 μF with $R_{\text{ESR}} = 10\,\text{m}\Omega$.

In the first case, a fixed minimum baseline efficiency of 85% is targeted across the entire load range. As inferred from (13), minimizing $R_{\text{EFF,PC}(i)}$ maximizes the load current range that meets this efficiency target. Since $R_{\text{EFF,PC}(i)}$ depends on both $R_{P,\text{PC}(i)}$ and $R_{N,\text{PC}(i)}$, it is reformulated as a one-dimensional function of $R_{N,\text{PC}(i)}$ by expressing $R_{P,\text{PC}(i)}$ in terms of $R_{N,\text{PC}(i)}$ using (16). To proceed with this minimization, a valid region of $R_{N,\text{PC}(i)}$ is first identified that ensures at least 85% efficiency using the proposed discriminant-aided methodology, as illustrated in Fig. 4. To determine the valid region for PC(1), the discriminant $\Delta'_{\text{PC}(1)}$ of the quadratic inequality in (20) is computed. Since $\Delta'_{\text{PC}(1)} > 0$, the secondary discriminant $\Delta'_{2,\text{PC}(1)}$ in (26) is evaluated, followed by $\Delta'_{1,\text{PC}(1)}$ in (25), both of which yields positive values. Thus, the valid search region for $R_{N,\text{PC}(1)}$ lies within the following intervals: $R_{\text{INT},N,\text{PC}(1)} < R_{N,\text{PC}(1)} < R_{N,2a,\text{PC}(1)}$, $R_{N,1a,\text{PC}(1)} < R_{N,\text{PC}(1)} < R_{N,1b,\text{PC}(1)}$, and $R_{N,2b,\text{PC}(1)} < R_{N,\text{PC}(1)} < \infty$. $R_{P1,\text{PC}(1)}$ and $R_{P2,\text{PC}(1)}$ are computed using (16) and plotted over the valid intervals of $R_{N,\text{PC}(1)}$, as shown in Fig. 6. The corresponding values of $R_{\text{EFF1,PC}(1)}$ and $R_{\text{EFF2,PC}(1)}$ are then calculated using $R_{P1,\text{PC}(1)}$ and $R_{P2,\text{PC}(1)}$, respectively, and plotted over the same intervals in Fig. 7. As observed from the plots, in the interval $R_{\text{INT},N,\text{PC}(1)} < R_{N,\text{PC}(1)} < R_{N,2a,\text{PC}(1)}$, both $R_{P1,\text{PC}(1)}$ and the corresponding $R_{\text{EFF1,PC}(1)}$ are negative, making this range impractical. Moreover, $R_{P2,\text{PC}(1)}$ and $R_{\text{EFF2,PC}(1)}$ exhibit significantly higher values in this interval compared to the others; therefore, this interval can be excluded from further consideration. On the other hand, among the remaining intervals, $R_{N,1a,\text{PC}(1)} < R_{N,\text{PC}(1)} < R_{N,1b,\text{PC}(1)}$ yields the lowest values

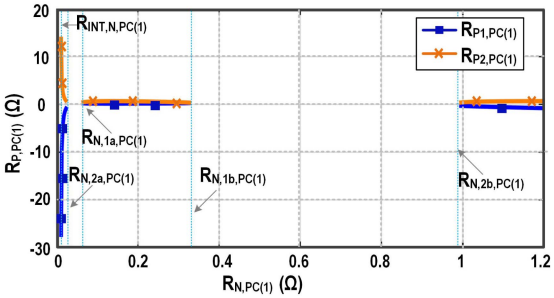


Fig. 6. Plot of $R_{P1,\mathrm{PC}(1)}$ and $R_{P2,\mathrm{PC}(1)}$ versus $R_{N,\mathrm{PC}(1)}$ across valid search intervals for $\eta_{\min} = 85\%$.

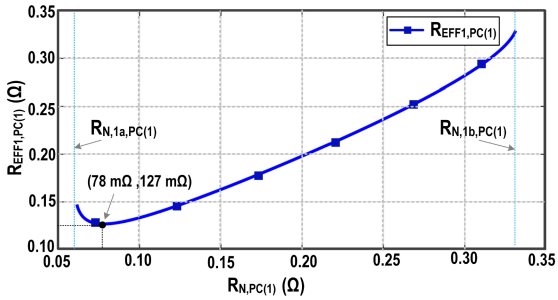


Fig. 9. Plot of $R_{\mathrm{EFF1},\mathrm{PC}(1)}$ versus $R_{N,\mathrm{PC}(1)}$ for PC(1) with $\eta_{\min} = 85\%$, indicating the optimal point.

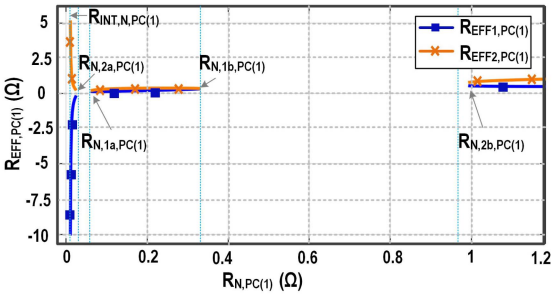


Fig. 7. Plot of $R_{\mathrm{EFF1},\mathrm{PC}(1)}$ and $R_{\mathrm{EFF2},\mathrm{PC}(1)}$ versus $R_{N,\mathrm{PC}(1)}$ across valid search intervals for $\eta_{\min} = 85\%$.

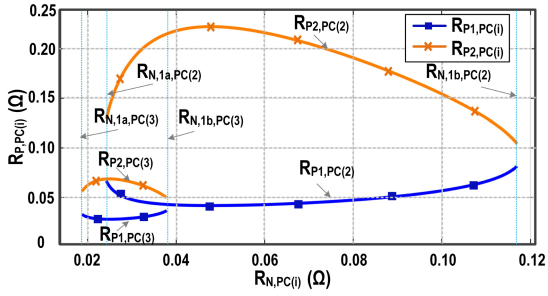


Fig. 10. Plot of $R_{P1,\mathrm{PC}(i)}$, $R_{P2,\mathrm{PC}(i)}$ versus $R_{N,\mathrm{PC}(i)}$ within $R_{N,1a,\mathrm{PC}(i)} < R_{N,\mathrm{PC}(i)} < R_{N,1b,\mathrm{PC}(i)}$ for i= 2,3 at $\eta_{\min} = 85\%$.

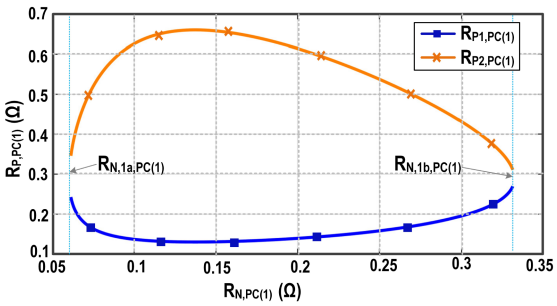


Fig. 8. Plot of $R_{P1,\mathrm{PC}(1)}$ and $R_{P2,\mathrm{PC}(1)}$ versus $R_{N,\mathrm{PC}(1)}$ within $R_{N,1a,\mathrm{PC}(1)} < R_{N,\mathrm{PC}(1)} < R_{N,1b,\mathrm{PC}(1)}$ for PC(1) at $\eta_{\min} = 85\%$.

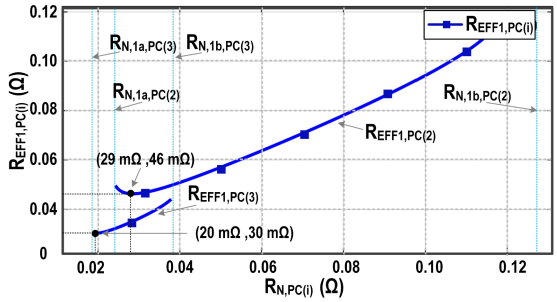


Fig. 11. Plot of $R_{\mathrm{EFF1},\mathrm{PC}(i)}$ plotted versus $R_{N,\mathrm{PC}(i)}$ for i = 2,3 at $\eta_{\min} = 85\%$.

for $R_{P1,\mathrm{PC}(1)}$, $R_{P2,\mathrm{PC}(1)}$, and their corresponding $R_{\mathrm{EFF1},\mathrm{PC}(1)}$ and $R_{\mathrm{EFF2},\mathrm{PC}(1)}$. Therefore, this interval is selected to search for the optimal power MOSFET switch size, with an enlarged view provided in Figs. 8 and 9 for detailed comparison. As observed in Fig. 8, $R_{P1,\mathrm{PC}(1)}$ is lower than $R_{P2,\mathrm{PC}(1)}$. Therefore, $R_{P1,\mathrm{PC}(1)}$ is chosen to plot $R_{\mathrm{EFF1},\mathrm{PC}(1)}$ to identify its minimum value at the optimal point, as shown in Fig. 9. In the plot, the optimal point is identified at the minimum $R_{\mathrm{EFF1},\mathrm{PC}(1)}$ of 127 mΩ, occurring at $R_{N,\mathrm{OPT},\mathrm{PC}(1)} = 78$ mΩ. Consequently, the optimal value of $R_{P,\mathrm{OPT},\mathrm{PC}(1)}$ is computed by substituting this $R_{N,\mathrm{OPT},\mathrm{PC}(1)}$ into (16). Similar to the PC(1) case, the valid search regions for PC(2) and PC(3) are determined using the methodology illustrated in Fig. 4. For PC(2), the valid intervals are $R_{\mathrm{INT},N,\mathrm{PC}(2)} < R_{N,\mathrm{PC}(2)} < R_{N,2a,\mathrm{PC}(2)}$, $R_{N,1a,\mathrm{PC}(2)} < R_{N,\mathrm{PC}(2)} < R_{N,1b,\mathrm{PC}(2)}$, and $R_{N,2b,\mathrm{PC}(2)} < R_{N,\mathrm{PC}(2)} < \infty$. Similarly, for PC(3), the valid intervals are $R_{\mathrm{INT},N,\mathrm{PC}(3)} < R_{N,\mathrm{PC}(3)} < R_{N,2a,\mathrm{PC}(3)}$, $R_{N,1a,\mathrm{PC}(3)} < R_{N,\mathrm{PC}(3)} < R_{N,1b,\mathrm{PC}(3)}$, and $R_{N,2b,\mathrm{PC}(3)} < R_{N,\mathrm{PC}(3)} < \infty$. Using a similar reason as in the PC(1) case, the interval $R_{N,1a,\mathrm{PC}(i)} < R_{N,\mathrm{PC}(i)} < R_{N,1b,\mathrm{PC}(i)}$ yields the lowest values for both $R_{P1,\mathrm{PC}(i)}$ and $R_{P2,\mathrm{PC}(i)}$ for PC(i), where $i = 2, 3$. Therefore, this region is selected and plotted in Fig. 10. As seen in the plot, $R_{P1,\mathrm{PC}(i)}$ is lower than $R_{P2,\mathrm{PC}(i)}$ for $i = 2, 3$; therefore, $R_{P1,\mathrm{PC}(i)}$ is selected to plot $R_{\mathrm{EFF1},\mathrm{PC}(i)}$, as shown in Fig. 11. In the plot, the optimal point for PC(2) is identified at $R_{N,\mathrm{OPT},\mathrm{PC}(2)} = 29$ mΩ, corresponding to a minimum $R_{\mathrm{EFF1},\mathrm{PC}(2)}$ of 46mΩ. Similarly, for PC(3), the optimal point is at $R_{N,\mathrm{OPT},\mathrm{PC}(3)} = 20$ mΩ, with a minimum $R_{\mathrm{EFF1},\mathrm{PC}(3)}$ of 30 mΩ. Consequently, $R_{P,\mathrm{OPT},\mathrm{PC}(2)}$ and $R_{P,\mathrm{OPT},\mathrm{PC}(3)}$ are computed by substituting the respective optimal values of $R_{N,\mathrm{OPT},\mathrm{PC}(2)}$ and $R_{N,\mathrm{OPT},\mathrm{PC}(3)}$ into (16). Table I summarizes the optimal power MOSFET switch resistances, $R_{P,\mathrm{OPT},\mathrm{PC}(i)}$

TABLE I
OPTIMAL $R_{P,\mathrm{OPT},\mathrm{PC}(i)}$, $R_{N,\mathrm{OPT},\mathrm{PC}(i)}$, SWITCH WIDTHS, AND LOAD CURRENT RANGES FOR PC(1), PC(2), AND PC(3) TARGETING $\eta_{\mathrm{MIN},\mathrm{PC}(i)} = 85\%$

PC(i)	$\eta_{\mathrm{MIN,PC(i)}}$ (%)	$R_{\mathrm{P,OPT,PC(i)}}$ (mΩ)	$R_{\mathrm{N,OPT,PC(i)}}$ (mΩ)	$W_{\mathrm{P,OPT,PC(i)}}$ (mm)	$W_{\mathrm{N,OPT,PC(i)}}$ (mm)	$I_{\mathrm{O,MIN,PC(i)}}$ (A)	$I_{\mathrm{O,MAX,PC(i)}}$ (A)
PC(1)	85	∼ 158	∼ 78	∼ 32	∼ 26	∼ 0.3	∼ 1.0
PC(2)	85	∼ 50	∼ 29	∼ 118	∼ 95	∼ 1.0	∼ 2.5
PC(3)	85	∼ 31	∼ 20	∼ 226	∼ 182	∼ 2.5	∼ 3.0

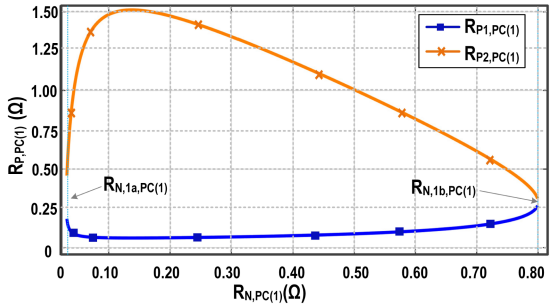


Fig. 12. Plot of $R_{P1,\mathrm{PC}(1)}$ and $R_{P2,\mathrm{PC}(1)}$ versus $R_{N,\mathrm{PC}(1)}$ within $R_{N,1a,\mathrm{PC}(1)} < R_{N,\mathrm{PC}(1)} < R_{N,1b,\mathrm{PC}(1)}$ for PC(1) at $\eta_{\mathrm{min}} = 80\%$.

and $R_{N,\mathrm{OPT},\mathrm{PC}(i)}$, along with their corresponding widths, $W_{P,\mathrm{OPT},\mathrm{PC}(i)}$ and $W_{N,\mathrm{OPT},\mathrm{PC}(i)}$, and the maximum supported load current for PC(1), PC(2), and PC(3).

To verify the tradeoff between efficiency flatness, phase count, and area, a second case is conducted using the same design specifications but with a reduced minimum fixed baseline efficiency target of 80% . All other design parameters remain unchanged. The relevant coefficients are computed in the same way as in the first case. The methodology in Fig. 4 is applied again, starting from the same minimum load current. The process begins with computing the discriminant $\Delta'_{\mathrm{PC}(i)}$ to determine the valid region for $R_{N,\mathrm{PC}(i)}$. In this case as well, $\Delta'_{\mathrm{PC}(i)} > 0$, which allows the evaluation of $\Delta'_{2,\mathrm{PC}(i)}$ and then $\Delta'_{1,\mathrm{PC}(i)}$, both of which are also positive. As a result, the valid solution regions for $R_{N,\mathrm{PC}(i)}$ in PC(1), PC(2), and PC(3) are as follows: $R_{\mathrm{INT},N,\mathrm{PC}(i)} < R_{N,\mathrm{PC}(i)} < R_{N,2a,\mathrm{PC}(i)}$, $R_{N,1a,\mathrm{PC}(i)} < R_{N,\mathrm{PC}(i)} < R_{N,1b,\mathrm{PC}(i)}$, and $R_{N,2b,\mathrm{PC}(i)} < R_{N,\mathrm{PC}(i)} < \infty$, where $i = 1, 2, 3$. In this case, the interval $R_{N,1a,\mathrm{PC}(1)} < R_{N,\mathrm{PC}(1)} < R_{N,1b,\mathrm{PC}(1)}$ yields valid and minimum values of $R_{P1,\mathrm{PC}(1)}$ and $R_{P2,\mathrm{PC}(1)}$ for PC(1), as shown in Fig. 12. Since $R_{P1,\mathrm{PC}(1)}$ is lower than $R_{P2,\mathrm{PC}(1)}$, it is used to plot $R_{\mathrm{EFF},\mathrm{PC}(1)}$, as shown in Fig. 13. In the plot, the optimal point is identified at the minimum $R_{\mathrm{EFF1},\mathrm{PC}(1)}$ of 80 mΩ, occurring at $R_{N,\mathrm{OPT},\mathrm{PC}(1)} = 45$ mΩ. Consequently, the optimal $R_{P,\mathrm{OPT},\mathrm{PC}(1)}$ is computed by substituting this value into (16). Similarly, for PC(2) and PC(3), valid and minimum values of $R_{P1,\mathrm{PC}(i)}$ and $R_{P2,\mathrm{PC}(i)}$ lie within the interval $R_{N,1a,\mathrm{PC}(i)} < R_{N,\mathrm{PC}(i)} < R_{N,1b,\mathrm{PC}(i)}$, where $i = 2$ and 3, respectively, as shown in Fig. 14. For both PC(2) and PC(3), $R_{P1,\mathrm{PC}(i)}$ is lower than $R_{P2,\mathrm{PC}(i)}$ and is therefore used to plot $R_{\mathrm{EFF},\mathrm{PC}(i)}$, as shown in Fig. 15. The plot also shows the optimal values of $R_{N,\mathrm{OPT},\mathrm{PC}(i)}$ as 15 and 13 mΩ, corresponding to the minimum $R_{\mathrm{EFF},\mathrm{PC}(i)}$

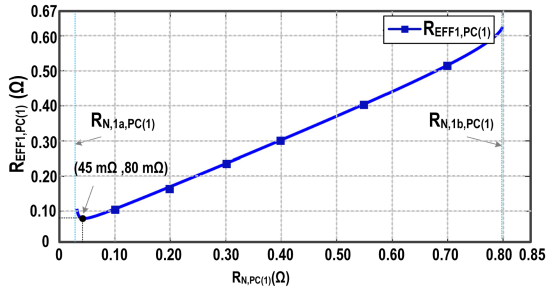


Fig. 13. Plot of $R_{\mathrm{EFF1},\mathrm{PC}(1)}$ versus $R_{N,\mathrm{PC}(1)}$ for PC(1) with R_N at $\eta_{\mathrm{min}} = 80\%$, indicating the optimal point.

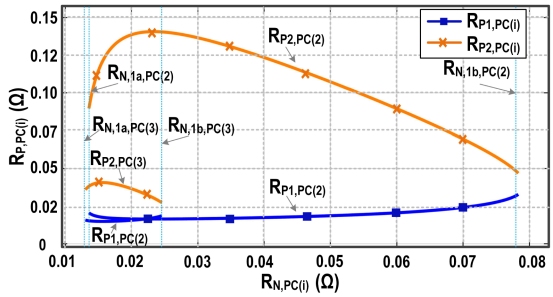


Fig. 14. Plot of $R_{\mathrm{EFF1},\mathrm{PC}(i)}$ plotted versus $R_{N,\mathrm{PC}(i)}$ for i = 2,3 at $\eta_{\mathrm{min}} = 80\%$.

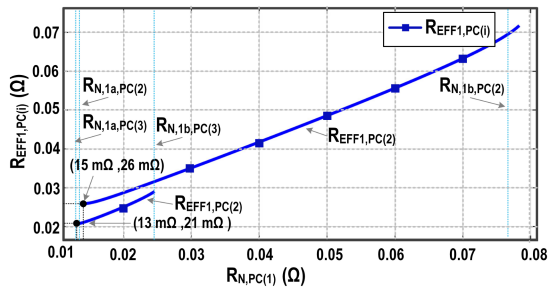


Fig. 15. Plot of $R_{\mathrm{EFF1},\mathrm{PC}(i)}$ plotted versus $R_{N,\mathrm{PC}(i)}$ for $i = 2,3$ at $\eta_{\mathrm{min}} = 80\%$.

TABLE II
OPTIMAL $R_{P,\mathrm{OPT},\mathrm{PC}(i)}$, $R_{N,\mathrm{OPT},\mathrm{PC}(i)}$, SWITCH WIDTHS, AND LOAD CURRENT RANGES FOR PC(1) AND PC(2) TARGETING $\eta_{\mathrm{MIN},\mathrm{PC}(i)} = 80\%$

PC(i)	$\eta_{\mathrm{MIN,PC(i)}}$ (%)	$R_{\mathrm{P,OPT,PC(i)}}$ (mΩ)	$R_{\mathrm{N,OPT,PC(i)}}$ (mΩ)	$W_{\mathrm{P,OPT,PC(i)}}$ (mm)	$W_{\mathrm{N,OPT,PC(i)}}$ (mm)	$I_{\mathrm{O,MIN,PC(i)}}$ (A)	$I_{\mathrm{O,MAX,PC(i)}}$ (A)
PC(1)	80	∼ 86	∼ 45	∼ 63	∼ 51	∼ 0.3	∼ 3.0
PC(2)	80	∼ 19	∼ 15	∼ 520	∼ 420	∼ 3.0	∼ 7.0
PC(3)	80	∼ 16	∼ 13	∼ 820	∼ 580	∼ 7.0	∼ 5.5

values of 26 and 21 mΩ for $i = 2$ and 3, respectively. Table II summarizes the optimal values of $R_{P,\mathrm{OPT},\mathrm{PC}(i)}$ and $R_{N,\mathrm{OPT},\mathrm{PC}(i)}$, along with the corresponding switch widths $W_{P,\mathrm{OPT},\mathrm{PC}(i)}$ and $W_{N,\mathrm{OPT},\mathrm{PC}(i)}$, and the supported load current ranges for $i = 1$, 2, and 3. As can be seen, relaxing the baseline efficiency to 80% increases the loss margin, allowing larger switch widths at the

TABLE III
OPTIMAL $R_{P,\mathrm{OPT,PC}(i)}$, $R_{N,\mathrm{OPT,PC}(i)}$, SWITCH WIDTHS, AND LOAD CURRENT RANGES FOR PC(I) AND $I = 1, 2$ AND 3 TARGETING ADAPTIVE $\eta_{\mathrm{MIN,PC}(i)}$ IN 1ST ITERATION

PC(i)	$\eta_{\mathrm{MIN,PC}(i)}$ (%)	$R_{\mathrm{P,OPT,PC}(i)}$ (mΩ)	$R_{\mathrm{N,OPT,PC}(i)}$ (mΩ)	$W_{\mathrm{P,OPT,PC}(i)}$ (mm)	$W_{\mathrm{N,OPT,PC}(i)}$ (mm)	$I_{\mathrm{O,MIN,PC}(i)}$ (A)	$I_{\mathrm{O,MAX,PC}(i)}$ (A)
PC(1)	86.4	∼ 257	∼ 123	∼ 19	∼ 16	∼ 0.3	∼ 0.5
PC(2)	86.7	∼ 178	∼ 87	∼ 28	∼ 23	∼ 0.5	∼ 0.6
PC(3)	86.7	∼ 123	∼ 62	∼ 42	∼ 34	∼ 0.6	∼ 0.9

TABLE IV
OPTIMAL $R_{P,\mathrm{OPT,PC}(i)}$, $R_{N,\mathrm{OPT,PC}(i)}$, SWITCH WIDTHS, AND LOAD CURRENT RANGES FOR PC(I) AND $I = 1, 2$ AND 3 TARGETING ADAPTIVE $\eta_{\mathrm{MIN,PC}(i)}$ IN 2ND ITERATION

PC(i)	$\eta_{\mathrm{MIN,PC}(i)}$ (%)	$R_{\mathrm{P,OPT,PC}(i)}$ (mΩ)	$R_{\mathrm{N,OPT,PC}(i)}$ (mΩ)	$W_{\mathrm{P,OPT,PC}(i)}$ (mm)	$W_{\mathrm{N,OPT,PC}(i)}$ (mm)	$I_{\mathrm{O,MIN,PC}(i)}$ (A)	$I_{\mathrm{O,MAX,PC}(i)}$ (A)
PC(1)	86.4	∼ 257	∼ 123	∼ 19	∼ 16	∼ 0.3	∼ 0.5
PC(2)	86.4	∼ 130	∼ 70	∼ 40	∼ 32	∼ 0.5	∼ 1.0
PC(3)	86.7	∼ 80	∼ 40	∼ 66	∼ 53	∼ 1.0	∼ 1.1

cost of greater silicon area. As a result, the supported load range increases due to reduced switch resistance. In Table II, the value of $I_{O,\mathrm{MAX,PC}(3)}$ is less than $I_{O,\mathrm{MIN,PC}(3)}$, as there is no valid solution at higher currents to achieve the fixed target baseline efficiency.

The two fixed baseline efficiency cases reveal a tradeoff: lowering the baseline improves load range but increases efficiency variation, while raising it flattens the efficiency profile but restricts the load range. This motivates a third case with variable baseline efficiency across the load range to balance both objectives. All other design parameters remain the same as in the previous cases. With the baseline efficiency raised to 90% , no feasible solution space is found, mainly due to the high switching frequency. The maximum baseline efficiency that yields a valid solution is 86.4% for PC(1), and 86.7% for both PC(2) and PC(3). Table III lists the optimized high-side ($R_{P,\mathrm{OPT,PC}(i)}$) and low-side ($R_{N,\mathrm{OPT,PC}(i)}$) resistances, their corresponding widths ($W_{P,\mathrm{OPT,PC}(i)}$ and $W_{N,\mathrm{OPT,PC}(i)}$), and the minimum ($I_{O,\mathrm{MIN,PC}(i)}$) and maximum ($I_{O,\mathrm{MAX,PC}(i)}$) load currents achieved using the proposed method for PC(1), PC(2), and PC(3). As observed from the table, the current spread for PC(1) is approximately 0.2 A, while for PC(2) it is only around 0.1 A. Since this range does not meet the design requirements, further iterations are needed to improve it. In the second iteration, the baseline efficiency is kept at 86.4% for PC(1), slightly reduced to 86.4% for PC(2) to widen the current spread, and maintained at 86.7% for PC(3). The updated optimised switch resistances, widths, and load current spreads for each phase configuration in this iteration are summarized in Table IV. As observed from the table, lowering the baseline efficiency for PC(2) increases the load current spread to approximately 0.5 A. However, for PC(3), the spread increases by only 0.1 A. Since this improvement is insufficient, the efficiency target for PC(3) must be further

TABLE V
OPTIMAL $R_{P,\mathrm{OPT,PC}(i)}$, $R_{N,\mathrm{OPT,PC}(i)}$, SWITCH WIDTHS, AND LOAD CURRENT RANGES FOR PC(I) AND $I = 1, 2$ AND 3 TARGETING ADAPTIVE $\eta_{\mathrm{MIN,PC}(i)}$ IN 3RD ITERATION

PC(i)	$\eta_{\mathrm{MIN,PC}(i)}$ (%)	$R_{\mathrm{P,OPT,PC}(i)}$ (mΩ)	$R_{\mathrm{N,OPT,PC}(i)}$ (mΩ)	$W_{\mathrm{P,OPT,PC}(i)}$ (mm)	$W_{\mathrm{N,OPT,PC}(i)}$ (mm)	$I_{\mathrm{O,MIN,PC}(i)}$ (A)	$I_{\mathrm{O,MAX,PC}(i)}$ (A)
PC(1)	86.4	∼ 257	∼ 123	∼ 19	∼ 16	∼ 0.3	∼ 0.5
PC(2)	86.4	∼ 130	∼ 70	∼ 40	∼ 32	∼ 0.5	∼ 1.0
PC(3)	86.6	∼ 70	∼ 40	∼ 82	∼ 66	∼ 1.0	∼ 1.4

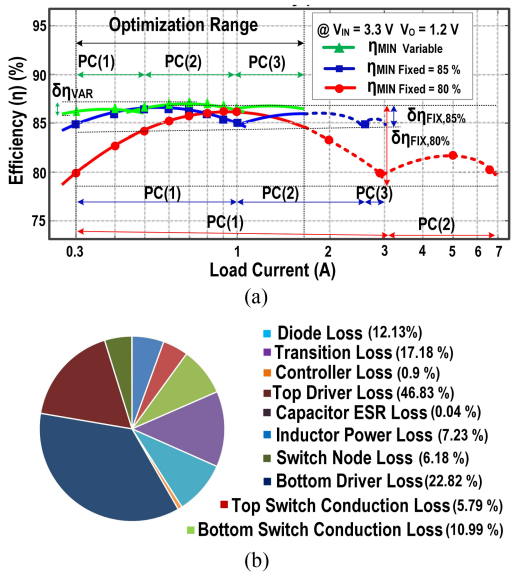


Fig. 16. (a) Comparison of efficiency profiles and total efficiency deviation ($\delta\eta$) for different case studies. (b) Loss distribution pie chart for η_{Variable} at 1.4 A.

relaxed. In the next iteration, the baseline efficiency is kept at 86.4% for both PC(1) and PC(2), and reduced to 86.6% for PC(3). The resulting optimized switch resistances and widths, along with the corresponding current spread, are presented in Table V. This iterative process can continue until a suitable tradeoff between efficiency flatness and phase-specific current spread is achieved, based on the designer's requirements.

To comparatively evaluate the three case studies as sized in Tables I, II, and V, Fig. 16(a) plots their efficiency curves, highlighting the total efficiency variation ($\delta\eta$) and the number of phases required in each case within the optimization range. The optimization range is fixed to ensure a fair comparison of efficiency, flatness, and phase utilisation across the different design strategies. As seen from the plot, for the case with a fixed baseline efficiency of $\eta_{\mathrm{MIN}} = 80\%$, the converter achieves the optimisation range using only PC(1) (single phase). However, this comes at the cost of a large efficiency variation ($\delta\eta_{\mathrm{FIX,80\%}}$), caused by switching losses at light load (0.3 A–1 A) and conduction losses at high load (1 A–1.4 A), resulting in suboptimal switch sizing, and reduced efficiency at both ends of the optimization range. In the next case, increasing the baseline efficiency to $\eta_{\mathrm{MIN}} = 85\%$

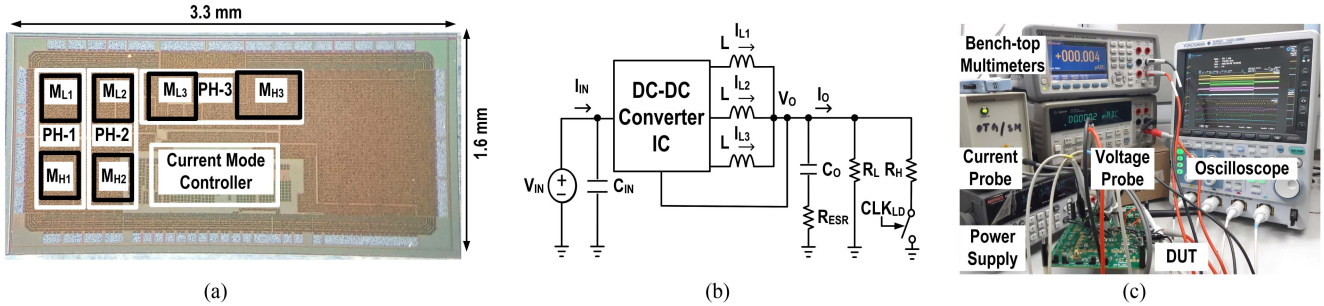


Fig. 17. (a) Chip micrograph. (b) Application circuit. (c) Experimental test set-up.

reduces the efficiency variation ($\delta\eta_{\text{FIX},85\%} < \delta\eta_{\text{FIX},80\%}$) by utilizing PC(2) (two phases) to span the load range. As shown in Table I, the switch size of PC(1) is smaller than its counterpart in Table II, effectively reducing switching losses at light loads. To address conduction losses at higher loads, PC(2) uses a larger switch than PC(1) in Table II. These results further validate the effectiveness of the proposed optimization methodology. To further flatten the efficiency curve, the third case employs a variable baseline efficiency target across the load range, enabling a flatter efficiency profile by utilizing three phases. Fig. 16(b) shows its loss distribution at a high load of 1.4 A.

The fixed baseline efficiency across the entire optimization range limits the ability to achieve maximum efficiency flatness, as it prevents the method from precisely identifying the regions where switching or conduction loss dominates, and accordingly selecting optimal switch sizes. By changing the baseline efficiency to the dominant loss mechanism across different load conditions, this approach achieves the lowest efficiency variation ($\delta\eta_{\text{VAR}} < \delta\eta_{\text{FIX},85\%} < \delta\eta_{\text{FIX},80\%}$), while covering the same load range with PC(3) (three phases). This case also gives the designer an extra degree of freedom to trade off between efficiency variation and phase count, depending on system priorities. It represents the best balance between efficiency, flatness, and phase count. Therefore, this case is selected for further experimental validation by implementing it in 180 nm CMOS technology, as detailed in the following section.

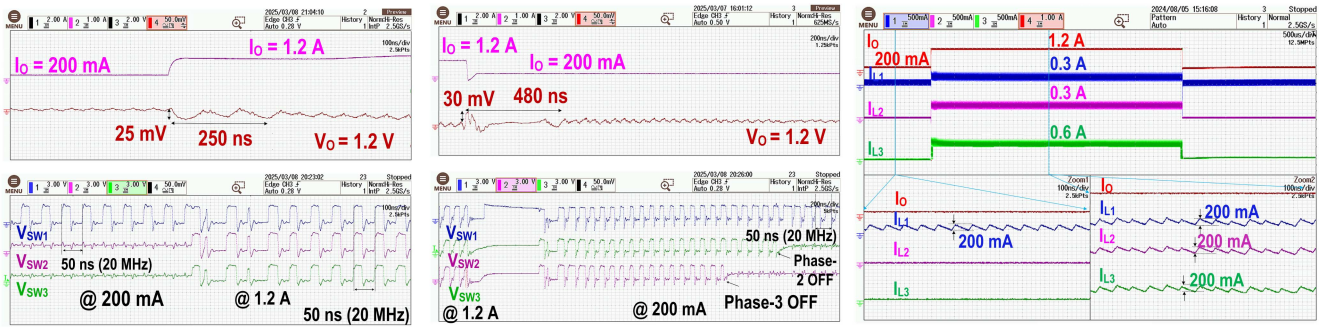
IV. Experimental Results

Using the proposed methodology, the optimal switch sizes derived from the third case are used to implement the current-mode dc–dc converter. This design is fabricated using a 180-nm CMOS technology, and the chip micrograph is shown in Fig. 17(a). The converter operates at a switching frequency (f_{SW}) of 20 MHz, with an input voltage range of 2.7–3.3 V and a fixed output voltage of 1.2 V. The converter is designed to support a maximum load current of 1.4 A. Fig. 17(b) shows its application circuit. Each phase employs an inductor of 100 nH (TDK, part no. TFM252012ALMAR10MTAA). The output capacitor (C_O) is chosen as 4.7 μF (Murata, part no. GRM188Z71A475KE15D), with an equivalent series resistance (R_{ESR}) of 10 mΩ. To mimic load transients, R_L and R_H are added with a power switch driven by a clock CLK_{LD}. Fig. 17(c) shows the typical experimental test setup of the prototype.

Fig. 18(a) shows the load transient response for a load (I_O) step-up from 0.2 to 1.2 A along with its corresponding switch-node voltages. At $I_O = 200$ mA, only one phase (V_{SW1}) is active. At $I_O = 1.2$ A, all three phases (V_{SW1}, V_{SW2}, V_{SW3}) are turned ON. The output voltage V_O recovers from an undershoot of 25 mV in 250 ns. Similarly, Fig. 18(b) presents the load step-down response from 1.2 to 0.2 A along with its associated switch-node voltages. In this case, an overshoot of 30 mV at V_O is observed with a recovery time of 480 ns. The converter operates at a switching frequency of 20 MHz. Fig. 18(c) shows the average phase currents at both load levels. At $I_O = 200$ mA, the entire current is supplied by a single phase [PC(1)]. At $I_O = 1.2$ A, all three phases are activated. In this condition, Phase 1 (I_{L1}) and Phase 2 (I_{L2}) each carry an average current of 0.3 A, while Phase 3 (I_{L3}) supplies an average current of 0.6 A.

Fig. 19 shows the measured efficiency of the fabricated converter in a load current range of 0.2–1.4 A, under input supply voltages of 2.7–3.3 V. The optimized switch sizes obtained using the proposed design methodology are listed in Table V. As observed in the plot (at $V_{\text{IN}} = 3.3$V and $V_O = 1.2$V), the efficiency profile remains maximally flat with a variation of $\sim$1% . It maintains an efficiency of $\sim$85% throughout the optimisation range. However, compared to the theoretical efficiency of $\sim$86% [shown in Fig. 16(a)], the measured result shows a degradation of less than 2% . This degradation can be attributed to the following. In the theoretical design methodology, effects such as PCB trace resistance, bond-wire parasitics and inductor core losses have not been considered. Also, using the proposed design methodology, the efficiency is optimised at $V_{\text{IN}} = 3.3$ V to account for maximum loss scenarios. At $V_{\text{IN}} = 2.7$ V, the efficiency increases to $\sim$90% due to reduced switching loss. These results demonstrate the effectiveness of the proposed design methodology. The measured results are in close agreement with the theoretical prediction. The efficiency profile is maximally flat with $\sim$1% variation across the optimisation range at both input voltages.

To evaluate the effectiveness of the proposed design methodology, a performance comparison with state-of-the-art works is presented in Table VI. Among all the works compared, the proposed design methodology achieves the lowest efficiency variation ($\sim$1%) throughout the optimisation range, while using only three phases. This is achieved by adopting a variable baseline efficiency strategy across different load sub-ranges. To more accurately compare the variations in the efficiency



(a) (b) (c)

Fig. 18. Transient response for: (a) load step-up of 0.2–1.2 A, (b) load step-down of 1.2–0.2 A, and (c) average inductor current in each phase at $I_O = 0.2$ A and $I_O = 1.2$ A.

TABLE VI
PERFORMANCE COMPARISON WITH RECENT WORKS

References	JSSC 2015 [18]	TPE 2015 [33]	JSSC 2018 [24]	JSSC 2019 [28]	ISSCC 2019 [17]	JSSC 2023 [30]	This Work
Technology (nm)	65 CMOS	130 BCDMOS	180 CMOS	350 CMOS	28 CMOS	180 CMOS	180 CMOS
Switching Frequency f_{SW} (MHz)	30	2.25	30	25	75	25	20
Input Voltage V_{IN} (V)	1.8	2.8-5	3.3	3.3	1.2	1.8	2.7-3.3
Output Voltage V_O (V)	0.7-1.2	0.68-1.92	0.7-3	0.3-2.6	0.6-1	0.6-1.5	1.2
Inductor/Phase L (nH)	90	470	220	200	15	60	100
Output Capacitor C_O (μF)	0.47	88	0.62	2.47	0.2	1.2	4.7
Phase Count	4	4	4	4	4	4	3
Peak Efficiency η_{max} (%) @ ($V_{IN} - V_O$) (V)	87 @ (1.8 - 1)	90 @ (3.7 - 1)	88 @ (3.3 - 2.5)	88 @(3.3 - 2.5)	89 @ (1.2 - 1)	90 @ (1.8 - 1.2)	90 @(2.7-1.2)
Min. Efficiency η_{min} (%) @ ($V_{IN} - V_O$) (V)	80 @ (1.8 - 1)	85 @ (3.7 - 1)	86 @ (3.3 - 2.5)	77 @ (3.3 - 2.5)	84 @ (1.2 - 1)	80 @ (1.8 - 1.2)	89 @(2.7-1.2)
Load Range I_O (A)	0.02-0.8	0.1-4	0.1-2.5	0.1-6	0.1-1.2	0.1-4	0.2-1.4
Max. Efficiency Variation ($\eta_{max} - \eta_{min}$) (%)	< 7	< 5	< 3	< 11	< 5	< 10	~1
FoM @ ($I_O(2) - I_O(1)$) A	0.75 @ (0.7 - 0.2)	10 @ (0.7 - 0.2)	0.30 @ (0.7 - 0.2)	1.98 @ (0.7 - 0.2)	0.24 @ (0.7 - 0.2)	0.72 @ (0.7 - 0.2)	0.45 @ (0.7 - 0.2)
FoM @ ($I_O(3) - I_O(2)$) A	NA	1.4 @ (1.4 - 0.7)	0.21 @ (1.4 - 0.7)	0.13 @ (1.4 - 0.7)	0.21 @ (1.4* - 0.7)	0.26 @ (1.4 - 0.7)	0.15 @ (1.4 - 0.7)

FoM = $\frac{\Delta\eta}{\Delta I_0} \cdot \frac{f_{SW,lowest}}{f_{SW}}$ *Extrapolation of efficiency plot

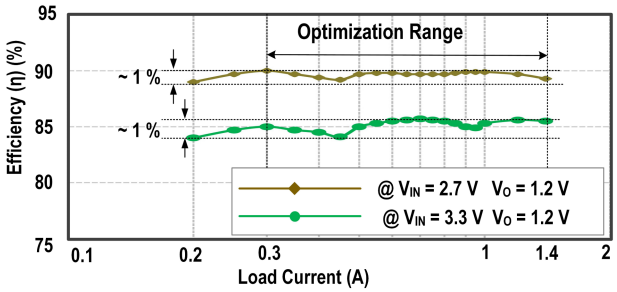


Fig. 19. Efficiency curve with the proposed switch sizes.

curve, the entire load range is divided into two sub-ranges, and flatness is quantified using a Figure of Merit (FoM), computed separately for each. For a fair comparison, the FoM is defined as $(\frac{\Delta\eta}{\Delta I_O}) \cdot (\frac{f_{SW,lowest}}{f_{SW}})$, where $\Delta\eta$ represents the variation in efficiency over the load current range ΔI_O, and $f_{SW,lowest}$ is the lowest switching frequency among the compared works. The first term, $(\Delta\eta/\Delta I_O)$, quantifies the flatness of the efficiency curve by measuring the slope of the efficiency curve. The second term, $(f_{SW,lowest}/f_{SW})$, normalises the comparison by taking into account different operating f_{SW}. A lower FoM indicates a better design. As the work in [17] implemented in a much lower technology node and efficiency is measured at low drop-out ($V_{IN} - V_O$) condition, it provides a slightly better FoM of 0.24 compared to this work in the load range of 0.2–0.7 A. In addition, it uses four phases with additional component counts. Similarly, the work in [24] achieves a FoM of 0.3 in the load range of 0.2–0.7 A using four phases that are activated at a load current of 0.65 A. Thus, these works ([17], [24]) not only require an extra phase with additional component count, but also the FoM degrades in the high load range (0.7− 1.4 A) due to unoptimized phase sizing and phase counts. Hence, efficiency variation in the entire load range is higher compared to this work. In summary, the proposed design methodology helps to achieve superior flatness with a low efficiency variation ($\sim 1\%$) in the load range with a smaller number of phase counts.

V. CONCLUSION

This work presents an analytically guided, discriminant-aided design methodology that determines both the optimal number of active phases and their corresponding power MOSFET switch sizes to flatten the efficiency profile over a wide load range in multiphase dc–dc converters. To further reduce design efforts, a discriminant-aided process is introduced to quickly check the feasibility of input design specifications by checking the sign (positive/negative) of the discriminant that helps in getting the valid solution space to search for minimum $R_{EFF,PC(i)}$, significantly reducing computational complexity and design iteration time compared to conventional trial-and-error approaches. The effectiveness of the methodology is validated through multiple efficiency-driven case studies, demonstrating its adaptability to

various design scenarios. Among these, the variable baseline efficiency in different load subranges offers a better tradeoff between flatness and phase counts. Therefore, the variable baseline efficiency is adopted to implement a current-mode dc–dc converter. The measured result shows an efficiency variation of $\sim$1% in the entire load range of 0.2–1.4 A.

Appendix A

The individual losses in the converter [32] are summarized here. The gate drive loss, caused by charging and discharging the gate capacitance of the high-side and low-side switches ($M_{P,\mathrm{PC}(i)}$ and $M_{N,\mathrm{PC}(i)}$) in each switching cycle, is given by (27). The inverter chain inside the gate drivers, which drives the power MOSFET switches, dissipates power due to the switching action, as calculated using (28). The transition loss and the diode conduction loss are given by (29) and (30). The controller's quiescent power loss is given by (31). Conduction losses arise from the load and ripple currents flowing through the resistive elements of the converter as given by (32)

$$P_{G,L,\mathrm{PC}(i)} = (C_{G,P,PC(i)} + C_{G,N,PC(i)}) \cdot V_{IN}^2 \cdot f_{SW} \tag{27}$$

$$P_{\mathrm{DR},L,\mathrm{PC}(i)} = T_F(\tau) \cdot (C_{G,P,\mathrm{PC}(i)} + C_{G,N,\mathrm{PC}(i)}) \cdot V_{\mathrm{IN}}^2 \cdot f_{\mathrm{SW}} \tag{28}$$

$$P_{\mathrm{TR},L,\mathrm{PC}(i)} = V_{\mathrm{IN}} \cdot f_{\mathrm{SW}} \cdot t_{R/F} \cdot I_O \tag{29}$$

$$P_{\mathrm{DI},L,\mathrm{PC}(i)} = 2 \cdot V_{\mathrm{DI}} \cdot I_O \cdot t_{\mathrm{DB}} \cdot f_{\mathrm{SW}} \tag{30}$$

$$P_{\mathrm{CT},L,\mathrm{PC}(i)} = V_{\mathrm{IN}} \cdot I_Q \tag{31}$$

$$\begin{aligned} P_{\mathrm{CD},L,\mathrm{PC}(i)} = {} & I_O^2 \cdot \{D \cdot R_{P,\mathrm{PC}(i)} + (1-D) \\ & \cdot R_{N,\mathrm{PC}(i)} + R_{\mathrm{DC}}/\mathrm{PC}(i)\} \\ & + \frac{\Delta I_O^2}{12} \cdot \left\{D \cdot R_{P,\mathrm{PC}(i)} + (1-D) \cdot R_{N,\mathrm{PC}(i)} + R_{\mathrm{ESR}}\right\}. \end{aligned} \tag{32}$$

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