DC Fault Modeling of Arm-Shared DC Transformers for Multivoltage HVDC Grids

Yilin Wu, *Student Member, IEEE*, Zhiyuan He, *Senior Member, IEEE*, Guangfu Tang, *Senior Member, IEEE*, Chong Gao, *Member, IEEE*, Zhiguang Lin, and Xinying Wang

***Abstract*—Short-circuit current calculations and fault characterizations are essential for designing protection systems and reducing fault hazards. Fault modeling for dc transformers connected to dc systems of different voltage levels is understudied. First, this article establishes a simple dc fault model for arm-shared dc transformers (ASDCTs) based on RLC circuits and equivalent current sources. Second, an improved dc fault model is proposed by characterizing the dynamic properties of the arms and the collapse of the internal ac system, which demonstrates long-term accurate performance (up to 50 ms) and can characterize the conduction of fault stress through ASDCT. The accuracy and durability of the proposed simple dc fault model and improved dc fault model are validated by means of a comparative analysis with the hardware-in-the-loop test waveforms.**

***Index Terms*—DC fault model, dc transformer (DCT), modular multilevel converter (MMC), multivoltage dc grid, short-circuit current.**

I. Introduction

THE demand for low-carbon and cleaner energy consumption is driving the development, transmission, and use of renewable energy, requiring the grid to upgrade its infrastructure to be more controllable and flexible. High-voltage direct current (HVDC) transmission and HVDC grid, especially based on the modular multilevel converter (MMC) [1], with higher control of the grid and higher transmission efficiency, are considered to be a prospective solution for the grid connection of offshore wind farms and the long-distance bulky-power transmission of renewable energy [2]. DC transformer (DCT) is the hub equipment of dc grid. It is required to interconnect two dc systems with different voltage levels. It will play an important role in the scene of new energy collection and transmission. For example, a new energy dc collection grid needs to be connected to an HVDC line to supply power to remote load centers, as shown in Fig. 1(a). Or at the receiving end of HVDC, multiple landing points with a lower voltage level need to be formed, as shown in Fig. 1(b).

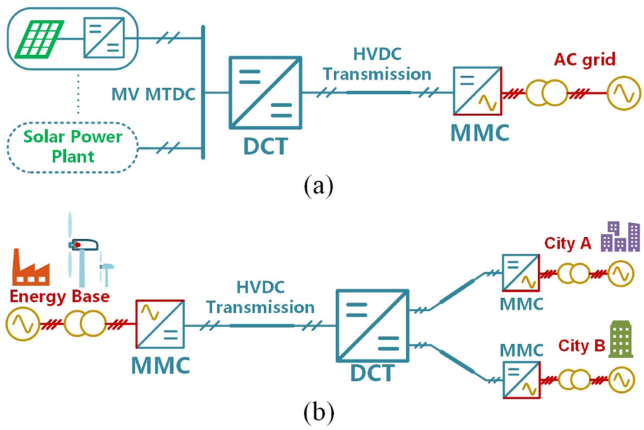

Fig. 1. Application scenarios of DCT. (a) New energy DC collection and transmission system. (b) HVDC with multiple landing points.

Several high-voltage (HV) bulk-capacity DCT topologies for HVDC grids have been proposed, including isolated DCTs and nonisolated DCTs. The isolated DCT consists of two ac–dc converters (usually MMCs) connected by an ac isolation transformer [3], [4], and the overall voltage or capacity can be increased by connecting multiple DCT ports in series or parallel [5], but this is rarely used in HVDC due to the limited insulation of ac transformers. The nonisolated DCTs override the isolation transformer, and the voltage conversion depends on the converter unit. In [6] and [7], a single-stage MMC DCT topology is introduced, in which two submodule (SM) arms are connected in series to transform the dc voltage. Ac paths are constructed for the energy balancing of SMs, and large passive filters are required to limit the ac voltage inside the DCT. In [8], an ac transformer is used to transfer the power flow for energy balancing, avoiding the use of passive filters. Tang et al. [9] reported an arm-shared dc transformer (ASDCT) consisting of three sets of SM arms, two of which are connected separately to the HV and low voltage (LV) ports, while the other set is shared. Some of the arms can also be replaced with series-connected IGBTs, thyristors, or doides [10], [11],

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Yilin Wu and Zhiguang Lin are with the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Beijing 102206, China, and also with State Key Laboratory of Advanced Power Transmission Technology, China Electric Power Research Institute Company Ltd., Beijing 102211, China (e-mail: wuyilin_510@ncepu.edu.cn; linzhiguang@epri.sgcc.com.cn).

Zhiyuan He, Guangfu Tang, Chong Gao, and Xinying Wang are with the State Key Laboratory of Advanced Power Transmission Technology, China Electric Power Research Institute Company Ltd., Beijing 102211, China (e-mail: hezhiyuan@epri.sgcc.com.cn; gftang@hrl.ac.cn; gaochong@epri.sgcc.com.cn; wangxinying@bise.hrl.ac.cn).

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[12]. The voltage conversion of ASDCT is entirely achieved by power electronic arms. Moreover, the ac components between the arms cancel each other out, with only the dc component being output at the ports. Hence, the ASDCT eliminates the need for ac transformers or large-scale filtering equipment. Given that its main components have already been maturely applied in engineering practices involving MMCs and line-commutated converter-based high-voltage direct current (HVDC) systems, the ASDCT exhibits significant advantages, such as high efficiency [13], compactness, and low device usage [14].

For dc systems, dc short-circuit faults are important extreme transient events that can jeopardize equipment safety. Modeling of fault transients and calculation of short-circuit currents are required to evaluate converter fault stress, fault protection, and circuit breaker configurations. Fault modeling methods for MMC-based dc systems have been studied in several works of literature. However, transient modeling studies of DCT are rarely reported. In [15], [16], and [17], a generic pole-to-pole (PTP) short-circuit fault current calculation method for the dc grid is proposed based on a simplified RLC equivalent of MMC. Ac currents and outer controller characteristics are taken into account as a parallel ideal power supply in [18], [19], and [20], and the model is sufficiently accurate within 10 ms of a dc fault. Detailed modeling that considers the switching process of the SMs can accurately simulate transient processes over longer time scales [21]. In [22], a discrete-time fault model associated with a piecewise analysis is proposed to assess the long-term evolution of ac-side fault currents accurately. However, the discrete models considering SM switching require more computational resources than average models and face the problem of increased computation volume and longtime consumption in engineering cases with a large number of SMs.

Multivoltage dc systems containing DCTs have more complex fault characteristics. The effects of the faults can be coupled to other subsystems through the DCTs, which may lead to incorrect converter blocking or false operation of dc circuit breakers due to the sensitivity of the protection device. There is no simple model for the transient analysis of DCTs, and the fault characterization of multivoltage dc systems requires the use of electromagnetic transient simulation, which is accurate but inefficient. Based on the above-mentioned analysis, the following work is worthy of attention in DCT fault modeling.

1) Approaches based on averaging-based RLC equivalent circuits should be used in DCT fault modeling to ensure that the model is sufficiently streamlined, thereby enabling efficient fault analysis and low computational resource requirements.
2) Verify whether the existing fault modeling methods of MMC systems are applicable to DCTs.
3) The DCT fault models need to take into account the dynamic characterization of the nonfaulted ports, which is key to evaluating the conduction of fault stresses across dc subsystems of different voltages.
4) Extend the effective duration of the fault model to serve the evaluation of strategies, such as nonblocking fault protection and fault ride-through.

Based on the above-mentioned requirements, this article first deduces the traditional RLC equivalent modeling method of ASDCT and analyzes its limitations. Furthermore, an improved model is proposed to enhance the accuracy and effective duration of fault analysis. The main contributions and innovations are two-fold. 1) A dual-coupled controlled source circuit is used to replace the equivalent capacitance for characterizing the dynamic properties of the arms, and an ac equivalent layer is added between the control and equivalent circuits to simulate the internal ac voltage collapse. 2) An improved ASDCT fault model is proposed, which can accurately equate various types of faults and the conduction of fault stresses in a long-time scale (effective duration up to 50 ms).

The remainder of this article is organized as follows. Section II gives the topology, operating principle, and control schemes of the ASDCT. Section III presents the simple dc fault model for the ASDCT. In Section IV, the improved fault model is derived by characterizing the dynamic properties of the arms and the collapse of the internal ac system. The influence of line models, fault locations, and transition resistances on the proposed model is evaluated in Section V. In Section VI, the model calculations are validated against the experimental waveforms. Finally, Section VII concludes this article.

II. Topology and Control of ASDCT

A. Topology and Operating Principle

The ASDCT adopts the concept of full power electronics, and its conversion function relies entirely on modular multilevel arms. The basic circuit topology of the ASDCT is shown in Fig. 2(a). It is composed of two phase units (j = a, b), each of which consists of three arms (arm-H, arm-L, and arm-W) connected in a "T" shape. Two phase units are connected in parallel, except for the common point of arms, named "point S." Each arm contains a string of SMs and an inductor in series connection. The SMs of arm-H and arm-W are half-bridge (HBSM) structures, respectively, while the design on the structure of the SMs in arm-L is full-bridge (FBSM). The symmetrical structure can be formed by connecting the ground points of a co-negative ASDCT and a co-positive ASDCT, as shown in Fig. 2(b), which may be a more commonly used structure since most of the existing HVDC projects mainly use symmetrical monopolar or symmetrical bipolar configuration.

Take the unipolar two-phase topology [see Fig. 2(a)] as an example to introduce the working principle of the ASDCT. The operating principles of symmetrical structures can be deduced by analogy. To begin, represent the SM number of each arm with N_{X} (X = H, W, L). By controlling the state of IGBTs, the HBSMs output 0 or the SM capacitor voltage (u_{C}). Therefore, the string of HBSMs can output approximately continuous voltage shapes ranging from 0 to $N_{\mathrm{X}}u_{\mathrm{C}}$. Correspondingly, FBSMs can output three voltage values, u_{C}, 0, and $-u_{\mathrm{C}}$, which means that the output voltage waveform of the string of FBSMs can be either positive or negative, ranging from $-N_{\mathrm{X}}u_{\mathrm{C}}$ to $N_{\mathrm{X}}u_{\mathrm{C}}$. As shown in Fig. 3, with specific control strategies and reference waves, each of the SM strings can be equivalent to a dc

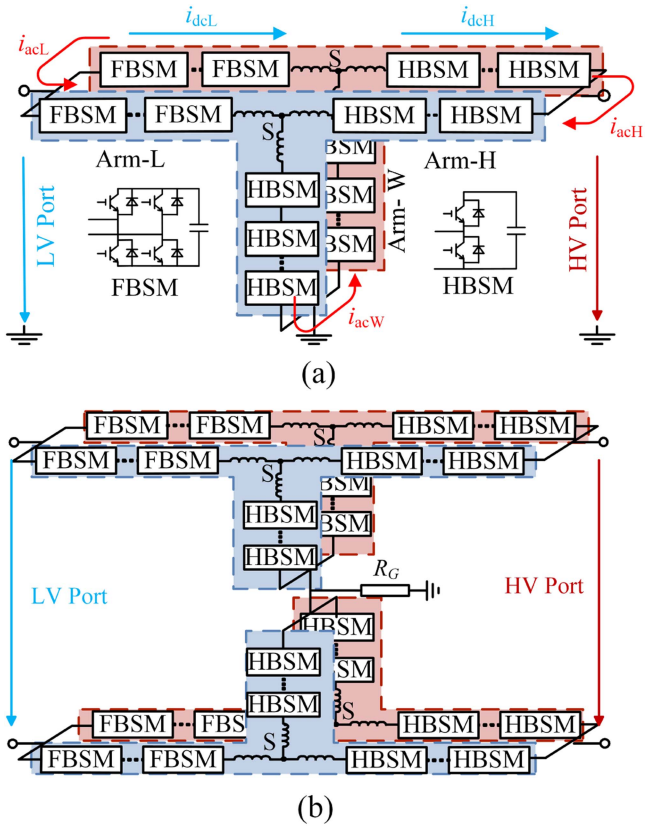

Fig. 2. Topology of the ASDCT. (a) Basic topology. (b) Bipolar topology.

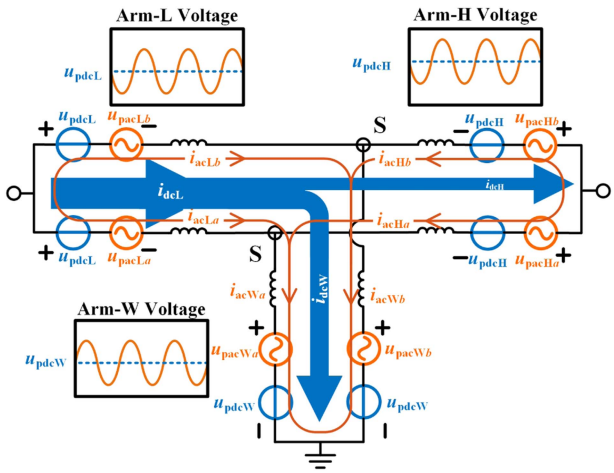

Fig. 3. Equivalent circuit and current distribution of ASDCT.

voltage source ($u_{\mathrm{pdcH}}, u_{\mathrm{pdcW}}, u_{\mathrm{pdcL}}$) and an ac voltage source ($u_{\mathrm{pacH}j}, u_{\mathrm{pacW}j}, u_{\mathrm{pacL}j}$) connected in series.

Each equivalent voltage source generates a corresponding current component. The dc currents ($i_{\mathrm{dcH}}, i_{\mathrm{dcW}}, i_{\mathrm{dcL}}$) established by arm dc voltage sources transfer power between LV and HV ports. The ac currents ($i_{\mathrm{acH}j}, i_{\mathrm{acW}j}, i_{\mathrm{acL}j}$) are constructed to ensure effective counteracting of any energy absorption or release of arms caused by the dc currents and remaining capacitance voltages of the SMs constant. Therefore, the dc and ac components of the arms satisfy the power constraint

$$0.5u_{\mathrm{pdcH}}i_{\mathrm{dcH}} = -\frac{1}{T}\int_T u_{\mathrm{pacH}j}i_{\mathrm{acH}}\mathrm{d}t \tag{1}$$

$$0.5u_{\mathrm{pdcW}}i_{\mathrm{dcW}} = \frac{1}{T}\int_T u_{\mathrm{pacW}j}i_{\mathrm{acW}}\mathrm{d}t \tag{2}$$

$$0.5u_{\mathrm{pdcL}}i_{\mathrm{dcL}} = -\frac{1}{T}\int_T u_{\mathrm{pacL}j}i_{\mathrm{acL}}\mathrm{d}t. \tag{3}$$

In order to ensure the outputs of the ASDCT do not include the ac voltage and ac current, the ac voltages of arm-H and arm-L ($u_{\mathrm{pacH}j}, u_{\mathrm{pacL}j}$) must cancel the ac voltage of arm-W ($u_{\mathrm{pacW}j}$), and the ac currents of each arm must be symmetrical. The ac voltage relationship for each arm is expressed as

$$\begin{aligned} u_{\mathrm{pacH}j} + L_{\mathrm{H}}\frac{\mathrm{d}i_{\mathrm{acH}j}}{\mathrm{d}t} &= u_{\mathrm{pacL}j} + L_{\mathrm{L}}\frac{\mathrm{d}i_{\mathrm{acL}j}}{\mathrm{d}t} \\ &= -u_{\mathrm{pacW}j} - L_{\mathrm{W}}\frac{\mathrm{d}i_{\mathrm{acW}j}}{\mathrm{d}t} \end{aligned} \tag{4}$$

where the ac currents meet

$$i_{\mathrm{acXa}} = -i_{\mathrm{acXb}}, \mathrm{X} = \mathrm{H}, \mathrm{W}, \text{ or } \mathrm{L}. \tag{5}$$

Hence, the port voltages are given by

$$u_{\mathrm{dcH}} = u_{\mathrm{pdcH}} + u_{\mathrm{pdcW}} \tag{6}$$

$$u_{\mathrm{dcL}} = u_{\mathrm{pdcL}} + u_{\mathrm{pdcW}}. \tag{7}$$

B. Circuit Design

For economic reasons, the design of the arm voltage components follows.

1) The dc voltage of arm-W (u_{pdcW}) is set to be equal to the LV port voltage (u_{dcL}). Therefore, the dc voltage of arm-L (u_{pdcL}) is set to 0, and the dc voltage of arm-H (u_{pdcH}) is set to ($u_{\mathrm{dcH}} - u_{\mathrm{dcW}}$).
2) Set the ac voltage amplitude (U_{ac}) equal to u_{pdcW}.

The summation of the SM voltages for each arm should provide the required maximum output value, which is the superposition of the dc voltages and ac voltages. The number of SMs to be configured for each arm can be calculated as

$$N_{\mathrm{H}} = (u_{\mathrm{pdcH}} + U_{\mathrm{ac}})/V_{\mathrm{cN}} = u_{\mathrm{dcH}}/V_{\mathrm{cN}} \tag{8}$$

$$N_{\mathrm{L}} = U_{\mathrm{ac}}/V_{\mathrm{cN}} = u_{\mathrm{dcL}}/V_{\mathrm{cN}} \tag{9}$$

$$N_{\mathrm{W}} = (u_{\mathrm{pdcW}} + U_{\mathrm{ac}})/V_{\mathrm{cN}} = 2u_{\mathrm{dcL}}/V_{\mathrm{cN}} \tag{10}$$

where V_{cN} is the rated capacitor voltage of SMs.

If the LV port requires voltage regulation function, the number of additional SMs for arm-L needs to be increased

$$N_{\mathrm{L}} = (U_{\mathrm{ac}} + \Delta u_{\mathrm{dcL}})/V_{\mathrm{cN}} = (u_{\mathrm{dcL}} + \Delta u_{\mathrm{dcL}})/V_{\mathrm{cN}} \tag{11}$$

where Δu_{dcL} is the voltage regulation range of the LV port.

The power factor of the internal ac system of ASDCT affects the transmission efficiency, the effective value of the arm current, and the quantity of SMs. Therefore, in the design of arm inductors, the minimum boundary of the power factor should be

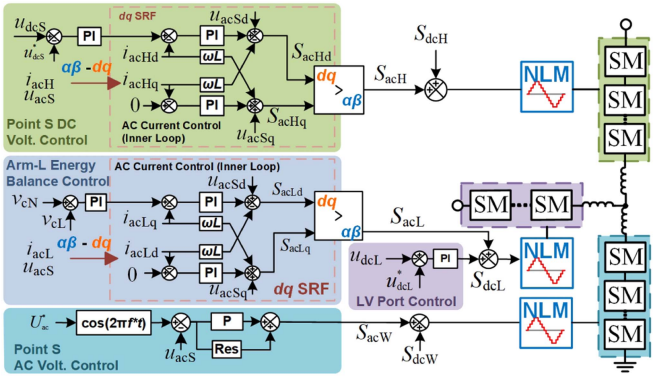

Fig. 4. Control schemes for the ASDCT.

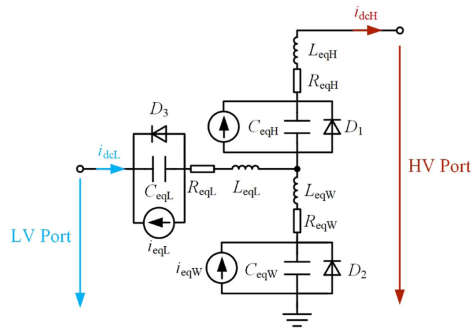

Fig. 5. Simple DC fault model of the ASDCT ($u_{\mathrm{dcL}} > u_{\mathrm{dcS}}$).

taken into consideration

$$\begin{cases} L_{\mathrm{armX}} = \dfrac{U_{\mathrm{ac}}^2 \tan\varphi_{\mathrm{X}}}{\omega u_{\mathrm{pdcX}} i_{\mathrm{dcX}}}, \text{X=H, W, L} \\ \cos\varphi_{\mathrm{X}} \geq 0.95 \end{cases} \tag{12}$$

where φ_{X} is the power factor angle of each arm.

C. Control Schemes

Appropriate control schemes for the ASDCT are developed in Fig. 4, including point S dc voltage control, point S ac voltage control, LV port control, and arm-L energy balance control. The arm-W produces the internal ac voltage through a proportional–resonant (PR) controller. According to (1) and (2), the arm-H and arm-L need to determine the ac currents to maintain the power balance. Hence, the dc voltage at point S is controlled by arm-H, which is configured with a proportional–integral (PI) controller at the outer loop of the vector current controller derived in the *dq* synchronous reference frame. The arm-L controls the voltage of the LV port by adjusting its dc output, and balances the energy stored in its SMs with the help of the ac component. The reference signals output by the control blocks are modulated to generate the status commands of SMs. The modulation technology used in this article is the nearest level modulation, which is suitable for converters with a large number of SMs.

In this control strategy, the energy balance control of arm-H and arm-W is discarded. A self-balancing mechanism is used as an alternative. Because the reference signals of arms corresponding to the dc component of arm-H and arm-W(S_{dcH} and S_{dcH}) are constant, the SM capacitance voltages v_{cH} and v_{cW} are linearly related to the point S dc voltage u_{dcS}. Therefore, in the control design, the reference dc voltages for arm-H and arm-W are set to $(u_{\mathrm{dcHN}} - u_{\mathrm{dcS}}^*)$ and u_{dcS}^* (where u_{dcHN} is the HV side rated voltage and u_{dcS}^* is the point S dc voltage reference). The energy balance of arm-H and arm-W is indirectly maintained by the point S dc voltage control

$$V_{\mathrm{cH}} = \frac{u_{\mathrm{dcH}} - u_{\mathrm{dcS}}}{N_{\mathrm{H}} S_{\mathrm{dcH}}} = \frac{u_{\mathrm{dcH}} - u_{\mathrm{dcS}}}{u_{\mathrm{dcHN}} - u_{\mathrm{dcS}}^*} v_{\mathrm{cN}} \approx v_{\mathrm{cN}} \tag{13}$$

$$V_{\mathrm{cW}} = \frac{u_{\mathrm{dcS}}}{N_{\mathrm{W}} S_{\mathrm{dcW}}} = \frac{u_{\mathrm{dcS}}}{u_{\mathrm{dcS}}^*} v_{\mathrm{cN}} \approx v_{\mathrm{cN}}. \tag{14}$$

III. ASDCT Simple Modeling Under Dc Fault

Based on the MMC average transient modeling idea, an ASDCT simple dc fault model (simple-FM) is built, as shown in Fig. 5. The switching behavior of SMs is not explicitly represented. Instead, the characteristics of arms are modeled with equivalent capacitors (C_{eqH}, C_{eqL}, C_{eqW}) and controlled current sources (i_{eqH}, i_{eqL}, i_{eqW}). In this model, multiple phase circuits are centrally equivalent, and L_{eqX}(X = H, L, W) and R_{eqX} are the parallel equivalent values of the arm reactors and the total resistances of arms, respectively. C_{eqX} is a centralized characterization of SM capacitors. Due to the limitation of the antiparallel diodes of the IGBTs in the SMs, the capacitor voltage of the SM cannot be discharged below 0 V, so the equivalent capacitors also require parallel diodes (D_1, D_2, D_3). If the point S dc voltage is less than the LV port voltage, arm-L outputs a positive dc voltage, and the diode orientation is as shown in Fig. 5, but if the point S dc voltage is greater than the LV port voltage, the opposite diode is required. The controlled current source represents the power effect of the internal ac system on each arm. Based on the conclusion of [18], only the characteristics of the outer loop control are considered, and the current inner loop is regarded as ideally tracking the reference currents.

The simple-FM is derived as follows. First, the assumptions required for the model are given in the following.

1) The SM voltage equalization control in the arm is considered ideal, and the capacitor voltages of the SMs in the same arm are equal.
2) During the fault period evaluated by the model, the ac current control characteristics are ignored and the internal ac currents are determined by the current reference values output by the outer loops.
3) The changes of the average switching functions of the arms are ignored.

The phase A average switching functions of arms are expressed as

$$S_{\mathrm{Ha}} = \frac{u_{\mathrm{dcHN}} - u_{\mathrm{dcSN}}}{N_{\mathrm{H}} V_{\mathrm{cN}}} + S_{\mathrm{acHm}} \cos(\omega t - \varphi_{\mathrm{vH}}) \tag{15}$$

$$S_{\mathrm{La}} = \frac{u_{\mathrm{dcLN}} - u_{\mathrm{dcSN}}}{N_{\mathrm{L}} V_{\mathrm{cN}}} + S_{\mathrm{acLm}} \cos(\omega t - \varphi_{\mathrm{vL}}) \tag{16}$$

$$S_{\mathrm{Wa}} = \frac{u_{\mathrm{dcSN}}}{N_{\mathrm{W}} V_{\mathrm{cN}}} + S_{\mathrm{acWm}} \cos(\omega t - \varphi_{\mathrm{vW}}) \tag{17}$$

where u_{dcHN} and u_{dcLN} are the rated voltages of the HV port and LV port; u_{dcSN} is the rated point S dc voltage; S_{acHm}, S_{acLm}, and S_{acWm} are the ac component amplitudes of the average switching functions; ω is the angular frequency of ac components; φ_{vH}, φ_{vL}, and φ_{vW} are the initial phase angles.

According to assumption 2) and Fig. 4, the ac currents contain only the d-axis components, so the arm currents of phase A are

$$i_{\mathrm{Ha}} = -0.5i_{\mathrm{dcH}} + I_{\mathrm{acHm}}\cos(\omega t) \tag{18}$$

$$i_{\mathrm{La}} = 0.5i_{\mathrm{dcL}} + I_{\mathrm{acLm}}\cos(\omega t) \tag{19}$$

$$i_{\mathrm{Wa}} = 0.5i_{\mathrm{dcL}} - 0.5i_{\mathrm{dcH}} + I_{\mathrm{acWm}}\cos(\omega t) \tag{20}$$

where I_{acHm}, I_{acLm}, and I_{acWm} are the ac component amplitude of arm currents, which are determined by the outer loop control

$$\begin{cases} i_{\mathrm{acHm}} = K_{\mathrm{pS}}(u_{\mathrm{dcS}} - u^*_{\mathrm{dcS}}) + K_{\mathrm{iS}}\int(u_{\mathrm{dcS}} - u^*_{\mathrm{dcS}})\mathrm{d}t \\ i_{\mathrm{acLm}} = K_{\mathrm{pL}}(v_{\mathrm{cN}} - v_{\mathrm{cL}}) + K_{\mathrm{iL}}\int(v_{\mathrm{cN}} - v_{\mathrm{cL}})\mathrm{d}t \\ i_{\mathrm{acWm}} = -(i_{\mathrm{acHm}} + i_{\mathrm{acLm}}) \end{cases} \tag{21}$$

where K_{pS} and K_{iS} are the proportional and integral gains of the outer loop PI controller in the point S dc voltage control; K_{pL} and K_{iL} are the proportional and integral gains of the outer loop PI controller in the arm-L energy balance control.

Dc components of the average SM capacitor voltage v_{cH}, v_{cL}, and v_{cW} satisfy the following equations:

$$C_{\mathrm{H}}\frac{\mathrm{d}v_{\mathrm{cH}}}{\mathrm{d}t} = i_{\mathrm{Ha}}S_{\mathrm{Ha}}$$

$$= -0.5\frac{u_{\mathrm{dcHN}} - u_{\mathrm{dcSN}}}{N_{\mathrm{H}}V_{\mathrm{cN}}}i_{\mathrm{dcH}} + 0.5S_{\mathrm{acHm}}I_{\mathrm{acHm}}\cos(\varphi_{\mathrm{vH}}) \tag{22}$$

$$C_{\mathrm{L}}\frac{\mathrm{d}v_{\mathrm{cL}}}{\mathrm{d}t} = i_{\mathrm{La}}S_{\mathrm{La}}$$

$$= -0.5\frac{u_{\mathrm{dcLN}} - u_{\mathrm{dcSN}}}{N_{\mathrm{L}}V_{\mathrm{cN}}}i_{\mathrm{dcL}} + 0.5S_{\mathrm{acLm}}I_{\mathrm{acLm}}\cos(\varphi_{\mathrm{vL}}) \tag{23}$$

$$C_{\mathrm{W}}\frac{\mathrm{d}v_{\mathrm{cW}}}{\mathrm{d}t} = i_{\mathrm{Wa}}S_{\mathrm{Wa}}$$

$$= -0.5\frac{u_{\mathrm{dcSN}}}{N_{\mathrm{W}}V_{\mathrm{cN}}}(i_{\mathrm{dcL}} - i_{\mathrm{dcH}}) + 0.5S_{\mathrm{acWm}}I_{\mathrm{acHm}}\cos(\varphi_{\mathrm{vW}}). \tag{24}$$

Considering the voltage of the arm reactance (L_{L}, L_{H}, and L_{W}) and the arm equivalent resistance (R_{L}, R_{H}, and R_{W}), the Kirchhoff's voltage equations of the HV side and the LV side are

$$\begin{aligned} u_{\mathrm{dcH}} = & -0.5L_{\mathrm{L}}\frac{\mathrm{d}i_{\mathrm{dcH}}}{\mathrm{d}t} - 0.5R_{\mathrm{H}}i_{\mathrm{dcH}} + N_{\mathrm{H}}\frac{u_{\mathrm{dcHN}} - u_{\mathrm{dcSN}}}{N_{\mathrm{H}}V_{\mathrm{cN}}}v_{\mathrm{cH}} \\ & + 0.5L_{\mathrm{W}}\frac{\mathrm{d}(i_{\mathrm{dcL}} - i_{\mathrm{dcH}})}{\mathrm{d}t} + 0.5R_{\mathrm{W}}(i_{\mathrm{dcL}} - i_{\mathrm{dcH}}) \\ & + N_{\mathrm{W}}\frac{u_{\mathrm{dcSN}}}{N_{\mathrm{W}}V_{\mathrm{cN}}}v_{\mathrm{cW}} \end{aligned} \tag{25}$$

$$\begin{aligned} u_{\mathrm{dcL}} = & 0.5L_{\mathrm{L}}\frac{\mathrm{d}i_{\mathrm{dcL}}}{\mathrm{d}t} + 0.5R_{\mathrm{L}}i_{\mathrm{dcL}} + N_{\mathrm{L}}\frac{u_{\mathrm{dcLN}} - u_{\mathrm{dcSN}}}{N_{\mathrm{L}}V_{\mathrm{cN}}}v_{\mathrm{cL}} \\ & + 0.5L_{\mathrm{W}}\frac{\mathrm{d}(i_{\mathrm{dcL}} - i_{\mathrm{dcH}})}{\mathrm{d}t} + 0.5R_{\mathrm{W}}(i_{\mathrm{dcL}} - i_{\mathrm{dcH}}) \\ & + N_{\mathrm{W}}\frac{u_{\mathrm{dcSN}}}{N_{\mathrm{W}}V_{\mathrm{cN}}}v_{\mathrm{cW}}. \end{aligned} \tag{26}$$

Then, substituting (22), (23), and (24) into (25) and (26), the model for the dc short-circuit fault can be obtained as follows, which corresponds to Fig. 5:

$$\begin{aligned} u_{\mathrm{dcH}} = & -L_{\mathrm{eqH}}\frac{\mathrm{d}i_{\mathrm{dcH}}}{\mathrm{d}t} - R_{\mathrm{eqH}}i_{\mathrm{dcH}} \\ & + L_{\mathrm{eqW}}\frac{\mathrm{d}(i_{\mathrm{dcL}} - i_{\mathrm{dcH}})}{\mathrm{d}t} + R_{\mathrm{eqW}}(i_{\mathrm{dcL}} - i_{\mathrm{dcH}}) \\ & + \frac{1}{C_{\mathrm{eqH}}}\left[\int_0^t(-i_{\mathrm{dcH}} + i_{\mathrm{eqH}})\,\mathrm{d}t + v'_{\mathrm{cH0}}\right] \\ & + \frac{1}{C_{\mathrm{eqW}}}\left[\int_0^t(i_{\mathrm{dcL}} - i_{\mathrm{dcH}} + i_{\mathrm{eqW}})\,\mathrm{d}t + v'_{\mathrm{cW0}}\right] \end{aligned} \tag{27}$$

$$\begin{aligned} u_{\mathrm{dcL}} = & L_{\mathrm{eqL}}\frac{\mathrm{d}i_{\mathrm{dcL}}}{\mathrm{d}t} + R_{\mathrm{eqL}}i_{\mathrm{dcL}} \\ & + L_{\mathrm{eqW}}\frac{\mathrm{d}(i_{\mathrm{dcL}} - i_{\mathrm{dcH}})}{\mathrm{d}t} + R_{\mathrm{eqW}}(i_{\mathrm{dcL}} - i_{\mathrm{dcH}}) \\ & + \frac{1}{C_{\mathrm{eqL}}}\left[\int_0^t(-i_{\mathrm{dcL}} + i_{\mathrm{eqL}})\,\mathrm{d}t + v'_{\mathrm{cL0}}\right] \\ & + \frac{1}{C_{\mathrm{eqW}}}\left[\int_0^t(i_{\mathrm{dcL}} - i_{\mathrm{dcH}} + i_{\mathrm{eqW}})\,\mathrm{d}t + v'_{\mathrm{cW0}}\right] \end{aligned} \tag{28}$$

where

$$L_{\mathrm{eqX}} = 0.5L_{\mathrm{X}},\ \text{X=L, H, or W} \tag{29}$$

$$R_{\mathrm{eqX}} = 0.5R_{\mathrm{X}},\ \text{X=L, H, or W} \tag{30}$$

$$C_{\mathrm{eqH}} = \frac{2C_{\mathrm{H}}}{N_{\mathrm{H}}}\left(\frac{N_{\mathrm{H}}V_{\mathrm{cN}}}{u_{\mathrm{dcHN}} - u_{\mathrm{dcSN}}}\right)^2 \tag{31}$$

$$C_{\mathrm{eqL}} = \frac{2C_{\mathrm{L}}}{N_{\mathrm{L}}}\left(\frac{N_{\mathrm{H}}V_{\mathrm{cN}}}{u_{\mathrm{dcLN}} - u_{\mathrm{dcSN}}}\right)^2 \tag{32}$$

$$C_{\mathrm{eqW}} = \frac{2C_{\mathrm{W}}N_{\mathrm{W}}V_{\mathrm{cN}}^2}{u_{\mathrm{dcSN}}^2} \tag{33}$$

$$i_{\mathrm{eqH}} = \frac{S_{\mathrm{acHm}}N_{\mathrm{H}}V_{\mathrm{cN}}I_{\mathrm{acHm}}}{u_{\mathrm{dcHN}} - u_{\mathrm{dcSN}}}\cos\varphi_{\mathrm{vH}} \tag{34}$$

$$i_{\mathrm{eqL}} = \frac{S_{\mathrm{acLm}}N_{\mathrm{L}}V_{\mathrm{cN}}I_{\mathrm{acLm}}}{u_{\mathrm{dcLN}} - u_{\mathrm{dcSN}}}\cos\varphi_{\mathrm{vL}} \tag{35}$$

$$i_{\mathrm{eqW}} = -\frac{S_{\mathrm{acWm}}N_{\mathrm{W}}V_{\mathrm{cN}}I_{\mathrm{acLm}}}{u_{\mathrm{dcSN}}}\cos\varphi_{\mathrm{vW}} \tag{36}$$

$$v'_{\mathrm{cH0}} = u_{\mathrm{dcHN}} - u_{\mathrm{dcSN}} \tag{37}$$

$$v'_{\mathrm{cH0}} = u_{\mathrm{dcLN}} - u_{\mathrm{dcSN}} \tag{38}$$

$$v'_{\mathrm{cW0}} = u_{\mathrm{dcSN}} \tag{39}$$

where I_{acHm}, I_{acLm}, andI_{acWm} are calculated by (21), and the ac average switching function amplitudes are

$$S_{\mathrm{acHm}} = \frac{\sqrt{U_{\mathrm{ac}}^2 + (\omega L_{\mathrm{H}}I_{\mathrm{acHm}})^2}}{N_{\mathrm{H}}V_{\mathrm{cN}}} \tag{40}$$

$$S_{\mathrm{acLm}} = \frac{\sqrt{U_{\mathrm{ac}}^2 + (\omega L_{\mathrm{L}}I_{\mathrm{acLm}})^2}}{N_{\mathrm{L}}V_{\mathrm{cN}}} \tag{41}$$

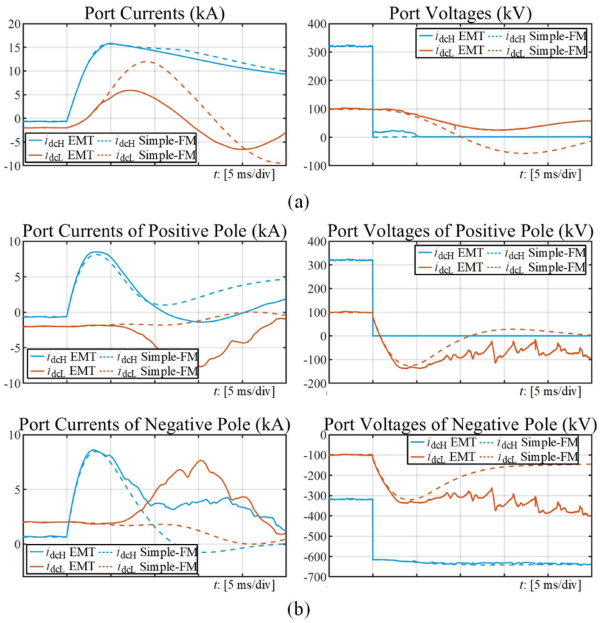

Fig. 6. Comparison of DC port currents and voltages between the simple-FM and PSCAD simulation. (a) PTP short-circuit of the HV port. (b) PTG short-circuit of the HV port.

$$S_{\mathrm{acWm}} = \frac{\sqrt{U_{\mathrm{ac}}^2 + (\omega L_{\mathrm{W}} I_{\mathrm{acWm}})^2}}{N_{\mathrm{W}} V_{\mathrm{cN}}}. \tag{42}$$

As shown in Fig. 6, the simple dc fault model described previously can accurately simulate the change of fault currents within 4 ms. However, it cannot be sustained for long periods, and the fault behaviors of the port voltages and nonfault-port currents are not equivalent.

IV. Improved High Accuracy DC Fault Modeling of ASDCT

The fundamental reason why simple-FM cannot maintain accuracy after 4 ms is that the assumption conditions cannot be established during a longer fault time. Under the assumption of a constant average switching function, the dc component dynamic control of the arm-L is ignored. In addition, the rapid release of arm energy during the fault causes the internal ac voltage to collapse, and ac current control cannot be considered ideal. This section will optimize for the above-mentioned two points to improve the accuracy and effective duration of the model. The required assumption is to retain only the first clause as follows. The SM voltage equalization control in the arm is considered ideal, and the capacitor voltages of the SMs in the same arm are equal.

A. Dynamic Characterization of the Arm-L

The dc voltage of the arm-L is given by the LV port control, which changes dynamically during faults. The use of a centralized capacitance equivalence method (such as arm-H and arm-W) requires variable capacitance, which leads to a more difficult integration operation and the need for discretizations. A dual-coupled controlled source circuit is more suitable for the dynamic simulation of the arm-L, as shown in Fig. 7. The interrelated controlled voltage source and controlled current source are used to establish the stress relationship between the main circuit and the SM equivalent circuit. u_{eqL} is used to equip the dc voltage of the arm-L

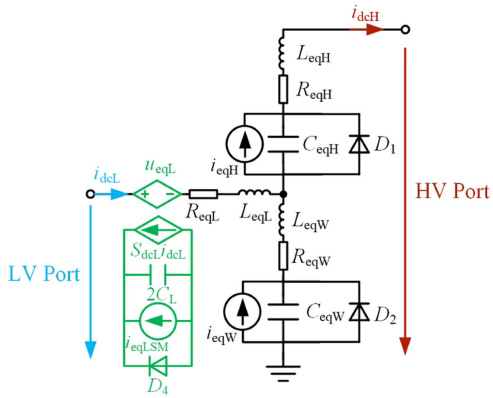

Fig. 7. ASDCT DC fault model with the dynamic characterization of the arm-L.

$$u_{\mathrm{eqL}} = N_{\mathrm{L}} S_{\mathrm{dcL}} v_{\mathrm{cL}} \tag{43}$$

where S_{dcL} is the dc average switching function of arm-L

$$S_{\mathrm{dcL}} = K_{\mathrm{pdcL}}(u_{\mathrm{dcL}} - u_{\mathrm{dcL}}^*) + K_{\mathrm{idcL}} \int (u_{\mathrm{dcL}} - u_{\mathrm{dcL}}^*) \mathrm{d}t \tag{44}$$

where K_{pdcL} and K_{idcL} are the proportional and integral gains of the PI controller in the LV port control.

The SM equivalent circuit can be characterized by the following equation:

$$C_{\mathrm{L}} \frac{\mathrm{d}v_{\mathrm{cL}}}{\mathrm{d}t} = 0.5 i_{\mathrm{dcL}} S_{\mathrm{dcL}} + 0.5 i_{\mathrm{eqLSM}} \tag{45}$$

where the dc average switching function S_{dcL} is given by the LV port control in Fig. 4, and i_{eqLSM} is the equivalent value of the arm-L ac current, which will be derived later.

B. Internal AC System Collapse and Modeling

The ac currents in the simple-FM are determined by the power command or the output of the outer control. Such an equivalence has high accuracy in the MMC model. The ac side of the MMC is connected to a strong grid, enabling the current inner control to accurately track the references. The voltage of the internal ac system of the ASDCT is established by the arm-W, which cannot be equated to an ideal power supply. As shown in Fig. 8, during the fault transient, the ac voltage decays rapidly as the capacitor energy of arm-W is released, so the current inner loops of arm-H and arm-L cannot follow the references.

Only by characterizing the collapse of the internal ac system due to capacitor discharges can we accurately equate the evolution of ac currents in fault transients. The dynamic equations of arms in the *dq* SRF are

$$L_{\mathrm{X}} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{acXd}} \\ i_{\mathrm{acXq}} \end{bmatrix} + R_{\mathrm{X}} \begin{bmatrix} i_{\mathrm{acXd}} \\ i_{\mathrm{acXq}} \end{bmatrix} = - \begin{bmatrix} u_{\mathrm{acXd}} \\ u_{\mathrm{acXq}} \end{bmatrix} - \begin{bmatrix} u_{\mathrm{acSd}} \\ u_{\mathrm{acSq}} \end{bmatrix}$$

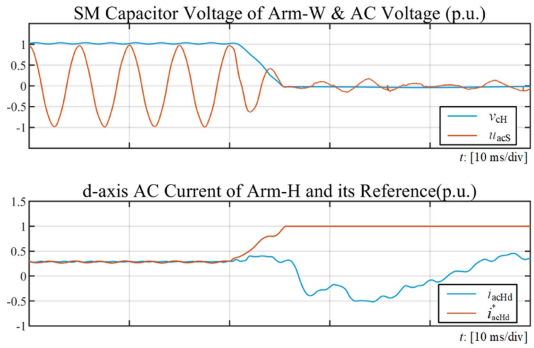

Fig. 8. Collapse of AC voltage and the failure of inner loop control.

$$+\begin{bmatrix} & \omega L_{\mathrm{X}} \\ -\omega L_{\mathrm{X}} & \end{bmatrix}\begin{bmatrix} i_{\mathrm{acXd}} \\ i_{\mathrm{acXq}} \end{bmatrix} \tag{46}$$

where X = H, L or W; i_{acXd}, i_{acXq} are the *dq* components of the arm ac currents; u_{acXd}, u_{acXq} are the *dq* components of the arm ac voltages; u_{acSd}, u_{acSq} are the *dq* components of the point S ac voltage. The *dq* transformation for each ac variable can be simply expressed as

$$\begin{cases} f_{\mathrm{d}}(t) = f_{\mathrm{acm}}(t)\cos\varphi_f \\ f_{\mathrm{q}}(t) = f_{\mathrm{acm}}(t)\sin\varphi_f. \end{cases} \tag{47}$$

The arm ac voltages u_{acXd}, u_{acXq} are expressed as

$$\begin{bmatrix} u_{\mathrm{acXd}} \\ u_{\mathrm{acXq}} \end{bmatrix} = \frac{v_{\mathrm{cX}}}{V_{\mathrm{cN}}}\begin{bmatrix} u^*_{\mathrm{acXd}} \\ u^*_{\mathrm{acXq}} \end{bmatrix} \tag{48}$$

where $v_{\mathrm{cX}}/V_{\mathrm{cN}}$ reflects the effect of transient development of capacitor voltage on the internal ac system; u^*_{acXd}, u^*_{acXq} are the command values of arm output ac voltages.

The ac current equations of arm-H and arm-L, considering the inner loop control characteristic, are

$$\begin{aligned} L_{\mathrm{X}}\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{acXd}} \\ i_{\mathrm{acXq}} \end{bmatrix} + R_{\mathrm{X}}\begin{bmatrix} i_{\mathrm{acXd}} \\ i_{\mathrm{acXq}} \end{bmatrix} &= \begin{bmatrix} & \omega L_{\mathrm{X}} \\ -\omega L_{\mathrm{X}} & \end{bmatrix}\begin{bmatrix} i_{\mathrm{acXd}} \\ i_{\mathrm{acXq}} \end{bmatrix} \\ &- \begin{bmatrix} u_{\mathrm{acSd}} \\ u_{\mathrm{acSq}} \end{bmatrix} - \frac{v_{\mathrm{cX}}}{V_{\mathrm{cN}}}\left(\begin{bmatrix} & \omega L_{\mathrm{X}} \\ -\omega L_{\mathrm{X}} & \end{bmatrix}\begin{bmatrix} i_{\mathrm{acXd}} \\ i_{\mathrm{acXq}} \end{bmatrix}\right. \\ &\left. - \begin{bmatrix} u_{\mathrm{acSd}} \\ u_{\mathrm{acSq}} \end{bmatrix} - g_{\mathrm{iX}}\left(\begin{bmatrix} i^*_{\mathrm{acXd}} \\ 0 \end{bmatrix} - \begin{bmatrix} i_{\mathrm{acXd}} \\ i_{\mathrm{acXq}} \end{bmatrix}\right)\right) \end{aligned} \tag{49}$$

where $X = H$ or L, g_{iX} is the transfer function of the current-inner-loop PI controllers; i^*_{acXd} is the reference of i_{acXd}.

The ac voltage at point S is solved by the control and the dynamic equation of the arm-W. As previously analyzed, the capacitor discharge of the arm-W leads to a rapid decay of the ac voltage, which is mainly reflected in the fact that the voltage output of the arm-W needs to be multiplied by $v_{\mathrm{cW}}/V_{\mathrm{cN}}$

$$u_{\mathrm{acS}} = \frac{v_{\mathrm{cW}}}{V_{\mathrm{cN}}}g_{\mathrm{pr}}(u^*_{\mathrm{acS}} - u_{\mathrm{acS}}) + L\frac{\mathrm{d}i_{\mathrm{acW}}}{\mathrm{d}t} + R_{\mathrm{W}}i_{\mathrm{acW}} \tag{50}$$

where g_{pr} is the transfer function of the PR controller, which is used to ensure the point S ac voltage tracks the given sinusoidal reference; u_{acS} is the point S ac voltage, and u^*_{acS} is its reference.

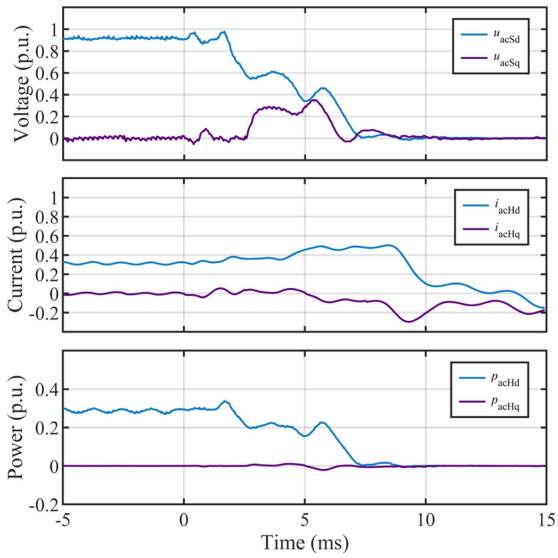

Fig. 9. Variation of *dq*-axis point S voltages, arm-H currents, and arm-H AC powers during an LV-side PTG fault. (Fault pole).

In addition, the average switching functions of arms should be further refined

$$\begin{cases} S_{\mathrm{acXm}}\cos\varphi_{\mathrm{vX}} = \frac{u^*_{\mathrm{acXd}}}{N_{\mathrm{X}}V_{\mathrm{cN}}} \\ S_{\mathrm{acXm}}\sin\varphi_{\mathrm{vX}} = \frac{u^*_{\mathrm{acXq}}}{N_{\mathrm{X}}V_{\mathrm{cN}}}. \end{cases} \tag{51}$$

The equivalent current expressions, taking into account the effect of reactive currents, are corrected to be

$$i_{\mathrm{eqH}} = \frac{N_{\mathrm{H}}V_{\mathrm{cN}}}{u_{\mathrm{dcHN}} - u_{\mathrm{dcSN}}}(S_{\mathrm{acHd}}i_{\mathrm{acHd}} + S_{\mathrm{acHq}}i_{\mathrm{acHq}}) \tag{52}$$

$$i_{\mathrm{eqW}} = -\frac{N_{\mathrm{W}}V_{\mathrm{cN}}}{u_{\mathrm{dcSN}}}(S_{\mathrm{acWd}}i_{\mathrm{acWd}} + S_{\mathrm{acWq}}i_{\mathrm{acWq}}) \tag{53}$$

$$i_{\mathrm{eqLSM}} = S_{\mathrm{acLd}}i_{\mathrm{acLd}} + S_{\mathrm{acLq}}i_{\mathrm{acLq}}. \tag{54}$$

C. Simplified Treatment of Q-Axis Currents

In (46), (49), and (51), the *d*-axis currents and the *q*-axis currents are both considered to ensure that changes in the internal ac link are accurately reflected. In the fault transient process, although there are *q*-axis current fluctuations, under the premise of the initial value of 0, the power exchanged by the *q*-axis current to the arms is extremely low, as shown in Fig. 9.

Hence, under the strategy that the control targets of both *q*-axis currents and *q*-axis voltages are 0, ignoring the *q*-axis current can further simplify the operation. Equations (46), (52), (53), and (54) can be simplified to

$$\begin{cases} L_{\mathrm{X}}\frac{\mathrm{d}i_{\mathrm{acXd}}}{\mathrm{d}t} + R_{\mathrm{X}}i_{\mathrm{acXd}} = -u_{\mathrm{acXd}} - u_{\mathrm{acSd}} \\ \omega L_{\mathrm{X}}i_{\mathrm{acXd}} = -u_{\mathrm{acXq}} - u_{\mathrm{acSq}} \end{cases} \tag{55}$$

$$i_{\mathrm{eqH}} = \frac{N_{\mathrm{H}}V_{\mathrm{cN}}}{u_{\mathrm{dcHN}} - u_{\mathrm{dcSN}}}S_{\mathrm{acHd}}i_{\mathrm{acHd}} \tag{56}$$

$$i_{\mathrm{eqW}} = -\frac{N_{\mathrm{W}}V_{\mathrm{cN}}}{u_{\mathrm{dcSN}}}S_{\mathrm{acWd}}i_{\mathrm{acWd}} \tag{57}$$

$$i_{\mathrm{eqLSM}} = S_{\mathrm{acLd}}i_{\mathrm{acLd}}. \tag{58}$$

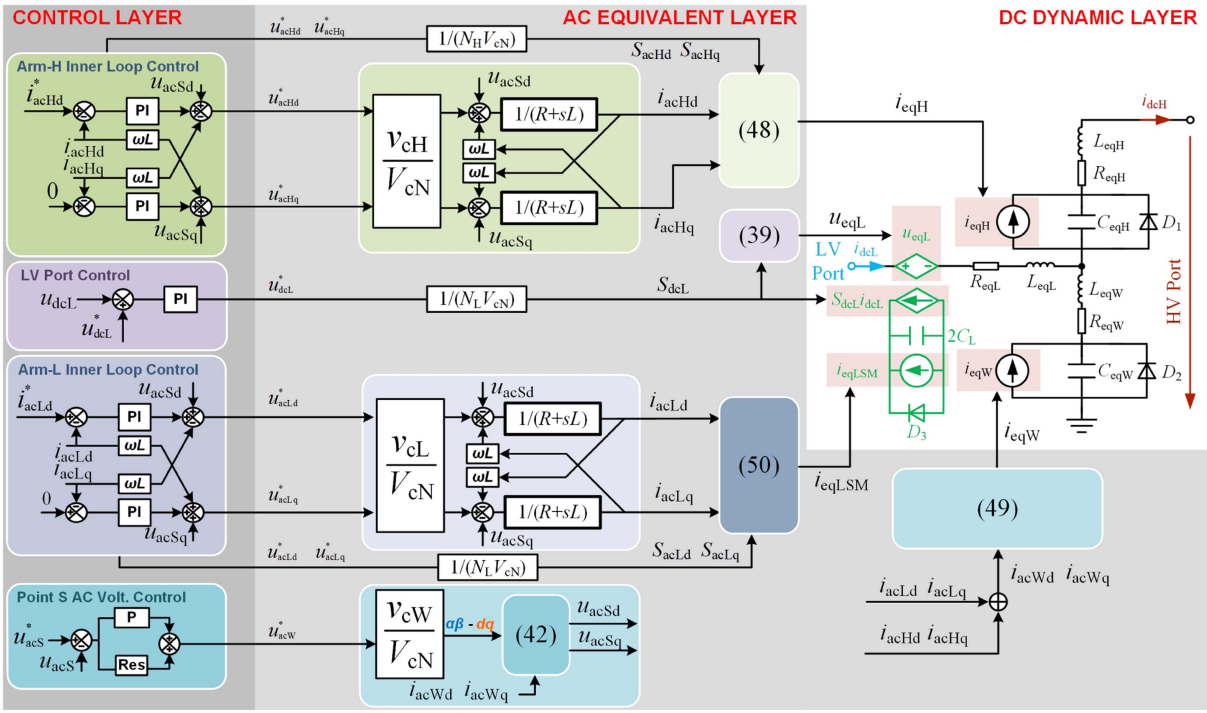

Fig. 10. High accuracy DC fault modeling of the ASDCT.

D. Improved Fault Model Structure

Based on the above-mentioned work, an improved dc fault model (improved-FM) with high accuracy of the ASDCT is proposed, as shown in Fig. 10.

Improved-FM is divided into three parts: control layer, ac equivalent layer, and dc dynamic layer. In the control layer, the average value control of ASDCT is modeled according to Fig. 4, and the reference voltages of arms are obtained. In the ac equivalent layer, the ac responses of arm-H, arm-L, and arm-W are equivalent according to (49) and (50), and the ac currents of arms are calculated. In this layer, the collapse of the internal ac system is considered. The ac currents are transformed into equivalent controlled current sources by (52), (53), and (54), and (44) gives the reference voltage of the arm-L equivalent voltage source. In the dc dynamic layer, the arm-H and arm-W are equivalent to RLC circuits and controlled current sources. The arm-L is equivalent to a dual-coupled controlled source circuit, in which a voltage source in conjunction with a capacitor circuit coupled to the aforementioned voltage source. The capacitors are connected in parallel with diodes (D_1, D_2, and D_3) to simulate the nonnegative constraint on the capacitor voltages by the antiparallel diodes of the IGBTs. The solution method of concentrated equivalent passive components in the circuit is the same as that of simple-FM.

If the q-axis currents are omitted, the model is simplified to Fig. 11. The q-axis current links in both the control layer and the ac equivalent layer are removed. The improved-FM without q-axis currents does not have an obvious deterioration in accuracy. Taking the PTG fault on the LV side as an example, the comparison is shown in Fig. 12.

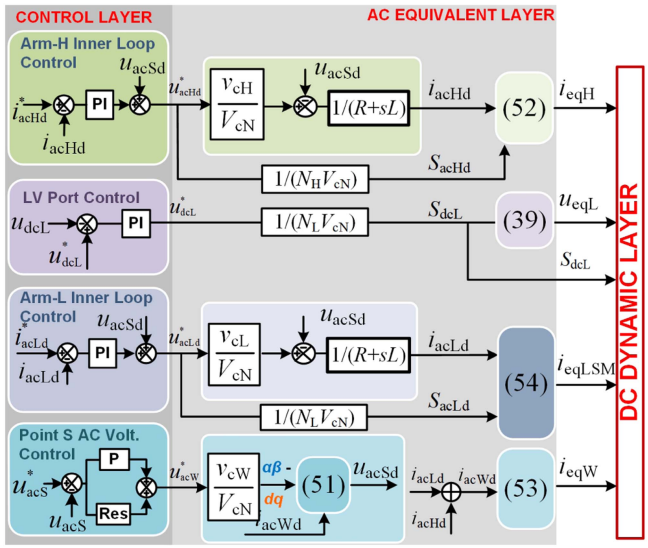

Fig. 11. Improved-FM without q-axis currents of the ASDCT.

E. Model Generalizability

The improved-FM is applicable to various ASDCTs with different arm configurations. Whether FBSMs or HBSMs are adopted does not change the derivation process of the average value characteristics of the arms. It should be noted that this model adopts two types of methods to characterize the arms, namely the RLC circuit and the dual-coupled controlled source circuit. The selection of the equivalent methods is related to the control strategy of the arms. If the dc component of the

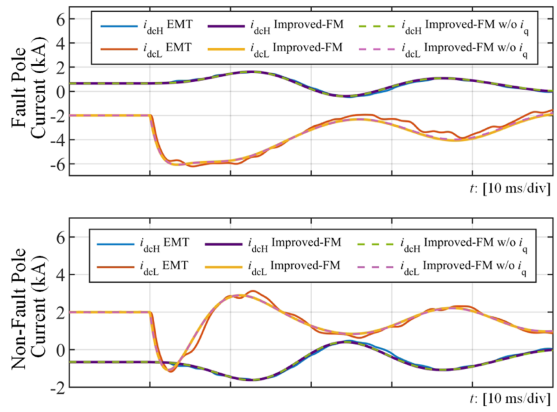

Fig. 12. Waveform comparison between the complete improved-FM model and the improved-FM model without the q-axis current. (Fault pole during an LV side PTG fault).

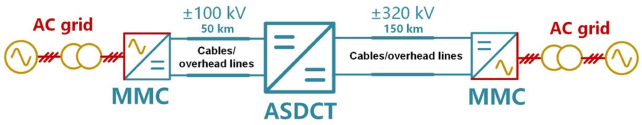

Fig. 13. System structure of the simulations.

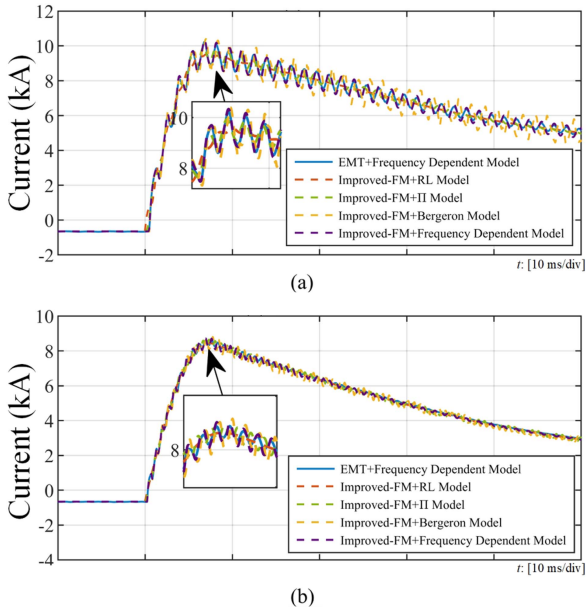

Fig. 14. Verification of various line models. (a) Cable. (b) Overhead line.

reference signal of the arm is constant, the RLC circuit is applicable. However, if the dc component of the reference signal of the arm is varying, a dual-coupled controlled source circuit is required, such as the arm-L in this article. When adopting a control strategy different from that described in this article, it is necessary to pay attention to whether the dc component of the arm control signal is constant, in order to select an appropriate arm equivalent method.

V. Model Performance Analysis

The computational performance of the model may be affected by the line model and the external conditions of dc short-circuit faults, such as fault locations and transition resistances. In order to assess the adaptability of the proposed model, the PSCAD/EMTDC simulation analysis is carried out under different overhead line/cable models, different fault locations, and transition resistances etc.

The system structure for simulation is shown in Fig. 13. The HV side and LV side ports of ASDCT are connected to two MMCs, respectively through lines. The voltage level of the HV subsystem is ±320 kV, and the line length is 150 km. The voltage level of the HV subsystem is ±100 kV, and the line length is 50 km.

A. Difference Evaluation of Line Models

The choice of line models may affect the accuracy of short-circuit fault analysis. Line models commonly used in transient analysis mainly include the lumped Π-type and *RL* equivalent models, as well as the distributed Bergeron and frequency dependent models. The frequency dependent model takes into account the frequency variation characteristics of the distributed parameters and is considered to be the most accurate type of transmission line model. The Bergeron model is based on the traveling wave equation, ignoring the frequency-varying characteristics of the parameters, but it is still sufficient to represent the traveling wave effect of the transmission line. The Π-type model adopts a lumped RLC two-port network equivalent transmission line, ignores the traveling wave effect of the transmission line, and improves the calculation speed. The *RL* model further ignores the capacitance to ground based on the Π-type model.

Fig. 14 shows the simulation results with various line models. For the cable dc system, the improved-FM with the Π-type model, Bergeron model and frequency dependent model can track the EMT model well. The *RL* model loses the characteristics of higher frequencies. Considering the calculation speed and accuracy of the model, the Π-type model is most suitable for cable dc systems. For overhead line dc systems, the *RL* model accurately represents fault current dynamics and low-frequency responses, with error from high-frequency characteristic loss due to ignored capacitance to ground. Because the capacitance to ground of the overhead lines is small, such an error is acceptable, so the *RL* model can be used as the choice for the overhead line dc systems. If a more accurate evaluation of the waveform during a fault is required, the frequency dependent model that accurately reflects the traveling wave effect is necessary.

B. Model Performance at Different Fault Locations

Based on the cable system, the effectiveness of the proposed improved-FM is validated at different fault locations. As shown in Fig. 15, PTP and pole-to-ground (PTG) fault simulations are performed at 0, 50, 100, and 150 km from ASDCT on the HV side, and 0, 25, and 50 km on the LV side, respectively. The EMT simulation for reference uses the frequency dependent cable model, while improved-FM uses the Π-type equivalent cable model.

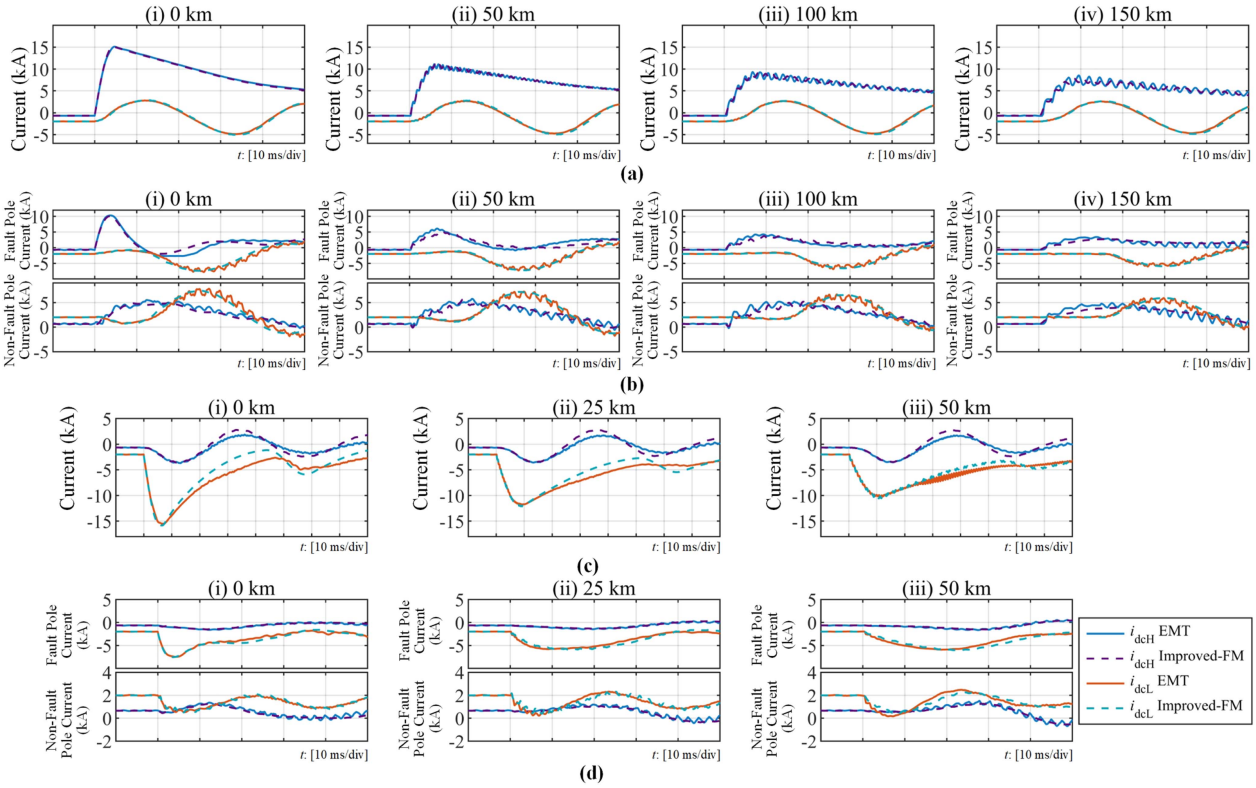

Fig. 15. Simulation waveforms at different fault locations. (Transition resistance $R_f = 0.01\,\Omega$). (a) HV-side PTP fault. (b) HV-side PTG fault. (c) LV-side PTP fault. (d) LV-side PTG fault.

It can be seen that at various fault locations, the difference between improved-FM and EMT does not change significantly. As the fault distance becomes longer, the peak value and slope of the fault side current decrease in turn, but the change of the nonfault side is not obvious. The improved-FM can reflect the evolution trend of fault currents at different fault locations, and the stress simulation of nonfault ports is also accurate enough for fault conduction between HV and LV sides. At remote fault distances, EMT simulations exhibit high frequency components that improved-FM does not accurately represent in amplitude and phase. This is mainly due to the differences in cable models, which have been described previously.

C. Model Performance at Different Transition Resistances

The simulated waveform at different transition resistances is shown in Fig. 16. Three transition resistance values of 0.01, 1, and 100 Ω are selected for PTP and PTG fault verification on the HV and LV side, respectively. The change of transition resistance has a great influence on the rise, peak, and attenuation process of fault currents. It can be seen from the simulation results that improved-FM can show the accurate trend of fault currents under different transition resistance conditions.

D. Model Performance Under Fault Ride-Through Process Based on Active Control

The improved-FM can be applied to the fault ride-through strategy based on active control. Fig. 17 shows the simulation waveforms of the ASDCT with LV-side port active current limiting control during an LV-side PTP fault. 2 ms after the fault occurs, the active current limiting control is put into operation, quickly limiting the LV-side current to zero. The improved-FM accurately tracks the LV port current and the HV port current.

VI. Experimental Verification

In order to verify the accuracy of the proposed modeling approach, the model calculations are compared with the hardware-in-the-loop (HiL) test results. The structure of the test platform is shown in Fig. 18, which is a digital–physical hybrid experimental system. The experimental platform simulates a 1000 MW dc offshore wind farm collection and transmission system. The wind farm is integrated via ±100 kV dc transmission line, stepped up to ±320 kV through the ASDCT, transmitted to an onshore MMC, and then inverted for interconnection with the ac power grid. In the test system, the wind farm is aggregated and equivalent to a 1000 MW, ±100 kV MMC. The converter circuit is equivalent by the FPGA, and the controller meets the engineering standard. There is no dc circuit breaker and converter blocking mechanism. The detailed system parameters follow the parameter design principles in Section II-B and are listed in Table I.

Fig. 19 shows the test results for the four types of faults (HV-side PTP, LV-side PTP, HV-side PTG, LV-side PTG). It is assumed that the faults occurred with a transition resistance $R_f = 0.01\,\Omega$ at t_0 . As demonstrated in Section III, the

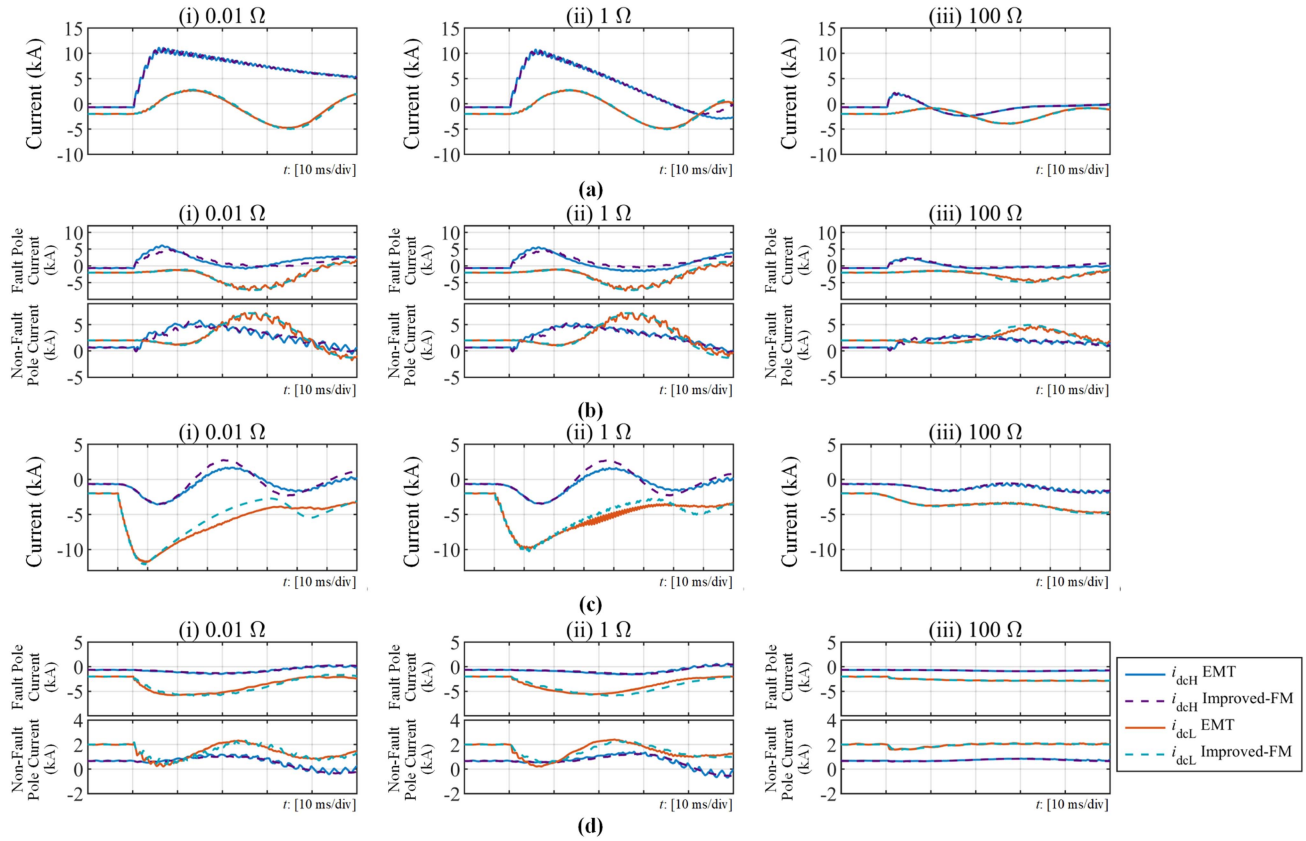

Fig. 16. Simulation waveforms with different transition resistances. (Fault distance: 50 km on the HV side and 25 km on the LV side). (a) HV-side PTP fault. (b) HV-side PTG fault. (c) LV-side PTP fault. (d) LV-side PTG fault.

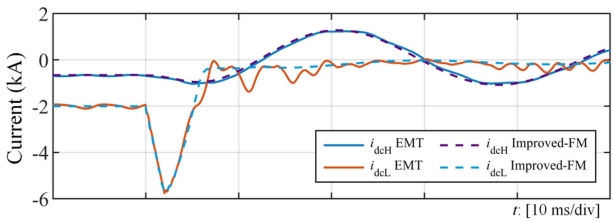

Fig. 17. Simulation waveforms during LV-side PTP fault ride-through process with LV-side current limit control.

simple-FM was precise within a 4 ms time frame. However, beyond this threshold, the discrepancy between the simple-FM and the HiL test waveform trend was considerable and, in some instances, entirely divergent. For instance, the HV-side PTG [see Fig. 19(c)] represents notable deviations at both HV side and LV side.

In contrast, the improved-FM has higher accuracy and longer validity time. It can track the dynamic process of the ASDCT after t_0 for up to 50 ms. Improved-FM is more accurate than simple-FM even within the 4 ms effective time of simple-FM. As shown in Table II, improved-FM calculation errors of the peak fault current were less than 3.9% , and the nonfault side current calculation errors were less than 3.4% . Compared with the simple-FM, the improved-FM has demonstrated notable

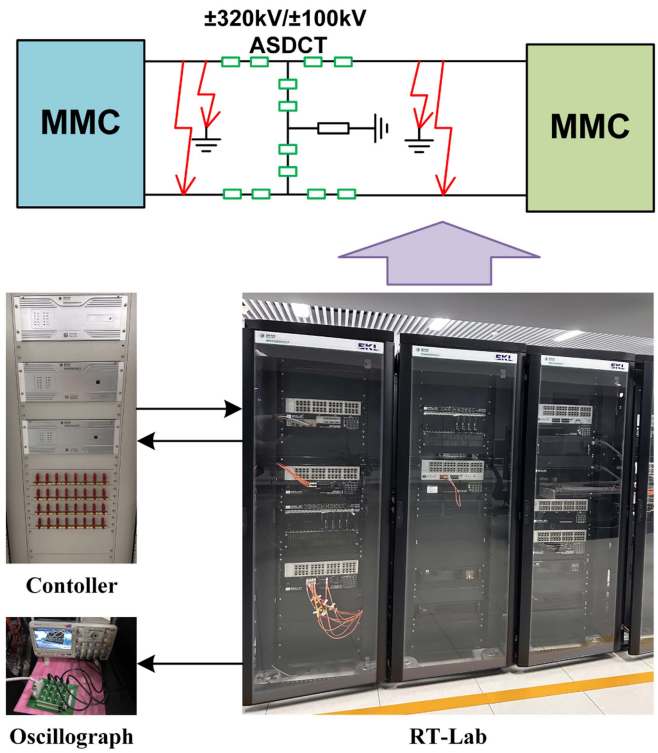

Fig. 18. System structure of the experimental platform.

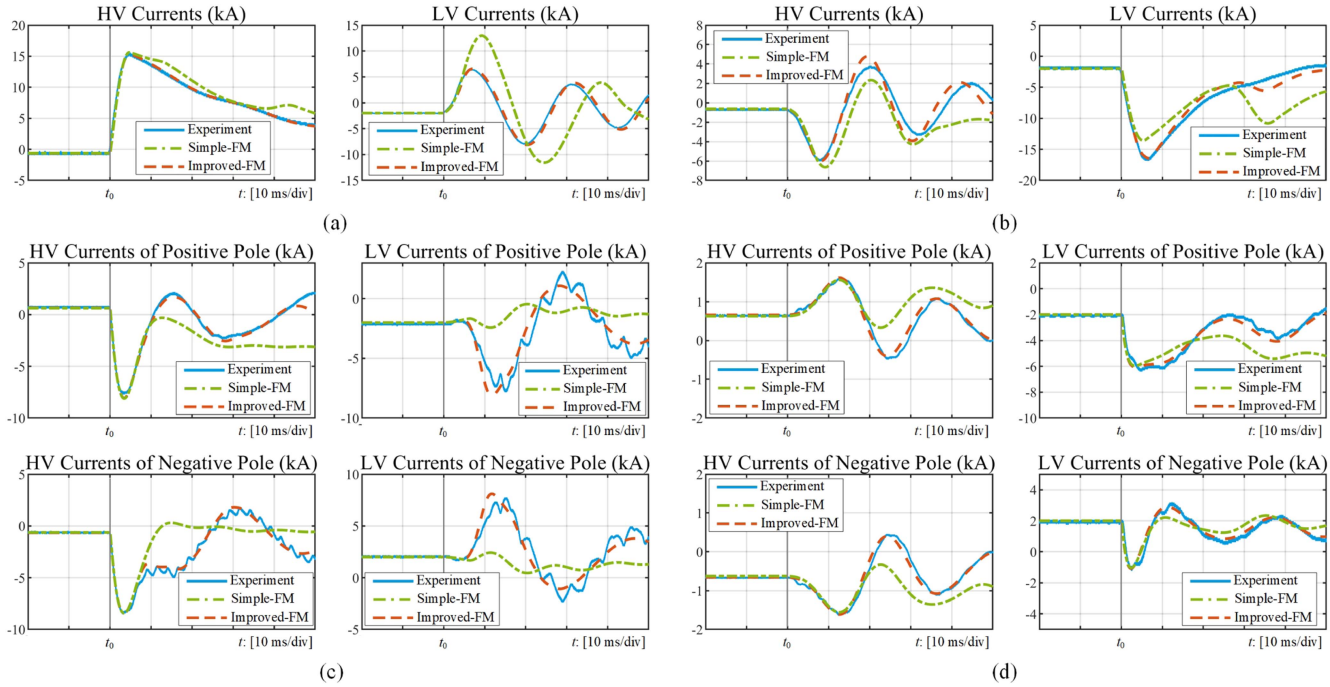

Fig. 19. Short-circuit currents when a fault occurs with a transition resistance $R_f = 0.01\,\Omega$. (a) HV-side PTP fault. (b) LV-side PTP fault. (c) HV-side PTG fault. (d) LV-side PTG fault.

TABLE I
SYSTEM PARAMETERS

Symbol	Quantity	Values
P	System Power	1000 MW
u_{dcLN}	Rated Voltage of the LV System	$\pm$100 kV
u_{dcHN}	Rated Voltage of the HV System	$\pm$320 kV
u_{dcSN}	Rated Point S DC Voltage	100 kV
$N_{\mathrm{L}}, N_{\mathrm{H}}, N_{\mathrm{W}}$	Number of SMs	90, 146, 90
$C_{\mathrm{L}}, C_{\mathrm{H}}, C_{\mathrm{W}}$	Capacitance of SMs	6 mF, 8 mF, 6 mF
V_{cN}	Rated SM Capacitor Voltage	2.2 kV
L	Arm Inductance	5 mH
U_{ac}	AC Voltage Amplitude of Point S	95 kV
R_G	Ground Resistance	10 Ω

TABLE II
ERRORS IN ESTIMATING PEAK FAULT CURRENTS

Model	Side	HV-side PTP	LV-side PTP	HV-side PTG	LV-side PTG
Simple-FM	fault	0.12 %	17.9 %	4.7 %	4.5 %
	non-fault	100.1 %	13.1%	69.1 %	1.9 %
Improved-FM	fault	0.08 %	0.5 %	3.9 %	2.7 %
	non-fault	1.2 %	2.2 %	3.4 %	1.2 %

advancements in terms of accuracy and durability. For dynamic characterization of the nonfault port, the improved-FM has excellent characterization.

From a practical point of view, simple-FM and improved-FM have mutually irreplaceable values. Simple-FM has an extremely simple modeling structure and provides an effective time of 4 ms, which is sufficient to evaluate the fault development of a dc system configured with blocking protection before blocking. Improved-FM extends the effective evaluation time to 50 ms, allowing the evaluation and analysis of dynamic processes and stress conduction in fault ride-through without blocking.

VII. CONCLUSION

An ASDCT simple dc fault model and an improved model are proposed in this article. The following conclusions can be drawn from both the theoretical analysis and the experimental verification.

1) The simple dc fault model of the ASDCT has acceptable accuracy within 4 ms. This model cannot characterize the fault stress conduction through ASDCT, and cannot guarantee long-term accuracy.
2) Dc control dynamic processes of the arm-L and the collapse of the internal ac system are critical in influencing the long-term fault characteristics of the ASDCT and the HV- and LV-side fault conduction.
3) The improved dc fault model, which uses the dual-coupled controlled source circuit and ac equivalent layer to characterize the dynamic process of arm-L and the internal ac collapse, can track the dynamic process after the faults for up to 50 ms. The model exhibits high accuracy and long persistence under various conditions of fault locations and transition resistances.
4) The choice of the line model affects the high-frequency performance of improved-FM. Using lumped line models is sufficient to present the change of fault currents. If the high-frequency characteristics of fault stress are required, high-precision line models, such as frequency dependent model, need to be used.

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