

# DC Chopper Function Extension of HCBs in DRU-MMC Based MTDC System for Offshore Wind Power Transmission

Zhe Zhang , Weijie Wen , Bin Li , and Botong Li 

**Abstract**—With remarkable features of low-cost, high-reliability, low-losses and light-weight, diode rectifier unit (DRU) and modular multilevel converter (MMC) based multiterminal dc system (DRU-MMC-MTDC) is a promising solution for offshore wind power transmission. DC chopper (DCC) and hybrid dc circuit breaker (HCB) are two different and essential facilities in the DRU-MMC-MTDC system for onshore ac and offshore dc fault ride-through, respectively. Considering that the structures of DCC and HCB are quite similar, in which the solid-state switches (SSSs) are the most expensive parts, emerging DCC function and dc interruption function seems to be a promising method to improve the utilization rate of SSSs. To realize this goal, the contributions of this paper is: DCC function extension method of HCBs is proposed, enabling HCBs to ride through both onshore ac and offshore dc faults. The working principle is: with MMC bypassed under an onshore ac fault, by tripping HCBs, part of the metal oxide varistors can serve as DCC to absorb the surplus power, so that no independent DCC is needed. Simulations and experiments are conducted for verification. The comparison between the proposed method and the conventional method of installing both DCC and HCB shows that the proposed method can save equipment investment and reduce control complexity in comparison with DCC.

**Index Terms**—DC chopper (DCC), diode rectifier unit (DRU), hybrid dc circuit breaker (HCB), modular multilevel converter (MMC), onshore ac fault.

## I. INTRODUCTION

COMPARED with the modular multilevel converter (MMC), diode rectifier unit (DRU) has remarkable features of low-cost, high-reliability, small-losses and light-weight [1], [2], [3]. In DRU and MMC based multiterminal dc system (DRU-MMC-MTDC), MMC acts as onshore station (receiving converter) and DRU acts as offshore station (sending converter). The grid-forming control based on  $P-U/Q-f$  strategy [4] is implemented in the line-side converter of wind farms to support the voltage and frequency of the offshore ac grid. Currently, DRU-MMC-MTDC is a promising solution for large-scale offshore wind power transmission [4], [5], [6]. Taking three terminals

as an example, the typical diagram is shown in Fig. 1(a): Wind farm (WF) 1 and WF2 transmit active power  $P_{WF1}$  and  $P_{WF2}$  through the sending converter DRU1 and DRU2, respectively, while the onshore ac grid receives active power  $P_0$  through the receiving converter MMC. The power transmission meets  $P_0 = P_{WF1} + P_{WF2}$ .

When onshore ac fault ( $F_2$ ) occurs, with voltage dipping,  $P_0$  drops; with DRUs not being controllable,  $P_{WF1} + P_{WF2}$ , which is determined by offshore wind farms, cannot change within a short time. The unbalanced power ( $P_{WF1} + P_{WF2} - P_0$ ) charges capacitors inside MMC rapidly and further leads to catastrophic risks of overvoltage and off-grid conditions for large-scale wind farms [7], [8]. To avoid this disaster, it is common practice to install dc chopper (DCC) for active absorption of the unbalanced power [9], [10], [11]. Referring to Fig. 1(b), DCC consists of solid-state switches (SSSs) and energy dissipation resistor ( $R_D$ ). By controlling duty cycle of SSSs ( $t_{on}$  and  $t_{off}$ ), equivalent resistance of DCC ( $R_{Deq}$ ) is dynamically adjusted in accordance with the unbalanced power. In DCC, SSS works in multipulse mode with high-frequency control; and seeing from dc side, DCC is in parallel with MMC.

When dc fault occurs ( $F_1$ ), both precharged capacitors inside MMC and ac grid feed surge current through fault point. To avoid outage of the whole system, hybrid dc circuit breakers (HCBs) are configured at positive and negative poles of each line for fault current interruption [12], [13]. Referring to Fig. 1(c), HCB consists of fast mechanical switch (FMS) and serial-connected SSSs. The topology of SSS in HCB differs slightly from that in DCC: To enable bidirectional current control, a full-bridge diode structure is employed in SSS, which has been implemented in HCB of Zhangbei Project [14]. By controlling IGBTs in SSSs, fault current is first commutated from FMS to SSSs through FMS tripping and IGBTs turning ON, and is subsequently interrupted by metal oxide varistors (MOVs) after IGBTs turning OFF [14], [15]. In this case, SSS works in mono-pulse mode with  $t_{on}$  of  $\sim 2$  ms; and seeing from dc side, HCB is in serial with MMC.

Therefore, DCC and HCB are two different and essential facilities for onshore ac and offshore dc fault ride-through. As shown in the comparison between Fig. 1(b) and (c), with SSSs serving as the core components, the structures of DCC and HCB are quite similar. Considering SSS is the most expensive component, emerging DCC function and dc interruption function seems to be a promising method to improve the utilization rate of SSS.

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The authors are with the State Key Laboratory of Intelligent Power Distribution Equipment and System, Tianjin University, Tianjin 300072, China (e-mail: weijie.wen@tju.edu.cn).

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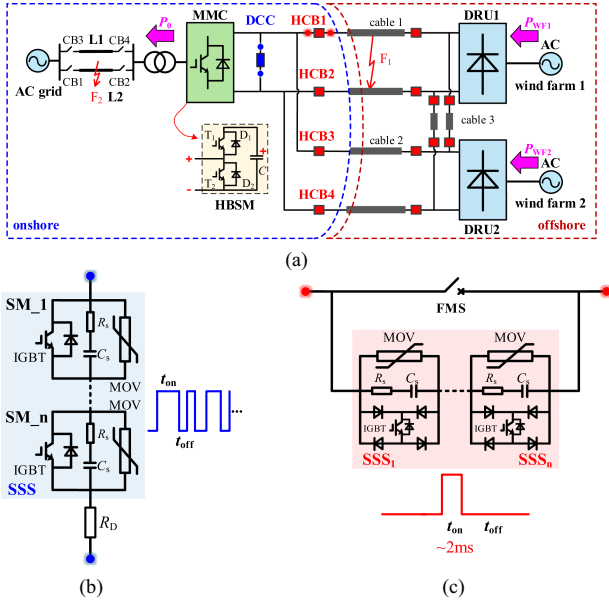


Fig. 1. Diagram of DRU-MMC-MTDC system, DCC and HCB. (a) Basic structure of DRU-MMC-MTDC system. (b) Detailed structure of typical DCC. (c) Detailed structure of typical HCB.

However, as mentioned before, working conditions of SSS in DCC and HCB are different; with different connections to MMC, energy absorption element in DCC is linear resistor and that in HCB is MOV. Given these differences, how to emerge DCC and dc interruption function within a single facility is a significant challenge to be overcome.

In this article, DCC function extension method of HCBs is proposed so that using only HCBs could ride through onshore ac and offshore dc faults, eliminating the need for independent DCC. DC chopping requirements for onshore ac fault are analyzed in Section II, including the function of DCC, duty cycle control and parameter design. Working principle, transient current characteristics, system requirements and parameter design of the proposed method are presented in Section III. Simulation and experiments are carried out in Section IV and Section V for verification. A comprehensive performance comparison is conducted in Section VI.

## II. DC CHOPPING REQUIREMENTS FOR ONSHORE AC FAULT

### A. Function of DCC Under Onshore AC Fault

In the DRU-MMC-MTDC system, the power imbalance caused by onshore ac fault could result in overvoltage at the dc side of MMC and even electromechanical safety issues for WFs.

Taking the DRU-MMC-MTDC system shown in Fig. 1(a) as an example, and ignoring the energy loss of DRU and MMC,  $P_0$  absorbed by ac grid is related to the ac voltage of MMC, which is also equal to the total power generated by wind farms, as expressed in the following equation:

$$P_0 = \frac{U_{s\text{Grid}}U_{s\text{MMC}}}{X_s} \sin \delta = \sum P_{\text{WF}} \quad (1)$$

where  $U_{s\text{Grid}}$  and  $U_{s\text{MMC}}$  are the ac voltages of ac grid and MMC respectively,  $\delta$  is the power angle,  $X_s$  is the ac equivalent reactance, and  $\sum P_{\text{WF}}$  is the total power generated by WF1 and WF2.

Once onshore ac fault occurs, the rapid drop of  $U_{s\text{MMC}}$  leads to a decrease in  $P_0$ . Since the response speed of  $\sum P_{\text{WF}}$  is much slower than that of  $P_0$ , the unbalanced surplus power is generated, which has to be absorbed by capacitors inside MMC, leading to overvoltage at the dc side of MMC. The above process can be expressed as follows:

$$\int_{t_0}^t (\sum P_{\text{WF}} - P_0) dt = \frac{3C}{2N} (U_{\text{MMC}}^2(t) - U_{\text{MMC}}^2(t_0)) \quad (2)$$

where  $t_0$  is the fault occurrence time,  $C$  is the capacitance of capacitor in each submodule,  $N$  is the number of submodules in the bridge arm,  $U_{\text{MMC}}(t_0)$  and  $U_{\text{MMC}}(t)$  are the dc voltages of MMC at  $t_0$  and  $t$ .

$U_{\text{MMC}}(t)$  can be expressed in (3), where  $U_{\text{dcN}}$  indicates the rated dc voltage used to equivalently replace  $U_{\text{MMC}}(t_0)$ . The overvoltage in (3) would be applied to capacitors and IGBTs inside MMC, posing severe risks of component damage and system failure

$$U_{\text{MMC}}(t) = \sqrt{U_{\text{dcN}}^2 + \frac{2N}{3C} (\sum P_{\text{WF}} - P_0) (t - t_0)}. \quad (3)$$

Under normal system operation, the dc voltage of DRU ( $U_{\text{DRU}}$ ) and the dc current ( $I_{\text{dc}}$ ) can be expressed as (4) and (5)

$$U_{\text{DRU}} = \frac{3\sqrt{2}n}{\pi} U_{\text{sDRU}} - \frac{3n}{\pi} X_s' I_{\text{dc}} \quad (4)$$

$$I_{\text{dc}} = \frac{U_{\text{DRU}} - U_{\text{MMC}}}{R_{\text{dc}}} \quad (5)$$

where  $U_{\text{sDRU}}$  is the ac voltage of DRU,  $n$  is the number of DRUs,  $X_s'$  is the equivalent reactance of DRU transformers,  $U_{\text{MMC}}$  is the dc voltage of MMC, and  $R_{\text{dc}}$  is the equivalent resistance of dc transmission lines.

The surplus power brings electromechanical safety issues to WFs. Affected by the increase of  $U_{\text{MMC}}$ , the control system of WFs has to increase  $U_{\text{sDRU}}$ , so that  $I_{\text{dc}}$  could be maintained to transmit the output power of WFs. However, constrained by the upper limit of the control system of WFs,  $U_{\text{sDRU}}$  should be within  $\sim 1.1$  p.u. [16].  $U_{\text{DRU}}$  limited by  $U_{\text{sDRU}}$  cannot be increased in accordance with  $U_{\text{MMC}}$ , resulting in  $I_{\text{dc}}$  decrease, as shown in (5). Therefore, affected by onshore ac fault,  $I_{\text{dc}}$  would gradually decrease, which is highly detrimental to the system.

In terms of WFs, the load of the WFs decreases as the dc current declines, but the high-inertia input mechanical power cannot be adjusted in time. The surplus mechanical energy must be fully converted into the kinetic energy of the rotor, which may cause serious mechanical damage to WFs.

Therefore, the surplus power caused by onshore ac fault constitutes a critical threat to the operational stability and security of MMC and WFs. The key to solving this problem is to provide a new path for dissipating the surplus power within tens of milliseconds, which can be expressed as (6). In practical

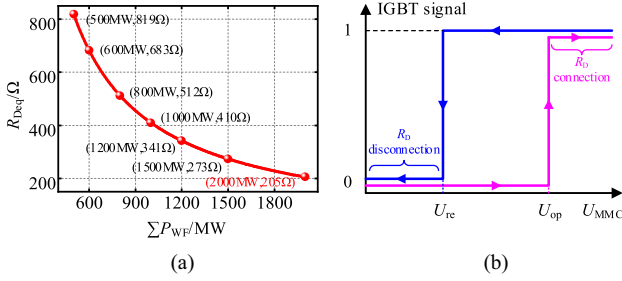


Fig. 2. Working characteristics of DCC. (a) Inverse nonlinear relation between  $R_{Deq}$  and  $\Sigma P_{WF}$ . (b) Working principle of duty cycle control.

application, DCC, as shown in Fig. 1(b), is installed to realize the new power balance [9], [10], [11]

$$\int_t^{t+t_D} (\sum P_{WF} - P_0) dt = \int_t^{t+t_D} P_D dt \quad (6)$$

where  $t_D$  is the energy dissipation time, and  $P_D$  is the dissipated power.

### B. Duty Cycle Control of DCC for Power Matching

The energy dissipation element in DCC is a linear resistor ( $R_D$ ) with determined resistance. Taking the three-phase ac fault, the most severe fault condition for ac system, as an example, the surplus power is  $\Sigma P_{WF}$  when  $P_0$  is zero, and its matching relation with the required resistance ( $R_{Deq}$ ) is expressed as follows:

$$R_{Deq} = \frac{U_{dcN}^2}{\sum P_{WF}}. \quad (7)$$

As  $\Sigma P_{WF}$  is variable, DCC should dissipate  $\Sigma P_{WF}$  at different levels while maintaining the dc voltage constant. According to (7), taking  $U_{dcN}$  of 640 kV as an example, the matching relation between  $\Sigma P_{WF}$  and  $R_{Deq}$  is illustrated in Fig. 2(a). It can be seen that  $R_{Deq}$  has an inverse nonlinear relation with  $\Sigma P_{WF}$ . As  $\Sigma P_{WF}$  decreases from 2000 to 500 MW,  $R_{Deq}$  increases from 205 to 819  $\Omega$ , meaning  $R_{Deq}$  in DCC should be variable to match with  $\Sigma P_{WF}$ .

However, referring to Fig. 1(b),  $R_D$  is a resistor with determined resistance, whose value ( $R_{Dset}$ ) is designed in accordance with the total rated power of WFs ( $\Sigma P_{WFN}$ ), as shown in (8). When  $\Sigma P_{WF}$  is  $m \Sigma P_{WFN}$  ( $0 < m < 1$ ), the support voltage of DCC ( $U_D$ ) is expressed as (9), and power dissipation ( $P_D$ ) is expressed as (10). As  $\Sigma P_{WF}$  decreases, both  $U_D$  and  $P_D$  established by  $R_{Dset}$  are lower than the normal level of the system

$$R_{Dset} = \frac{U_{dcN}^2}{\sum P_{WFN}} \quad (8)$$

$$U_D = I_{dc} R_{Dset} = \frac{m \sum P_{WFN}}{U_{dcN}} R_{Dset} = m U_{dcN} \quad (9)$$

$$P_D = I_{dc}^2 R_{Dset} = \left( \frac{m \sum P_{WFN}}{U_{dcN}} \right)^2 R_{Dset} = m^2 \sum P_{WFN}. \quad (10)$$

To solve the above-mentioned problems, duty cycle control has to be adopted to regulate  $R_{Dset}$  to be  $R_{Deq}$  for matching with  $\Sigma P_{WF}$ . Taking  $U_{MMC}$  as the control object, when  $U_{MMC}$  is higher than the operation threshold  $U_{op}$ , IGBTs in DCC are turned ON, causing  $R_D$  to dissipate  $\Sigma P_{WF}$  and leading to a decrease in  $U_{MMC}$  to  $U_D$ ; when  $U_{MMC}$  is lower than the return threshold  $U_{re}$ , IGBTs are turned OFF, resulting in  $R_D$  being switched out of the system and  $U_{MMC}$  starting to rise. The above process is repeated continuously, as shown in Fig. 2(b). By controlling duty cycle,  $R_{Dset}$  can be converted into  $R_{Deq}$ , which is expressed as follows:

$$R_{Deq} = \frac{t_{on} + t_{off}}{t_{on}} R_{Dset} \quad (11)$$

where  $t_{on}$  and  $t_{off}$  are the on-time and off-time of IGBTs.

$R_D$ ,  $R_{Dset}$ , and  $R_{Deq}$  are introduced to clarify the working principle of DCC. Their relationship can be summarized as follows.  $R_{Dset}$  is the determined resistance of energy dissipation resistor  $R_D$ , and  $R_{Dset}$  is converted into  $R_{Deq}$  through duty cycle control to match  $\Sigma P_{WF}$  according to Fig. 2(b) and (11).

### C. Parameter Design of DCC

As shown in Fig. 1(a), DCC is connected at the outlet of MMC, and it should absorb the total power generated by WF1 and WF2 when MMC cannot transmit power to onshore ac system. Thus, DCC withstands the pole-to-pole dc voltage, and its current and power capacity should be the sum of those provided by WF1 and WF2. Taking the DRU-MMC-MTDC system with  $\Sigma P_{WFN} = 2000$  MW and  $U_{dcN} = 640$  kV as an example, the number of IGBTs and the energy dissipation capacity of DCC are designed.

The 5SNA 3000K452300 (4.5 kV, 3 kA) [17] IGBTs are used in DCC. Based on the withstand voltage of 640 kV and a safety margin of 1.1, the number of IGBTs in series for DCC is calculated as 157. Since the dc chopping current requirement ( $\sim 3.125$  kA) is close to the rated current of IGBT, there is no need to parallel IGBTs.

The energy dissipation time ( $T_D$ ) is an important determinant of the energy dissipation capacity, which is set to 100 ms for the following reasons. Due to the double-circuit lines of onshore ac system in Fig. 1(a), which enable a reduction in the power outage duration at onshore ac system and enhance the system stability, the ac grid recovers power transmission through L2 once the fault line L1 is isolated, indicating that  $T_D$  should cover the fault isolation time. The fault isolation time is approximately 70–90 ms, including the ac fault detection time (40–50 ms) and the operation time of ac circuit breakers (CBs) (30–40 ms). Therefore,  $T_D$  of 100 ms is sufficient to meet the energy dissipation requirements.

Energy dissipation capacity ( $E_D$ ) can be calculated by the following equation:

$$E_D = k \sum P_{WFN} T_D. \quad (12)$$

According to (12),  $E_D$  is determined to be 240 MJ in the case where  $k$  is the safety margin of 1.2,  $T_D$  is 100 ms and  $\Sigma P_{WFN}$  is 2000 MW.

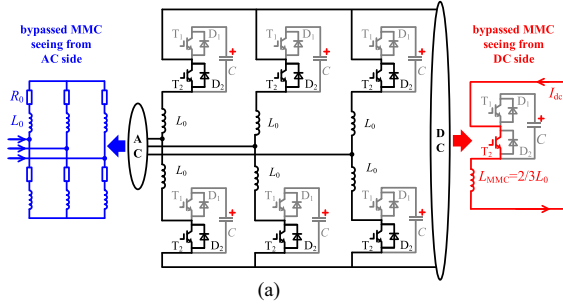


Fig. 3. Equivalent circuits of DRU-MMC-MTDC system. (a) Equivalent circuit of bypassed MMC from different sides. (b) Equivalent circuit of DC system.

### III. PROPOSED DCC FUNCTION EXTENSION OF HCBs AND ITS WORKING CHARACTERISTICS

#### A. Working Principle and Circuit Modeling

The basic function of DCC is to switch linear resistor into the dc system to be in parallel with MMC, resulting in a controllable load for DRUs. While HCBs are switching nonlinear resistor (MOV) into dc system to be in series with MMC, which results in transient interruption voltage ( $U_{TIV}$ ) to force fault current to zero. Considering MOV is also an energy absorption element, if output voltage of MMC is controlled to zero, by regulating voltage of HCBs properly, MOVs in HCBs could be switched into dc system, acting as controllable loads for DRUs.

Therefore, when riding through onshore ac fault, with  $T_1$  and  $T_2$  in the submodules (SMs) of MMC turned OFF and ON, MMC is bypassed. The equivalent circuit of bypassed MMC seeing from dc side is shown in Fig. 3(a) and (b). MMC can be regarded as a lumped reactor with inductance of  $(2/3L_0)$ . In this case, HCBs cooperating with the bypassed MMC can act as the controllable loads for DRUs.

In reference to the parameters of HCBs,  $U_{TIV}$  established by turning OFF all SSSs in HCBs is  $\sim 1.5$  p.u., which is higher than the rated dc voltage so that fault current can be forced to zero. However, different from dc fault interruption, during the ride-through of onshore ac fault,  $U_{TIV}$  established by HCBs should match the rated dc voltage ( $\sim 1$  p.u.) to maintain continuous dc current and power transmission. Therefore, partial SSSs in HCBs should be operated to ensure only part of MOVs are switched into the power system to obtain  $U_{TIV}$  of  $\sim 1$  p.u., and the nonoperated SSSs forms a current path through a series connection of diodes and IGBT, as shown in Fig. 3(b).

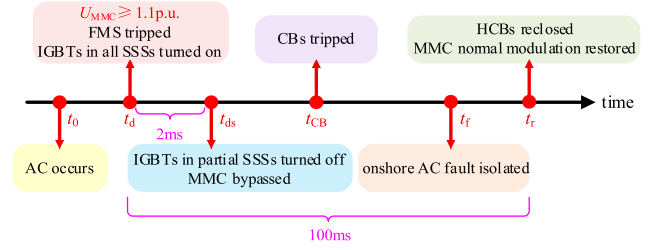


Fig. 4. Process of the proposed DCC function extension of HCBs.

When using HCBs to ride through onshore ac fault, the coordination of ac CBs, HCBs and MMC are required. The proposed DCC function extension of HCBs can be summarized as follows.

After onshore ac fault occurs at  $t_0$ , WFs continue to inject power into MMC, resulting in dc voltage of MMC keeps rising until it exceeds 1.1 p.u. at  $t_d$ . Then, the proposed method is activated. FMS is tripped and all IGBTs in SSSs are turned ON. After 2 ms, contacts of FMS are separated far enough, resulting in adequate dielectric recovery strength to withstand  $U_{TIV}$ . IGBTs in partial SSSs are turned OFF at  $t_{ds}$ , while MMC is bypassed at the same time. HCBs and MMC are controlled to serve as DCC to dissipate the surplus power. After ac fault is detected at  $t_{CB}$ , CBs at both sides of the fault line (CB1 and CB2) are tripped to isolate the ac fault, and the fault is isolated successfully at  $t_f$ . Then, after the fixed energy dissipation time (100 ms), SMs in MMC works with normal modulation state, and HCBs are reclosed at  $t_r$ . The system returns to normal operation and power transmission. The above process is depicted in Fig. 4.

The working principle of HCB serving as DCC has two differences compared with that of HCB dealing with dc fault: 1) The operation of HCB is activated by the overvoltage detection at dc side and 2) After FMS is tripped, only IGBTs of partial SSSs are turned OFF, while the others are still turned ON.

#### B. Transient Current Characteristics Inside MMC

The ac current of MMC is affected by the bypass operation in the proposed method, which determines the transient current characteristics of the MMC bridge arms. Therefore, a detailed analysis of the ac current of MMC is conducted in this part.

From the occurrence of the onshore ac fault to the completion of dc chopping, the transient process can be divided into three stages according to the key time points of Fig. 4.

*Stage I— $t_0$ – $t_{ds}$ , ac fault occurs but MMC is not bypassed.*

In Stage I, onshore ac fault occurs at  $t_0$ , and MMC remains in the normal modulation mode since  $U_{MMC}$  has not exceeded 1.1 p.u. Due to the double-circuit line of ac system, there are two current paths for the ac grid shown in Fig. 5(a). One is from L1 to the fault point ( $i_{L1}$ , yellow dotted line), and the other is through L2 ( $i_{L2}$ , pink dotted line), via the right bus BUS2 and then partly through the right side of L1 to the fault point.

MMC also feeds current to the fault point (red dotted line). The ac output of MMC can be modeled as a current source with increasing amplitude instead of a constant one [18] since the

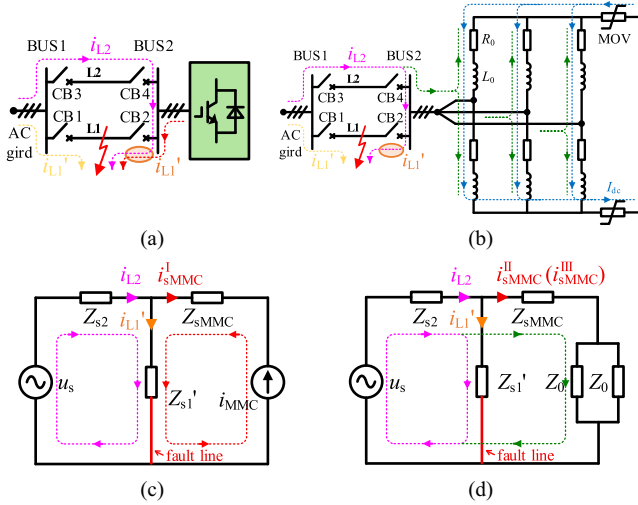


Fig. 5. Current paths and equivalent circuits. (a) Current paths in Stage I. (b) Current paths in Stage II. (c) Equivalent circuit of Stage I. (d) Equivalent circuit of Stage II and Stage III (ignoring the branch of  $Z_{s1}'$  and fault line in Stage III).

current in the MMC control system has not reached the limit in this stage.

It should be noted that since  $i_{L1}$  has no impact on the ac current of MMC ( $i_{sMMC}$ ), it is ignored in the subsequent analysis and simulation results. The equivalent circuit of Stage I is shown in Fig. 5(c), where  $u_s$  is the ac voltage of the ac grid;  $Z_{s2}$ ,  $Z_{s1}'$  and  $Z_{sMMC}$  are the equivalent impedances of L2, L1 to the right of the fault point, and the ac side of MMC to BUS2, respectively. The ac current of MMC in Stage I ( $i_{sMMC}^I$ ) can be expressed as

$$i_{sMMC}^I = -i_{MMC} \quad (13)$$

where  $i_{MMC}$  is the ac current of MMC equivalent current source.

*Stage II— $t_{ds}$ – $t_f$ , ac fault exists and MMC is bypassed.*

The bypass of MMC occurs at  $t_{ds}$  earlier than the ac fault isolation at  $t_f$ , meaning that MMC has been bypassed when ac fault still exists. The current paths in Stage II are shown in Fig. 5(b). As the bypassed MMC is in a passive state, the ac grid feeds current to bridge arms of MMC.

The equivalent circuit of Stage II is shown in Fig. 5(d), where  $Z_0$  is the equivalent impedance of the bridge arm ( $R_0 + j\omega L_0$ ). The forced component of ac current of MMC in Stage II ( $i_{spMMC}^{II}$ ) can be expressed as follows:

$$i_{spMMC}^{II} = \frac{u_s}{Z_{s2} + Z_{s1}' \parallel (Z_{sMMC} + \frac{1}{2}Z_0)} \frac{Z_{s1}'}{Z_{s1}' + Z_{sMMC} + \frac{1}{2}Z_0}. \quad (14)$$

As the inductance in the circuit suppresses the current surge during the stage transitions [19], the natural component of ac current of MMC ( $i_{snMMC}^{II}$ ) is generated, which can be expressed as follows:

$$i_{snMMC}^{II} = (i_{sMMC}^I - i_{spMMC}^{II}) \Big|_{t_{ds}} e^{-\frac{t-t_{ds}}{L_{eq}^{II}/R_{eq}^{II}}} \quad (15)$$

where  $L_{eq}^{II}$  and  $R_{eq}^{II}$  are respectively the equivalent inductance and resistance of the equivalent circuit in Stage II.

Ultimately, the ac current of MMC in Stage II ( $i_{sMMC}^{II}$ ) can be expressed as follows:

$$i_{sMMC}^{II} = i_{spMMC}^{II} + i_{snMMC}^{II}. \quad (16)$$

*Stage III— $t_f$ – $t_r$ , ac fault is cleared but MMC is in bypass mode.*

The ac fault is isolated by CB1 and CB2 at  $t_f$ . Due to the margin for energy dissipation time from  $t_f$  to  $t_r$ , MMC remains in bypass mode. The equivalent circuit is the remaining part ignoring the branch of  $Z_{s1}'$  and the fault line in Fig. 5(d). The forced and natural components of the ac current of MMC in Stage III can be respectively expressed as (17) and (18)

$$i_{spMMC}^{III} = \frac{u_s}{Z_{s2} + Z_{sMMC} + \frac{1}{2}Z_0} \quad (17)$$

$$i_{snMMC}^{III} = (i_{sMMC}^{II} - i_{spMMC}^{III}) \Big|_{t_f} e^{-\frac{t-t_f}{L_{eq}^{III}/R_{eq}^{III}}} \quad (18)$$

where  $L_{eq}^{III}$  and  $R_{eq}^{III}$  are respectively the equivalent inductance and resistance of the equivalent circuit in Stage III.

The ac current of MMC in Stage III ( $i_{sMMC}^{III}$ ) can be expressed as follows:

$$i_{sMMC}^{III} = i_{spMMC}^{III} + i_{snMMC}^{III}. \quad (19)$$

Based on the above-mentioned analysis, the upper and lower bridge arm current of MMC ( $i_p$  and  $i_n$ ) can be expressed as (20), which is composed of ac current of MMC and dc current

$$\begin{cases} i_p = \frac{1}{2}i_{sMMC} + \frac{1}{3}I_{dceq} \\ i_n = \frac{1}{2}i_{sMMC} - \frac{1}{3}I_{dceq} \end{cases} \quad (20)$$

where  $i_{sMMC}$  is the currents of the three stages in the above-mentioned analysis;  $I_{dceq}$  is the equivalent dc current, which is the system dc current in Stage I, and dc chopping current in Stages II and III.

### C. System Requirements for HCBs Serving as DCC

In the dc chopping process, the key to HCBs serving as DCC is to establish  $U_{TIV}$  of  $\sim 1$ p.u., ensuring that the dc chopping current ( $I_D$ ) as expressed in (21) is similar to the  $I_{dc}$  during normal system operation in (5)

$$I_D = \frac{U_{DRU} - U_{TIV}}{R_{dc}}. \quad (21)$$

The set values of  $U_{TIV}$  and  $I_D$  are  $U_{TIVset}$  and  $I_{Dset}$  respectively, which can be expressed as follows:

$$\begin{cases} U_{TIVset} = U_{dcN} \\ I_{Dset} = \frac{P_{WFN}}{U_{dcN}} \end{cases} \quad (22)$$

where  $P_{WFN}$  is the rated power of WF in a single DRU-MMC circuit.

Equation (22) determines the operating point on the volt-ampere characteristics of MOVs for partially operated SSSs. Based on the operating point, the total MOV rated voltage ( $U_{MOVN}$ ) established by the partially operated SSSs can be calculated as follows:

$$U_{MOVN} = \frac{U_{TIVset}}{f_{MOV}(I_{Dset})} = \frac{U_{dcN}}{f_{MOV}(P_{WFN}/U_{dcN})} \quad (23)$$

where  $f_{MOV}(I)$  is the residual voltage coefficient corresponding to the current  $I$  by referring to volt-ampere characteristics of MOVs.

Based on (22) and (23), the total number of operated SSSs ( $n_D$ ) can be calculated as follows:

$$n_D = \left\lceil \frac{U_{MOVN}}{U_{MOVN1}} \right\rceil = \left\lceil \frac{U_{dcN}}{f_{MOV}(P_{WFN}/U_{dcN})U_{MOVN1}} \right\rceil \quad (24)$$

where the rated voltage of MOV in each SSS is set to  $U_{MOVN1}$ , and the ceiling function is employed.

#### D. Parameter Design of HCBs With Extended DCC Function

As illustrated in Fig. 1(a), for the branch path of DRU1-MMC, the two HCBs (HCB1 and HCB2) dissipates  $P_{WF1}$ . Thus, these two HCBs can be regarded as an integrated unit. This unit establishes a pole-to-pole dc voltage, and its current and power capacity align with those in normal operation of the branch path ( $U_{dcN}$  and  $P_{WFN}$ ). The IGBT quantity and energy dissipation capacity of the integrated unit (HCB1+HCB2) are designed as follows.

Given that the voltage and current of HCBs in dc interruption are greatly higher than those in dc chopping, the number of IGBTs (5SNA 3000K452300; 4.5 kV/3 kA) should be determined based on dc interruption. According to the DRU-MMC-MTDC system as shown in Fig. 1(a) with  $P_{WFN} = 1000$  MW and  $U_{dcN} = 640$  kV, HCBs have a withstand voltage of  $\sim 1.5$  p.u. (960 kV) for dc interruption. Considering a safety margin of 1.1, the number of IGBTs in series is 236. Since the 4.5kV/3kA IGBT is able to turn off a fault current of  $\sim 19$  kA [17], only IGBTs in series connection can meet the interruption requirement.

The energy dissipation capacity of MOV is determined by the maximum energy between dc interruption and dc chopping. The energy dissipation capacity of dc interruption ( $E_{D1}$ ) is the total energy of two dc interruptions, which depends on the magnetic field energy stored in the fault circuit [20], and can be calculated as follows:

$$E_{D1} = k(L_{dc} + L_{line})I_{peak}^2 \quad (25)$$

where  $k$  is the safety margin of 1.2,  $L_{dc}$  and  $L_{line}$  are the dc inductance and equivalent inductance of dc transmission line,  $I_{peak}$  is the peak dc current.

In this example,  $L_{dc}$  is 300 mH,  $L_{line}$  is 1.5 mH/km  $\times$  200 km [21], and  $I_{peak}$  is 20 kA. The energy dissipation capacity of dc interruption is 288 MJ.

The energy dissipation capacity of HCBs serving as DCC ( $E_{D2}$ ) can be expressed as follows:

$$E_{D2} = kP_{WFN}T_D. \quad (26)$$

In this example,  $k$  is 1.2,  $P_{WFN}$  is 1000 MW, and  $T_D$  is 100 ms. The energy dissipation capacity of HCBs serving as DCC is 120 MJ.

The energy dissipation capacities of each MOV unit under dc interruption and dc chopping are defined as  $E_{MOV1}$  and  $E_{MOV2}$ , which can be calculated as follows:

$$\begin{cases} E_{MOV1} = \frac{E_{D1}}{n_{MOV}} \\ E_{MOV2} = \frac{E_{D2}}{n_D} \end{cases} \quad (27)$$

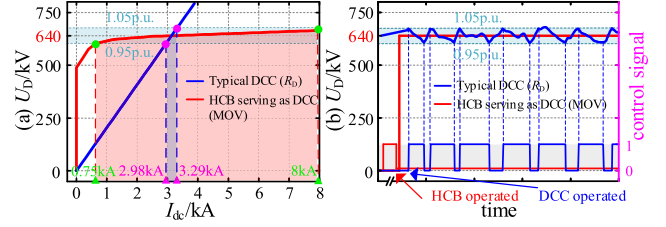


Fig. 6. Characteristics of  $R_D$  in DCC and MOVs in HCBs serving as DCC. (a) Volt-ampere characteristics. (b) Control mode and corresponding  $U_D$ .

where  $n_{MOV}$  is the total number of MOV units,  $n_D$  is the operated MOVs in HCBs serving as DCC.

In this example,  $n_{MOV}$  is 320 and  $n_D$  is 223.  $E_{MOV1}$  and  $E_{MOV2}$  are 0.9 MJ and 0.54 MJ respectively.

Based on the above-mentioned analysis, the energy dissipation capacity of MOV is designed according to dc interruption, which is 288 MJ. In this case, after the integration of DCC function into HCB, it is unnecessary to expand the energy dissipation capacity of MOV. However, after the energy dissipation of MOV insides HCBs, 2–3 h should be preserved for the cooling of MOVs, until the next operation of HCB can be activated for dc interruption or dc chopping.

#### E. Natural Power Matching of HCB Serving as DCC Without Duty Cycle Control

As mentioned in Section II-B, duty cycle control has to be adopted by DCC for power matching. However, with MOV in HCB serves as the energy dissipating element, the matching relation between MOV and  $\Sigma P_{WF}$  can be realized naturally without any duty cycle control.

Taking DRU-MMC-MTDC system in Fig. 1(a) with  $\Sigma P_{WFN} = 2000$  MW,  $P_{WFN} = 1000$  MW and  $U_{dcN} = 640$  kV as an example,  $R_D$  in DCC and MOVs in HCBs are designed according to  $\Sigma P_{WFN}$  and  $P_{WFN}$  respectively. For DCC,  $R_D$  can be configured according to (8), while the parameters of HCBs can be determined by (23) and (24).

The volt-ampere characteristics of  $R_D$  in DCC and MOVs in HCBs serving as DCC are depicted in Fig. 6(a). The switching thresholds of DCC are set between 0.95 and 1.05 p.u., which limits the adjustable current range to 2.98–3.29 kA without duty cycle control. Compared with DCC, HCBs serving as DCC have a wider current range of 0.75–8 kA, which indicates that HCBs have better natural power matching characteristics.

As shown in Fig. 6(b), the support voltage ( $U_D$ ) of DCC oscillates at high-frequency within the voltage threshold by controlling duty cycle, leading to multiple switching operations of DCC. In contrast, HCBs are operated by 2 ms mono-pulse control signal with  $U_D$  sustaining a stable voltage of 1 p.u., which significantly enhances the system stability in dc chopping process.

Therefore, when HCB serves as DCC, natural power matching can be realized without any extra control, which is simpler than the duty cycle control of DCC for power matching.

TABLE I  
MODEL PARAMETERS

Index	Parameters	Value
MMC	Rated DC voltage	640 kV
	Number of sub modules in MMC	100
	Capacitance of sub module	10 mF
	Inductance of bridge arm	100 mH
	DC inductance	300 mH
DRU and wind farm	Rated active power of wind farm1/wind farm2	1000/1000 MW
	Reactive power compensation	400 MVar
	Transformer of 12-pulse DRU (Y/Δ)	66/260 kV
HCB	Number of SSSs in HCBs ( $n_{MOV}$ )	320
	Rated voltage of MOV in SSS ( $U_{MOVNI}$ )	2 kV
	Number of operated SSSs in HCBs serving as DCC ( $n_D$ )	223
Line and fault setting	Line length of DRU1-MMC/DRU2-MMC transmission line	200/160 km
	Line length of AC transmission line L1/L2	20/20 km
	Fault line	L1
	Fault location	10 km away from MMC

TABLE II  
VOLT-AMPERE CHARACTERISTICS OF MOV

Current (kA)	Voltage (p.u.)	Current (kA)	Voltage (p.u.)
$1.00 \times 10^{-6}$	1	5	1.49
$5.00 \times 10^{-6}$	1.12	10	1.55
0.5	1.37	12.5	1.56
1.25	1.43	25	1.57
2.5	1.46	37.5	1.58

#### IV. SIMULATION AND RESULT DISCUSSION

##### A. Model Parameters

The DRU-MMC-MTDC system, as shown in Fig. 1(a), is established in PSCAD/EMTDC. Main parameters of various models and fault settings are summarized in Table I. It should be noted that equivalent integrated grid-forming wind farms (WF1 and WF2) are built in this model to simplify the simulation.

The volt-ampere characteristics of MOV inside SSS provided by the manufacturer are listed in Table II.

##### B. Simulation Results

At  $t = 2.000$  s, a three-phase ac fault occurs at  $F_2$  in the onshore ac grid, as shown in Fig. 1(a). Simulation results of the branch path of DRU1-MMC with the proposed method are shown in Fig. 7.

At  $t = 2.008$  s, the proposed method is activated as the dc voltage of MMC ( $U_{MMC}$ ) exceeds 1.1 p.u. After FMS reaches a certain breaking distance, IGBTs in partial SSSs are turned OFF and MMC is bypassed at  $t = 2.010$  s.  $U_{MMC}$  rapidly decays to zero as shown in Fig. 7(b), effectively preventing overvoltage of SMs in MMC as shown in Fig. 7(d). Meanwhile, the integrated unit of HCB1 and HCB2 establishes a  $U_{TIV}$  of  $\sim 640$  kV as shown in Fig. 7(c). The dc chopping current and power stabilize after transient fluctuations from 0.985–1.010 p.u., reaching levels nearly similar to rated values, as shown in Fig. 7(a) and (e). The operated MOVs dissipate the energy of 95.790 MJ in Fig. 7(c). This process proves that HCBs serving as DCC fully have the dc chopping capability.

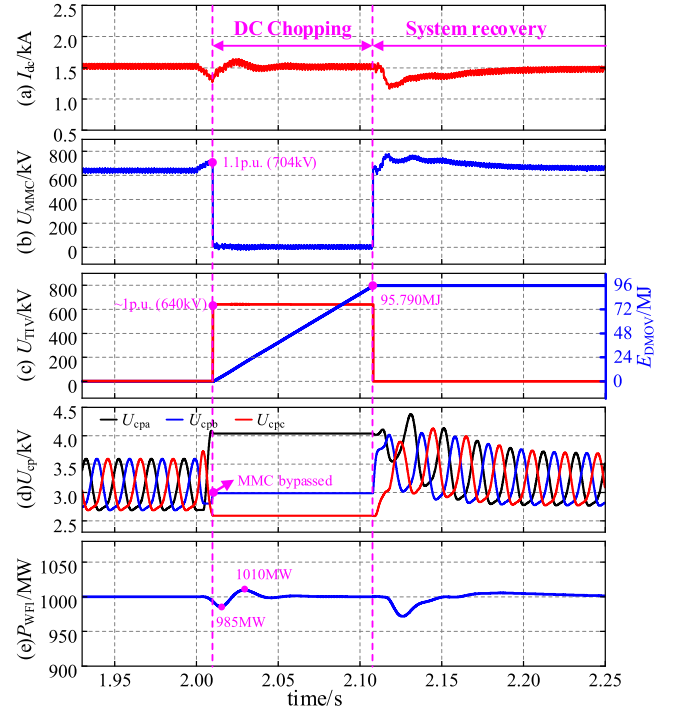


Fig. 7. Simulation results of the proposed method dealing with an onshore AC fault for DRU1-MMC branch path. (a) DC current. (b) DC voltage of MMC. (c) Transient interruption voltage and energy dissipation of HCB. (d) Average capacitor voltage of upper bridge arm. (e) Active power of generated by WF1.

Upon the ac fault is cleared completely, the system recovery is acted at  $t = 2.108$  s. MMC is restored to normal modulation and the HCBs are reclosed. The dc current is reinjected into the MMC, resuming the power transmission to MMC. The power absorbed on the onshore ac side gradually increases to a normal level, while the power on the dc side still transmits to MMC. Therefore, the power imbalance between the ac and dc sides leads to a voltage rise of MMC capacitors, as shown in Fig. 7(d), which is a transient process.

The ac current and bridge arm current are shown in Fig. 8. In Stage I (2.000–2.008 s), as depicted in Fig. 8(b) and (c),  $i_{L2}$  and  $i_{sMMC}$  increase rapidly due to the ac fault, which forms  $i_{L1}'$  as shown in Fig. 5(a) and Fig. 8(a) to feed current to the fault point. In Stage II (2.008–2.061 s), the sum of  $Z_{sMMC}$  and  $1/2Z_0$  is larger than  $Z_{L1}'$ , causing ac grid to feed a smaller forced component of ac current to MMC. Affected by the stage transition, the dc offset caused by the natural component of ac current is more severe.  $i_{sMMC}$  and  $i_p$  in Stage II exhibit pulsating characteristics with exponential decay, as shown in Fig. 8(c) and (d). In Stage III (2.061–2.108 s), the ac grid still feeds power to MMC through L2 in Fig. 8(b). As the ac current is greater than the dc chopping current in upper bridge arm current ( $i_p$ ) according to (20), the peak current of  $i_p$  is  $\sim 6$  kA in Phase B, as shown in Fig. 8(d). In these three stages,  $i_p$  is consistently within the tolerable range of the bridge arm current, ensuring safe operation and reliability of MMC during dc chopping.

To verify the natural power matching characteristics of the proposed method, different WF power conditions (1000, 750, and 500 MW) of  $P_{WFN}$  are simulated. The WF power affects the

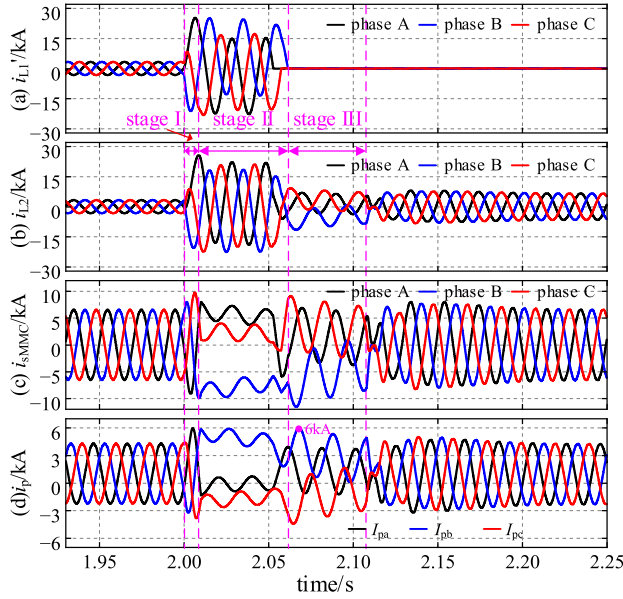


Fig. 8. Simulation results of AC current and bridge arm current. (a) AC current of L1 to the right of the fault point. (b) AC current of L2. (c) AC current of MMC. (d) Current of upper bridge arm.

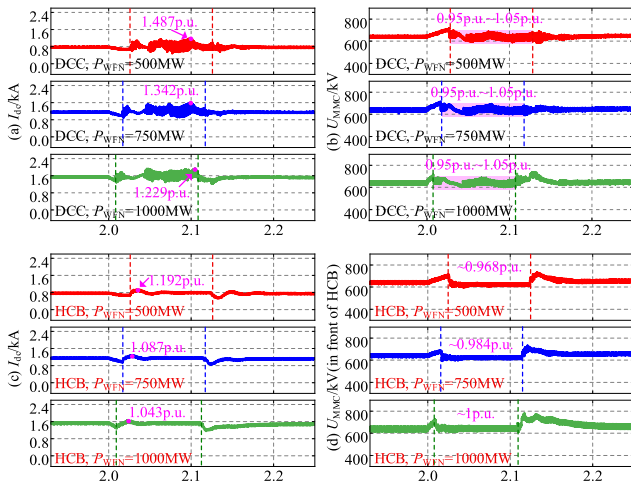


Fig. 9. Simulation results of DCC and HCB serving as DCC under different WFN power conditions. (a) DC current when using DCC. (b) DC voltage of MMC when using HCB. (c) DC current when using HCB. (d) DC voltage of MMC in front of HCB when using HCB.

overtoltage rise rate of MMC under ac fault, which influences the activation time of dc chopping (1000 MW, 2.008 s; 750 MW, 2.014 s; 500 MW, 2.024 s).

The simulation results of DCC are shown in Fig. 9(a) and (b) with the thresholds are set between 0.95 and 1.05 p.u. Although  $R_D$  is matched with  $\sum P_{WFN}$  of 2000 MW, the duty cycle control is affected by the transient fluctuations of system state transition, resulting in frequent switching of DCC. When  $P_{WFN}$  is 750 and 500 MW, the operation time of the duty cycle control increases compared to  $P_{WFN}$  of 1000 MW, causing the duration of current and voltage oscillation to be prolonged. In these three conditions, the peak of current fluctuation reaches up to 1.487 p.u.

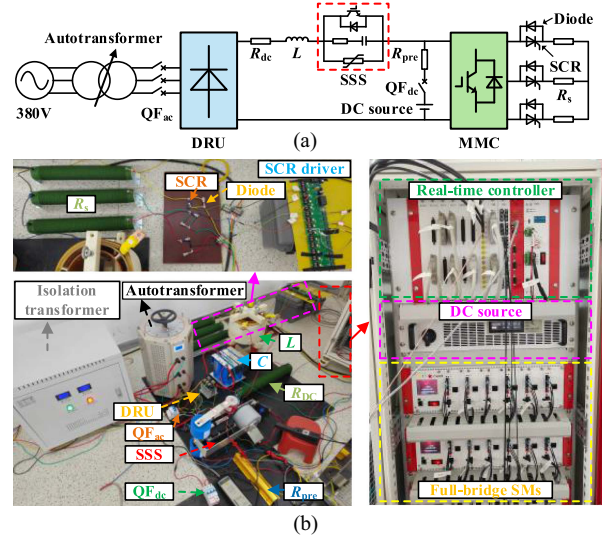


Fig. 10. Experimental platform. (a) Circuit. (b) Picture.

TABLE III  
EXPERIMENTAL PARAMETERS

Parameters	Value	Parameters	Value
Number of sub modules in MMC	5	Pre-charged resistance ( $R_{pre}$ )	40 $\Omega$
Capacitance of sub module	4340 $\mu\text{F}$	DC inductance ( $L$ )	50 $\mu\text{H}$
Inductance of bridge arm	2.5 mH	Buffer capacitance of SSS	5 $\mu\text{F}$
DC resistance ( $R_{dc}$ )	10 $\Omega$	Buffer resistance of SSS	5 $\Omega$
AC resistance ( $R_s$ )	10 $\Omega$	$U_{TIV}$ of SSS	395 V

The simulation results of the proposed method are shown in Fig. 9(c) and (d). It should be noted that the dc voltage of MMC in front of HCBs is measured in Fig. 9(d). Benefiting from the natural power matching characteristics of MOV,  $U_{TIV}$  in the three cases are 1, 0.984, and 0.968 p.u., respectively, which can support the dc voltage without duty cycle control. The peaks of dc currents in three cases are 1.043, 1.087, and 1.192 p.u., respectively. Compared with DCC, the dc voltage and the current remain in a stable state for HCBs serving as DCC.

## V. EXPERIMENTAL VERIFICATION

### A. Experimental Platform

To verify the proposed method, a down-scaled DRU-MMC experimental system shown in Fig. 10(a) is established. A picture of the experimental platform is shown as Fig. 10(b).

Key parameters are listed in Table III, where the MOV MYN2-300/20 kJ provided by Kesaier is configured in SSS. The entire experiment are controlled by RTU-BOX206 controller provided by RTUnit.

To validate the proposed method under the voltage level of  $U_{TIV}$ , the line voltage at ac side of DRU and modulation ratio of MMC are adjusted to change dc current and power transmission: case1 (345 V, 0.5); case2 (355 V, 0.6) and case3 (365 V, 0.7). In these cases,  $U_{DRU}$  is set to 435, 450, and 465 V, respectively. Meanwhile,  $U_{MMC}$  is configured to 400 V to match  $U_{TIV}$ .

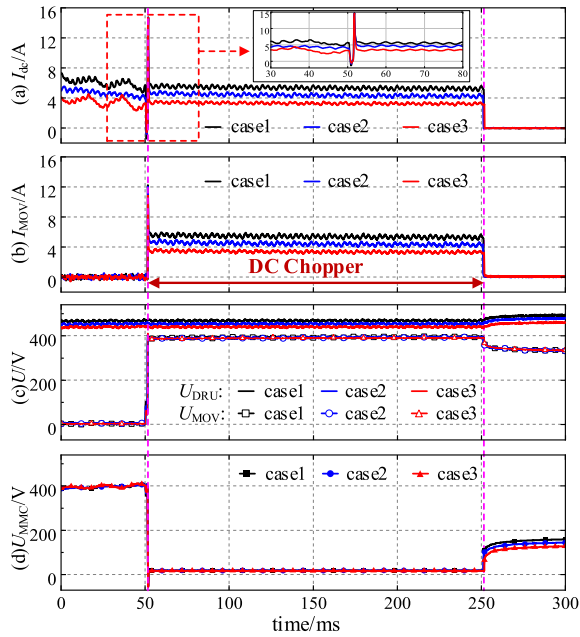


Fig. 11. Experimental results of proposed method. (a) DC current (b) MOV current. (c) DRU voltage and MOV voltage. (d) MMC voltage.

## B. Results and Discussion

In the normal operation of experimental system at  $t = 0\text{--}50$  ms in Fig. 11, the ac source transmits power to MMC through DRU. As shown in Fig. 11(c) and (d), by setting  $U_{MMC}$  to 400 V and  $U_{DRU}$  to 435, 450, and 465 V, three cases with different power conditions are tested. Referring to (5), the corresponding  $I_{dc}$  for three cases are about 3.5, 5, and 6.5 A, as shown in Fig. 11(a).

At  $t = 50$  ms, the proposed method is activated. For system safety, the operation of SSS precedes the bypass of MMC. The IGBT in SSS is turned off at  $t = 50$  ms, followed by MMC bypass after 1 ms delay. As shown in Fig. 11(c), regardless of  $U_{DRU}$  variations,  $U_{SSS}$  maintains  $\sim 395$  V. The chopping current flows through MOV, matching  $I_{dc}$  of system normal operation, as shown in Fig. 11(a) and (b). After the chopping process lasts for 200 ms, following MMC blocked, the experiment ends. The currents shown in Fig. 11(a) and (b) drop to zero and voltages shown in Fig. 11(c) and (d) are meaningless after  $t = 251$  ms.

It should be noted that when MMC is bypassed at  $t = 51$  ms,  $U_{SSS}$  is established immediately, but transient spikes occur in both  $I_{dc}$  and  $I_{MOV}$ , which are attributed to measurement issues of the current sensor.

## VI. PERFORMANCE COMPARISON

For the DRU-MMC-MTDC system shown in Fig. 1(a), a DCC is needed in the conventional method, while the proposed method utilizes four HCBs (HCB1+HCB2 and HCB3+HCB4) to meet dc chopping requirements of two branch paths. The comprehensive performance comparison of the proposed method and the conventional method is summarized in Table IV, where the total parameters of HCBs for two branch paths are considered. Compared with the conventional method of HCBs+DCC, the proposed method integrates the dc interruption and DCC functions into HCBs. Owing to the functional integration, the

TABLE IV  
COMPARISON OF THE CONVENTIONAL AND PROPOSED METHODS

Index	Conventional method	Proposed method
<b>Configured equipment</b>	HCBs + DCC	HCBs (serving as DC interruption device and DC chopper)
Total number of IGBTs	$236 \times 2$ (HCBs, 2 paths) + 157 (DCC)	$236 \times 2$ (2 paths)
Energy dissipation elements	MOV(HCBs) + $R_D$ (DCC)	MOV
Energy dissipation capacity	$288\text{MJ} \times 2$ (HCBs, 2 paths) + $240\text{MJ}$ (DCC)	$288\text{MJ} \times 2$ (2 paths)
<b>Investment cost</b>	high	low
Power matching ability in DC chopping	low	high
Control method	high-frequency control + mono-pulse control	mono-pulse control
<b>Control complexity</b>	high	low

total number of IGBTs in the proposed method is reduced by 25%. Meanwhile, the MOV energy dissipation capacity in HCBs is  $288\text{MJ} \times 2$ , fully meeting the requirements of dc interruption and dc chopping. The proposed method completely eliminates the investment cost of DCC.

The natural power matching performance of the proposed method is superior to that of DCC. Therefore, HCBs serving as DCC only requires mono-pulse control instead of high-frequency duty cycle control in DCC to meet different chopping requirements.

In conclusion, the proposed method uses HCBs to integrate the DCC function and dc interruption function, and improves the utilization rate of HCBs, which saves equipment investment and simplifies the control complexity compared to DCC.

## VII. CONCLUSION

This article proposes a DCC function extension method for HCBs in the DRU-MMC-MTDC system. First, the dc chopping requirements for ensuring the safety of MMC and wind farms are emphasized through modeling analysis, and the working principle and parameter design of DCC are analyzed. Second, the working principle and characteristics of the proposed method are analyzed. By tripping HCBs and bypassing MMC, MOVs in a preset number of SSSs are operated to establish the transient interruption voltage of 1 p.u., absorbing surplus power from offshore wind farms. Then, simulations and experiments are carried out to validate the proposed method. In the end, a performance comparison is conducted. Compared with DCC, the proposed method achieves a 25% reduction in the number of IGBTs and demonstrates better natural power matching characteristics. The proposed method integrates DCC function and dc interruption function, reducing the equipment investment and simplifying the control complexity for onshore ac fault ride-through.

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**Zhe Zhang** was born in Tianjin, China, in 2000. He received the B.S. degree in electrical engineering, in 2023, from Tianjin University, Tianjin, China, where he is currently working toward the M.S. degree in electrical engineering.

His research focuses on dc circuit breakers.



**Weijie Wen** was born in Shandong Province, China, in 1989. She received the B.S. degree in electrical engineering from Sichuan University, Chengdu, China, in 2012, and the Ph.D. degree in electrical engineering with Tsinghua University, Beijing, China, in 2017.

She is currently an Associate Professor with the State Key Laboratory of Intelligent Power Distribution Equipment and System, Tianjin University, Tianjin, China. She is currently working in the fields of direct current circuit breakers, fast mechanical switch, and current limiters.



**Bin Li** received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from Tianjin University, Tianjin, China, in 1999, 2002, and 2005, respectively.

He is currently a Professor with the School of Electrical Engineering and its Automation, Tianjin University. His research interests include the protection and control of power systems and microgrids.



**Botong Li** received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from Tianjin University, Tianjin, China, in 2004, 2007, and 2010, respectively.

He is currently a Professor with the School of Electrical and Information Engineering, Tianjin University. His research interest focuses on protection and control of power systems.