Boost Mode Analysis and ZVS-Guaranteed Control Strategy for Frozen Leg Operation of Three-Phase Dual Active Bridge Converters

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***Abstract*—The frozen leg method is an effective fault-tolerant approach for addressing open-circuit faults in three-phase dual-active-bridge converters, requiring no additional hardware. This method isolates the faulty leg by disabling its two switches so that the converter can continue operating at reduced power levels. Prior literature on the frozen leg method primarily focuses on cases with unity voltage gain or buck mode. However, in boost mode where a higher voltage difference must be overcome, the faulty phase may enter discontinuous current mode (DCM), introducing additional complexity and necessitating a new mathematical framework. Thus, this article presents the first comprehensive investigation of boost mode frozen leg operation, proposing a novel analytical framework for the DCM. The analysis of boost mode is divided into five distinct cases, with corresponding derivations for power, current, and voltage equations. The findings show significant differences in operation compared to buck and unity gain modes. Additionally, this research derives the maximum power transfer achievable in boost mode and conducts a detailed soft-switching analysis. Based on this analysis, a ZVS-guaranteed control strategy is proposed to ensure that the operating points remain within the high-efficiency ZVS region. Experimental results are provided to validate the theoretical analysis.**

***Index Terms*—DC–DC converter, fault tolerance, reliability.**

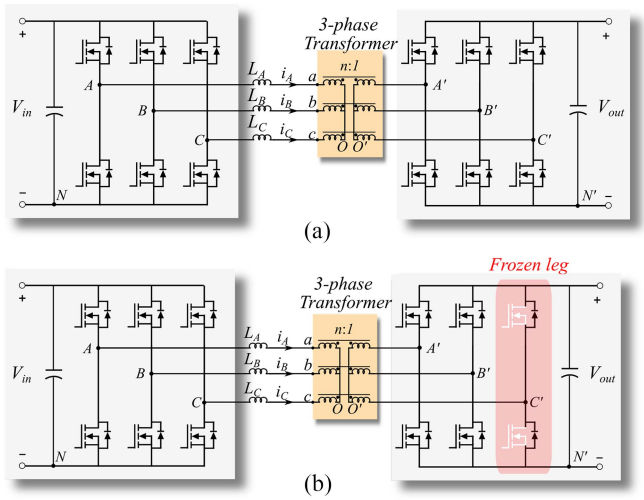

Fig. 1. (a) Circuit topology of the 3p-DAB converter. (b) Equivalent circuit topology in frozen leg mode.

I. Introduction

THE single-phase dual-active-bridge (1p-DAB) and three-phase dual-active-bridge (3p-DAB) converters are both widely employed in dc–dc power conversion applications [1], [2]. Among them, the 3p-DAB, as shown in Fig. 1(a), provides distinct benefits including improved electromagnetic interference, increased power density, and reduced filter capacitor size [3], [4], [5], [6]. These advantages make it particularly well-suited for high-power-density applications, such as power interfaces in naval vessels, electric aircraft, and railway systems [7], [8], [9], [10]; solid-state transformers within dc grids [11], [12], [13], [14]; auxiliary power modules (APMs) and onboard chargers in electric vehicles [3], [15], [16]; battery-connected energy storage interfaces [17], [18]; and photovoltaic systems [19].

While the increased number of switches in the 3p-DAB converter can raise the likelihood of failures in switches or gate drivers [20], the topology's inherent structural redundancy contributes to enhanced fault tolerance. This allows the system to maintain operation under specific fault scenarios, thereby improving overall reliability [21], [22]. Industry surveys indicate that gate driver failures (15%) and semiconductor device failures (31%) are major contributors to component failures [23], with the former causing open-circuit failures (OCFs) and the latter leading to both OCFs and short-circuit failures.

Since OCFs generally have a less critical impact on converter operation, the 3p-DAB can still support partial power transfer by leveraging appropriate fault-tolerant techniques [22], [24], [25]. A typical fault-tolerant technique involves identifying the specific switch affected by the OCF, then using a fault-tolerant control method to sustain system functionality until maintenance or replacement can be carried out.

Much research has been dedicated to fault detection and fault-tolerant control of DAB-type converters with OCFs [22], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35],

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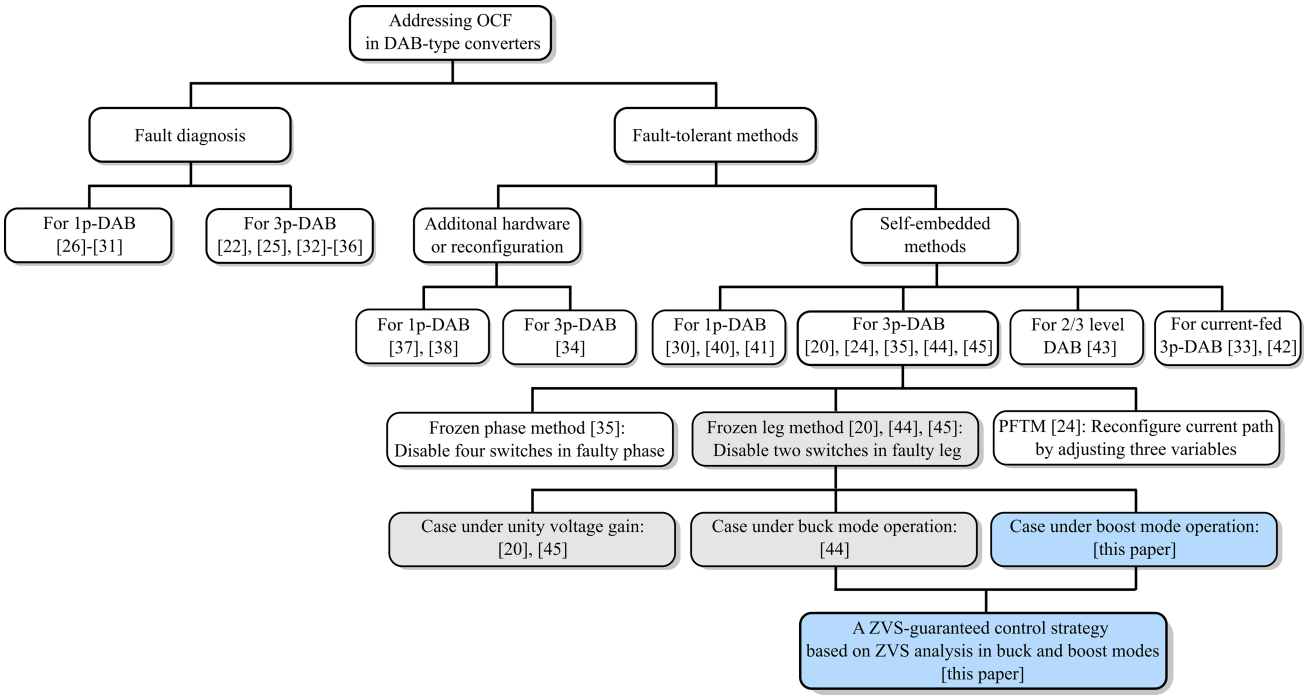


Fig. 2. Diagram of the literature review on addressing open-circuit failures in DAB-type converters.

[36], as shown in Fig. 2. After identifying an OCF, fault-tolerant control should be deployed to minimize its effects on system performance. Research on these strategies can be categorized into two main approaches. The first involves increasing system redundancy through additional hardware or topological modifications. For example, Berger et al. [34] proposes integrating three bidirectional switches into the 3p-DAB converter to isolate the faulty phase under OCF conditions. In [37], the 1p-DAB converter is modified with a center-tapped transformer along with auxiliary inductors. Moreover, Bhakar and Jayaraman [38] proposes inserting a fast-acting fuse and capacitor in series with the transformer of a 1p-DAB system. Despite their effectiveness, these hardware-based methods inevitably increase design complexity and implementation costs [24].

The second approach, which this article focuses on, is self-embedded fault-tolerant control [39], where fault tolerance can be achieved without the need for extra hardware. A variety of self-embedded fault-tolerant techniques for DAB converters are investigated in [30], [33], [40], [41], [42], [43], [44], [45], as shown in Fig. 2. However, only limited studies specifically explored the self-embedded fault-tolerant methods for 3p-DAB converters under OCF. One representative approach is the frozen leg method [20], which disables both switches in the faulty leg upon fault detection, as shown in Fig. 1(b). This enables the 3p-DAB converter to operate at lower power, with the antiparallel diodes in the faulty leg providing a freewheeling path. In contrast, Davoodi et al. [35] suggests deactivating all four switches in the primary and secondary sides of the damaged phase, leading to four anti-parallel diodes conducting in freewheeling mode. This significantly complicates the waveform analysis and further reduces the power transfer capability compared to the frozen leg method. Another approach, the path-based method proposed in [24], dynamically adjusts three distinct phase-shift angles to reconfigure current paths, thereby alleviating current stress and enhancing power transfer. However, its reliance on multiple control variables makes implementation complex and optimization challenging. Moreover, this method may introduce dc bias in the current under certain conditions, potentially leading to magnetic core saturation, increased device stress, and reduced system efficiency [46].

Compared to other methods, the frozen leg method from [20] has multiple benefits. It employs a relatively straightforward control scheme that requires adjusting only one phase shift angle and naturally eliminates dc bias due to the symmetrical disabling of the lower and upper switches in the faulty leg. However, the study in [20] is confined to the unity voltage gain condition ($V_{\rm in} = nV_{\rm out}$), which limits its generalizability to practical applications. In real-world scenarios, the converter frequently operates under nonunity gain conditions, including buck ($V_{\rm in}>nV_{\rm out}$) and boost ($V_{\rm in}<nV_{\rm out}$) modes, driven by various factors [1], [47], [48]. For example, significant voltage variation is common within battery-based systems such as energy storage units [17], [18] and onboard chargers and APMs in electric vehicles [15], [16], due to changing battery state-of-charge which leads to buck and boost operation. Similarly, in railway dc microgrids, the input voltage can vary by up to 700 V, requiring the converter to adapt beyond unity gain [10]. Additionally, in renewable energy applications [49], power output variability from sources like solar panels or wind turbines results in unstable dc voltages, often shifting the converter into non-unity gain. Although assuming unity voltage gain facilitates theoretical analysis [20], [45], this simplification does not hold

under these buck and boost conditions. To address this gap, Wang and Bauman [44] has extended the analysis of frozen leg operation to buck mode through three representative cases, yet the corresponding boost mode analysis remains unaddressed in the literature. While the 3p-DAB converter exhibits theoretical equivalence between reverse buck and forward boost operations under normal conditions, this symmetry breaks down during frozen leg operation due to the critical dependence on fault location and power flow direction. In boost mode, the faulty phase current becomes discontinuous as it must overcome an increased voltage potential difference, introducing additional complexity and necessitating an entirely new mathematical framework. Furthermore, the power transfer characteristics and soft-switching conditions in boost mode differ significantly from those in buck mode. Therefore, a dedicated analysis of boost mode operation is essential, which forms the primary focus of this article. The main contributions of this article can be summarized as follows.

1) **A novel discontinuous current mode (DCM) analysis** for 3p-DAB frozen leg operation in boost mode, addressing the discontinuous current behavior caused by the increased voltage potential difference.
2) **New derivations of voltage and current equations** for 3p-DAB frozen leg operation in boost mode, incorporating the proposed DCM analysis. A key finding is that as the phase shift angle increases, the duration of the DCM gradually decreases, leading to five distinct operational cases in boost mode.
3) **New derivations of power transfer expressions** for the five identified cases. The results show that the power transfer behavior under the boost mode significantly differs from both normal operation and the buck-mode frozen leg case. Understanding these power transfer expressions can facilitate the development of effective control strategies.
4) **New calculation of the maximum transferred power** for 3p-DAB frozen leg operation in boost mode. These findings demonstrate that the maximum power transfer diverges further from normal operation as the voltage rises. Understanding the maximum power available at different voltage rises is useful for system control in practical applications.
5) **A comprehensive investigation of the soft-switching operational regions.** The results show that while secondary-side healthy switches always achieve zero-voltage switching (ZVS), primary-side healthy switches can only maintain ZVS under specific operating conditions. This finding provides valuable insights for thermal management design.
6) **A novel ZVS-guaranteed control strategy** for 3p-DAB frozen leg operation is proposed, which can ensure ZVS for all switches and thereby enhance efficiency.

Furthermore, these contributions are thoroughly validated through experimental tests.

The rest of this article is organized as follows: Section II presents the mathematical modeling and power transfer equations of the 3p-DAB in boost mode in normal operating conditions, Section III introduces a new mathematical model for faulty phase DCM and derives voltage and current expressions for five distinct cases in boost mode under frozen leg operation, Section IV formulates the corresponding power transfer equations, Section V investigates the soft-switching operational regions, Section VI proposes a ZVS-guaranteed control strategy based on the derived ZVS region, Section VII presents the experimental setup and results. Finally, Section VIII concludes the article.

II. Analysis of Boost Mode of 3p-DAB Under Normal Operation

The 3p-DAB mathematical model and power transfer characteristics for normal operation in boost mode are presented here as a reference for comparison. It is assumed that the 3-phase transformer is ideal (infinite magnetizing inductance, equal leakage inductances across all phases such that $L = L_A = L_B = L_C$, and negligible resistance in the windings [50]), as presented in Fig. 1. The mathematical model that relates the leg voltages to the phase currents, voltages, and inductor voltages is given in (1), with detailed derivations provided in [44] and [45]

$$\begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} v_{AN} - nv_{A'N'} \\ v_{BN} - nv_{B'N'} \\ v_{CN} - nv_{C'N'} \end{bmatrix} = \begin{bmatrix} v_{LA} \\ v_{LB} \\ v_{LC} \end{bmatrix} = \begin{bmatrix} L\frac{di_A}{dt} \\ L\frac{di_B}{dt} \\ L\frac{di_C}{dt} \end{bmatrix}. \tag{1}$$

The leg voltages (v_{AN}, v_{BN}, v_{CN}, $v_{A'N'}$, $v_{B'N'}$, and $v_{C'N'}$) are used as the control variables in the mathematical model because they are directly modulated by the switching signals and are also affected by the dc input and output voltages, V_{in} and V_{out}.

This article adopts single-phase shift modulation as the standard control scheme, as it is commonly employed in fault-tolerant methods for 3p-DAB converters [20], [34], [35]. The power transfer under normal operation in boost mode can be calculated using (2), as derived in [48]

$$P_{\text{norm}} = \begin{cases} \frac{nV_{\text{in}}V_{\text{out}}}{2\pi f_s L}\phi\left(\frac{2}{3} - \frac{\phi}{2\pi}\right), & 0 \le \phi \le \frac{\pi}{3} \\ \frac{nV_{\text{in}}V_{\text{out}}}{2\pi f_s L}\left(\phi - \frac{\phi^2}{\pi} - \frac{\pi}{18}\right), & \frac{\pi}{3} < \phi \le \frac{\pi}{2} \end{cases} \tag{2}$$

where f_s is the switching frequency and ϕ is the phase shift angle. Notably, this equation also holds for cases of normal operation under buck mode and unity gain mode.

III. Analysis of Boost Mode of 3p-DAB Under Frozen Leg Operation

Unlike in buck mode, the frozen-leg operation of the 3p-DAB converter in boost mode can result in discontinuous faulty phase currents at certain times, which is the most significant difference between the analyses of buck and boost modes and has been experimentally verified. The reason is that in boost mode, the converter must overcome a higher voltage potential difference, whereas in buck mode, the current naturally flows toward the lower voltage potential on the secondary side. Consequently, the emergence of discontinuous current mode (DCM) in boost mode necessitates a new analytical framework.

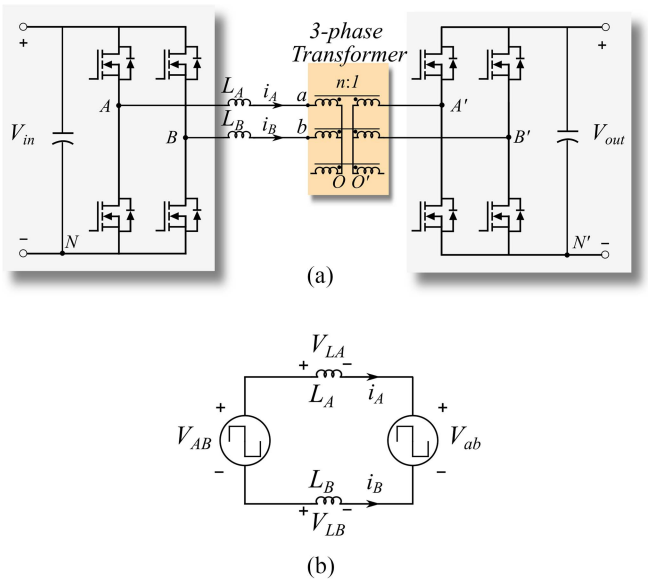


Fig. 3. (a) Topology and (b) equivalent circuit of the 3p-DAB converter under the discontinuous current mode of phase *C*.

A. Discontinuous Current Mode Analysis of the Faulty Phase

It is assumed that leg *C'* on the secondary side is the faulty leg. However, due to the symmetrical operation of all three secondary-side legs, the results are equally applicable to faults occurring in any leg.

When the faulty phase in boost mode enters DCM, the faulty branch can be neglected, leading to a new topology and equivalent circuit for the DCM, as shown in Fig. 3(a) and (b). The justification for this treatment stems from three key observations in DCM: zero current through all switches and diodes in the faulty phase, zero voltage across the leakage inductor and transformer of the faulty phase, and consequently, no interaction with the healthy phases. The Superposition Theorem provides the theoretical foundation for this branch elimination in the equivalent circuit.

Based on the newly established equivalent circuit, the new equations for phase currents and inductor voltages in DCM are derived as follows:

$$\begin{bmatrix} \frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{AN} - nv_{A'N'} \\ v_{BN} - nv_{B'N'} \end{bmatrix} = \begin{bmatrix} v_{LA} \\ v_{LB} \end{bmatrix} = \begin{bmatrix} L\frac{di_A}{dt} \\ L\frac{di_B}{dt} \end{bmatrix}. \quad (3)$$

Compared to the equivalent circuit and mathematical model of continuous current mode (CCM), the mathematical model for DCM exhibits significant modifications. These changes indicate that the derivation of current and voltage waveforms in boost mode differs fundamentally from that in buck mode, impacting all subsequent analyses, figures, equations, and findings related to boost mode operation. Also, the classification of boost mode operation must be expanded to five distinct cases.

B. Case I: Long Discontinuous Current Mode for $0 \leq \phi \leq \pi/3$

Since no faults occur in phases *A* and *B*, the corresponding phase voltages V_{AN}, $nV_{A'N'}$, V_{BN}, and $nV_{B'N'}$ remain the same as those in the normal operation case. However, in the faulty phase *C*, a long period of DCM arises when ϕ is small, as illustrated in Fig. 4. The faulty phase current only exists for a duration of ϕ_{c1} when the leg *B* upper switch is turned ON. Based on the current direction in the short CCM, the phase voltages V_{CN} and $nV_{C'N'}$ can be derived, as shown in Fig. 4.

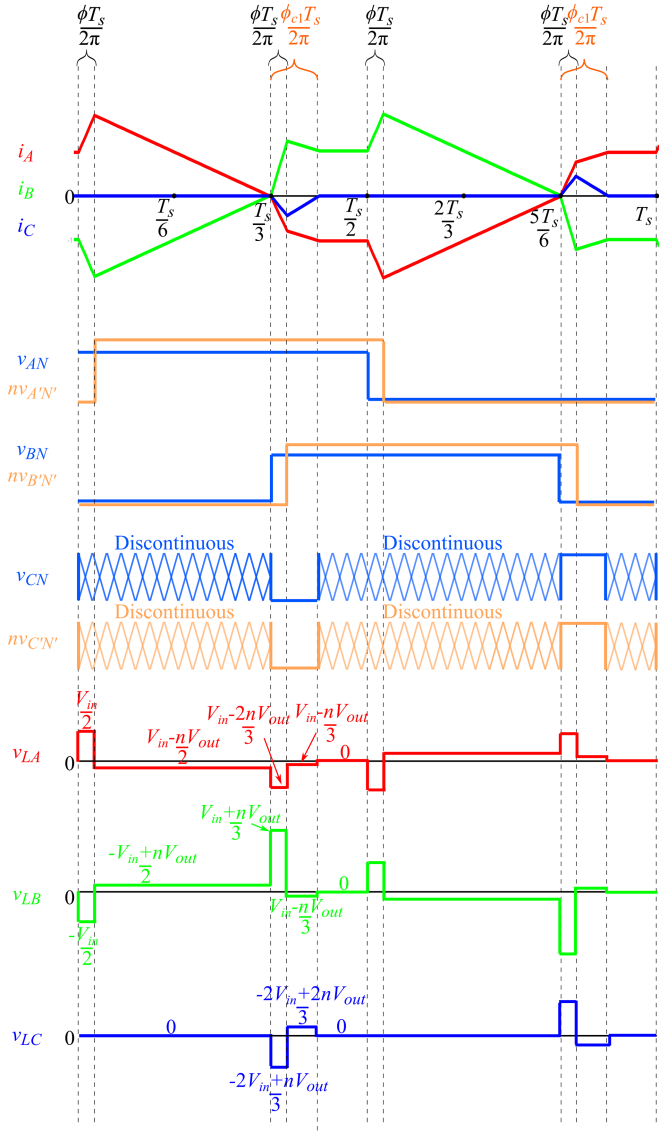


Fig. 4. Case I: phase currents and voltages, and leakage inductor voltages for boost mode of the 3p-DAB under frozen leg operation.

Since there is symmetry of the current and voltage waveforms within a single switching cycle, it is adequate to analyze only a half-cycle of each phase [48]. This half-cycle can be split into five segments, which is illustrated in Fig. 4. Given that the phase voltages follow a known pattern, the corresponding voltages of leakage inductors are found using (1) for CCM and (3) for DCM. The expressions for the calculated leakage inductor voltages are also shown in Fig. 4. Based on these voltage expressions, the current expressions for the three phases in each segment can be found using in Appendix A, Table II, using the analysis method in [48]. Here, it is assumed that the initial current value in the

first segment is $I_{AI\text{-}0}$, while the final current value at the end of the fifth segment is $I_{AI\text{-}5}$. The intermediate variables M and N are given by

$$M = \frac{T_s V_{\text{in}}}{12\pi L}, \quad N = \frac{T_s n V_{\text{out}}}{12\pi L}. \tag{4}$$

The defined value ϕ_{c1} can be calculated as

$$\phi_{c1} = \frac{nV_{\text{out}}}{-2V_{\text{in}} + 2nV_{\text{out}}}\phi. \tag{5}$$

It can be observed that ϕ_{c1} is affected by V_{in} and V_{out}, as well as ϕ. When ϕ increases to a large value but remains within [0, π/3], ϕ_{c1} will exceed π/3, transitioning the operation into the next case (case II).

C. Case II: Short Discontinuous Current Mode for $0 \le \phi \le \pi/3$

As ϕ increases within the range [0, π/3], the DCM shortens, while the duration of the CCM extends beyond π/3, which is defined as ϕ_{c2} . The healthy phase voltages still remain consistent with normal operation, as shown in Fig. 5. Based on the current direction in CCM, the phase voltages V_{CN} and $nV_{C'N'}$ can be derived as shown in Fig. 5.

Notably, in case II, ϕ_{c2} exceeds π/3, in contrast to Case I where ϕ_{c1} is less than π/3. This difference results in distinct waveform characteristics between cases I and II.

As shown in Fig. 5, the half-cycle can be divided into five segments, similar to case I. And the corresponding leakage inductor voltages are also determined using (1) for CCM and (3) for DCM. Fig. 5 also shows the expressions for the calculated leakage inductor voltages. The current equations for phases A, B, and C in each segment are given in Appendix A, Table III. The defined value ϕ_{c2} is calculated as follows:

$$\phi_{c2} = \frac{-V_{\text{in}}\frac{\pi}{3} - nV_{\text{out}}\phi}{V_{\text{in}} - 2nV_{\text{out}}}. \tag{6}$$

It can be observed that ϕ_{c2} is also influenced by V_{in} and V_{out}, as well as ϕ. However, the expression for ϕ_{c2} is more complex than that in case I. The boundary between case I and case II is reached when ϕ_{c1} is equal to π/3, which is expressed as

$$\text{boundary}_{12} = (2 - \frac{2V_{\text{in}}}{nV_{\text{out}}})\frac{\pi}{3}. \tag{7}$$

D. Case III: Two Segments of Discontinuous Current Mode for $\pi/3 < \phi \le \pi/2$

When ϕ falls within the (π/3, π/2] range, the analysis becomes more complex. Due to the increased ϕ, the duration of DCM is significantly reduced, while the healthy phase voltages V_{AN}, $nV_{A'N'}$, V_{BN}, and $nV_{B'N'}$ remain consistent with the normal operation case. However, the phase C current remains continuous for a period whenever the upper switches of phases B and C on the primary side are activated, as shown in Fig. 6. Consequently, the half-cycle includes two distinct DCM intervals, defined as ϕ_{dc1} and ϕ_{dc2}, as indicated Fig. 6. Based on the current direction in CCM, the phase voltages V_{CN} and $nV_{C'N'}$ can be derived, as shown in Fig. 6.

The half-cycle can be divided into seven segments. Similar to the previous cases, the corresponding leakage inductor voltages

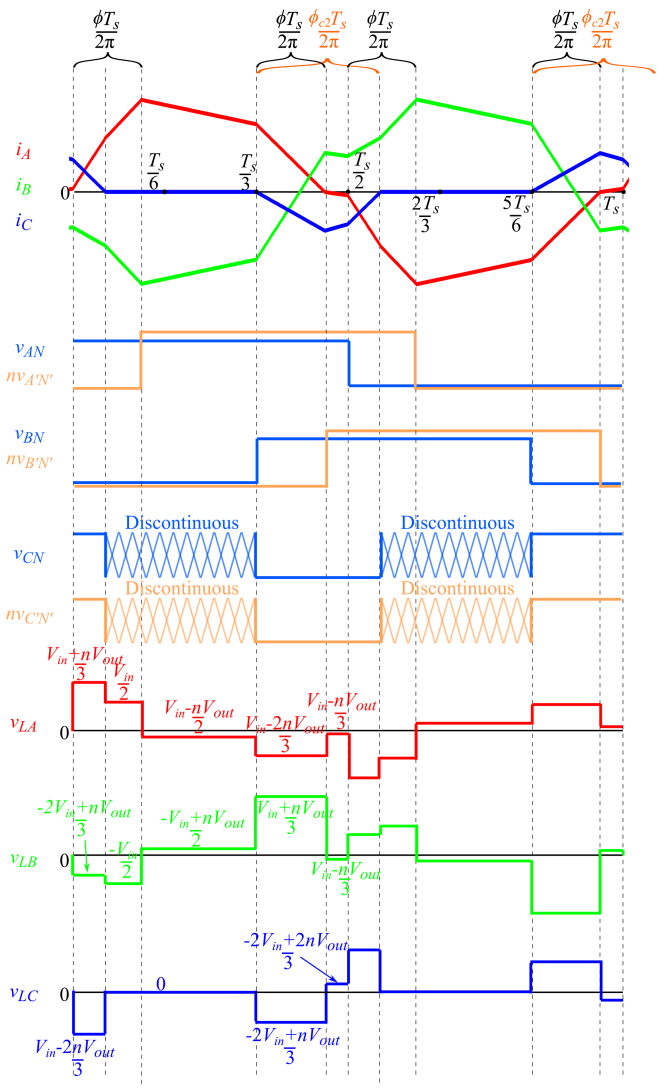


Fig. 5. Case II: phase currents and voltages, and leakage inductor voltages for boost mode of the 3p-DAB under frozen leg operation.

are determined using (1) for CCM and (3) for DCM, and Fig. 6 shows the calculated values. The current equations for phases A, B, and C in each segment are given in Appendix A, Table IV. The defined values ϕ_{dc1} and ϕ_{dc2} are calculated as follows:

$$\phi_{\text{dc1}} = \frac{nV_{\text{out}}\phi + (3V_{\text{in}} - 4nV_{\text{out}})\frac{\pi}{3}}{V_{\text{in}} - 2nV_{\text{out}}} \tag{8}$$

$$\phi_{\text{dc2}} = \frac{-nV_{\text{out}}\phi + (-V_{in} + 2nV_{\text{out}})\frac{\pi}{3}}{-V_{\text{in}} + nV_{\text{out}}}. \tag{9}$$

E. Case IV: Single Segment of Discontinuous Current Mode for $\pi/3 < \phi \le \pi/2$

As ϕ further increases within the (π/3, π/2] range, the duration of the DCM continues to decrease. Consequently, as one of the DCM segments observed in case III vanishes, only a single DCM segment remains in case IV, denoted as ϕ_{dc3}.

In this scenario, the half-cycle can be divided into six segments due to the single DCM segment. The corresponding leakage inductor voltages are also determined using (1) for CCM

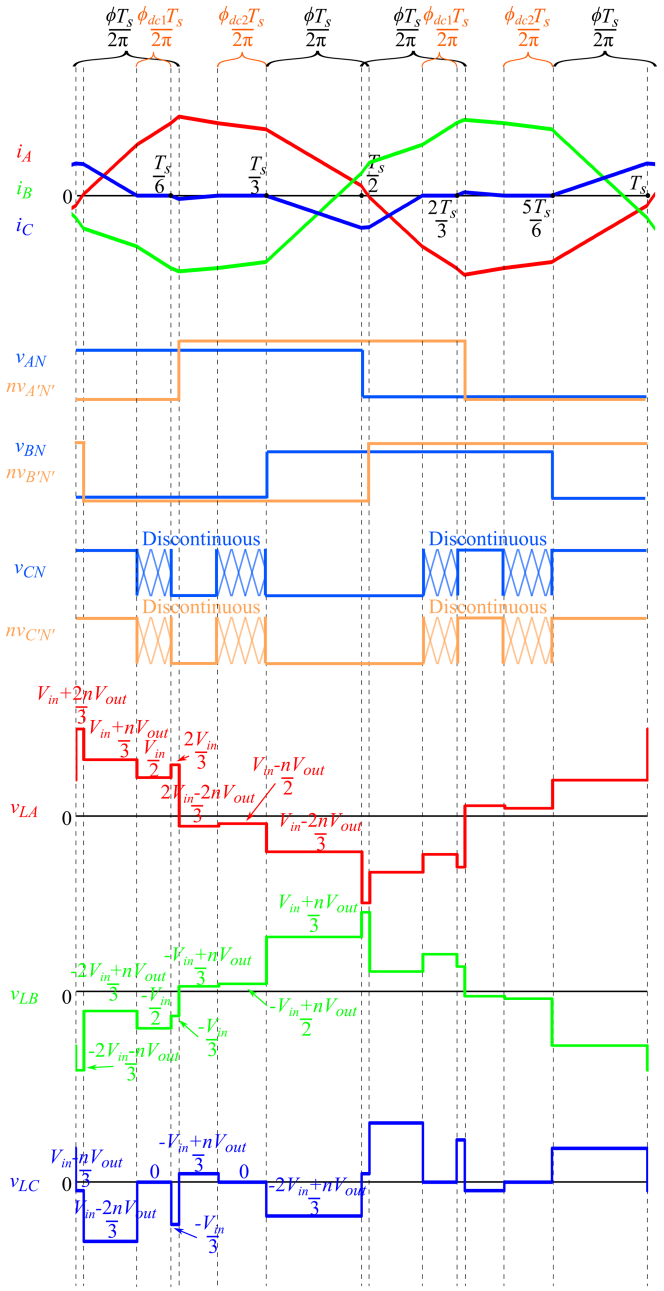


Fig. 6. Case III: phase currents and voltages, and leakage inductor voltages for boost mode of the 3p-DAB under frozen leg operation.

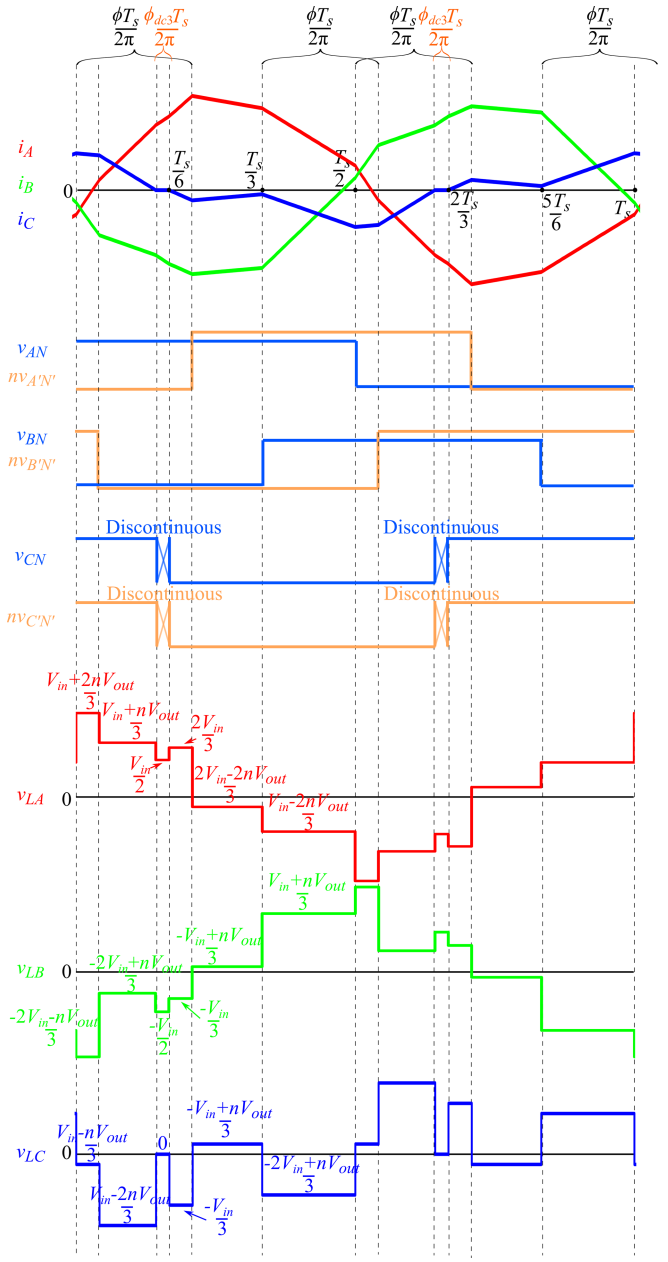


Fig. 7. Case IV: phase currents and voltages, and leakage inductor voltages for boost mode of the 3p-DAB under frozen leg operation.

and (3) for DCM, with the values illustrated in Fig. 7. The current equations for each phase in each segment are given in Appendix A, Table V. The defined value ϕ_{dc3} is calculated as follows:

$$\phi_{\mathrm{dc3}} = \frac{2nV_{\mathrm{out}}\phi + (4V_{\mathrm{in}} - 6nV_{\mathrm{out}})\frac{\pi}{3}}{V_{\mathrm{in}} - 2nV_{\mathrm{out}}}. \tag{10}$$

The boundary between Case III and case IV is reached when ϕ_{dc2} equals 0, as expressed in

$$\mathrm{boundary}_{34} = \left(2 - \frac{V_{\mathrm{in}}}{nV_{\mathrm{out}}}\right)\frac{\pi}{3}. \tag{11}$$

F. Case V: Continuous Current Mode for $\pi/3 < \phi \leq \pi/2$

As ϕ further increases within the (π/3, π/2] range, the ϕ_{dc3} in case IV decreases to zero, indicating that the faulty phase current becomes continuous. Nevertheless, due to the uncontrolled conduction of the diode, the actual phase shift angle of phase *C* still deviates from the nominal angle ϕ and is redefined as a new value, ϕ'. This deviation causes notable changes in the phase *A* and *B* waveforms compared to normal operation, resulting in imbalances in the three-phase currents and voltages, as shown in Fig. 8.

The half-cycle can be divided into six segments. The leakage inductor voltages are given by (1), with the calculated values shown in Fig. 8.

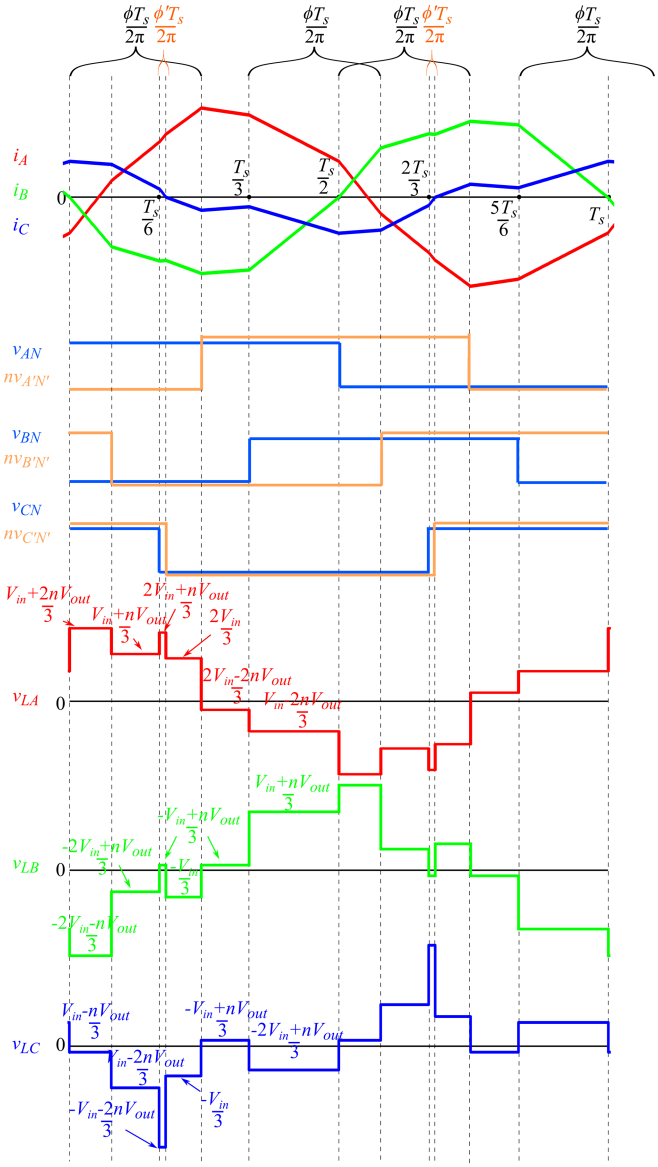


Fig. 8. Case V: phase currents and voltages, and leakage inductor voltages for boost mode of the 3p-DAB under frozen leg operation.

The current expressions for each phase are given in Appendix A, Table VI. The defined value ϕ' is calculated as follows:

$$\phi' = \frac{nV_{\text{out}}\phi + (2V_{\text{in}} - 3nV_{\text{out}})\frac{\pi}{3}}{V_{\text{in}} + nV_{\text{out}}}. \tag{12}$$

The transition from case IV to case V occurs when ϕ_{dc3} equals 0, as defined by the following boundary equation:

$$\text{boundary}_{45} = \left(3 - \frac{2V_{\text{in}}}{nV_{\text{out}}}\right)\frac{\pi}{3}. \tag{13}$$

Using the boundary (7), (11), and (13), the case distribution diagram for the boost mode can be derived, as shown in Fig. 9. It can be observed that as the boost ratio $nV_{\text{out}}/V_{\text{in}}$ increases, case V progressively diminishes and eventually disappears when the ratio reaches 1⅓. Thus, past this ratio, no CCM operation will occur in the faulty phase.

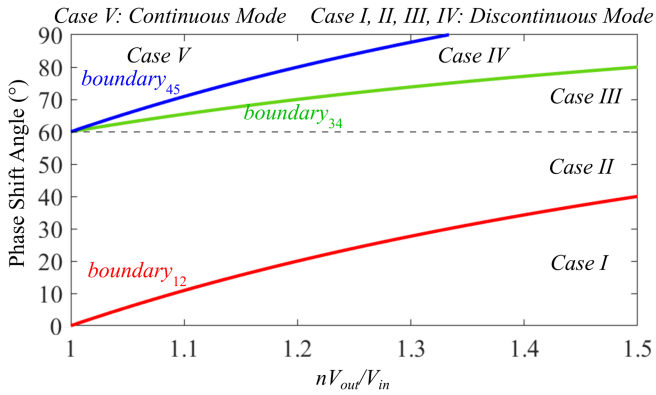


Fig. 9. Derived case distribution diagram for boost mode.

The analysis in this article primarily examines boost mode operation with ratios not exceeding 2, as such moderate values represent the most prevalent operating conditions in practical applications. However, for comprehensive understanding, system behavior under boost ratio exceeding 2 has also been investigated. Under these elevated boost conditions, the case distribution simplifies to just two operational modes: case I (0 to $\pi/3$) and case III ($\pi/3$ to $\pi/2$).

For case I with boost ratio above 2, the defined angle ϕ_{c1} decreases below the phase shift angle ϕ, resulting in fully discontinuous current in the faulty phase. In Case III at these higher boost ratios, the defined ϕ_{dc1} extends across the majority of the cycle while ϕ_{dc2} remains below $\pi/3$. This produces a current waveform where only a minimal portion remains continuous, with the faulty phase current becoming predominantly discontinuous throughout most of the cycle.

It should be noted that the present analysis specifically addresses frozen leg operation with secondary-side OCFs. The case of primary-side OCFs requires the development of a fundamentally different analytical framework due to its distinct operational characteristics, representing an important direction for future research.

IV. Analysis of Power Transfer in Boost Mode of 3p-DAB Under Frozen Leg Operation

A. Power Transfer Analysis for the Five Cases

To simplify the analysis, ideal and lossless conditions are assumed, such that the input and output power are equal to the transformer power [44], [45], [48]. This transferred power can be calculated based on the phase currents and voltages of the transformer, as given by

$$\begin{aligned} P &= P_A + P_B + P_C \\ &= \frac{1}{\pi}\int v_{AO} i_A d\theta + \frac{1}{\pi}\int v_{BO} i_B d\theta + \frac{1}{\pi}\int v_{CO} i_C d\theta. \end{aligned} \tag{14}$$

For case 1, the transformer waveforms can be split into six distinct segments. Within each segment, the primary-side transformer phase voltage can be determined [44], [45], as illustrated by Fig. 10. The corresponding current equations are given in Appendix A, Table II.

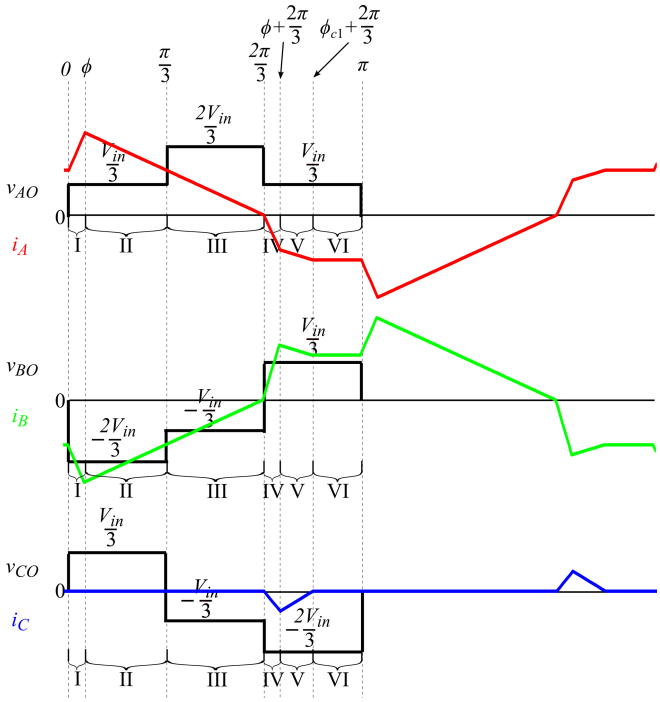


Fig. 10. Phase voltages and currents waveforms used for power transfer calculation in case I.

For Case I, the transferred power of phase X is determined by adding the average powers of each interval, given by

$$\overline{P_{XI}} = \overline{P_{XI-I}} + \overline{P_{XI-II}} + \overline{P_{XI-III}} + \overline{P_{XI-IV}} + \overline{P_{XI-V}} + \overline{P_{XI-VI}} \quad (15)$$

where the average power is the average voltage multiplied by the average current over the interval, divided by the half-cycle (π). For instance, the phase A power in the first interval in case I is found by

$$\overline{P_{AI-I}} = \left(\frac{I_{AI-0} + I_{AI-1}}{2} \frac{V_{in}}{3} \phi \right) / \pi \quad (16)$$

where $I_{AI\text{-}0}$ and $I_{AI\text{-}1}$ are specified in Table II. Using this approach, the power transfer in each interval for phases A, B, and C of Case I can be computed, and the total three-phase transferred power is calculated as

$$\begin{aligned}\overline{P_I} &= \overline{P_{AI}} + \overline{P_{BI}} + \overline{P_{CI}} \\ &= \frac{V_{in}}{6\pi}\left[-11N\phi^2 + 38N\frac{\pi}{3}\phi + (4M-4N)\frac{\pi}{3}\phi_{c1} \right. \\ &\quad \left. +(-4M+4N)\phi_{c1}^2 + (8M-4N)\phi\phi_{c1}\right] \end{aligned} \quad (17)$$

where the average transferred power for all phases in Case I can be found using (15). Similarly, the waveforms for power transfer in cases II to V are shown in Appendix B, Figs. 30–33, and the corresponding total power transfer is given by

$$\begin{aligned}\overline{P_{II}} &= \overline{P_{AII}} + \overline{P_{BII}} + \overline{P_{CII}} \\ &= \frac{V_{in}}{6\pi}\left[-15N\phi^2 + 44N\frac{\pi}{3}\phi + (4M-4N)\frac{\pi}{3}\phi_{c2} \right. \\ &\quad \left. +(-M+2N)\phi_{c2}^2 + (5M-6N)\frac{\pi^2}{9} + 2N\phi\phi_{c2}\right] \end{aligned} \quad (18)$$

$$\begin{aligned}\overline{P_{III}} &= \overline{P_{AIII}} + \overline{P_{BIII}} + \overline{P_{CIII}} \\ &= \frac{V_{\text{in}}}{6\pi}\left[-20N\phi^2 + (8M+56N)\frac{\pi}{3}\phi + (2M-8N)\frac{\pi}{3}\phi_{\text{dc1}} \right. \\ &\quad + 2N\frac{\pi}{3}\phi_{\text{dc2}} + (4M-12N)\frac{\pi^2}{9} + (-2M+2N)\phi\phi_{\text{dc1}} \\ &\quad \left. +(-2M)\phi\phi_{\text{dc2}} + (-M+2N)\phi_{\text{dc1}}^2 + (-M+N)\phi_{\text{dc2}}^2\right] \end{aligned} \quad (19)$$

$$\begin{aligned}\overline{P_{IV}} &= \overline{P_{AIV}} + \overline{P_{BIV}} + \overline{P_{CIV}} \\ &= \frac{V_{\text{in}}}{6\pi}\left[-20N\phi^2 + (8M+68N)\frac{\pi}{3}\phi + (-4N)\frac{\pi}{3}\phi_{\text{dc3}} \right. \\ &\quad + (16M-36N)\frac{\pi^2}{9} + (-2M)\phi\phi_{\text{dc3}} \\ &\quad \left. +(-M+2N)\phi_{\text{dc3}}^2\right] \end{aligned} \quad (20)$$

$$\begin{aligned}\overline{P_V} &= \overline{P_{AV}} + \overline{P_{BV}} + \overline{P_{CV}} \\ &= \frac{V_{\text{in}}}{6\pi}\left[-24N\phi^2 + 88N\frac{\pi}{3}\phi + (-24M+20N)\frac{\pi}{3}\phi' \right. \\ &\quad \left. +(4M-2N)\phi'^2 + (32M-60N)\frac{\pi^2}{9} - 4N\phi\phi'\right]. \end{aligned} \quad (21)$$

Based on these power transfer equations for cases I to V, Fig. 11 shows the transferred power for both normal and frozen leg operation for various voltage rise conditions. For unity gain (voltage rise = 0), the frozen leg operation consists of two cases: Cases II and V, as shown in Fig. 11(a), corresponding to the boundary conditions in Fig. 9. As the voltage rise increases from 0 to ⅓V_{in}, the ranges of cases II and V gradually decrease, while cases I, III, and IV emerge and expand, as illustrated by Fig. 11(b)–(e). When the voltage rise reaches or surpasses ⅓V_{in}, case V disappears because the converter is unable to sustain CCM due to the excessive voltage potential difference (though ϕ is at its maximum), as analyzed in Section III. The experimental test results validate these power transfer characteristics in Section VII.

B. Derivation of Maximum Power Transfer Expressions

Furthermore, since fault-tolerant methods aim to preserve operation close to the pre-fault condition, identifying the maximum transferable power is also essential. Fig. 11 shows that when the voltage rise is $<$ ⅓V_{in}, the maximum transferred power occurs in case V when $\phi = \pi/2$ [given by (22)]. When the voltage rise $>$ ⅓V_{in}, the maximum transferred power is observed in Case IV, also when $\phi = \pi/2$ [given by (23)]

$$P_{\text{MAX}} = \frac{T_s V_{\text{in}}^2}{36L}\left[\frac{nV_{\text{out}}}{V_{\text{in}}} + \frac{16}{9} + \frac{\left(-\frac{2}{3} + \frac{7nV_{\text{out}}}{18V_{\text{in}}}\right)\left(4 - \frac{3V_{\text{out}}}{V_{\text{in}}}\right)}{1 + \frac{nV_{\text{out}}}{V_{\text{in}}}}\right.$$

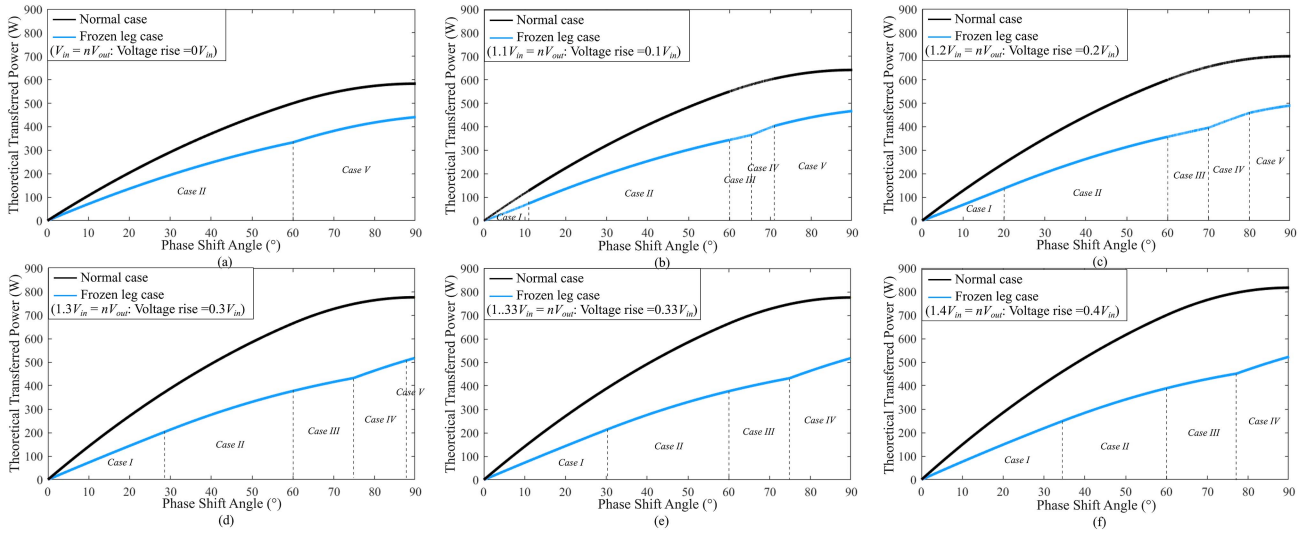


Fig. 11. Theoretical transferred power for frozen leg and normal operations under voltage rises of (a) $0V_{\text{in}}$, (b) $0.1V_{\text{in}}$, (c) $0.2V_{\text{in}}$, (d) $0.3V_{\text{in}}$, (e) $0.33V_{\text{in}}$, and (f) $0.4V_{\text{in}}$.

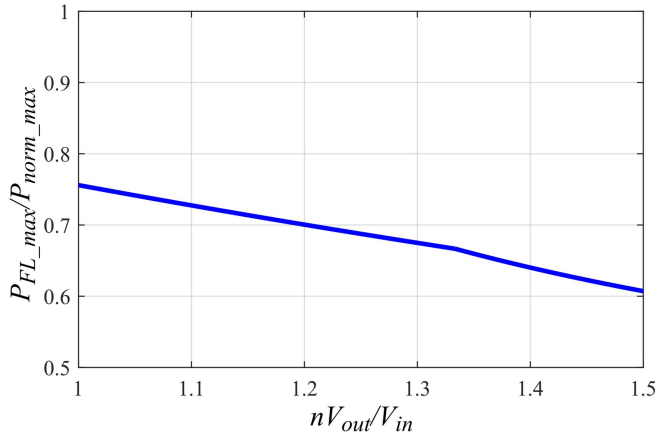


Fig. 12. Ratio of maximum transferred power in frozen leg operation to normal operation with voltage rises ranging from 0 to $0.5V_{\text{in}}$.

$$+\frac{\left(\frac{1}{18}-\frac{nV_{\text{out}}}{36V_{\text{in}}}\right)\left(4-\frac{3V_{\text{out}}}{V_{\text{in}}}\right)^2}{\left(1+\frac{nV_{\text{out}}}{V_{\text{in}}}\right)^2}\Bigg] \quad (V_{\text{in}} \le nV_{\text{out}} \le 1.33V_{\text{in}}) \tag{22}$$

$$P_{\text{MAX}} = \frac{T_s V_{\text{in}}^2}{36L}\left[\frac{7nV_{\text{out}}}{6V_{\text{in}}}+\frac{14}{9}-\frac{\frac{1}{72}\left(8-\frac{6nV_{\text{out}}}{V_{\text{in}}}\right)^2}{1-\frac{2nV_{\text{out}}}{V_{\text{in}}}}\right.$$
$$\left.-\frac{\left(\frac{1}{12}+\frac{nV_{\text{out}}}{9V_{\text{in}}}\right)\left(8-\frac{6nV_{\text{out}}}{V_{in}}\right)}{1-\frac{2nV_{\text{out}}}{V_{\text{in}}}}\right] \quad (nV_{\text{out}} \ge 1.33V_{\text{in}})\,. \tag{23}$$

Fig. 12 shows the ratio of maximum transferred power for frozen leg operation and normal non-fault operation. Initially, at zero voltage rise, the ratio is 75.6% and gradually declines to around 60% when the voltage rise reaches $0.5V_{\text{in}}$. This trend indicates that as the voltage rise increases, the frozen leg operation maximum transferred power decreases further from non-fault operation. Section VII validates this distinctive result through experimental testing.

Besides the maximum power transfer limitation, a critical design consideration is whether frozen leg operation could exceed the switches' safe operating area when operating at maximum capacity. The worst-case scenario, characterized by the highest current stress, occurs at unity voltage gain with the peak ratio shown in Fig. 12 (75.6% of normal power). Utilizing the derived segmental current expressions from Table VI, the maximum RMS current in the worst-case scenario can be analytically determined, as presented in Appendix A, (A.1). A comparison with normal operation [52] reveals that the current stress of all switches at maximum power under frozen leg operation remains below the designed rated current stress.

V. Analysis of Soft-Switching in Boost Mode of 3p-DAB Under Frozen Leg Operation

Soft-switching techniques are commonly employed to mitigate switching stress on power semiconductor devices. The fundamental requirement for ZVS is that the voltage across the switch decreases to zero before it turns ON. This ensures the current commutates through the anti-parallel body diode before the switch begins to conduct.

Although some comprehensive ZVS analyses account for both current direction and dead time duration [53] (because excessively long dead time may cause the current to reverse polarity before switching, potentially invalidating the ZVS condition), this research excludes dead time modeling to reduce complexity. This is a common approach within the context of fault-tolerant control strategies for 3p-DAB converters [24], [34], [47], and relies on the assumption that the dead time is properly selected and so its impact on ZVS is negligible. Consequently, this article and these prior studies assess ZVS exclusively based on the current direction at the turn-ON instant.

This section provides a detailed analysis of the soft-switching behavior in the five identified boost-mode cases, which have not been explored in prior studies. ZVS conditions must be examined for each leg due to the asymmetry of the fault. Additionally, since the secondary-side switches of leg *C'* are assumed to be open-circuited, ZVS is not applicable in leg *C'*.

For case I, switches should satisfy (24) to ensure ZVS, where (24) is derived from Fig. 4. For the switches in primary-side leg *C*, the current is zero at turn-ON, indicating that zero current switching (ZCS) is achieved

$$\begin{cases} \text{Primary-side Leg } A\text{: } I_{AI-0} < 0 \\ \text{Primary-side Leg } B\text{: } I_{BI-2} < 0 \\ \text{Secondary-side Leg } A'\text{: } I_{AI-1} > 0 \\ \text{Secondary-side Leg } B'\text{: } I_{BI-3} > 0 \end{cases}. \tag{24}$$

Similarly, for cases II to V, the ZVS conditions are described by (25)–(28), derived from the waveforms shown in Figs. 5–8. In cases II, III, and IV, the switches in primary-side leg *C* achieve ZCS at turn-ON. However, in case V, since leg *C* operates in CCM, its ZVS condition is specifically given in (28)

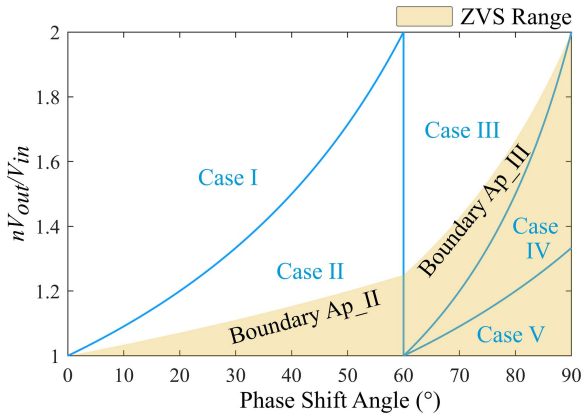
$$\begin{cases} \text{Primary-side Leg } A\text{: } I_{AII-0} < 0 \\ \text{Primary-side Leg } B\text{: } I_{BII-3} < 0 \\ \text{Secondary-side Leg } A'\text{: } I_{AII-2} > 0 \\ \text{Secondary-side Leg } B'\text{: } I_{BII-4} > 0 \end{cases} \tag{25}$$

$$\begin{cases} \text{Primary-side Leg } A\text{: } I_{AIII-0} < 0 \\ \text{Primary-side Leg } B\text{: } I_{BIII-6} < 0 \\ \text{Secondary-side Leg } A'\text{: } I_{AIII-4} > 0 \\ \text{Secondary-side Leg } B'\text{: } -I_{BIII-1} > 0 \end{cases} \tag{26}$$

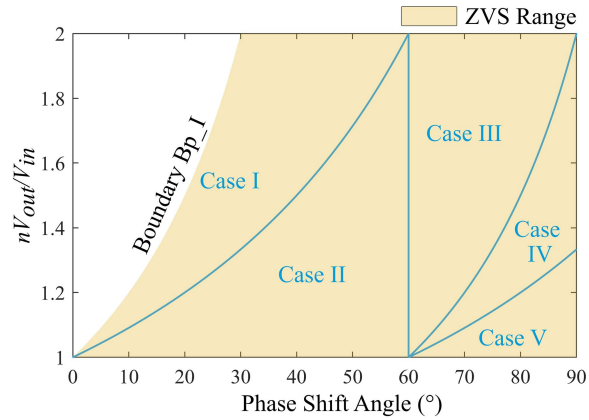
$$\begin{cases} \text{Primary-side Leg } A\text{: } I_{AIV-0} < 0 \\ \text{Primary-side Leg } B\text{: } I_{BIV-4} < 0 \\ \text{Secondary-side Leg } A'\text{: } I_{AIV-5} > 0 \\ \text{Secondary-side Leg } B'\text{: } -I_{BIV-1} > 0 \end{cases} \tag{27}$$

$$\begin{cases} \text{Primary-side Leg } A\text{: } I_{AV-0} < 0 \\ \text{Primary-side Leg } B\text{: } I_{BV-5} < 0 \\ \text{Primary-side Leg } C\text{: } -I_{CV-2} < 0 \\ \text{Secondary-side Leg } A'\text{: } I_{AV-4} > 0 \\ \text{Secondary-side Leg } B'\text{: } -I_{BV-1} > 0 \end{cases}. \tag{28}$$

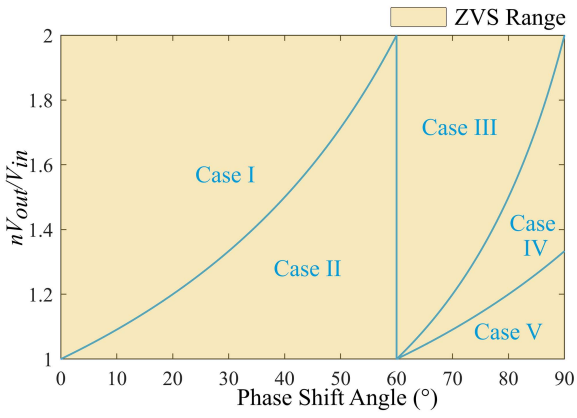
Fig. 13 shows the corresponding ZVS operational regions determined by solving these conditions. These results indicate the secondary-side healthy switches always maintain ZVS across the full range of phase shift angles and voltage rise, as shown in Fig. 13(c). Meanwhile, the primary-side leg *C* switches operate either in ZCS or ZVS across all cases. However, for the leg *A* and *B* switches, ZVS is not always achievable and their ZVS range varies, as shown in Fig. 13(a) and (b). The ZVS boundaries for



(a)



(b)



(c)

Fig. 13. ZVS operational regions for (a) leg *A*, (b) leg *B*, and (c) legs *A'* and *B'*.

legs *A* and *B* are defined as

$$\begin{cases} \text{Boundary Ap\_II} = \frac{5\pi}{5\pi-3\phi} & \phi \in [0, \frac{\pi}{3}) \\ \text{Boundary Ap\_III} = \frac{5\pi}{7\pi-9\phi} & \phi \in [\frac{\pi}{3}, \frac{\pi}{2}] \\ \text{Boundary Bp\_I} = \frac{\pi}{\pi-3\phi} & \phi \in [0, \frac{\pi}{3}) \end{cases}. \tag{29}$$

The derived ZVS operational regions are further validated through experimental results presented in Section VII. A

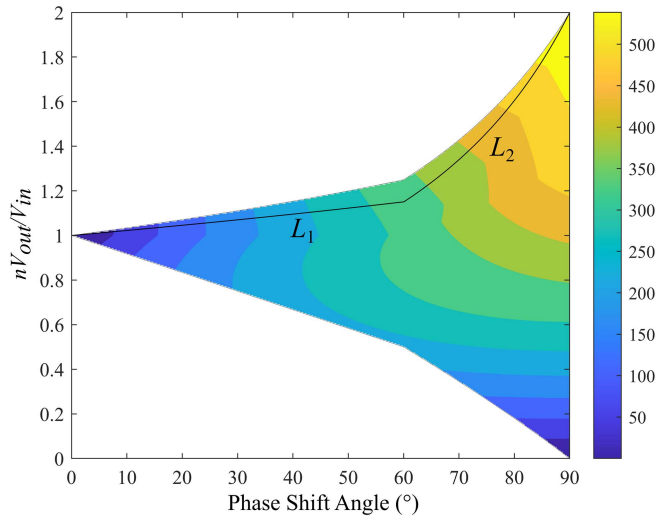


Fig. 14. ZVS region and the power map in accordance with phase shift angle and $nV_{\text{out}}/V_{\text{in}}$.

comprehensive understanding of these identified ZVS boundaries, as shown in Fig. 13, is essential for optimizing thermal management and control strategies, as switching losses significantly increase in non-ZVS regions.

VI. Proposed ZVS-Guaranteed Control Strategy for Frozen Leg Operation

In many 3p-DAB converter applications, the primary-side dc voltage V_{in} is typically determined by the power source, such as the traction battery in APM applications or the MPPT-regulated output in PV systems [15], [16], [19]. Meanwhile, the output power and phase shift angle are generally governed by the load on the secondary side. Therefore, in practical applications, the output voltage is typically the only controllable variable [51]—for example, the voltage of the 12 V battery in an EV can be adjusted within a certain safe range on the output side of the APM.

However, based on the ZVS analysis for both the buck mode in [44] and the boost mode presented in this article, certain operating points under frozen leg operation prevent some switches from achieving ZVS. To ensure ZVS for all switches at all times, better adhere to switch thermal limitations and increase converter efficiency, this article proposes a ZVS-guaranteed control strategy. The strategy can regulate the output voltage reference in a predetermined manner to ensure that the converter consistently operates within the ZVS region while operating in frozen leg mode after an OCF.

A. Description of the Proposed Strategy

The ZVS operation region for all switches is derived from the analytical ZVS conditions in [44] for buck mode and in this article for boost mode, as shown in Fig. 14. Since both buck and boost modes involve five legs, each with its own ZVS region, the objective is to determine a common region where all five legs can simultaneously achieve ZVS. In boost mode, leg A is the most challenging leg for achieving ZVS. If ZVS is achieved in leg A, the remaining legs will also operate under ZVS conditions. Similarly, in buck mode, leg A' is the most difficult to achieve ZVS. Ensuring ZVS in leg A' implies that the other legs are also within the ZVS region. Therefore, the combined ZVS region defined by leg A in boost mode and leg A' in buck mode, as shown in Fig. 14, serves as the required safe ZVS region. Within this region, ZVS is achievable across all switches. The control objective is to ensure that all operating points lie within this safe ZVS region.

Given a measured V_{in}, the power expressions for boost mode [(17)–(21) in this article] and for buck mode ((24), (26), and (28) in [44]) can be used to calculate the achievable power within the ZVS region, generating a power map as shown in Fig. 14. It should be noted that the frozen leg operation cannot transfer the maximum power achievable under normal operation. The $P_{\max}$ occurs at a phase shift angle of $\pi/2$ with $nV_{\text{out}}/V_{\text{in}}$ equaling 2, while zero power is obtained at a phase shift angle of 0 under unity voltage gain. This map confirms that any output power from 0 to $P_{\max}$ can be realized while maintaining ZVS via proper operating point selection.

For practical implementations, the desired output power $P*$ is typically known—for instance, via the vehicle supervisory controller in EVs [54]—and V_{in} is sampled. With these inputs, the corresponding combinations of V_{out} and phase shift angle ϕ within the ZVS region that achieve $P*$ can be determined. However, because multiple valid solutions may exist, an optimal operating point must be selected. To streamline this selection process, two characteristic curves, L_1 and L_2, are proposed within the power map, as shown in Fig. 14

$$\begin{cases} L_1: \frac{nV_{\text{out}}}{V_{\text{in}}} = \frac{8}{8-\phi}, & \phi \in [0, \frac{\pi}{3}) \\ L_2: \frac{nV_{\text{out}}}{V_{\text{in}}} = \frac{23\pi}{37\pi-51\phi}, & \phi \in [\frac{\pi}{3}, \frac{\pi}{2}] \end{cases}. \tag{30}$$

These curves satisfy the following criteria.

1) They cover the full power range from 0 to $P_{\max}$.
2) For a given output power, they minimize the required phase shift angle ϕ to reduce power circulation losses [55].
3) They maintain a safety margin from the ZVS boundary to avoid operation near critical ZVS limits.

With these curves substituted in (17)–(21), one specific V_{out} and ϕ_0 can be calculated to achieve the target $P*$. The implementation process is shown in the control flowchart in Fig. 15. Notably, the calculated ϕ_0 is used as a feedforward signal ϕ_{ff} to the PI controller in the closed-loop system. This is because the power map and characteristic curves are derived from a lossless model, and real-world converter losses require a slightly larger ϕ to deliver the desired power. Thus, the feedforward term helps improve the system's dynamic response. Moreover, V_{out} typically has a limited allowable range—for example, 10–16 V in APM systems [3]. If the calculated $V_{\text{out}}*$ exceeds this range, the control will instead target the maximum allowable voltage, as shown in Fig. 15. In this case, the feedforward phase shift ϕ_{ff} is still set to the calculated value ϕ_0 and the actual phase shift ϕ will automatically adjust to maintain the required power, potentially operating to the right of curves L_1 and L_2. In the worst-case scenario, the converter may be forced to operate exclusively

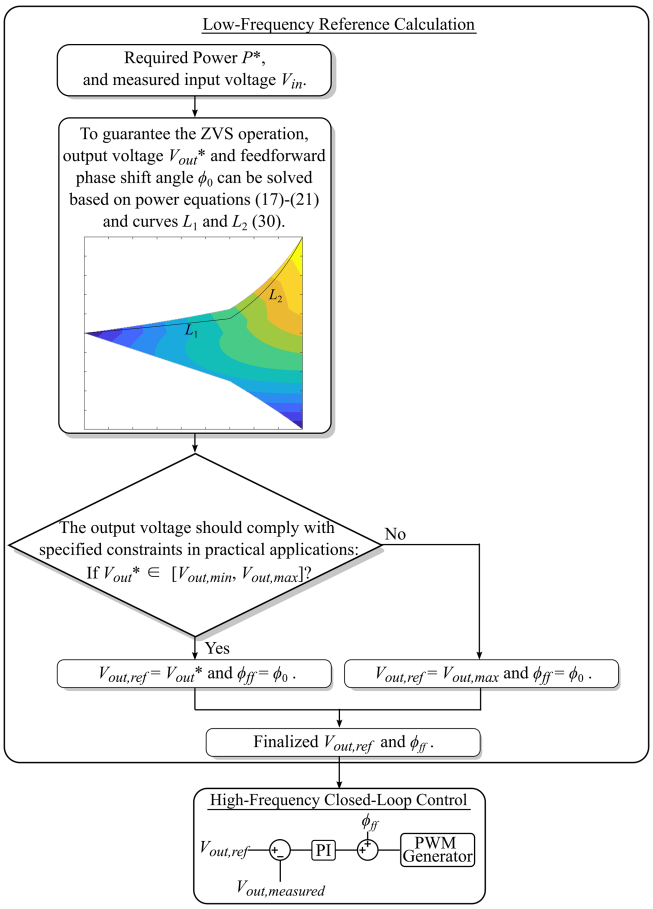


Fig. 15. Flowchart of the proposed ZVS-guaranteed control strategy.

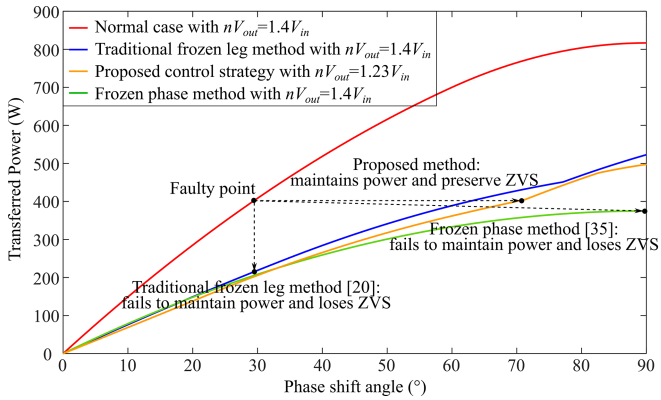
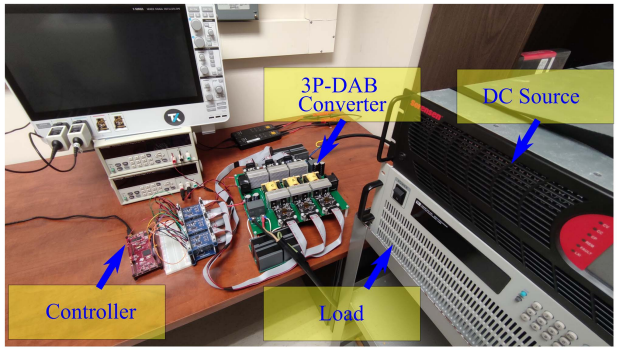
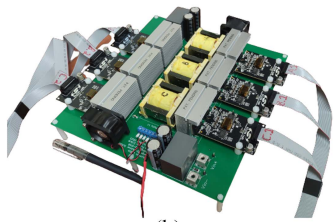


Fig. 16. Performance comparison of different OCF-tolerant strategies for 3p-DAB converter for an illustrative case of 400 W transferred power and $nV_{\rm out}/V_{\rm in}$ = 1.4 at the time the fault occurs.



(a)



(b)

Fig. 17. (a) Experimental platform and (b) the 3p-DAB converter prototype.

in buck mode due to output voltage constraints. Under this condition, the operating point may lie below the curves L_1 and L_2, making it impossible to solve for a valid combination of $V_{\rm out}$ and ϕ_0 from the characteristic equations. As a result, the controller defaults to using the maximum allowable output voltage, and the feedforward phase shift ϕ_{ff} is assigned a value of zero. Finally, the calculations of $V_{\rm out}$ and ϕ are performed at a low frequency, unlike the high-frequency nature of closed-loop control, which helps maintain the stability of the control system.

B. Comparison With Other OCF-Tolerant Methods for 3p-DAB

To demonstrate the improvement of the proposed method over conventional fault-tolerant approaches for OCFs in a 3p-DAB converter, a comparative analysis is shown in Fig. 16. For this illustrative case, the system is assumed to be operating at 400 W with a voltage ratio of $nV_{\rm out}/V_{\rm in} = 1.4$ when the OCF happens, as shown in Fig. 16.

Under the traditional frozen leg method [20], the system maintains the same phase shift angle as in the pre-fault condition, without accounting for power variations. As a result, the output power drops to approximately 200 W. Moreover, this method lacks ZVS analysis, leading to a loss of ZVS performance.

In the frozen phase method [35], although tracking pre-fault power is attempted during OCF, the control remains in open-loop form and lacks any ZVS consideration. Furthermore, its maximum transferable power is inherently limited compared to frozen leg operation, as previously discussed. Consequently, this method cannot maintain the prefault power level and also fails to achieve ZVS, as shown in Fig. 16.

In contrast, the proposed control strategy is designed to maintain the pre-fault output power and ensure ZVS operation. As shown in Fig. 16, through closed-loop control that adjusts the output voltage to $1.23V_{\rm in}$, assuming this is in the safe allowable range for the specific application, the proposed method successfully sustains the output power and retains ZVS characteristics.

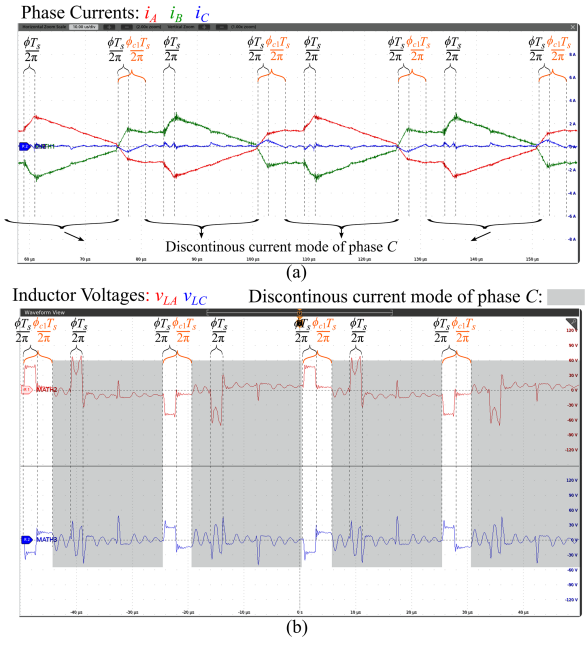


Fig. 18. Experimental results for 10° phase shift angle in case I. (a) Phase currents. (b) Leakage inductor voltages.

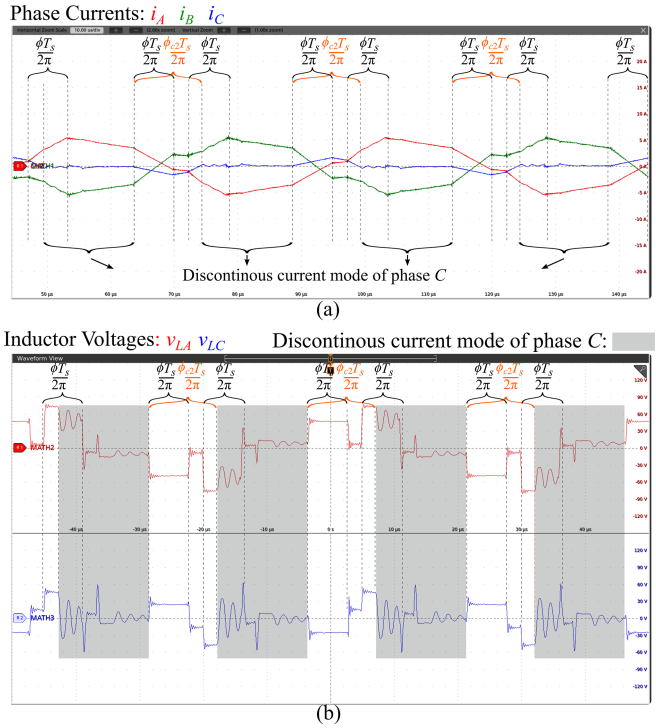


Fig. 19. Experimental results for 45° phase shift angle in case II. (a) Phase currents. (b) Leakage inductor voltages.

VII. Experimental Results

Fig. 17 shows the 3p-DAB converter prototype used to experimentally validate the theoretical analysis. Table I gives the main system parameters. The control implementation is based on a TI TMS320F28379 microcontroller, while Wolfspeed C3M0045065K silicon carbide MOSFETs are employed as the switching devices. The input is supplied by a Sorenson SGX 600-25 DC source, whereas the output is connected to an ITECH IT8906E electronic load.

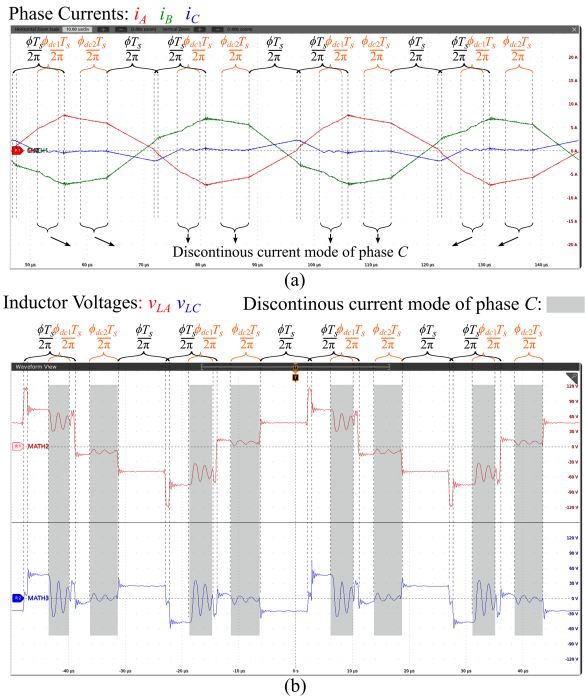


Fig. 20. Experimental results for 65° phase shift angle in case III. (a) Phase currents. (b) Leakage inductor voltages.

TABLE I
3P-DAB Converter Prototype Parameters

Description	Parameters
Primary-side DC voltage (V_{in})	100 V
Secondary-side DC voltage (V_{out})	100 V–160 V
Rated power (P_{rated})	1.125 kW
Transformer turns ratio (n:1)	1:1
Leakage inductance ($L_{A,B,C}$)	83.33 µH
Switching frequency (f_s)	20 kHz
Switch dead time (t_d)	0.2 µs
Input capacitance (C_{in})	275 µF
Output capacitance (C_{out})	275 µF
Switches	C3M0045065K
Gate drivers	Si823H

A. Verification of Theoretical Analysis on Leakage Inductor Voltages and Phase Currents

This subsection presents the experimental validation of the theoretical analysis for cases I to V. The experiments were conducted with an input voltage of 100 V and an output voltage of 120 V. To represent the five cases, phase shift angles of 10°, 45°, 65°, 75°, and 88° were selected. The corresponding experimental results for leakage inductor voltages and phase currents are illustrated in Figs. 18–22. Since the direct measurement of the leakage inductor voltages was not possible, the experimental waveforms were obtained by calculating the voltage difference between the primary and secondary transformer terminals using the oscilloscope's mathematical function.

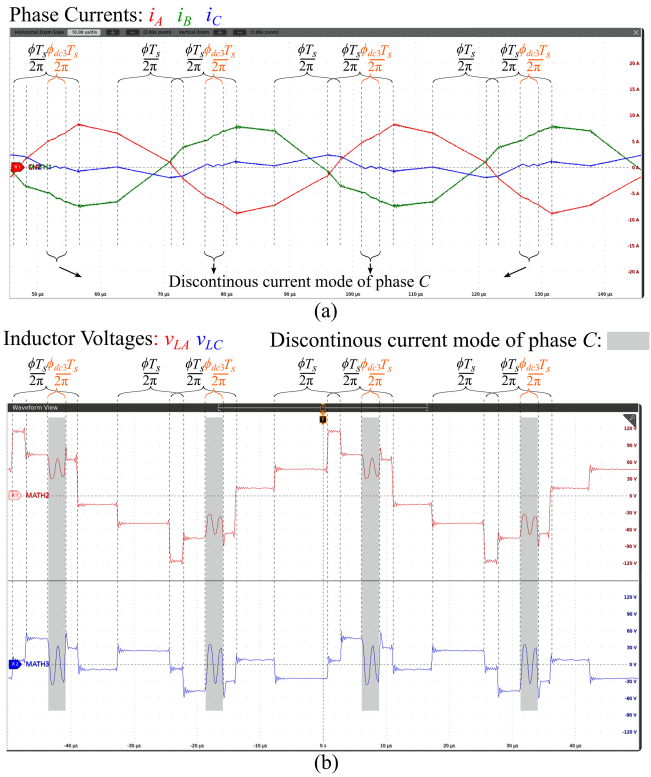


Fig. 21. Experimental results for 75° phase shift angle in case IV. (a) Phase currents. (b) Leakage inductor voltages.

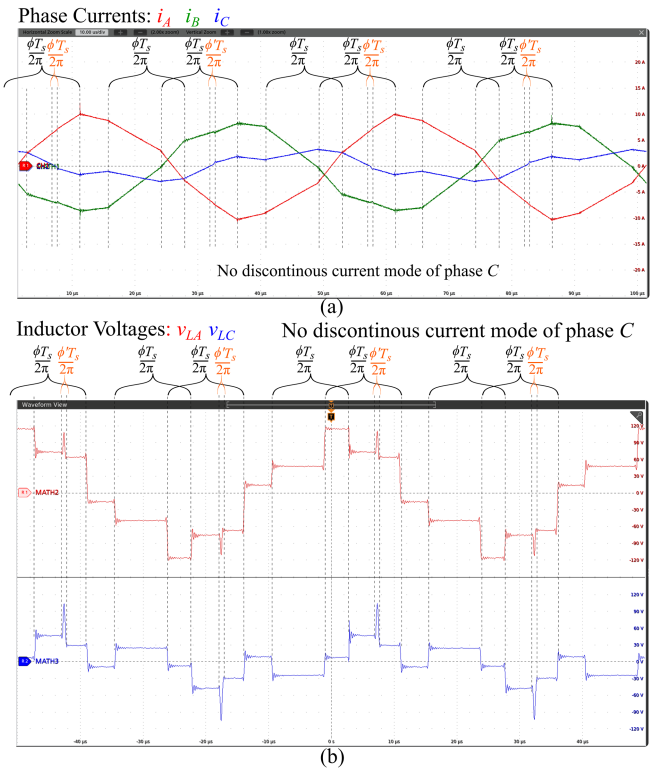


Fig. 22. Experimental results for 88° phase shift angle in Case V: (a) phase currents and (b) leakage inductor voltages.

For the selected phase shift angles of 10°, 45°, 65°, 75°, and 88°, the corresponding calculated values of $\phi_{c1}(10°)$, $\phi_{c2}(45°)$, $\phi_{\mathrm{dc1}}(65°)$, $\phi_{\mathrm{dc2}}(65°)$, $\phi_{\mathrm{dc3}}(75°)$, and $\phi'(88°)$ are 30°, 81.43°, 21.42°, 30°, 8.57° and 4.36°, respectively. These values are validated by the experimental results presented in Figs. 18–22. Additionally, the experimental waveforms in Figs. 18–22 exhibit strong agreement with the theoretical predictions in Figs. 4–8 when the phase C current remains continuous. However, in the conditions where phase C current enters the discontinuous conduction mode, slight fluctuations in the current waveform and resonant ringing in the leakage inductor voltage are observed. These phenomena arise due to resonance between the primary-side switch output capacitances and the transformer leakage inductance when the phase C current becomes discontinuous [56], a behavior that has also been observed in many prior studies [56], [57], [58], [59]. Conversely, when phase C operates in CCM, its switches maintain periodic conduction, clamping their node voltages to either the input voltage or ground. This clamping applies forced voltage excitation to the output capacitances of conducting switches, preventing them from resonating with the leakage inductances [60]. Consequently, no significant resonance appears in the leakage inductor voltages during CCM.

B. Verification of Derived Power Transfer Curves

To experimentally verify the theoretical transferred power expressions derived in (17)–(21) and the corresponding power transfer curves in Fig. 11, tests were conducted under both normal and frozen leg operations. The phase shift angle varied from 0° to 90° in 5° increments. The input voltage was maintained at 100 V, while the output voltage was adjusted between 110 V and −140 V. The measured power transfer results, shown in Fig. 23, indicate a strong agreement between the experimental data and the derived equations in both operational cases.

Fig. 23 shows that the measured values are slightly smaller than the theoretically calculated values, which is expected due to the intrinsic prototype losses, which are not considered in the idealized power transfer equation [1], [48]. These deviations primarily stem from conduction losses, switching losses, and dead time effects. This discrepancy becomes more pronounced at higher power levels, as switching and conduction losses increase. Despite these minor variations, the experimental results effectively corroborate the derived power transfer equations.

C. Verification of Derived Maximum Power Transfer

To verify the theoretical predictions regarding the ratio of maximum transferred power in frozen leg operation to normal operation under varying voltage rises, a series of experiments were conducted. The maximum transferred power was experimentally measured for voltage rises from 0 to $0.4V_{\mathrm{in}}$, and is compared with the theoretical values in Fig. 24. Fig. 24 shows that the predicted theoretical ratio is supported by the experimental results, though prototype losses lead to slightly lower measured ratios.

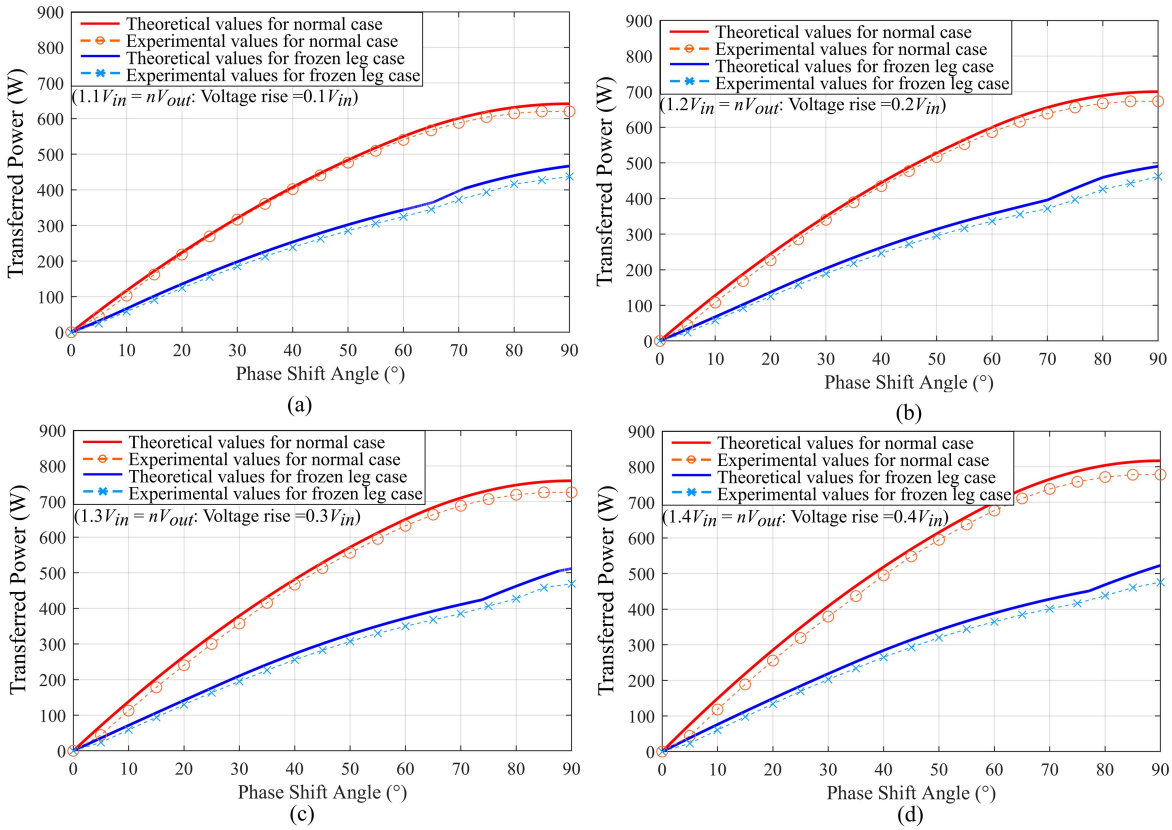


Fig. 23. Comparison of experimental transferred power results between frozen leg and normal operations under voltage rises of (a) $0.1V_{\rm in}$, (b) $0.2V_{\rm in}$, (c) $0.3V_{\rm in}$, and (d) $0.4V_{\rm in}$.

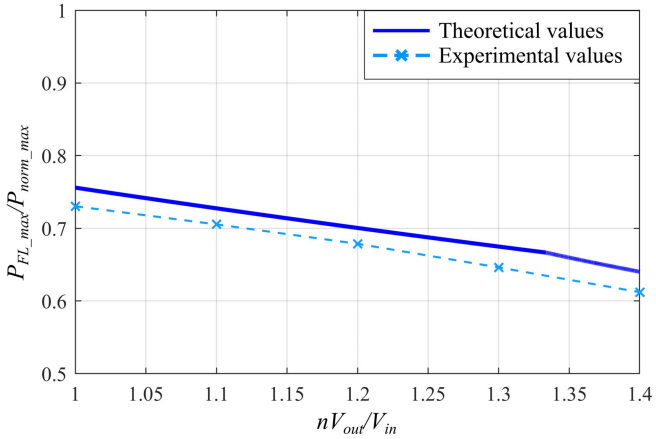


Fig. 24. Experimental ratios of maximum transferred power in frozen leg operation to normal operation with voltage rises ranging from 0 to $0.4V_{\rm in}$.

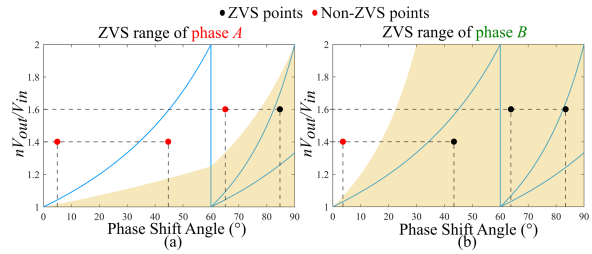


Fig. 25. ZVS test points for (a) the primary-side switches of phase *A* and (b) the primary-side switches of phase *B*.

D. Verification of Derived ZVS Operational Regions

Section V demonstrated that the healthy switches on the secondary side operate always under ZVS, yet the switches in legs *A* and *B* have a specific ZVS boundary area. To verify these derived ZVS operational areas, four test points are chosen, as shown in Fig. 25. These test points correspond to ϕ values of 5° and 45° with $nV_{\rm out} = 1.4V_{\rm in}$, and 65° and 85° with $nV_{\rm out} = 1.6V_{\rm in}$. According to the theoretical analysis in Fig. 13, these points should yield three non-ZVS cases and one ZVS case for phase *A*, and one non-ZVS case and three ZVS cases for phase *B*. Fig. 26 shows the drain-source voltages (V_{ds}) of the upper switches and the phase currents of legs *A* and *B* at these four test points—the currents in the upper switches are negative at the turn-ON instant for the points expected to be in ZVS in Fig. 25, which validates the theoretical predictions.

E. Verification of Proposed ZVS-Guaranteed Control Strategy

To verify the feasibility of the proposed control strategy, two experiments were conducted. In both experiments, the input voltage was fixed at 100 V, while the required power was set to 300 and 400 W, respectively. In each experiment, only the required power and the measured input voltage were provided to the controller, which then computed the corresponding output

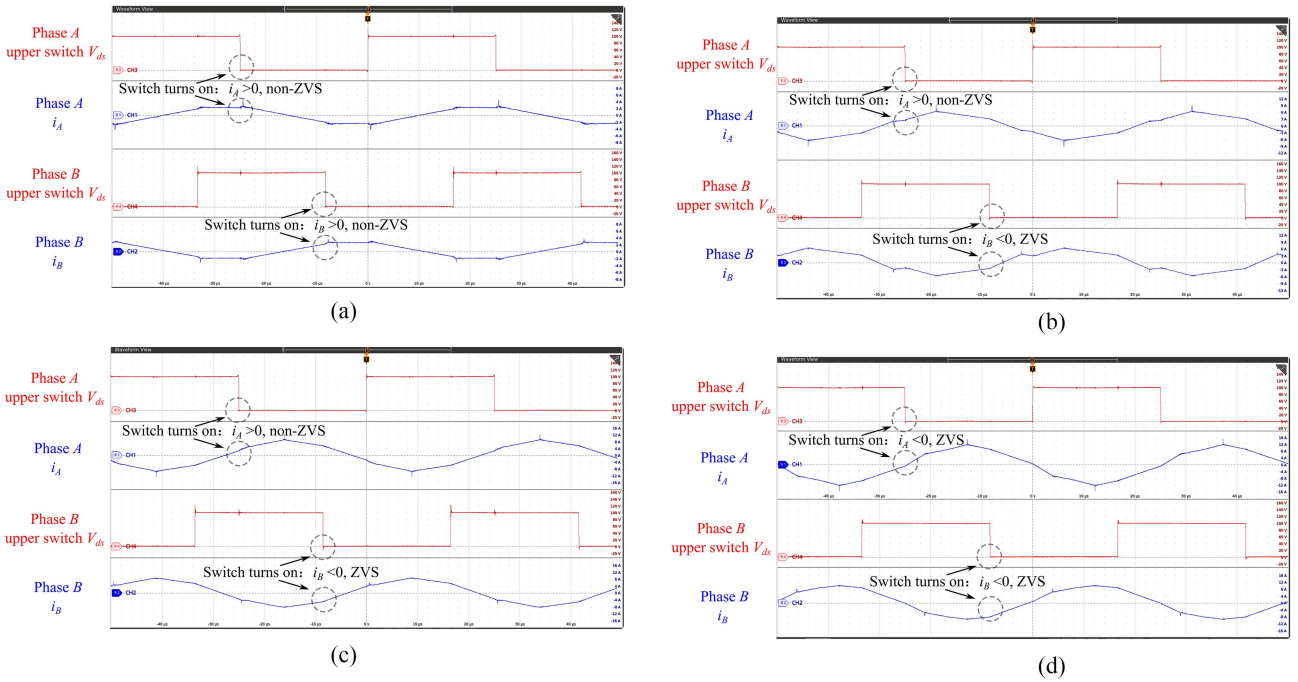


Fig. 26. Drain-source voltage of the upper switches and legs A and B phase currents at selected test points. (a) 5°. (b) 45° phase shift angles with $nV_{\text{out}} = 1.4V_{\text{in}}$. (c) 65°. (d) 85° phase shift angles with $nV_{\text{out}} = 1.6V_{\text{in}}$.

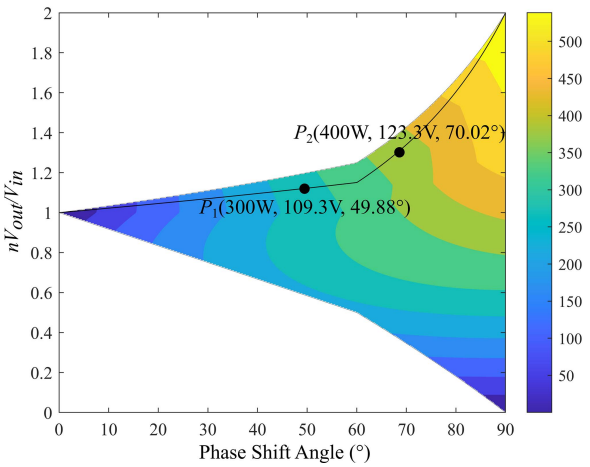


Fig. 27. Theoretical power points P_1 and P_2 corresponding to required output powers of 300 W and 400 W.

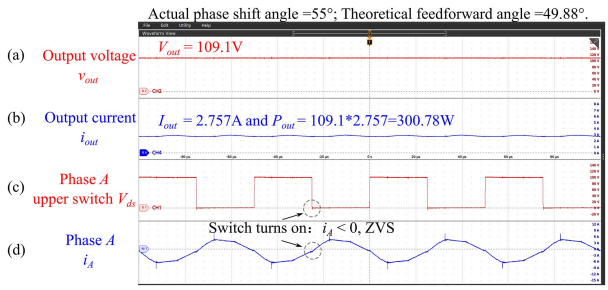


Fig. 28. Experimental results at P_1 with (a) output voltage, (b) output current, (c) upper switches V_{ds} of phase A, and (d) phase currents of phase A.

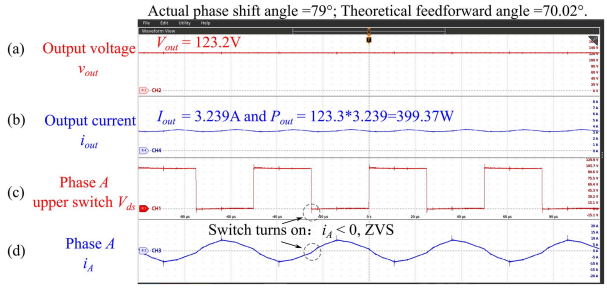


Fig. 29. Experimental results at P_2 with (a) output voltage, (b) output current, (c) upper switches V_{ds} of phase A, and (d) phase currents of phase A.

voltage reference $V_{\text{out,ref}}$ and feedforward phase shift angle ϕ_{ff} based on the control logic. The computed values were subsequently applied in the closed-loop control of the 3p-DAB converter operating under the frozen leg condition, as shown in Fig. 15. According to the theoretical power map and proposed curves in Fig. 27, the theoretical values for $V_{\text{out,ref}}$ and ϕ_{ff} are 109.3 V and 49.88° for the 300 W case, and 123.3 V and 70.02° for the 400 W case, corresponding to points P_1 and P_2 in Fig. 27.

The experimental results are illustrated in Figs. 28 and 29, showing the output voltage V_{out}, output current I_{out}, upper switch V_{ds} of phase A, and the phase current of phase A. The latter two are used to assess the ZVS condition of phase A. Phase A is monitored specifically because it is typically the most difficult phase in which to achieve ZVS. As previously discussed and verified in this article, if ZVS is achieved in phase A, it can be assumed that the other phases are also in ZVS. In Fig. 28, the output voltage is regulated to approximately 109.1 V, and

the output current is about 2.75 A, resulting in an output power of 300.78 W, which matches the required value. The phase *A* switches operate under ZVS conditions, as indicated by the fact that the phase current remains negative at the moment of turn-ON. In Fig. 29, the output voltage is regulated to approximately 123.2 V, and the output current is around 3.239 A, resulting in 399.37 W of output power, again matching the required value. ZVS is also achieved in this case, as evidenced by the negative phase current at the switch turn-ON instant.

The only deviation from theoretical predictions is that the experimental phase shift angles are slightly higher than the theoretical values—55° and 79° instead of 49.88° and 70.02°, respectively. This discrepancy is due to the fact that the power map and characteristic curves are derived from a lossless model, whereas real-world losses in the converter necessitate a slightly larger ϕ to deliver the same amount of power. However, the proposed use of the calculated phase shift as a feed-forward value into the PI closed-loop controller allows the system to adjust to the required phase shift while using the calculated value as a starting point. These results confirm that the proposed method performs as expected and effectively guarantees ZVS operation.

VIII. Conclusion and Future Work

This article, for the first time, tackles the pressing challenge of extending the frozen-leg operation analysis of the 3p-DAB converter to the boost mode. In boost mode, the faulty phase current becomes discontinuous due to the increased voltage potential difference. To address this, the article introduces a novel DCM analytical framework. By incorporating this framework, new voltage and current equations for frozen-leg operation of the 3p-DAB converter in boost mode are derived, and five distinct cases are identified. The article further calculates the transferred power for each case and reveals how the power transfer characteristics in boost mode diverge from those observed in both frozen leg operations at unity gain and in buck mode. Additionally, the frozen leg maximum power transfer in boost mode is observed to gradually decline from the normal operating power level as the output voltage increases. Understanding these transferred power characteristics can provide valuable insights for designing control strategies. Moreover, the analysis of ZVS operation shows that while healthy switches on the secondary side consistently achieve ZVS, the legs *A* and *B* switches have specific ZVS boundary operating regions. Operating within these regions can be important to ensure the thermal health of the switch and to improve converter efficiency. Lastly, based on the ZVS analysis, a novel ZVS-guaranteed control strategy is proposed. By precisely regulating the output voltage reference according to a predefined pattern, this strategy reliably ensures the ZVS operation of all healthy switches at the target power level during frozen leg operation in buck or boost modes. Future work will focus on incorporating dead time in the converter modeling to enhance accuracy in the case of widely varying dead times, performing an analysis of frozen leg operation with primary-side OCFs, and investigating the more severe case with two frozen legs.

Appendix A

$$\begin{cases} I_{A,\mathrm{RMS\_MAX}} = \frac{T_s V_{\mathrm{in}}}{6L}\sqrt{\frac{3323}{10368}} \\ I_{B,\mathrm{RMS\_MAX}} = \frac{T_s V_{\mathrm{in}}}{6L}\sqrt{\frac{2825}{10368}} \\ I_{C,\mathrm{RMS\_MAX}} = \frac{T_s V_{\mathrm{in}}}{6L}\sqrt{\frac{97}{1296}} \end{cases}. \tag{A.1}$$

TABLE II
Segmental Current Expressions of Phases *A*, *B*, *C* for Case I

Phase *A*	Phase *B*	Phase *C*
$I_{A1-0}=-\frac{1}{2}N\phi$ $+(-M+N)\phi_{c1}$ $+(-3M+3N)\frac{\pi}{3}$	$I_{B1-0}=(-\frac{N}{2})\phi$ $+(-M+N)\phi_{c1}$ $+(3M-3N)\frac{\pi}{3}$	$I_{C1-0}=0$
$I_{A1-1}=(3M-\frac{N}{2})\phi$ $+(-M+N)\phi_{c1}$ $+(-3M+3N)\frac{\pi}{3}$	$I_{B1-1}=(-3M-\frac{N}{2})\phi$ $+(-M+N)\phi_{c1}$ $+(3M-3N)\frac{\pi}{3}$	$I_{C1-1}=0$
$I_{A1-2}=\frac{5N}{2}\phi$ $+(-M+N)\phi_{c1}$ $+(3M-3N)\frac{\pi}{3}$	$I_{B1-2}=(-\frac{7N}{2})\phi$ $+(-M+N)\phi_{c1}$ $+(-3M+3N)\frac{\pi}{3}$	$I_{C1-2}=0$
$I_{A1-3}=(2M-\frac{3N}{2})\phi$ $+(-M+N)\phi_{c1}$ $+(3M-3N)\frac{\pi}{3}$	$I_{B1-3}=(2M-\frac{3N}{2})\phi$ $+(-M+N)\phi_{c1}$ $+(-3M+3N)\frac{\pi}{3}$	$I_{C1-3}=(-4M+2N)\phi$
$I_{A1-4}=\frac{N}{2}\phi$ $+(M-N)\phi_{c1}$ $+(3M-3N)\frac{\pi}{3}$	$I_{B1-4}=\frac{N}{2}\phi$ $+(M-N)\phi_{c1}$ $+(-3M+3N)\frac{\pi}{3}$	$I_{C1-4}=0$
$I_{A1-5}=-I_{A1-0}$	$I_{B1-5}=-I_{B1-0}$	$I_{C1-5}=0$

TABLE III
Segmental Current Expressions of Phases *A*, *B*, *C* for Case II

Phase *A*	Phase *B*	Phase *C*
$I_{A2-0}=-\frac{1}{2}N\phi$ $+(\frac{M}{2}-N)\phi_{c2}$ $+(-\frac{9M}{2}+5N)\frac{\pi}{3}$	$I_{B2-0}=-\frac{1}{2}N\phi$ $+(\frac{M}{2}-N)\phi_{c2}$ $+(\frac{3M}{2}-N)\frac{\pi}{3}$	$I_{C2-0}=2N\phi+(4M-4N)\frac{\pi}{3}$
$I_{A2-1}=-\frac{1}{2}N\phi$ $+(\frac{5M}{2}+N)\phi_{c2}$ $+(-\frac{13M}{2}+3N)\frac{\pi}{3}$	$I_{B2-1}=-\frac{1}{2}N\phi$ $+(-\frac{7M}{2}+N)\phi_{c2}$ $+(\frac{11M}{2}-3N)\frac{\pi}{3}$	$I_{C2-1}=0$
$I_{A2-2}=(3M-\frac{1}{2}N)\phi$ $+(-\frac{M}{2}+N)\phi_{c2}$ $+(-\frac{7M}{2}+3N)\frac{\pi}{3}$	$I_{B2-2}=(-3M-\frac{1}{2}N)\phi$ $+(-\frac{M}{2}+N)\phi_{c2}$ $+(\frac{5M}{2}-3N)\frac{\pi}{3}$	$I_{C2-2}=0$
$I_{A2-3}=\frac{5}{2}N\phi$ $+(-\frac{M}{2}+N)\phi_{c2}$ $+(\frac{5M}{2}-3N)\frac{\pi}{3}$	$I_{B2-3}=-\frac{7}{2}N\phi$ $+(-\frac{M}{2}+N)\phi_{c2}$ $+(-\frac{7M}{2}+3N)\frac{\pi}{3}$	$I_{C2-3}=0$
$I_{A2-4}=(2M-\frac{3}{2}N)\phi$ $+(-\frac{M}{2}+N)\phi_{c2}$ $+(\frac{5M}{2}-3N)\frac{\pi}{3}$	$I_{B2-4}=(2M-\frac{3}{2}N)\phi$ $+(-\frac{M}{2}+N)\phi_{c2}$ $+(-\frac{7M}{2}+3N)\frac{\pi}{3}$	$I_{C2-4}=(-4M+2N)\phi$
$I_{A2-5}=-I_{A2-0}$	$I_{B2-5}=-I_{B2-0}$	$I_{C2-5}=-I_{C2-0}$

TABLE IV
SEGMENTAL CURRENT EXPRESSIONS OF PHASES *A, B, C* FOR CASE III

Phase *A*	Phase *B*	Phase *C*
$I_{AIII-0}=-3N\phi$ $+(-4M+6N)\frac{\pi}{3}$ $+(-\frac{M}{2}+N)\phi_{dc1}$ $+(\frac{M}{2}-\frac{N}{2})\phi_{dc2}$	$I_{BIII-0}=3N\phi$ $+(2M-6N)\frac{\pi}{3}$ $+(-\frac{M}{2}+N)\phi_{dc1}$ $+(\frac{M}{2}-\frac{N}{2})\phi_{dc2}$	$I_{CIII-0}=(4M-2N)\frac{\pi}{3}$
$I_{AIII-1}=(2M+N)\phi$ $+(-6M+2N)\frac{\pi}{3}$ $+(-\frac{M}{2}+N)\phi_{dc1}$ $+(\frac{M}{2}-\frac{N}{2})\phi_{dc2}$	$I_{BIII-1}=(-4M+N)\phi$ $+(6M-4N)\frac{\pi}{3}$ $+(-\frac{M}{2}+N)\phi_{dc1}$ $+(\frac{M}{2}-\frac{N}{2})\phi_{dc2}$	$I_{CIII-1}=(2M-2N)\phi+2M\frac{\pi}{3}$
$I_{AIII-2}=-N\phi$ $+(-2M+6N)\frac{\pi}{3}$ $+(-\frac{5M}{2}-N)\phi_{dc1}$ $+(\frac{M}{2}-\frac{N}{2})\phi_{dc2}$	$I_{BIII-2}=-N\phi$ $+(-2M)\frac{\pi}{3}$ $+(\frac{7M}{2}-N)\phi_{dc1}$ $+(\frac{M}{2}-\frac{N}{2})\phi_{dc2}$	$I_{CIII-2}=0$
$I_{AIII-3}=-N\phi$ $+(-2M+6N)\frac{\pi}{3}$ $+(\frac{M}{2}-N)\phi_{dc1}$ $+(\frac{M}{2}-\frac{N}{2})\phi_{dc2}$	$I_{BIII-3}=-N\phi$ $+(-2M)\frac{\pi}{3}$ $+(\frac{M}{2}-N)\phi_{dc1}$ $+(\frac{M}{2}-\frac{N}{2})\phi_{dc2}$	$I_{CIII-3}=0$
$I_{AIII-4}=(4M-N)\phi$ $+(-6M+6N)\frac{\pi}{3}$ $+(\frac{M}{2}-N)\phi_{dc1}$ $+(\frac{M}{2}-\frac{N}{2})\phi_{dc2}$	$I_{BIII-4}=(-2M-N)\phi$ $+(\frac{M}{2}-N)\phi_{dc1}$ $+(\frac{M}{2}-\frac{N}{2})\phi_{dc2}$	$I_{CIII-4}=-2M\phi+2M\frac{\pi}{3}$
$I_{AIII-5}=3N\phi$ $+(2M-2N)\frac{\pi}{3}$ $+(\frac{M}{2}-N)\phi_{dc1}$ $+(-\frac{7M}{2}+\frac{7N}{2})\phi_{dc2}$	$I_{BIII-5}=-3N\phi$ $+(-4M+4N)\frac{\pi}{3}$ $+(\frac{M}{2}-N)\phi_{dc1}$ $+(\frac{5M}{2}-\frac{5N}{2})\phi_{dc2}$	$I_{CIII-5}=0$
$I_{AIII-6}=3N\phi$ $+(2M-2N)\frac{\pi}{3}$ $+(\frac{M}{2}-N)\phi_{dc1}$ $+(-\frac{M}{2}+\frac{N}{2})\phi_{dc2}$	$I_{BIII-6}=-3N\phi$ $+(-4M+4N)\frac{\pi}{3}$ $+(\frac{M}{2}-N)\phi_{dc1}$ $+(-\frac{M}{2}+\frac{N}{2})\phi_{dc2}$	$I_{CIII-6}=0$
$I_{AIII-7}=-I_{AIII-0}$	$I_{BIII-7}=-I_{BIII-0}$	$I_{CIII-7}=-I_{CIII-0}$

TABLE V
SEGMENTAL CURRENT EXPRESSIONS OF PHASES *A, B, C* FOR CASE IV

Phase *A*	Phase *B*	Phase *C*
$I_{AIV-0}=-3N\phi$ $+(-4M+6N)\frac{\pi}{3}$ $+(-\frac{M}{2}+N)\phi_{dc3}$	$I_{BIV-0}=3N\phi$ $+(2M-6N)\frac{\pi}{3}$ $+(-\frac{M}{2}+N)\phi_{dc3}$	$I_{CIV-0}=2N\phi+(6M-6N)\frac{\pi}{3}$
$I_{AIV-1}=(2M+N)\phi$ $+(-6M+2N)\frac{\pi}{3}$ $+(-\frac{M}{2}+N)\phi_{dc3}$	$I_{BIV-1}=(-4M+N)\phi$ $+(6M-4N)\frac{\pi}{3}$ $+(-\frac{M}{2}+N)\phi_{dc3}$	$I_{CIV-1}=2M\phi+(4M-4N)\frac{\pi}{3}$
$I_{AIV-2}=-N\phi$ $+(-2M+6N)\frac{\pi}{3}$ $+(-\frac{5M}{2}-N)\phi_{dc3}$	$I_{BIV-2}=-N\phi$ $+(-2M)\frac{\pi}{3}$ $+(\frac{7M}{2}-N)\phi_{dc3}$	$I_{CIV-2}=0$
$I_{AIV-3}=-N\phi$ $+(-2M+6N)\frac{\pi}{3}$ $+(\frac{M}{2}-N)\phi_{dc3}$	$I_{BIV-3}=-N\phi$ $+(-2M)\frac{\pi}{3}$ $+(\frac{M}{2}-N)\phi_{dc3}$	$I_{CIV-3}=0$
$I_{AIV-4}=(4M-N)\phi$ $+(-6M+6N)\frac{\pi}{3}$ $+(\frac{M}{2}-N)\phi_{dc3}$	$I_{BIV-4}=(-2M-N)\phi$ $+(\frac{M}{2}-N)\phi_{dc3}$	$I_{CIV-4}=-2M\phi+(2M)\frac{\pi}{3}$
$I_{AIV-5}=3N\phi$ $+(2M-2N)\frac{\pi}{3}$ $+(\frac{M}{2}-N)\phi_{dc3}$	$I_{BIV-5}=-3N\phi$ $+(-4M+4N)\frac{\pi}{3}$ $+(\frac{M}{2}-N)\phi_{dc3}$	$I_{CIV-5}=-2N\phi+(-2M+4N)\frac{\pi}{3}$
$I_{AIV-6}=-I_{AIV-0}$	$I_{BIV-6}=-I_{BIV-0}$	$I_{CIV-6}=-I_{CIV-0}$

TABLE VI
SEGMENTAL CURRENT EXPRESSIONS OF PHASES *A, B, C* FOR CASE V

Phase *A*	Phase *B*	Phase *C*
$I_{AV-0}=-3N\phi+$ $(-4M+6N)\frac{\pi}{3}-N\phi'$	$I_{BV-0}=3N\phi+$ $(2M-6N)\frac{\pi}{3}-N\phi'$	$I_{CV-0}=2N\phi+$ $(6M-6N)\frac{\pi}{3}-2M\phi'$
$I_{AV-1}=(2M+N)\phi+$ $(-6M+2N)\frac{\pi}{3}-N\phi'$	$I_{BV-1}=(-4M+N)\phi+$ $(6M-4N)\frac{\pi}{3}-N\phi'$	$I_{CV-1}=2M\phi+$ $(4M-4N)\frac{\pi}{3}-2M\phi'$
$I_{AV-2}=(-N)\phi+$ $(-2M+6N)\frac{\pi}{3}-N\phi'$	$I_{BV-2}=-N\phi$ $-2M\frac{\pi}{3}-N\phi'$	$I_{CV-2}=4N\phi+$ $(8M-12N)\frac{\pi}{3}-2M\phi'$
$I_{AV-3}=(-N)\phi+$ $(-2M+6N)\frac{\pi}{3}+(4M+N)\phi'$	$I_{BV-3}=(-N)\phi$ $-2M\frac{\pi}{3}+(-2M+N)\phi'$	$I_{CV-3}=0$
$I_{AV-4}=(4M-N)\phi+$ $(-6M+6N)\frac{\pi}{3}+N\phi'$	$I_{BV-4}=(-2M-N)\phi$ $+N\phi'$	$I_{CV-4}=(-2M)\phi$ $+2M\frac{\pi}{3}+2M\phi'$
$I_{AV-5}=3N\phi+$ $(2M-2N)\frac{\pi}{3}+N\phi'$	$I_{BV-5}=(-3N)\phi+$ $(-4M+4N)\frac{\pi}{3}+N\phi'$	$I_{CV-5}=(-2N)\phi+$ $(-2M+4N)\frac{\pi}{3}+2M\phi'$
$I_{AV-6}=-I_{AV-0}$	$I_{BV-6}=-I_{BV-0}$	$I_{CV-6}=-I_{CV-0}$

APPENDIX B

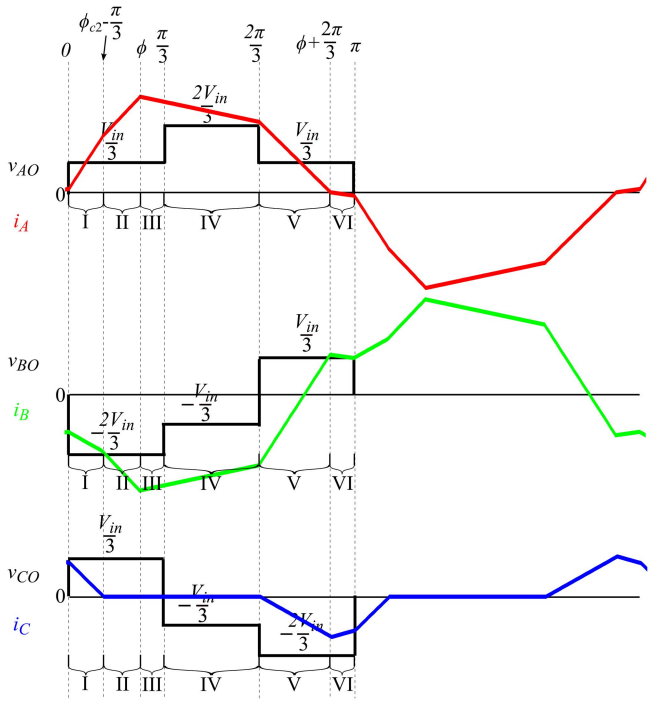


Fig. 30. Phase voltages and currents waveforms used for power transfer calculation in case II.

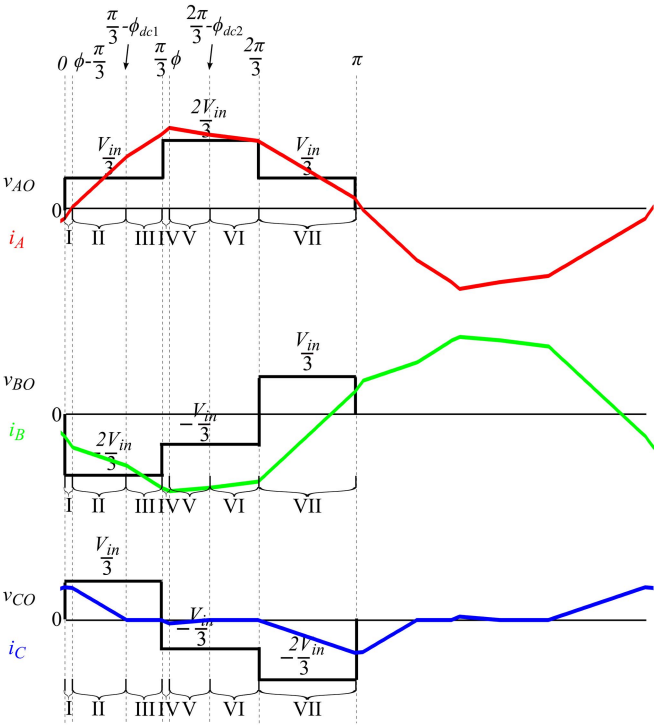


Fig. 31. Phase voltages and currents waveforms used for power transfer calculation in case III.

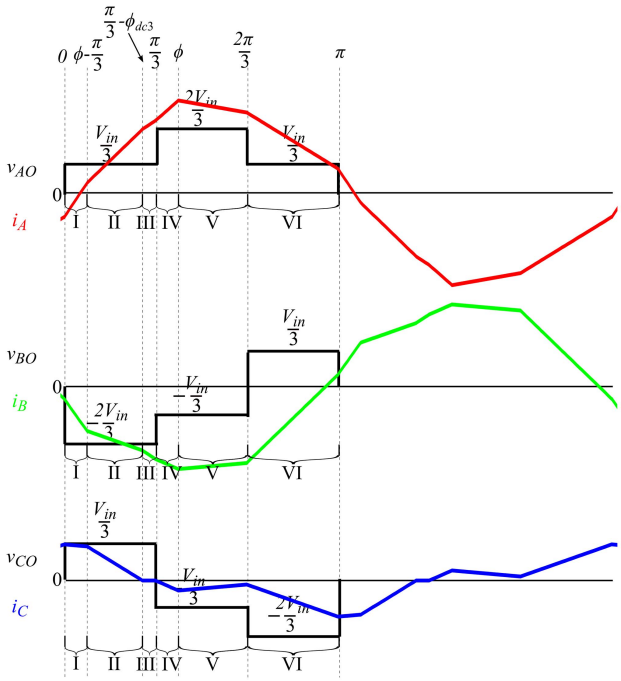


Fig. 32. Phase voltages and currents waveforms used for power transfer calculation in case IV.

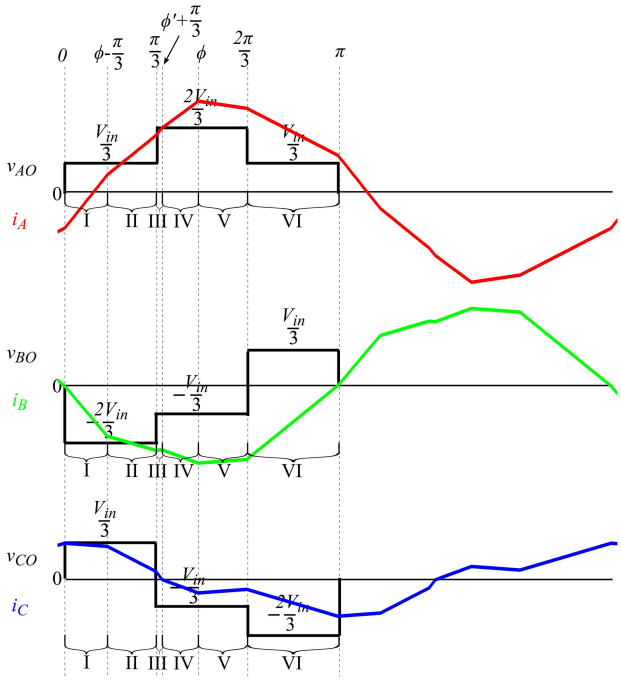


Fig. 33. Phase voltages and currents waveforms used for power transfer calculation in case V.

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