Automated Design of Power Module Packaging With Multiobjectives Based on Artificial Neural Network and Deep Reinforcement Learning

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***Abstract*—Traditional design methods for power module packaging heavily rely on manual experiences. Although the computer-aided optimization methods utilizing metaheuristic algorithms, for example, have accelerated the design process, they are still affected by lengthy iterative cycles when including 3-D numerical simulations. Regarding these issues, this article proposes a multiobjective automated design method for power modules based on machine learning, combining artificial neural networks (ANNs) and deep reinforcement learning (DRL). The proposed ANN model can save massive time of iterative 3-D numerical calculations in multiobjective optimization design of the power module packaging, meanwhile avoiding the complex interaction of different software. The DRL algorithm can output the optimal design variables efficiently, even when design requirements change after the agent are well trained. A 1200-V/300-A double-sided cooled module is used as a case study to validate the proposed method. Aiming to the four objectives—parasitic inductance (L), junction temperature (T_j), temperature difference (ΔT_j), and power density (ρ)—the power module is optimized and assembled. The proposed method is validated respectively with simulation and experiment.**

***Index Terms*—Artificial neural networks (ANNs), deep reinforcement learning (DRL), machine learning, multiobjective automated design (MOAD), power module.**

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I. Introduction

With the rapid advancement of new energy generation, electrified transportation, etc., the industrial applications have imposed increasingly higher requirements on the power modules [1], [2]. The encapsulation design of power modules is critically important because it significantly affects their performance [3], [4], [5].

Traditional power module design methods rely heavily on manual experience and typically focus on optimizing a single objective, such as parasitic inductance, parasitic capacitance, junction temperature, or lifetime. Huang et al. [6] proposed a hybrid packaging module using direct bonded copper (DBC) stacking, which reduces module parasitic inductance to 2.4 nH through a 3-D commutation structure. Domurat-Linde and Hoene [7] reduced output-to-ground parasitic capacitance by using flip-chip soldering for the lower bridge arm chips, effectively lowering common-mode electromagnetic interference (EMI). Tang et al. [8] introduced a double-sided water-cooled module with chips embedded in an active metal brazing (AMB) substrate, reducing junction-to-case thermal resistance by 50% and improving the module's cooling performance. Ding et al. [9] replaced solid copper interposers with sintered silver, reducing the thermomechanical stress on SiC chips in the module by 50%. In recent years, multiobjective optimization (MOO) design has gradually become a research hot spot in power module packaging design. Ke et al. [10] improved the electrical and thermal performance of a commercial 62-mm power module by optimizing the terminal structure and chip layout. Similarly, Zhang and Wang [11] reduced module inductance and enhanced thermal performance by optimizing chip layout. However, these studies still primarily focus on electrical characteristics, particularly parasitic inductance, as the main optimization target. For thermal characteristics, simulations were often used for validation, but effective co-design was lacking. Furthermore, the optimization processes in these studies heavily relied on trial-and-error procedures. In reality, power modules often involve three or more objectives, and there are tradeoffs between these objectives. Relying on human experience and extensive trial-and-error methods leads to longer design cycles and higher design costs.

Currently, computer-aided MOO design methods have been widely used in power module packaging design. Ji et al. [12]

utilized a mathematical model of thermal resistance and a finite-element (FE) model of plastic deformation, along with the second-generation nondominated sorting genetic algorithm (NSGA-II), to search for Pareto-optimal solutions, achieving optimal module structure design. In [13], thermal resistance and mechanical stress models were established for a double-sided water-cooled module, and MOO was conducted using NSGA-II, revealing that spacer thickness and ceramic layer thickness are key factors in balancing thermal and mechanical properties. However, existing MOO methods still suffer from limitations of insufficient accuracy and computationally intensive processes. First, objectives such as parasitic parameters and thermal resistance are mostly modeled using approximate analytical formulas. For complex power module structures such as double-sided cooled (DSC) modules, the accuracy of analytical models is quite limited. Besides, effects such as inductive coupling between different current paths and thermal coupling between chips are often neglected. Second, while some studies have established FE models for stresses, these models require extensive parametric simulations. Particularly for complex structures, iterative optimization with multiple design variables and objectives can lead to excessive computation time.

To improve design efficiency, several studies have investigated multiobjective automated layout methods for power modules. Zhou et al. [14] innovatively proposed an autonomous heterogeneous layout generation framework based on a constraint graph model. This framework employs integer programming algorithms to generate power module layouts with variable geometric topologies and further utilizes genetic algorithms (GAs) to automatically solve for Pareto-optimal solutions, enabling MOO design. To enhance computational efficiency, the method rapidly extracts parasitic inductance based on a multiport impedance matrix. However, simplifications in modeling high-frequency coupling effects, such as neglecting the frequency-dependent characteristics of the skin effect and approximating proximity effects, help to reduce the time for multiple simulations, but leading to degradation in inductance extraction accuracy. Ning et al. [15], [16] achieved automated layout generation with variable geometric topologies through automatic mesh discretization technology. These works employ the method of moments to analytically establish the correlation between current distribution and geometric parameters, thereby facilitating rapid acquisition of parasitic inductance under different layout configurations. Similarly, the accuracy of this inductance extraction method diminishes at high frequencies. Software tools based on the GA and randomization techniques for automated MOO design of power modules have been effectively proposed in [17], [18], and [19], exemplified by PowerSynth. This platform utilizes FastHenry for parasitic inductance extraction and ParaPower for thermal performance evaluation. The main advantage of the aforementioned tools is its ability to enhance computational efficiency through targeted simplification of complex 3-D structures. While enabling rapid estimation of parasitic inductance and junction temperature performance metrics, the attainable accuracy still presents potential for further refinement. In contrast, ANSYS Q3D and Thermal use higher order FE methods and adaptive mesh techniques, allowing precise simulation of complex geometries and electromagnetic–thermal multiphysics coupling effects. Although the simulation accuracy of the performance targets improves, when faced with a large number of design parameters and objectives, the required number of simulations increases dramatically. Regardless of the software used, the computational time required becomes unacceptable [20], [21], [22]. More importantly, when design requirements change, such as voltage, current, or power density, the aforementioned methods need to be reexecuted, leading to significant manual intervention and time consumption.

To address the issues, this article proposes a novel multiobjective automated design method for the packaging of power modules based on machine learning, combining artificial neural networks (ANNs) and deep reinforcement learning (DRL). The ANN and DRL have been respectively tried in prediction and design issues in power electronics. For example, Dragičević et al. [23] used the ANN to predict complex input solar radiation and output lifetime regarding the power converter reliability. In [24], a DRL-based approach is proposed to solve the problem of a static synchronous compensator parameter adjusting, which considers the uncertainty of the wind power production. The environment of the DRL methodology employed in the aforementioned designs relies heavily on analytical formulations and circuit simulation models. If the existing methods are used for the packaging of the power module, massive numerical simulations are required for electromagnetic–thermal multiphysical fields that can result in very long simulation time, which is not feasible. Thus, this article proposes a machine-learning-based method for fast design of the MOO of multiphysical field in the power module. The main innovations of this article are as follows.

1) A unified ANN model is proposed to replace numerical simulations in different physical domains, which can save massive time of iterative 3-D numerical calculations in the MOO design of the power module packaging and avoid the complex interaction of different software.
2) DRL embedding the aforementioned ANN models is first proposed for the MOO design of the packaging of power modules, which significantly improves design efficiency while increasing accuracy. With the DRL-based design, not only can MOO be achieved, but also new optimal design variables can be obtained within very short time when a new design requirement is input.

The rest of this article is organized as follows. Section II introduce the design case and the basic framework of the prosed method. Section III presents the specific methodology and the design process. Section IV evaluates the optimization performance of the proposed method and compares it with existing MOO methods to demonstrate its effectiveness. Section V presents the assembly of power module and experimental results. Finally, Section VI concludes this article.

II. Framework of the Proposed Automated Design Method

A. Multiobjective Packaging Design of the Power Module

In power module packaging design, there are numerous design variables, including chip selection, chip layout, substrate

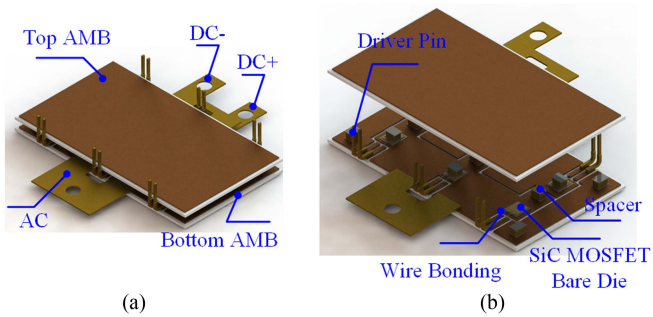

Fig. 1. Structure of the DSC power module. (a) CAD model of the module. (b) Explore view of the module.

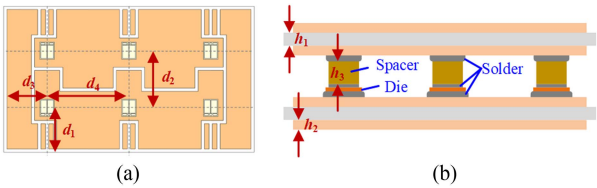

Fig. 2. Key physical dimensions of the power module. (a) Substrate layout dimensions. (b) Thickness of each substrate layer.

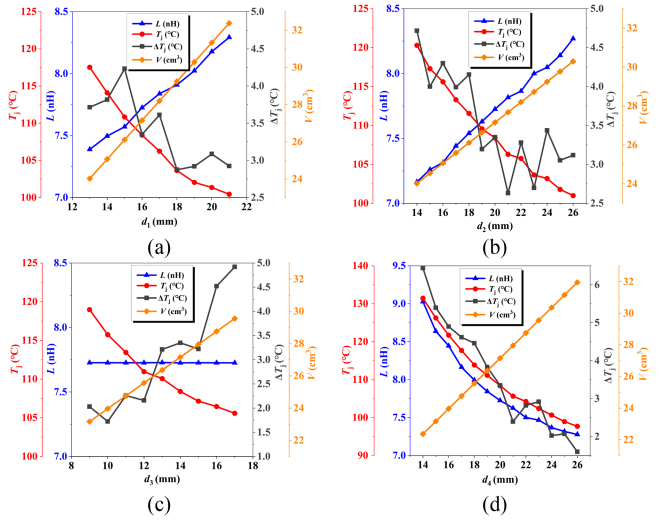

Fig. 3. Dependence of module parasitic inductance, chip temperature, temperature difference, and power density on key physical dimensions. (a) Dependence of module performances on d_1. (b) Dependence of module performance on d_2. (c) Dependence of module performance on d_3. (d) Dependence of module performance on d_4.

dimensions, and the selection of solder and encapsulant materials. These design parameters directly affect key performance objectives, such as parasitic inductance, parasitic capacitance, thermal resistance, heat capacity, and the coefficient of thermal expansion. In turn, these factors have a significant and direct impact on the module's electrical characteristics, such as overvoltage, overcurrent, current sharing, and EMI, as well as thermal characteristics, such as junction temperature, temperature uniformity, and thermal stress. For example, DSC modules have challenges in multiobjective electrical–thermal performance design due to the relatively complex 3-D structure. Wang et al. [25] addressed that the chip spacing has conflicting effects on current sharing and temperature uniformity in DSC modules. While increasing the chip spacing, a more uniform temperature distribution across the chips can be realized; it exacerbates differences in parasitic inductance between branches, leading to current imbalance.

Fig. 1 shows a half-bridge DSC module, with each bridge composing of three parallel chips. The packaging structure includes parts, such as the upper and lower AMB substrates, chips, spacers, and terminals. Fig. 2 illustrates several key design variables of the DSC module, where critical dimensions d_1, d_2, d_3, and d_4 determine the layout on the substrate. Parasitic inductance L of the commutation loop under different dimensions is extracted through Ansys Q3D, while the junction temperature T_j and temperature difference ΔT_j of the chips are extracted using COMSOL. It is worth clarifying that T_j is defined as the bulk maximum temperature of the chip, which is probe-extracted in COMSOL. ΔT_j, in turn, refers to the difference between the bulk maximum temperatures of the edge chip and the middle chip. The module volume V is derived from the product of the module's length, width, and height. The dependence of the aforementioned performances on key layout dimensions is shown in Fig. 3. Taking Fig. 3(a) as an example, as d_1 increases, T_j decreases, and the overall trend for ΔT_j is also decreasing, while L increases. This is because the increase in d_1 leads to a larger substrate area, which increases the effective heat transfer area. However, the longer commutation loop resulting from a larger d_1 increases L. Moreover, increasing d_1 obviously leads to a larger substrate volume, thereby reducing the module's power density. In Fig. 3(b)–(d), similar conflicting dependence of various performance indicators can be observed.

Therefore, balancing these design objectives and mitigating the adverse effects are among the main challenges in the power module packaging design process. Resolving these conflicts requires a comprehensive consideration of the interdependencies between the design objectives, along with careful tradeoffs and optimization of each objective, to achieve the optimal performance balance for the power module.

B. Simplified Design Variables and Objectives in the Case Study

MOO design of power modules has attracted significant attention in recent years. Most existing studies rely on either mathematical modeling or extensive FE simulations to establish the dependence between design variables and performance objectives. However, analytical models can only be suitable for very simple structure, and for most module packaging, they are limited. On the other hand, FE simulations can accommodate complex structures and material nonlinearities, but they are computationally expensive and time consuming. When multiple design variables are involved, the number of simulations required increases drastically, resulting in a prolonged and resource-intensive optimization process. Moreover, if the design requirements, such as current rating, change, the existing optimization process should be rerun from scratch, further increasing the computational burden.

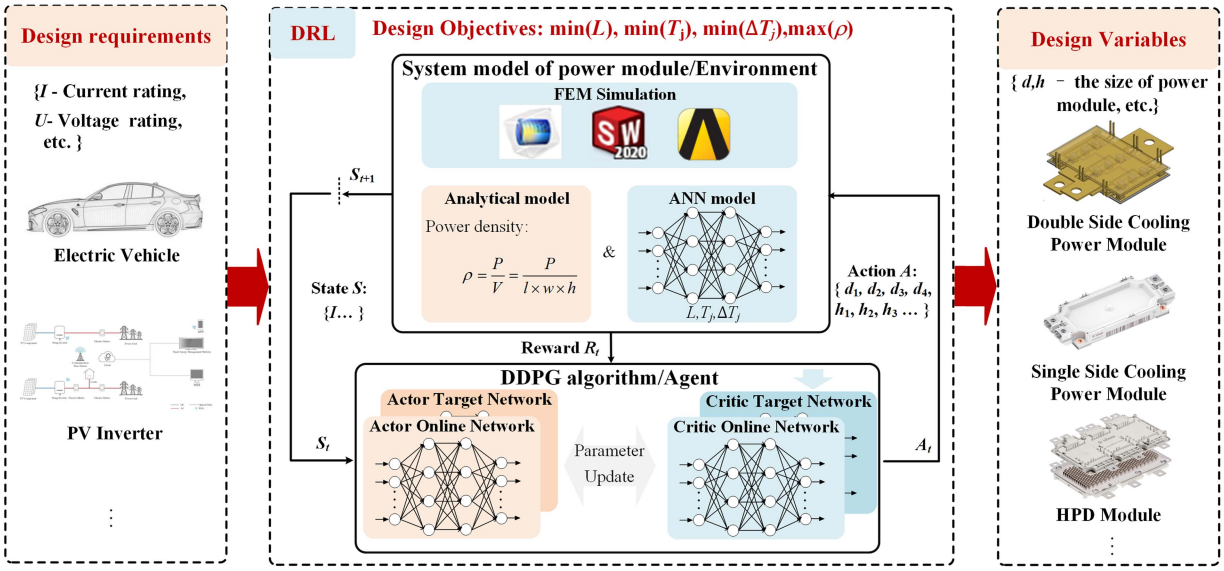

Fig. 4. Framework of the proposed MOAD method for the power module.

To address these challenges, this study proposes a novel multiobjective automated packaging design framework for power modules based on ANNs and DRL. First, ANNs are capable of learning complex nonlinear dependence of outputs on multiple inputs using small batches of training data, thereby reducing reliance on time-consuming 3-D FE simulations for fields. Second, DRL excels at decision making in environments characterized by high-dimensional data, complex dynamics, and uncertainty. It enables adaptive optimization in response to evolving design requirements [26], [27]. Compared to conventional multiobjective design methodologies, the proposed approach demonstrates significant potential in enhancing the efficiency and flexibility of power module packaging design.

To validate the effectiveness of the proposed method, a DSC, as shown in Fig. 1, is used as the design case. The key layout dimensions of the substrate (d_1, d_2, d_3, and d_4), ceramic layer thickness (h_1), copper layer thickness (h_2), spacer thickness (h_3), and current (I) are selected as design variables, while L, T_j, ΔT_j, and ρ are chosen as the design objectives for the multiobjective automated optimization. It is worthy to mention that MOO of a real power module is more complex that involves more design variables, such as chip type, solder materials, and so on. However, a simplified case is enough for the validation of the proposed machine learning method, which already contains the key factors including multidesign variables, objectives, system requirements and complex dependence in between that requires 3-D numerical calculations.

C. Principle of the Proposed MOAD Method

This section mainly introduces principle of the proposed DRL-based MOAD method. The framework of the method is shown in Fig. 4. Three basic concepts are defined as follows.

1) *Design requirements:* They are defined as the changing requirements from the client for a power module, e.g., the rating current I here in our simplified case.
2) *Design variables:* They are defined as key parameters of the power module to be designed by engineers, e.g., the dimensions mentioned earlier in Section II-B.
3) *Design objectives:* They are defined as the design objectives of the power module, e.g., parasitic inductance L, junction temperature T_j, temperature difference ΔT_j, and power density ρ here.

Overall, the MOAD method contains two steps that are the modeling and the self-learning.

Regarding the first modeling step, the system model that reflects the dependence of the design objectives on the design variables is established, which is also defined as environment in the next DRL step. The system model contains both the analytical model and the proposed ANN model. The ANN model is a replacement of the 3-D numerical simulations, which can dramatically reduce the calculation time of the iterative optimization processes.

Regarding the second step, a DRL method using deep deterministic policy gradient (DDPG) algorithm is proposed for the self-learning of the agent. The self-learning process that bases on the Markov decision-making process (MDP) is an iterative interaction between the so-called environment and agent [28], as shown in the middle block of Fig. 4. In our design case, the environment is defined as the system model discussed earlier. The agent is the executive unit that receives the updated state S, defined as design requirements, and reward R, defined as the weighting of multidesign objectives, and responds with new action A, defined as design variables. The agent composes of actor and critic networks, which interact based on the DDPG algorithm. With the successful self-learning, the agent can fast output the design variables with a given design requirement to achieve the best performances, which is detailed in Section III.

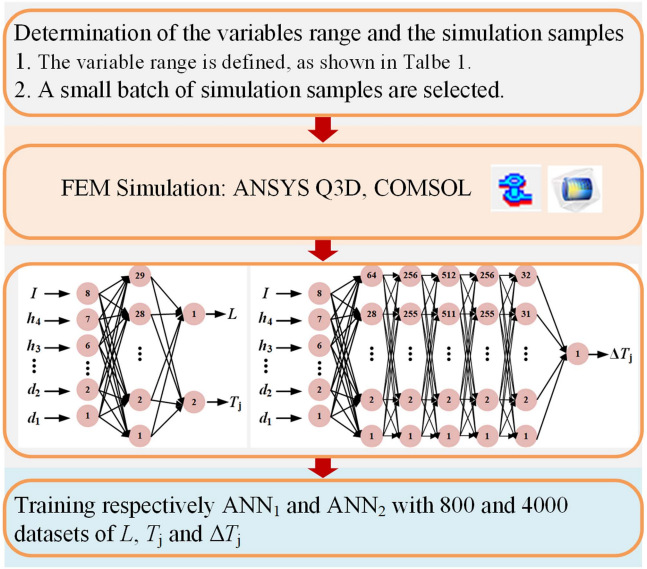

Fig. 5. Steps of the modeling of parasitic inductance, junction temperature, and temperature difference based on the ANN.

TABLE I
VARIABLE RANGE AND THE DISCRETIZATION STEPS

Variables	Range	Number of samples for the variable N_i
d_1	[13, 2, 21]	5
d_2	[14, 3, 26]	5
d_3	[9, 2, 17]	5
d_4	[14, 3, 26]	5
h_1	[0.3, 0.2, 0.9]	4
h_2	[0.2, 0.2, 1]	5
h_3	[2, 1, 5]	4
I	[200, 20 ,300]	6

The principle is not only suitable for the DSC module design but also can be expanded to the design of other power modules with different applications.

III. Design Case of MOAD for the DSC Power Module

In this section, the proposed MOAD of the DSC power module is presented as a case study. The modeling and self-learning are introduced, respectively.

A. Modeling of Design Objectives

1) Parasitic Inductance and Junction Temperature: The modeling process is shown in Fig. 5. First, the range and discretization step of the design variables are defined based on the DSC module, which is shown in Table I. In particular, since this design case is a sample module developed for power electronic converters, the upper limit of the module size is determined by a combination of system space requirements and manufacturing process constraints. The possible design requirement is also set, which is the rating current I here from 200 to 300 A as a simplified example. Traditionally, an optimized solution can be found by the brute search (BS) by performing massive simulations with all the possible combinations. Here, the total number based on the discretization step can be calculated by the product $N_1 \times N_2 \times N_3 \times \cdots \times N_i$, which is equal to 300 000. If the 3-D FE simulations are carried out for the parasitic inductance and the temperature for all the possibilities, around 1.27 years are required for the simulation, the calculation of which is detailed in Section IV. Thus, it is impossible for the MOO design by the traditional BS method. Correspondingly, an ANN-based method is proposed, which only requires a small batch of the simulation samples.

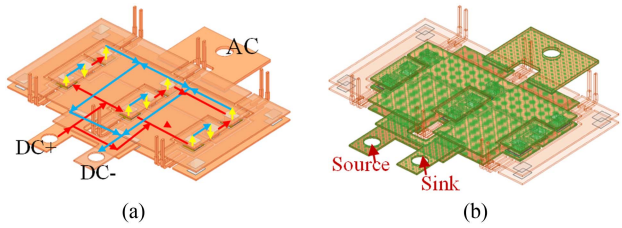

Fig. 6. Extraction of the parasitic inductance of the power module in ANSYS Q3D. (a) Schematic of the current path during commutation transient. (b) Excitation assignment in Q3D.

Here, only 800 sets of variable combinations are randomly selected, and FE simulations are carried out to extract the parasitic inductance and junction temperature. ANSYS Q3D is employed to extract the parasitic inductance of the module. Fig. 6(a) illustrates the current path during the commutation transient of the module for the simulation, where the red indicates the current in the lower substrate copper layer, the yellow represents the current in the spacers, and the blue shows the current in the upper substrate copper layer. The high-frequency current flows in from the positive terminal and enters the upper bridge MOSFET's drain through the lower substrate copper layer. Then, from the MOSFET's source, the current flows through the spacer soldered to its surface into the upper substrate copper layer, and then through the spacer back into the lower substrate copper layer, further flowing to the lower bridge MOSFET's drain. Finally, from the MOSFET's source, the current flows through another spacer back into the upper substrate copper layer and out through the negative terminal. In summary, the current path forms a stacked commutation loop within the module. Correspondingly, in Q3D, excitation sources and sinks are set at the screw hole positions of the positive and negative terminals, as shown in Fig. 6(b), to form a current loop and extract the parasitic inductance of the module.

The temperature distribution of the power module can be extracted using COMSOL's electrothermal coupling simulation. In the simulation model, the chip is modeled as a resistor, and the temperature-dependent resistance values from the datasheet are converted into corresponding conductivity values. The negative dc terminal of the power module is grounded, and a current excitation is applied to the positive dc terminal, as shown in Fig. 7(a). At this point, the module generates conduction losses. A thermal convection coefficient of 2000 W/(m^2·K) is set on the upper and lower substrate copper layers to simulate water-cooled

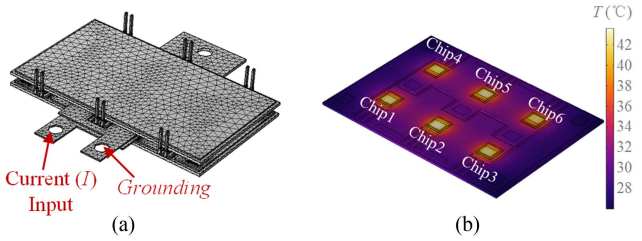

Fig. 7. Temperature extraction of the power module in COMSOL. (a) Module model in COMSOL. (b) Temperature distribution contour plot inside the module.

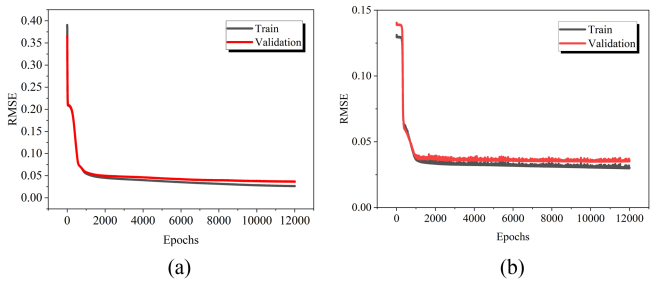

Fig. 8. Learning curves of the ANN model. (a) Learning curve of ANN_1. (b) Learning curve of ANN_2.

heat dissipation, so that the generated heat is conducted out through the upper and lower substrates. Fig. 7(b) shows a contour plot of the internal temperature distribution of the power module under a specific current. The maximum junction temperature of the chips is selected as the optimization design target T_j.

Furthermore, the parasitic inductance and junction temperature from the 800 simulations are used as training samples for the ANN_1 model with eight input variables and two output variables.

2) Temperature Difference: The temperature difference between chips is defined as the difference between the maximum and minimum junction temperatures among the six chips. The ANN_2 model is used to establish the dependence of the temperature difference on design variables. Similar to ANN_1, the design variables consist of d_1, d_2, d_3, d_4, h_1, h_2, h_3, and current level I. However, the temperature difference is a relatively small-magnitude metric and exhibits higher sensitivity to design parameters compared to parasitic inductance and junction temperature. This heightened sensitivity increases the difficulty of training the ANN model for temperature difference prediction. To mitigate noise-induced errors in regions with low temperature gradients and improve overall model accuracy, dense sampling of the temperature difference data was performed in this study. Therefore, during the training process, a total of 4000 datasets from COMSOL simulation are used to obtain the temperature difference. Ultimately, an ANN_2 model with eight input variables and one output variable for the temperature difference is obtained, as shown in Fig. 5.

3) Power Density: Power density is defined as the ratio of the module's rated power to its volume, where the rated power is the product of the module's rated voltage and rated current. To simplify the volume calculation, the power module is approximated as a regular cuboid, and the volumes of terminals and gate driver pins are neglected. The module volume is, thus, calculated as the product of its length, width, and height, and the power density ρ is given by (1).

The module volume is determined by the geometric design parameters d_1, d_2, d_3, d_4, h_1, h_2, and h_3, and its expression is shown in (2)

$$\rho = \frac{P}{V} \tag{1}$$

$$V = (2d_1 + d_2) \times 2(d_3 + d_4) \times (2h_1 + 4h_2 + h_3 + 0.48). \tag{2}$$

B. Verification of the ANN Models

The purpose of the ANN model is to effectively capture the design variables and in the multidimensional design space. The ANN model is trained with data that obtained from the small batch simulations. The data are divided into three parts: training set, validation set, and test set. The training set is used to train the initial ANN model, consisting of input data and corresponding output data. Through iterative training, the connection weights and biases are continuously adjusted to minimize the prediction error. The validation set is used to adjust the hyperparameters and structure of the ANN model, evaluating its performance on data outside the training set. By assessing the model's performance on the validation set, the best hyperparameter settings can be selected to improve the model's generalization ability. The test set is used to evaluate the performance and generalization capability of the ANN model. After training is complete, the test set is used to assess the model's accuracy and performance on unfamiliar data, verifying its generalization ability.

An important method for determining whether the ANN training is sufficient is observing the trend of the learning curves [29]. The learning curve shows the changes in training and validated errors as the number of training iterations increases. If both the training and validated errors stabilize without significant overfitting, it indicates that the model has converged, and the training is sufficient. Fig. 8 shows the learning curves for the two aforementioned ANNs. Using root-mean-square error as the loss function, it can be observed that both the training and validated errors show no significant changes after 2000 iterations and eventually fall below 4%. In addition, the gap between the training and validated errors is minimal, demonstrating that the model has not overfitted, which indicates that the model has good generalization capability.

In addition, the performance of the ANN model can also be quantified using the coefficient of determination (R^2) [30], as shown in the following equation:

$$R^2 = 1 - \frac{\sum_{i=1}^{n} \left(y_i - \hat{y_i}\right)^2}{\sum_{i=1}^{n} \left(y_i - \bar{y}_i\right)^2} \tag{3}$$

where yi is the actual value, $\hat{y_i}$ is the predicted value, $\bar{y}_i$ is the mean of the actual values, and n is the sample size. The value of R2 ranges from [0, 1], and the closer R2 is to 1, the better the fit. Using the equation, the training results of the two ANN models are further evaluated. After 12 000 iterations, the R2 values on the validation set for the two ANNs reached 0.9726 and 0.9389, respectively. This demonstrates that the model has strong fitting

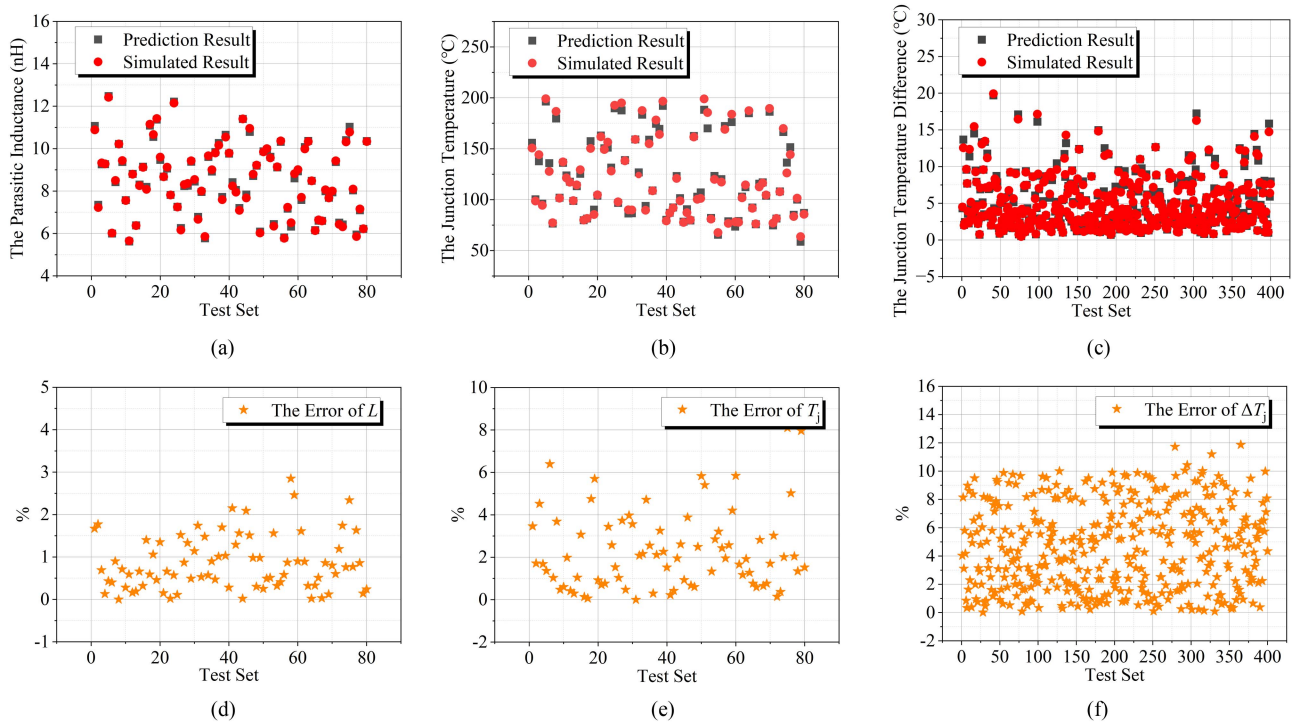

Fig. 9. Validation of ANN model training results. (a) Comparison between ANN predictions and simulation values. (b) Error analysis.

Furthermore, the predictions of the ANN model are compared with the actual simulation results to verify the accuracy of the ANN model. Fig. 9(a) presents a comparison between the actual simulation data and the ANN-predicted results based on the test set, where the red curves represent the actual values, and the black curves represent the predicted values. As shown, the ANN demonstrates high prediction accuracy for parasitic inductance, junction temperature, and temperature difference, with excellent agreement with the simulation results. Fig. 9(b) further provides an error analysis between the predicted and actual values. It can be observed that the prediction error for parasitic inductance remains below 3% across all test samples. For junction temperature, the overall prediction error is below 10%, with over 95% of the test data exhibiting errors less than 4%. The prediction error for temperature difference is generally within 10%, with only a few isolated points reaching up to 12%. This slightly higher relative error is mainly due to the small absolute magnitude of temperature difference values, which mostly fall in the 0–5 °C range, making percentage errors appear a little bit larger.

Overall, the training results are satisfactory. They not only demonstrate that the ANN model can accurately reflect the impact of design parameters on system performance, but also offer a system model with the ability of fast computation in the next self-learning process.

C. Self-Learning Based on DRL

In various DRL-based algorithms, DDPG can output continuous actions and performs well in high-dimensional action spaces, making it suitable for solving complex design problems with many continuous variables [31]. Therefore, it is

1) DDPG Algorithm: The process of self-learning of the agent is an iterative interaction of data between the agent and the environment. After well trained, the agent is capable of providing the optimal action fast to satisfy the design goal of the multiobjectives L, T_j, ΔT_j, and ρ. The design framework of the DDPG algorithm is shown in Fig. 10. The DDPG agent consists of four neural networks: online actor network μ, target actor network μ', online critic network Q, and target critic network Q'. First, the online networks are initialized randomly, while the target networks are initialized by replication as

$$\begin{cases} \theta^{Q'} \leftarrow \theta^{Q} \\ \theta^{\mu'} \leftarrow \theta^{\mu}. \end{cases} \tag{4}$$

Then, in each episode, the state is randomly set. At each step t in an episode, under the state $s_t = (I)_t$, the action $a_t = (d_1, d_2, d_3, d_4, h_1, h_2, h_3)_t$ is obtained by the actor network and noise $\mathcal{N}$. By adding noise, the algorithm can be guaranteed to explore effectively in the continuous action space. The specific process can be expressed as

$$a_t = \mu(s_t) + \mathcal{N}(\mu(s_t), \sigma). \tag{5}$$

According to the interaction of the MDP, the actor network μ of the agent gives the action a_t according to the state s_t, which is input into the power module system environment to obtain the reward r and the next state s_{t+1}.The states, actions, and rewards during the interaction will be transformed into a sequence (s_t, a_t, r, s_{t+1}) and stored in the experience replay pool. N sets of data are randomly selected according to the mini-batch sampling strategy to train the actor network.

The online critic network $Q^{\theta_Q}(s, a)$ approximates the action–

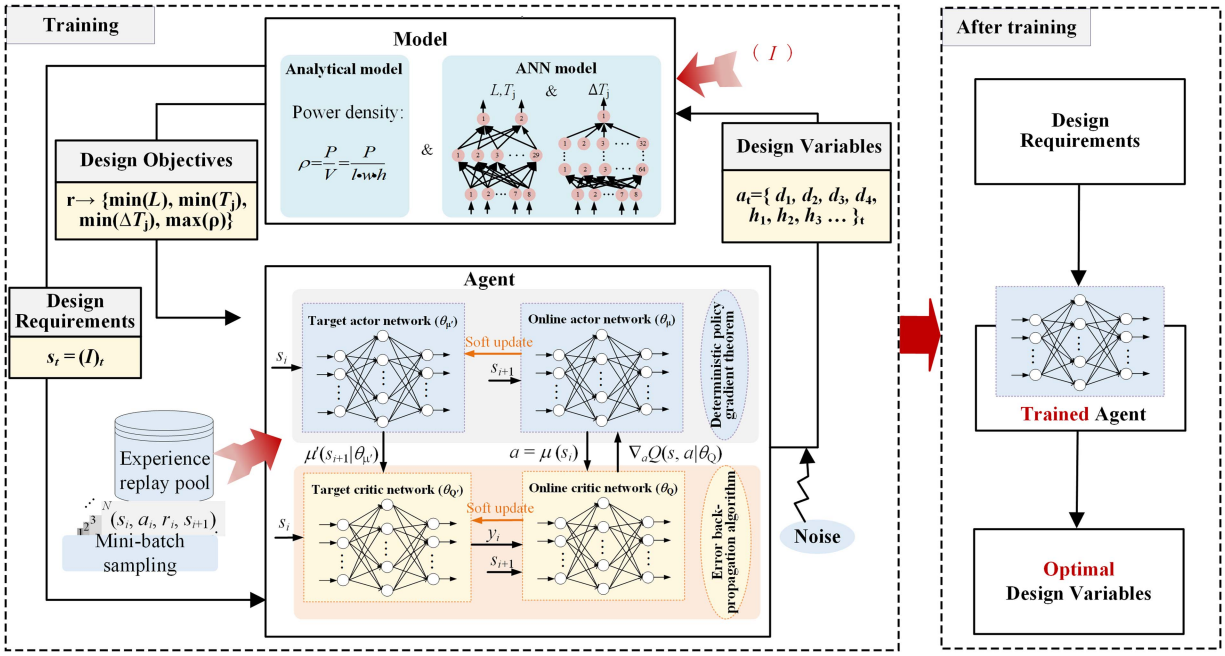

Fig. 10. Design framework of L, T_j, ΔT_j, and ρ based on the DDPG algorithm for the power module.

$Q^{\theta_Q}(s_t, a_t)$ is defined as follows:

$$Q^{\theta_Q}(s_t, a_t) = \mathbb{E}_{s_{t+1}}\left[r(s_t, a_t) + \gamma Q^{\theta_Q}(s_{t+1}, \mu_\theta(s_{t+1}))\right]. \tag{6}$$

The network parameters of the online critic network Q and the online actor network μ are updated by the error back-propagation algorithm and the deterministic strategy gradient theorem, respectively [32]. The error backpropagation algorithm and deterministic policy gradient are calculated as shown in the following equations:

$$y_t = r(s_t, a_t) + \gamma Q'(s_{t+1}, \mu'_\theta(s_{t+1}|\theta_{\mu'})|\theta_{Q'}) \tag{7}$$

$$L(\theta_Q) = \mathbb{E}_{\mu'_\theta}\left[\left(Q(s_t, a_t|\theta_Q) - y_t\right)^2\right] \tag{8}$$

$$\nabla_{\theta_\mu} J = \mathbb{E}_{\mu'_\theta}\left[\nabla_a Q(s, a|\theta_Q)|_{s=s_t, a=\mu_\theta(s_t)} \cdot \nabla_{\theta_\mu}\mu_\theta(s|\theta_\mu)|_{s=s_t}\right] \tag{9}$$

where y_t is the target score value jointly generated by the target actor network μ' and the target critic network Q', and L is the loss function. The standard-error-based backpropagation algorithm can obtain the gradient $\nabla_{\theta_Q} L$ of L with respect to θ_Q, which can be optimally updated for the parameter θ_Q. The actor network μ updates parameters θ_μ by maximizing the Q-value; $\mu_\theta(s|\theta_\mu)$ is the output of the online actor network μ.

The target actor network μ' and the target critic network Q' are updated by the soft update method [32], as shown in the following equation:

$$\text{soft update} \begin{cases} \theta^{Q'} \leftarrow \alpha\theta^{Q} + (1-\alpha)\theta^{Q'} \\ \theta^{\mu'} \leftarrow \alpha\theta^{\mu} + (1-\alpha)\theta^{\mu'} \end{cases} \tag{10}$$

where α denotes the update rate. $\theta^{Q'}$ and $\theta^{\mu'}$ are the updated target actor network μ' parameters and target evaluation network Q' parameters, respectively. Based on this, the updating speed of the target values can be restricted effectively, and the stability of the training procedure can be improved significantly.

After successful training, the trained actor network can promptly provide the optimal design parameters (d_1, d_2, d_3, d_4, h_1, h_2, h_3) for any input system requirement (I), achieving the design goals of L, T_j, ΔT_j, and ρ.

2) DDPG Algorithm Settings: The state space and action space are, respectively, set as the design requirements and variables, as mentioned in Section II. The reward function is defined as follows, in which the weight ratio of each objective is set as 1:1:1:1 in this case. The weight ratio can be adjusted according to different applications [33]

$$R = -w1 \cdot L\text{norm} - w2 \cdot T\text{norm} - w3 \cdot \Delta T\text{norm} - w4 \cdot (1 - \rho\text{norm}) \tag{11}$$

where Lnorm, Tjnorm, ΔTjnorm, and ρnorm represent the normalized parasitic inductance, junction temperatures, and power density, respectively, while w1, w2, w3, and w4 represent the weight of each term.

Furthermore, the algorithm hyperparameter is set, as shown in Table II. The actor network and the critic network of DDPG both contain a hidden layer of 128 neurons. The maximum training round is 1500, and the number of steps contained in each training round is 20. The learning rates of both the actor and critic networks are 0.0002 and 0.002, respectively, the capacity of the experience replay pool is 100 000, and the mini-batch sampling is 64.

3) Training Result of the DDPG Agent: The average rewards during the DDPG training process are depicted in Fig. 11. The reward remains very low in the exploring stage. This is because the agent takes random actions in the beginning, which cannot guarantee a high reward. As training goes, the agent accumulates

TABLE II
KEY PARAMETERS OF THE DDPG ALGORITHM

Variables	Range of value	Parameters	Value
d_1	[13, 21]	Learning rate of the actor network	0.0002
d_2	[14, 26]	Learning rate of the critic network	0.002
d_3	[9, 17]	Capacity of the experience replay pool	100 000
d_4	[14, 26]	Mini-batch sampling N	64
h_1	[0.3, 0.9]	/	/
h_2	[0.2, 1]	/	/
h_3	[2, 5]	/	/
Current	[200, 300]	/	/

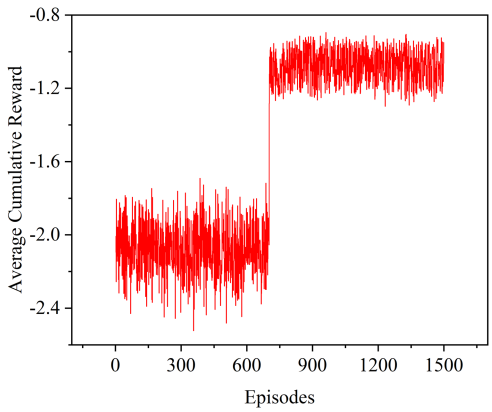

Fig. 11. Average cumulative reward during the training process of the DDPG algorithm.

experience and gives better actions for different states within the design goals. In this study, after around 700 episodes of self-learning, the reward soars to a very high value and remains high, which indicates that the learning process finishes successfully, and the agent has been well trained.

The larger fluctuations in the reward curve primarily arise from the diversity of state distributions. In our task, current level I (200–300 A) is encoded as the state, with each current level I corresponding to a distinct reward and a corresponding set of optimal packaging parameters. If the current level I drawn in adjacent episodes differs significantly, the reward will fluctuate, even if the policy network is stable. Overall, the curve stabilizes at a higher level, indicating that the policy has effectively converged, which means that the agent has been successfully learned.

IV. NUMERICAL VALIDATION OF THE PROPOSED METHOD

This section covers the validation of the calculation speed and optimization results of the proposed DRL method, which are compared with those of the BS and GA methods.

A. Traditional Optimization via BS and GA

BS explores all possible combinations of design variables with enough small searching steps and calculates the corresponding reward. In this article, a 0.1-mm step size is used to traverse all combinations of dimensional parameters within the design variable range. The models embedded in BS are the same as those in the DRL method. Thus, the errors from the modeling itself are identical to different search algorithms. Based on the models, the BS can be regarded as the benchmark for the comparison of the optimization ability and the calculation speed of DRL.

In the GA, combinations of design variables and their corresponding fitness function (set same as rewards) are treated as individuals, and the collection of individuals is called a population. The parent population generates offspring populations, with individuals having higher fitness values surviving in the combined population to form a new parent population, while others are eliminated [34]. The number of times the GA model is invoked is set to be the same as DRL. By selecting individuals with the highest fitness values, the corresponding design variables are obtained. The maximum reward and corresponding design variables in the last episode are defined as the outcome of the GA.

B. Comparison of Computation Speed

In this article, two modeling methods—simulation method (SM) and ANN—and three optimization algorithms—BS, GA, and DRL—are discussed. Thus, there are six combinations, and their overall runtimes (including data gathering and networks training) are obtained respectively. Regarding the time of the algorithms embedding the SM, only principled calculation is performed because it is not feasible to run massive numerical simulations. For the others, the time is obtained by running the program.

First, the runtime of the SM combined with three algorithms is calculated in principle just for comparison. The single thermal and inductance simulations take 103 and 30 s, respectively, and the SM-BS and SM-GA methods based on the simulation model require 3 449 628 and 40 000 simulation iterations, respectively, resulting in a single runtime of 458 800 524 s for $T_{\mathrm{SM,BS\_it}}$ and 5 320 000 s for $T_{\mathrm{SM,GA\_it}}$, respectively. In addition, the SM-DRL method based on the simulation model is divided into two parts, training and response, with 30 000 iterations of simulation in the training phase, which consumes 3 990 000 s for $T_{\mathrm{SM,DRL\_tra}}$, while the response phase consumes 0.1 ms for $T_{\mathrm{SM,DRL\_res}}$, which is negligible.

The runtime of the aforementioned three simulation-model-based optimization design methods is summarized in Table III.

When the number of design requirements N_{req} is greater than 1, the computation time of SM-BS and SM-GA will increase exponentially with the number of design requirements. The running times of SM-BS, SM-GA, and SM-DRL methods are defined as follows:

$$T_{\mathrm{SM,BS}} = N_{\mathrm{req}} \cdot T_{\mathrm{SM,BS\_it}} \tag{12}$$

$$T_{\mathrm{SM,GA}} = N\mathrm{req} \cdot T_{\mathrm{SM,GA\_it}} \tag{13}$$

TABLE III
RUNTIME COMPARISON OF SIMULATION-MODEL-BASED METHODS: SM-BS, SM-GA, AND SM-DRL

Step	Time（s）
$T_{\mathrm{SM,BS\_it}}$	458 800 524
$T_{\mathrm{SM,GA\_it}}$	5 320 000
$T_{\mathrm{SM,DRL\_tra}}$	3 990 000
$T_{\mathrm{SM,DRL\_res}}$	0.1×10^{-3}

TABLE IV
RUNTIME OF EACH STEP IN THE MODELING AND OPTIMIZATION PROCESS FOR ANN-BASED METHODS: ANN-BS, ANN-GA, AND ANN-DRL

Step	Time（s）
$T_{\mathrm{ANN,tra}}$	436 000
$T_{\mathrm{ANN,BS\_it}}$	10 857
$T_{\mathrm{ANN,GA\_it}}$	812
$T_{\mathrm{ANN,DRL\_tra}}$	774
$T_{\mathrm{ANN,DRL\_res}}$	0.1×10^{-3}

$$T_{\mathrm{SM,DRL}} = T_{\mathrm{SM,DRL\_tra}} + N_{\mathrm{req}} \cdot T_{\mathrm{SM,DRL\_res}}. \tag{14}$$

It can be seen that the DRL algorithm is the fastest one for the optimization and can immediately respond with a new design when given a new requirement. However, it is obvious that if the finite simulations are really performed for this case, even if the fastest DRL algorithm is performed, 1108 h, namely, 3 990 000 s, are required, which is a quite long time for design.

Then, the ANN-based models are utilized to replace the simulation-based models. Still, the three optimization algorithms are combined with the ANN models, which are named as ANN-BS, ANN-GA, and ANN-DRL. The time required for the ANN training process, $T_{\mathrm{ANN,tra}}$, mainly consists of the time consumed to collect 4000 COMSOL thermal simulations and 800 Q3D inductance simulations, which totals 436 000 s. In addition, the ANN-BS and ANN-GA single optimization runtimes, $T_{\mathrm{ANN,BS\_it}}$ and $T_{\mathrm{ANN,GA\_it}}$, are 10857 and 812 s, respectively; the training time $T_{\mathrm{ANN,\ DRL\_tra}}$ for the DRL optimization phase in the ANN-DRL method is 774 s, and the response time $T_{\mathrm{ANN,DRL\_res}}$ is negligible.

Table IV summarizes the runtime of each step involved in the modeling and optimization processes for the three ANN-based design methods, providing a comprehensive comparison of their computational efficiency.

When the number of design requirements, N_{req}, is greater than 1, the optimization algorithm runtime for ANN-BS and ANN-GA will increase exponentially with the number of design requirements. The runtime for the ANN-BS, ANN-GA, and ANN-DRL methods is defined as follows:

$$T_{\mathrm{ANN,BS}} = T_{\mathrm{ANN\_tra}} + N_{\mathrm{req}} \cdot T_{\mathrm{ANN,BS\_it}} \tag{15}$$

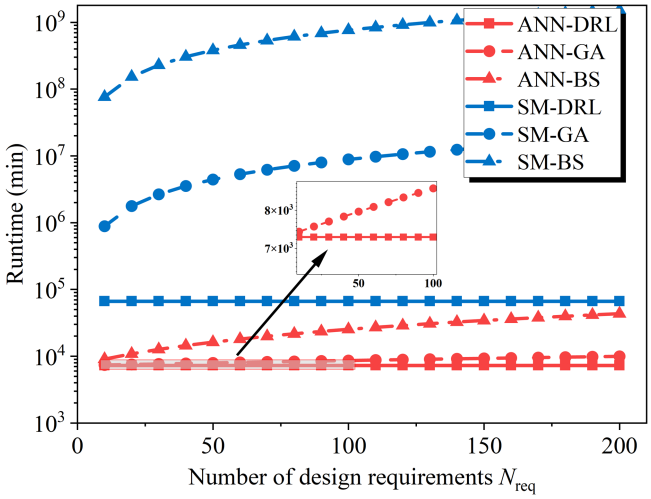

Fig. 12. Runtime of six modeling–optimization combinations.

$$T_{\mathrm{ANN,GA}} = T_{\mathrm{ANN\_tra}} + N\mathrm{req} \cdot T_{\mathrm{ANN,GA\_it}} \tag{16}$$

$$T_{\mathrm{ANN,DRL}} = T_{\mathrm{ANN\_tra}} + T_{\mathrm{ANN,DRL\_tra}} + N\mathrm{req} \cdot T_{\mathrm{ANN,DRL\_res}}. \tag{17}$$

The dependence of N_{req} on runtime is depicted in Fig. 12. For both modeling methods, the ANN is significantly faster than the SM because it requires only a few simulations to gather data, which reduce the need for numerous iterative simulations. For the three algorithms, when N_{req} increases, the runtime of BS and GA grows proportionally, while DRL almost holds the line. This is because $T_{\mathrm{DRL\_res}} \approx 0.1$ ms and can almost be ignored. Regarding the preparation of DRL training, if $N_{\mathrm{req}} \leq 10$, the runtimes of GA and DRL are comparative. However, as N_{req} increases, as more design requirements are given, the proposed ANN-DRL combination is much faster than the GA due to the absence of the need to run the search program again.

C. Comparison of Optimization Results

Using the optimization results obtained from ANN-BS as a benchmark, the optimization results based on ANN-DRL can be compared to prove the optimization ability of the proposed method. Table V presents the design variable values optimized by ANN-DRL and ANN-BS under different current design requirements, with the weight ratios w_1:w_2:w_3:w_4 set to 1:1:1:1. The definition of weight w_1, w_2, w_3, and w_4 is given in (11). The current specifications are 200, 220, 240, 260, 280, and 300 A. It should be noted that these current values do not refer to the actual operating current of the module, but rather to the designed rated current of the power module. It can be observed that the optimization results of the two algorithms are almost identical. In practice, the performance requirements for power modules vary across different applications. Different weight ratios can be set according to the priority of objectives, allowing for a balanced multiobjective design of power modules. Table VI shows the design variable values optimized by the ANN-DRL and ANN-BS under different weight ratios when the current is 300 A. Similarly, it can be observed that the optimization

TABLE V
COMPARISON OF OPTIMIZATION RESULTS BETWEEN BS AND DRL METHODS UNDER DIFFERENT DESIGN REQUIREMENTS

Current I (A)		d_1(mm)	d_2 (mm)	d_3 (mm)	d_4 (mm)	h_1 (mm)	h_2 (mm)	h_3 (mm)
200	ANN-BS	13.0	14.0	9.0	18.7	0.1	0.38	2.0
	ANN-DRL	13.0	14.0	9.0	18.7	0.1	0.38	2.0
	Error	0	0	0	0	0	0	0
220	ANN-BS	13.0	14.0	9.0	19.9	0.1	0.38	2.0
	ANN-DRL	13.0	14.0	9.0	19.3	0.1	0.38	2.0
	Error	0	0	0	3.0%	0	0	0
240	ANN-BS	13.0	14.0	12.7	26	0.3	0.38	2.0
	ANN-DRL	13.0	14.0	12.5	26	0.3	0.38	2.0
	Error	0	0	1.6%	0	0	0	0
260	ANN-BS	13.0	14.0	13.1	26	0.3	0.38	2.0
	ANN-DRL	13.0	14.0	12.8	26	0.3	0.38	2.0
	Error	0	0	2.2%	0	0	0	0
280	ANN-BS	13.0	14.0	12.9	26	0.3	0.38	2.0
	ANN-DRL	13.0	14.0	13	26	0.3	0.38	2.0
	Error	0	0	0.7%	0	0	0	0
300	ANN-BS	13.0	18.0	12.8	26	0.5	1.0	2.0
	ANN-DRL	13.0	18.0	12.5	26	0.5	1.0	2.0
	Error	0	0	2.3%	0	0	0	0

TABLE VI
COMPARISON OF OPTIMIZATION RESULTS BETWEEN BS AND DRL METHODS UNDER DIFFERENT WEIGHT RATIOS

w_1:w_2:w_3:w_4		Optimum size parameters (mm)						
		d_1	d_2	d_3	d_4	h_1	h_2	h_3
1:1:1:1	ANN-BS	13.0	18.0	12.5	26	0.5	1.0	2.0
	ANN-DRL	13.0	18.0	12.8	26	0.5	1.0	2.0
	Error	0	0	2.4%	0	0	0	0
2:1:1:1	ANN-BS	13.0	14.3	12.7	26	0.5	1.0	2.0
	ANN-DRL	13.0	14.0	12.5	26	0.5	1.0	2.0
	Error	0	2.1%	1.6%	0	0	0	0
1:2:1:1	ANN-BS	20.7	26.0	14.9	26.0	0.5	1.0	2.0
	ANN-DRL	21.0	26.0	15.0	26.0	0.5	1.0	2.0
	Error	1.4%	0	0.7%	0	0	0	0
1:1:2:1	ANN-BS	13.0	19.2	12.5	26.0	0.5	1.0	2.0
	ANN-DRL	13.0	19.2	12.4	26.0	0.5	1.0	2.0
	Error	0	0	0.8%	0	0	0	0
1:1:1:2	ANN-BS	13.0	14.0	9.0	15.5	0.1	0.38	2.0
	ANN-DRL	13.0	14.0	9.0	15.3	0.1	0.38	2.0
	Error	0	0	0	1.3%	0	0	0

results of both algorithms are almost identical. In summary, the outcome of ANN-DRL can closely track the reliable outcomes of BS without its computational burden.

Furthermore, Fig. 13 presents the normalized values of parasitic inductance, junction temperature, temperature difference, and power density under a fixed input current requirement of 300 A, corresponding to various weight ratios. For intuitive comparison, all values in the figure are normalized. For example, when the weight ratio is set to 2:1:1:1, the parasitic inductance of the power module is the most important objective to reduce compared with the others during optimization. As shown, the simulated parasitic inductance under this configuration is the lowest among all compared cases. Similarly, when the weight ratio is 1:2:1:1, the focus shifts to minimizing the junction temperature,

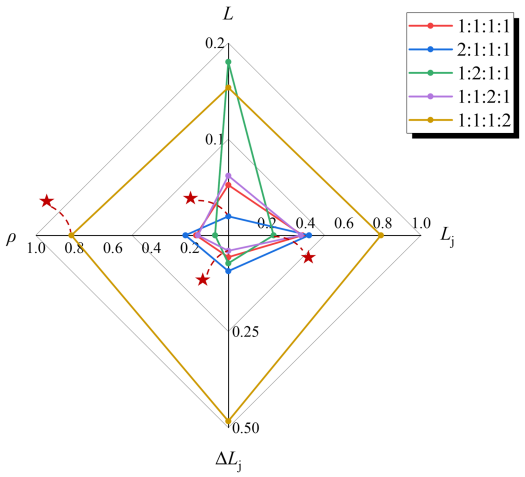

Fig. 13. Comparison of optimized results of multiobjective performance of power modules under different weight ratios.

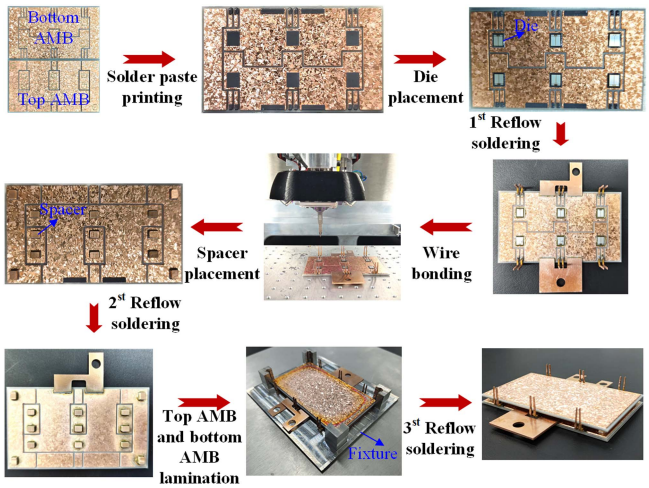

Fig. 14. Fabrication process of the optimized DSC power module.

TABLE VII
BILL OF MATERIALS FOR THE DESIGNED POWER MODULE

Part	Material	Specification
Bare Die	WM2HB016120B	1200 V,134 A
Substrate	AlN AMB	0.1 mm Cu; 0.38 mm Ceramic; 0.38 mm Cu
Wire Bonding	Al	8 mil
Solder	SAC305 and SP95	Thickness:100 μm
Terminal	Cu	DC Terminal Thickness: 0.5 mm DC Terminal Thickness: 1 mm
Spacer	Mo alloy	Molybdenum surface

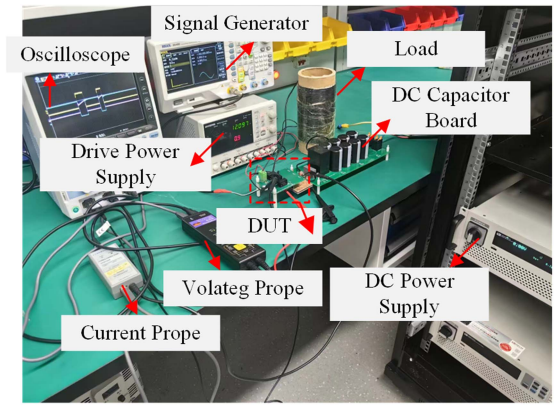

Fig. 15. Platform of DPT test.

and the corresponding result confirms that the junction temperature reaches its lowest value under this setting. The variations in the other optimization metrics under different weight ratios consistently align with the respective optimization objectives. This further demonstrates the effectiveness and adaptability of the proposed method in addressing MOO challenges in power module design.

V. EXPERIMENTAL VALIDATION OF THE POWER MODULE

Section IV proves the MOO ability of the proposed DRL and shows its obvious advantage on the short computation time. In this section, the modules designed based on DRL are fabricated, and the accuracy of the computation is verified through experimental tests. Based on relevant commercial products and common converter requirements, the optimization results corresponding to a 300-A current, as shown in Table V, were used as design variables for module manufacturing.

A. Fabrication of the Designed Power Module

Table VII summarizes the materials for the prototype of the designed power module. Fig. 14 illustrates the assembly process of the power module. First, the chip, positive terminal, ac terminal, and drive terminal are connected to the lower DBC substrate through the first reflow soldering process. Next, an 8-mil aluminum wire is bonded to the chip gate, Kelvin source, and corresponding substrate traces using a bonding machine. Then, the spacer and negative terminal are connected to the upper substrate via the second reflow soldering process. Finally, the upper and lower substrates are aligned and positioned using a fixture, and the electrical interconnection between the two substrates is completed through the third reflow soldering process.

B. Electrical and Thermal Characteristic Tests

1) Electrical Characteristics: The double-pulse test (DPT) platform is established in Fig. 15. The low bridge is taken as for the measurement. The gate and Kelvin source of the high bridge are directly shorted to turn OFF the MOSFETs. The driver board is given with a drive signal by a signal generator and can thus output a drive voltage of 15 V–3.5 V. The driver board is directly plugged into the drive terminals of the lower phase of the module to minimize the length of the drive loop. A passive probe is used to measure V_{gs}, while a voltage differential probe is clamped between the ac terminal and the negative terminal to measure

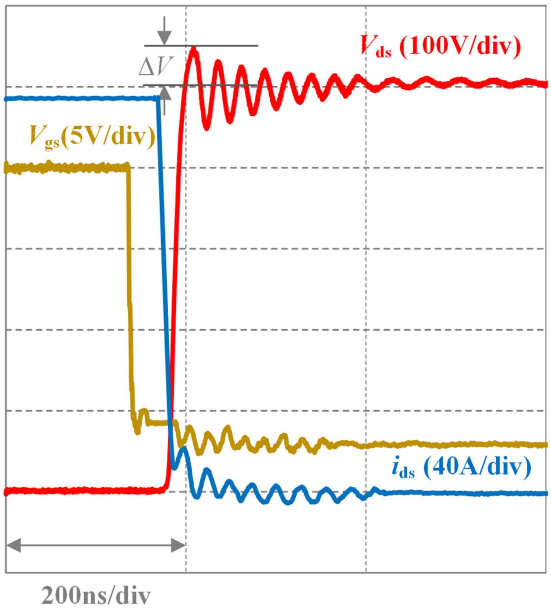

Fig. 16. Turn-OFF switching waveform of DPT.

V_{ds} of the lower phase. A Rogowski coil is wrapped around the dc terminal to measure the current i_{ds} in the lower bridge arm. The waveforms are captured by a Yokogawa oscilloscope with 500-MHz bandwidth. The dc-side voltage is provided by a dc source, and the driver board is powered by an adjustable switching power supply.

The parasitic inductance of the power module can be obtained by measuring the voltage spike during the turn-OFF transient and the corresponding rate of current change. The calculation formula is shown in (18), where ΔV is the voltage spike caused by the parasitic inductance, di/dt is the current fall rate, and L_{loop} is the parasitic inductance of the entire test circuit

$$L_{loop} = \frac{\Delta V}{di/dt}. \tag{18}$$

When the dc-side voltage is 500 V, the measured turn-OFF transient waveform is shown in Fig. 16. The measured overvoltage at this time is 45 V, and the maximum rate of current change is 6.92 A/ns. Therefore, the parasitic inductance of the entire module loop is calculated to be 6.5 nH.

For the same structural dimensions, the simulated parasitic inductance of the module is 5.7 nH. The difference between the test value and the simulation result is 0.8 nH. This discrepancy is primarily due to the fact that the simulation result represents the ideal value, only including the parasitic inductance of the module itself. However, during the experiment, the probe is clamped to the screw connected to the terminal to facilitate the measurement of v_{ds}. This caused the measured loop parasitic inductance to include not only the module's parasitic inductance but also the equivalent parasitic inductance of part of the screw. In addition, parasitic effects from the testing probes and connecting wires during the experiment can also introduce unnecessary parasitic inductance. Overall, since the base value of the parasitic inductance is relatively small and considering the aforementioned error sources, this discrepancy is deemed to be within a reasonable range.

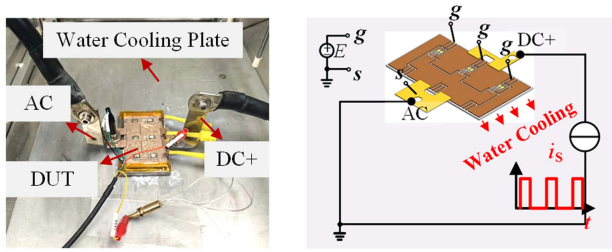

Fig. 17. Platform of the thermal test. (a) Test platform. (b) Circuit diagram of the test.

Fig. 18. Infrared thermometry test result.

2) Thermal Characteristics: The thermal characteristic test platform is shown in Fig. 17(a). The designed power module is mounted onto a water-cooling platform using thermal grease. Due to the symmetrical layout of the upper and lower phase legs, only the temperature distribution of the upper phase-leg chips needs to be measured. To directly measure the internal chip temperature, the source pad and upper substrate are removed. The source of the upper phase-leg chips is wire-bonded directly to the lower phase leg to achieve electrical interconnection. For more accurate testing by the thermal camera, black paint is evenly applied to the module under test before the measurement. The schematic of the test setup is shown in Fig. 17(b). A 15-V gate drive voltage is applied to the upper phase-leg device to keep it in the ON-state. A square-wave current excitation i_s is applied between the positive terminal and the ac terminal, causing the chips to generate heat. At an input current amplitude of 160 A and a water flow rate of 5 L/min, the internal temperature of the module is measured using an FLIR T650sc thermal imaging camera. Furthermore, the analysis software FLIR Tools, provided with the thermal imaging system, is used to calculate the maximum and average temperatures of the chip. The test results are shown in Fig. 18, where Bx1–3 represent the positions of the chip. As seen in the figure, the

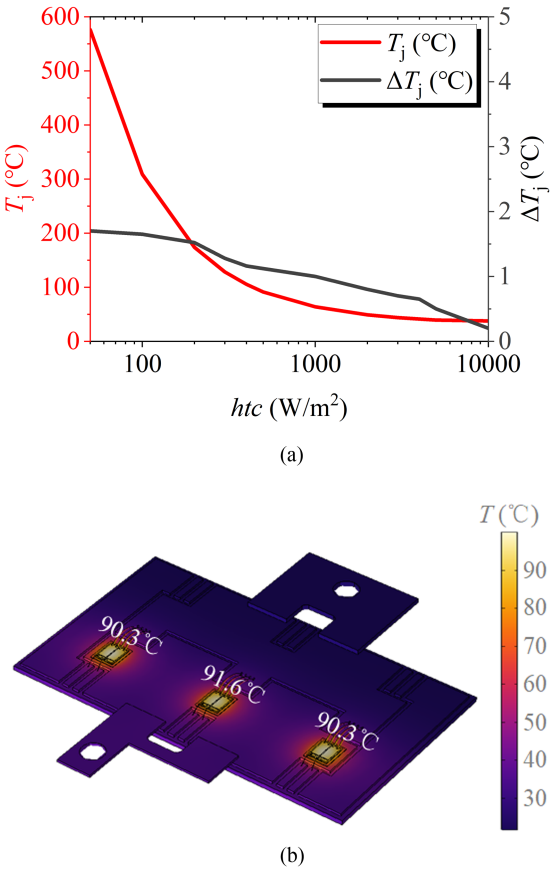

Fig. 19. Thermal characteristic simulation comparison. (a) Temperature difference distribution under different heat transfer coefficients. (b) Temperature distribution contour plot under a specific heat transfer coefficient.

temperature difference between the maximum and average temperatures of the chip is less than 1.5 °C, indicating good thermal uniformity.

To simulate the experimental testing, a half-bridge power module model without the upper substrate is established in COMSOL. The negative terminal of the module is grounded, and a current of 160 A is applied to the positive terminal. In the simulation environment, the heat dissipation via water cooling is modeled by setting the thermal conductivity coefficient on the lower substrate. However, the equivalent heat transfer coefficient in experimental testing is difficult to obtain accurately, making it challenging to truly simulate the cooling conditions. According to [35], the heat transfer coefficient for water cooling generally ranges from 500 to 10000 W/(m^2·K). Therefore, parametric simulation analysis is conducted within this range of heat transfer coefficients to obtain the maximum chip temperature and temperature difference under different coefficients, as shown in Fig. 19(a). It can be observed that the temperature difference between the module chips is relatively small in this structure, remaining below 2 °C across a wide range of heat transfer coefficients. Fig. 19(b) presents the temperature distribution contour plot obtained from the simulation when the module's absolute temperature is close to the experimental testing temperature. It

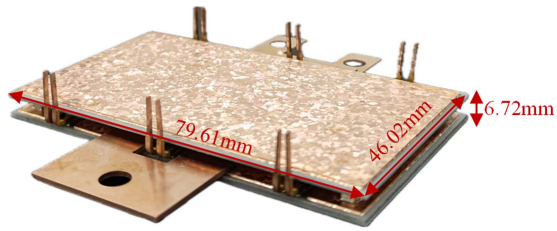

Fig. 20. Dimensions of the fabricated power module.

TABLE VIII
COMPARISON OF THE DESIGNED AND FABRICATED POWER MODULE

Parameter	Designed	Fabricated	Error
l (mm)	79.6	79.61	0.01
w (mm)	46.0	46.02	0.02
h (mm)	6.48	6.72	0.24

visually shows that the simulated relative temperature difference in the module remains below 1.5 °C.

C. Power Density

The physical dimensions of the fabricated power module are shown in Fig. 20 and summarized in Table VIII. The module length, width, and height are measured using vernier calipers, which are 79.61, 46.02, and 6.72 mm, respectively. The overall height error of the module after assembly is relatively large. This is due to the presence of three solder layers between the upper and lower substrates: between the chip and the lower substrate, between the chip and the spacer, and between the spacer and the upper substrate. During the actual assembly process, a degree of inevitable error is presented in both the printed thickness of the solder paste and the thickness after soldering. These errors accumulate in the height direction, leading to a relatively large difference between the assembled height of the module and the designed height.

VI. CONCLUSION

This article proposes a novel multiobjective automated design method for the packaging of power modules based on machine learning, combining ANNs and DRL, which can significantly improve the design efficiency of power modules. The use of the ANN facilitates the rapid establishment of complex nonlinear dependence of design objectives on design variables, thereby reducing reliance on lengthy iterative numerical simulations. Meanwhile, DRL enables intelligent exploration of the design space, allowing for the quick identification of optimal design variables under varying input conditions. Validation through a case study involving a 1200-V/300-A DSC power module demonstrates the method's effectiveness. Comparisons with traditional optimization methods BS and GA indicate that the proposed method can substantially reduce the optimization time. Furthermore, using the ANN-BS method as a benchmark, the optimization results across various design requirements and weight

ratios showed a high degree of consistency with benchmark results, which can affirm the optimization ability of the proposed method. Under the weight ratio of 1:1:1:1, the module structure was optimized and assembled. The experimental results show that the parasitic inductance of the module is 6.5 nH, the temperature difference is less than 1.5 °C, and the power density is 16.27 W/mm^3, which closely aligns with the simulation results. This further validates the accuracy of the modeling. The aim of this article is to present the basic principle of the proposed artificial intelligent design method for the packaging of power modules; thus, simplifications have been made in the design variables and objectives. The proposed approach can be further extended to more complicated designs, but it comes with some caveats. These include modifications to specific algorithms when employing more sophisticated models and additional training data if necessary. In the future, detailed explanations and demonstrations of these aspects will be provided in the forthcoming publications.

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