Analysis and Design of Freewheeling Current Commutating Methods to Low Voltage-Rated Diode

Ji-Yeon Kim, Dae-Hun Kwon, Jae-Hoon Sim, Seok-Woo Jeong, and Jae-Kuk Kim, *Member, IEEE*

***Abstract*—A center-tapped rectifier is widely employed in applications requiring low output voltage and high output current. However, the rectifier diodes experience high voltage stresses, resulting in high conduction losses. To solve this problem, a low voltage-rated freewheeling diode was adopted in previous studies. It improves the overall efficiency by commutating the freewheeling current in the secondary side to the low voltage-rated diode instead of the high voltage-rated diodes. However, the detailed commutation process was not thoroughly explained in the previous studies. Actually, only a small portion of the total freewheeling current flows through a low voltage-rated diode, and most of it still flows through the high voltage-rated diodes, leading to slight improvement in efficiency. Therefore, this article offers the operation principle during the freewheeling interval in detail. Furthermore, it presents two simple methods for increasing the freewheeling current commutated to the low voltage-rated diode. These methods also reduce the circulating current in the primary side, resulting in low overall conduction losses. The article also explains the features and design considerations of each method and topological extensions for other types of rectifiers. Finally, a 250-W prototype is implemented, achieving a 94.8% peak efficiency.**

***Index Terms*—Center-tapped rectifier (CTR), freewheeling diode, low conduction loss, low voltage stress, phase-shift full-bridge (PSFB) converter.**

I. Introduction

DC/DC converters with low output voltage and high output current are required in numerous applications, such as electric vehicles and server power supplies [1], [2]. In the secondary side of these converters, a center-tapped rectifier (CTR) is commonly employed because it has low conduction losses due to the small number of conducting components, as illustrated in Fig. 1(a) [3], [4]. The diodes are generally used in rectifier to minimize the control complexity and cost of the system. However, the diodes in the CTR suffer from high voltage stresses—twice the reflected input voltage, i.e., $2V_S/n$—, where V_S and n represent the input voltage and turns ratio of transformer, respectively. Consequently, high voltage-rated diodes with a high forward voltage drop V_F are inevitably used, and the total freewheeling current in the secondary side flows through high voltage-rated diodes.

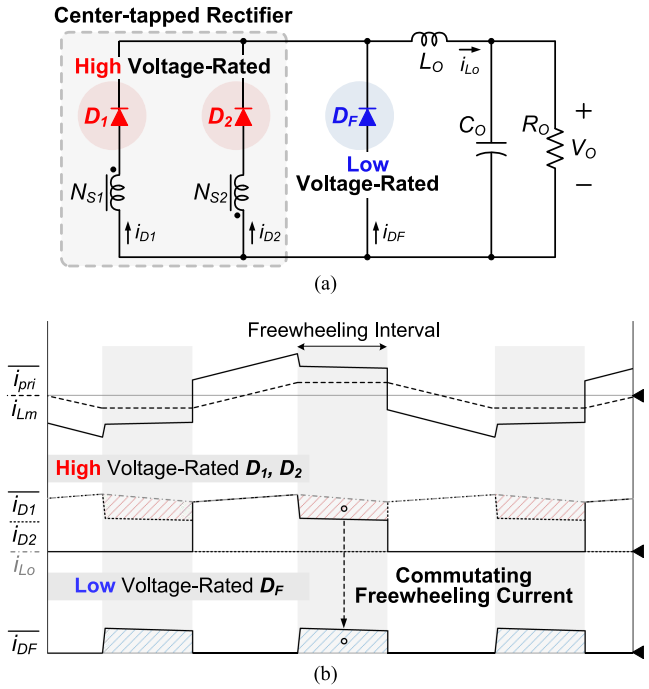

Fig. 1. Center-tapped rectifier (CTR) with D_F [12], [13], [14]. (a) Circuit diagram. (b) Key waveforms.

To reduce conduction losses, various rectifiers with low voltage-rated components have also been studied [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. In [5], a rectifier with a low voltage charging technique was proposed. Since the two capacitors were alternatively charged, voltage stresses on the rectifier components were reduced. However, this technique required additional active switches, increasing the number of conducting components. In [6], a hybrid dual full-bridge converter was proposed. Due to the hybrid connection of secondary diodes, the output current ripple and voltage stresses on rectifier diodes were mitigated, but eight switches and two transformers were required. In [7], [8], and [9], rectifiers employing coupled inductors and low voltage-rated components were described. However, in [7], two additional diodes and capacitors were demanded. In [8], although the voltage stresses on specific diodes were reduced, other diodes experienced higher voltage stresses compared to the conventional phase-shift full-bridge

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(PSFB) converter. Furthermore, the rectifiers in [7], [8], and [9] required a complex magnetic design process due to the coupled inductors. In [10], a two-transformer PSFB converter with a low voltage-rated diode was discussed, but two-transformer were inevitably used, resulting in low power density. In [11], a voltage Doubler rectifier was discussed, in which the voltages across the secondary diodes were clamped to the output voltage. For this configuration, the output inductor was eliminated, which affected the secondary root-mean-square (RMS) and peak currents. Consequently, the rectifiers in [5], [6], [7], [8], [9], [10], and [11] had some limitations: a larger number of active switches and magnetic components, a complex design process, and high secondary RMS and peak currents. In [12], [13], and [14], an additional diode D_F was employed to make a freewheeling path for the output inductor current without modification of the conventional CTR configuration. Since the diode D_F had a low voltage stress—half the voltage stresses on the diodes in the CTR, i.e., V_S/n—with a low V_F, the conduction losses in the rectifier diodes were reduced. Fig. 1 illustrates the circuit diagram and key waveforms of CTR with D_F. The freewheeling current in the secondary side is commutated to D_F instead of the high voltage-rated diodes, as depicted in Fig. 1(b). Thus, the overall efficiency is improved simply and effectively without any additional active switches, magnetic components, and an increase in the secondary RMS or peak current.

The effect of D_F was briefly described in [12], [13], and [14]; however, these studies mainly focused on snubber circuits proposed in each paper rather than on the effects of D_F. Thus, the detailed commutation process, the magnitude of the freewheeling current commutated to D_F, i.e., i_{DF}, and the impact of i_{DF} on the entire system were not comprehensively addressed in [12], [13], and[14]. Actually, when D_F is adopted alone, only a small portion of the total freewheeling current flows through D_F, and most of it still flows through the high voltage-rated diodes. Thus, the addition of D_F alone cannot have a significant impact on overall efficiency. This article provides the following contributions, which have not been offered in [12], [13], and [14].

1) The detailed operation principle during the freewheeling interval is provided in Section II.
2) Two simple methods for reducing circulating current and increasing i_{DF} are analyzed in Section III: using primary capacitor C_P and secondary capacitor C_S.
3) The advantages and disadvantages of each method are compared and design guidelines for C_P and C_S are provided in Section IV.
4) Topological extensions adopting D_F for other types of rectifiers are proposed in Section V: full-bridge and current Doubler rectifiers.

Experiments are conducted with a 250-W prototype to verify the effect of D_F and i_{DF} according to C_P or C_S in Section VI.

II. Operation Principle

In this article, the PSFB converter is applied with the CTR. Figs. 2 and 3 illustrate the topological states and key waveforms of the PSFB converter using CTR with D_F, respectively. The following assumptions are made as follows:

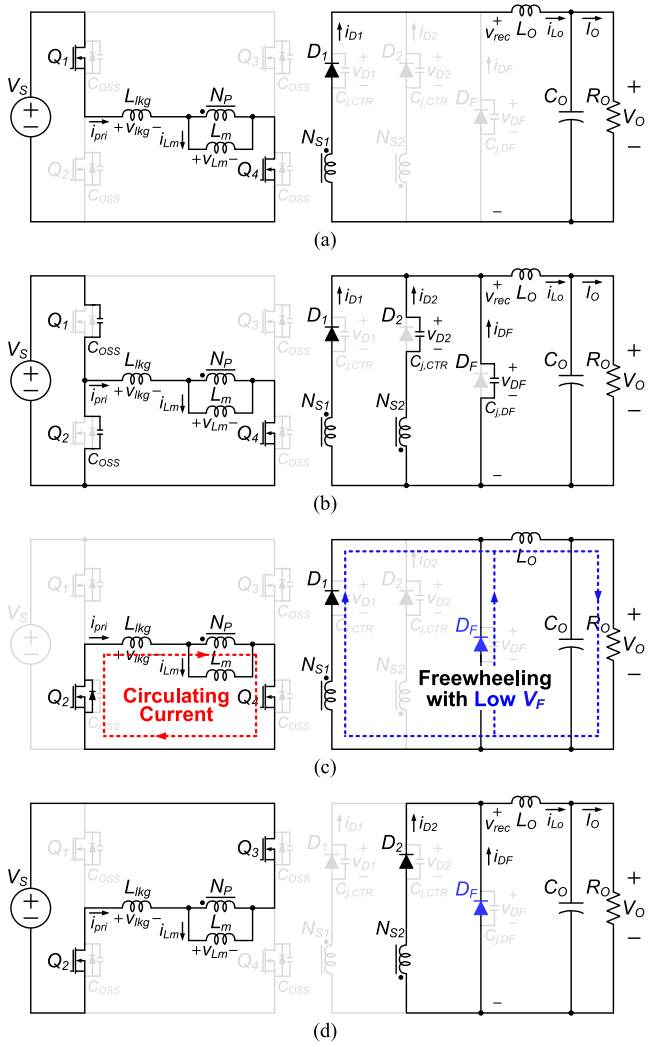

Fig. 2. Topological states of PSFB converter with D_F. (a) Mode 1 [t_0–t_1]. (b) Mode 2 [t_1–t_2]. (c) Mode 3 [t_2–t_3]. (d) Mode 4 [t_3–t_4].

1) All parasitic components not depicted in Fig. 2 and the secondary voltage oscillations resulting from parasitic components are ignored.
2) The transformer has a turns ratio n defined by $n = N_P/N_S$, where $N_S = N_{S1} = N_{S2}$.
3) Since the secondary diodes D_1 and D_2 are identical, they have the same forward voltage drop $V_{F,CTR}$ and junction capacitance $C_{j,CTR}$; $V_{F,\mathrm{CTR}} = V_{F,D1} = V_{F,D2}$ and $C_{j,CTR} = C_{j,D1} = C_{j,D2}$.
4) The forward voltage drop of D_F, i.e., $V_{F,DF}$, is smaller than those of D_1 and D_2 since the lower voltage-rated diode generally has a lower forward voltage drop [15]; $V_{F,DF} < V_{F,CTR}$.
5) The output voltage ripple is omitted because the output capacitor C_O is sufficiently large.

***Mode 1* [t_0 – t_1]:** Mode 1 begins when i_{DF} reaches zero. During this mode, the converter operates as a conventional PSFB converter. The switches Q_1 and Q_4 are conducted, and magnetizing current i_{Lm} increases because V_S is applied to magnetizing inductor L_m. The power is transferred to the output through D_1, as illustrated in Fig. 2(a). Since V_S/n is

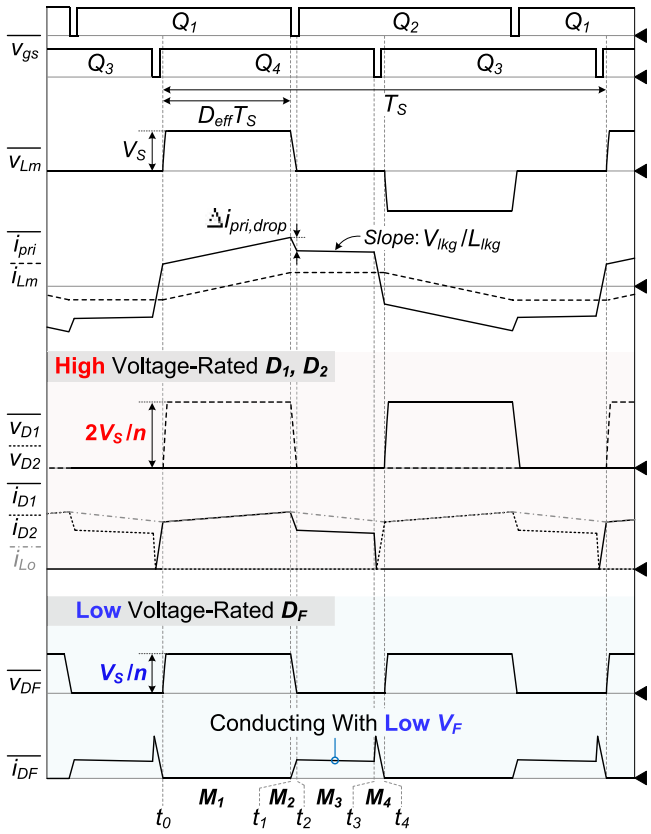

Fig. 3. Key waveforms of PSFB converter with D_F.

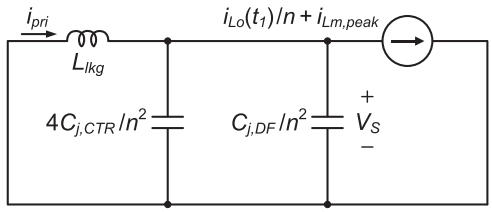

Fig. 4. Equivalent circuit when $C_{\rm OSS}$ is fully discharged during mode 2.

applied to the rectified voltage on the secondary side, i.e., v_{rec}, the voltages across D_2 and D_F are $2V_S/n$ and V_S/n, respectively. Therefore, the lower voltage-rated diode with a low V_F can be adopted for D_F compared to D_2, resulting in low conduction losses.

***Mode 2* [t_1 – t_2]:** After Q_1 is turned OFF at t_1 , the primary current $i_{\rm pri}$ discharges both output capacitors of the leading-leg switches, i.e., $C_{\rm OSS}$, and the junction capacitors of D_2 and D_F, i.e., $C_{j,\rm CTR}$ and $C_{j,\rm DF}$, simultaneously, as illustrated in Fig. 2(b). Assuming that $C_{\rm OSS}$ is discharged much faster than $C_{j,\rm CTR}$ and $C_{j,\rm DF}$, the equivalent circuit after $C_{\rm OSS}$ has been fully discharged is illustrated in Fig. 4. Since the voltage across $C_{j,\rm DF}$ is reflected to leakage inductor L_{lkg}, $i_{\rm pri}$ is reduced until t_2, as shown in Fig. 3. Thus, after C_{OSS} is discharged, $i_{\rm pri}$ and $v_{\rm DF}$ are as follows:

$$i_{\rm pri}(t) = \frac{i_{Lo}(t_1)}{n} + i_{Lm,\rm peak} - V_S\sqrt{\frac{4C_{j,\rm CTR}+C_{j,\rm DF}}{n^2 L_{\rm lkg}}}\sin(\omega(t-t_1)) \quad (1)$$

$$v_{\rm DF}(t) = \frac{V_S}{n}\cos(\omega(t-t_1)) \quad (2)$$

where i_{Lo} is the output inductor current and $\omega = 1/[L_{\rm lkg}(4C_{j,\rm CTR} + C_{j,\rm DF})]^{1/2}$. $i_{Lm,\rm peak}$ represents the peak magnetizing current where $i_{Lm,\rm peak} = V_S D_{\rm eff}\, T_S/(2L_m)$. Based on (2), $v_{\rm DF}$ decreases from V_S/n to zero because $C_{j,CTR}$ and $C_{j,\rm DF}$ are discharged. Therefore, t_2 when $C_{j,\rm CTR}$ and $C_{j,\rm DF}$ are fully discharged is as follows:

$$t_2 = \left(t_1 + \frac{\pi}{2}\right)\frac{1}{\omega}. \quad (3)$$

From (1) and (3), $i_{\rm pri}$ at t_2 is as follows:

$$i_{\rm pri}(t_2) = \frac{i_{Lo}(t_1)}{n} + i_{Lm,\rm peak} - V_S\sqrt{\frac{4C_{j,\rm CTR}+C_{j,\rm DF}}{n^2 L_{\rm lkg}}}. \quad (4)$$

Hence, a reduction in primary current from $i_{\rm pri}(t_1)$ to $i_{\rm pri}(t_2)$, i.e., $\Delta i_{\rm pri,drop}$, is derived as follows:

$$\Delta i_{\rm pri,drop} = V_S\sqrt{\frac{4C_{j,\rm CTR}+C_{j,\rm DF}}{n^2 L_{\rm lkg}}}. \quad (5)$$

Since the difference between $i_{\rm pri}$ and i_{Lm} is reflected to i_{D1}, $i_{\rm DF}$ is as follows:

$$i_{\rm DF}(t) = i_{Lo}(t) - i_{D1}(t) = i_{Lo}(t) - n\left|i_{\rm pri}(t) - i_{Lm,\rm peak}\right|. \quad (6)$$

From (4)–(6), $i_{\rm DF}$ at t_2 is as follows:

$$i_{\rm DF}(t_2) = i_{Lo}(t_2) - n\left|\frac{i_{Lo}(t_1)}{n} - \Delta i_{\rm pri,drop}\right|. \quad (7)$$

Equations (5) and (7) indicate that $i_{\rm DF}$ is proportional to the sum of the secondary junction capacitances. Therefore, by increasing the sum of secondary junction capacitances, $i_{\rm DF}$ can increase, subsequently reducing the conduction losses in rectifier diodes. The detailed design process of the secondary capacitances to increase $i_{\rm DF}$ is presented in Section III-B.

***Mode 3* [t_2 – t_3]:** Mode 3 starts when the voltage across L_m, i.e., v_{Lm}, becomes zero. Q_2 is turned ON by zero-voltage switching (ZVS) operation. Then, $i_{\rm pri}$ circulates through the primary side, as illustrated in Fig. 2(c). i_{pri} flows with a slope of $v_{\rm lkg}/L_{\rm lkg}$ as follows:

$$i_{\rm pri}(t) = i_{\rm pri}(t_2) + \frac{v_{\rm lkg}}{L_{\rm lkg}}(t-t_2) \quad (8)$$

where $v_{\rm lkg}$ is the voltage across $L_{\rm lkg}$. Assuming that $v_{\rm lkg}$ is zero in this mode, $i_{\rm pri}$ maintains its value of $i_{\rm pri}(t_2)$ until t_3. Equation (6) demonstrates that the reduced $i_{\rm pri}$ increases $i_{\rm DF}$. Thus, $i_{\rm pri}$ during mode 3 can be decreased by designing the slope of $i_{\rm pri}$, which is determined by $v_{\rm lkg}$. The detailed design process of the slope of $i_{\rm pri}$ is provided in Section III-A.

***Mode 4* [t_3–t_4]:** After Q_4 is turned OFF at t_3, output capacitors of Q_3 and Q_4 are discharged and charged, respectively. $i_{\rm pri}$ decreases steeply because $–V_S$ is impressed on $L_{\rm lkg}$. Thus, i_{D2} increases and $i_{\rm DF}$ decreases. Subsequently, the operations are

identical those in the previous modes, except for the direction of power flow.

III. Two Methods for Increasing Freewheeling Current Commutated to D_F

When only D_F is adopted, a small portion of the total freewheeling current flows through D_F, and most of it still flows through the high voltage-rated diode D_1 or D_2. Thus, the addition of D_F cannot have a significant impact on overall efficiency. In this section, two simple methods are analyzed to increase the freewheeling current commutated to D_F, i.e., $i_{\rm DF}$, inducing the current flowing through D_1 or D_2 to be lower. These methods also reduce the circulating current, which is not connected to the input and output and only circulates in the primary side, and turn-OFF current of lagging-leg switches. Therefore, the overall efficiency is more improved by reducing the conduction and switching losses. The two methods are as follows:

1) Adding primary capacitor C_P [16], [17].
2) Adding secondary capacitor C_S [18].

The concept of method using C_P or C_S was briefly discussed in [16], [17], and [18]. However, they mainly focused on using C_P or C_S to increase transformer turns ratio, suppress voltage oscillations, and achieve zero-voltage and zero-current switching operation, and D_F was not adopted in [16], [17], and [18]. Thus, these studies did not offer the magnitudes of $i_{\rm DF}$ according to C_P or C_S and the design process of C_P or C_S considering $i_{\rm DF}$. In the followings, the characteristics of each method are explained, including the advantages and disadvantages. Then, $i_{\rm pri}$ and $i_{\rm DF}$ are calculated to verify the effectiveness of each method, and design guidelines for C_P and C_S are provided. Finally, the comparisons between the effects of C_P and C_S and with existing studies are discussed.

A. Primary Capacitor $C_{\rm P}$

1) Effect of Primary Capacitor $C_{\rm P}$: To reduce the circulating and turn-OFF currents and increase $i_{\rm DF}$, C_P can be used in series with the primary side of the transformer, as illustrated in Fig. 5(a). As described in mode 3 of Section II, $i_{\rm pri}$ is decreased with the rate of $v_{\rm lkg}/L_{\rm lkg}$ during the freewheeling interval. When C_P is not adopted, $i_{\rm pri}$ maintains its value of $i_{\rm pri}(t_b)$ until t_c because $v_{\rm lkg}$ is zero, as depicted in Fig. 5(b). Thus, the converter still has high circulating and turn-OFF currents and low $i_{\rm DF}$.

Meanwhile, by using C_P, $i_{\rm pri}$ is reduced at the rate of $v_{Cp}/L_{\rm lkg}$ because the voltage across the primary capacitor, i.e., v_{Cp}, is applied to $L_{\rm lkg}$ during the freewheeling interval [16], [17]. Thus, the circulating current and turn-OFF current of lagging-leg switches are reduced. This also increases $i_{\rm DF}$ and reduces i_{D1} or i_{D2}, resulting in low conduction losses. However, this approach degrades the ZVS capability, and causes power loss from C_P because C_P is continuously charged and discharged by $i_{\rm pri}$ during a switching cycle.

2) Freewheeling Current Commutated to $D_{\rm F}$: To simplify the analysis, it is assumed that the operating modes during a half cycle are divided into two: powering interval, i.e., t_a–t_b, and freewheeling interval, i.e., t_b–t_c. To calculate $i_{\rm DF}$, v_{Cp} should be obtained, which affects the slope of $i_{\rm pri}$ during the freewheeling interval. As illustrated in Fig. 5(b), C_P is charged and discharged while $i_{\rm pri}$ flows in the positive and negative directions, respectively. Since $i_{\rm pri}$ flows symmetrically in both directions during a switching cycle, the capacitor voltage ripple Δv_{Cp} is as follows:

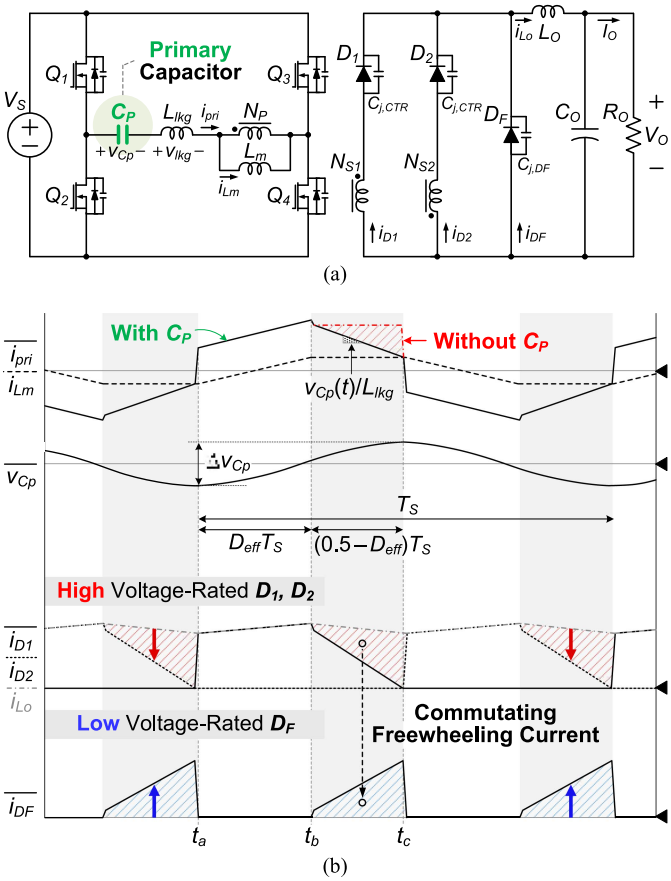

Fig. 5. PSFB converter with D_F and C_P. (a) Circuit diagram. (b) Key waveforms.

$$\Delta v_{Cp} = \left\{ \frac{I_O}{n} D_{\rm eff} + \left(\frac{I_O}{n} + i_{Lm,\rm peak} \right) \left(\frac{1}{2} - D_{\rm eff} \right) \right\} \times \frac{1}{C_P} \times T_S \tag{9}$$

where $D_{\rm eff}$ is the effective duty ratio and T_S is a switching period. The maximum value of v_{Cp}, i.e., $V_{Cp,\max}$, is half of Δv_{Cp}, and it has the same magnitude with opposite polarity after half a switching cycle as follows:

$$V_{Cp,\max} = -V_{Cp,\min} = \frac{\Delta v_{Cp}}{2} \tag{10}$$

where $V_{Cp,\min}$ is the minimum value of v_{Cp}.

Since $v_{Cp}(t_a)$ is equal to $V_{Cp,\min}$, $v_{Cp}(t_b)$ can be calculated using (9) and (10). During t_a–t_b, C_P is charged by the reflected output current I_O/n, as shown in Fig. 6(a). Hence, $v_{Cp}(t_b)$ is as follows:

$$v_{Cp}(t_b) = V_{Cp,\min} + \frac{I_O/n}{C_P} D_{\rm eff} T_S. \tag{11}$$

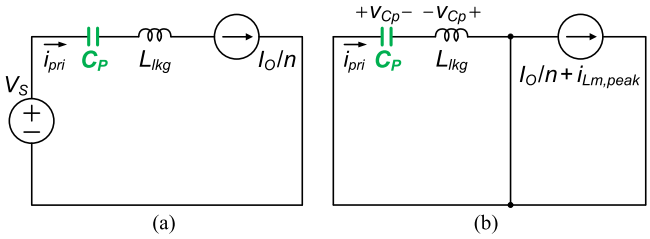

Fig. 6. Equivalent circuit of PSFB converter with D_F and C_P. (a) t_a–t_b. (b) t_b–t_c.

After t_b, $i_{\rm pri}$ circulates in the primary side, and D_1 and D_F are conducted, as illustrated in Fig. 6(b). Thus, $i_{\rm pri}$ during t_b–t_c can be expressed as follows, based on (11):

$$i_{\rm pri}(t) = \left(\frac{I_O}{n} + i_{Lm,\rm peak}\right)\cos\omega(t-t_b) - v_{Cp}(t_b)\sqrt{\frac{C_P}{L_{\rm lkg}}}\sin\omega(t-t_b) \tag{12}$$

where $\omega = 1/(L_{\rm lkg}\ C_P)^{1/2}$. Therefore, from (6) and (12), i_{DF} and the average freewheeling current commutated to D_F, i.e., $<i_{\rm DF}>$, are as follows when C_P is employed:

$$i_{\rm DF}(t) = I_O - n\,|i_{\rm pri}(t) - i_{Lm,\rm peak}| \tag{13}$$

$$\langle i_{\rm DF}\rangle \simeq \frac{I_O - n\,|i_{\rm pri}(t_c) - i_{Lm,\rm peak}|}{2}\,(1-2D_{\rm eff})\,. \tag{14}$$

Consequently, as C_P decreases, v_{Cp} increases, which leads to steep decrease in the primary current $i_{\rm pri}$. Thus, the circulating and turn-OFF currents are reduced and $<i_{\rm DF}>$ is increased, resulting in low conduction losses.

3) Primary Capacitor $C_{\rm P}$ *Design:* To operate the converter properly and satisfy the ZVS condition of lagging-leg switches, C_P should be selected appropriately. If $V_{Cp,\max}$ exceeds V_S, the converter is not within normal operation because a reverse-polarity voltage is applied across L_m during the powering interval. Therefore, the minimum value of C_P, i.e., $C_{P,\min}$, which guarantees normal operation is as follows:

$$\left\{\frac{I_O}{n}D_{\rm eff} + \left(\frac{I_O}{n} + i_{Lm,\rm peak}\right)\left(\frac{1}{2} - D_{\rm eff}\right)\right\}\frac{T_S}{2V_S} \le C_{P,\min}. \tag{15}$$

Applying the parameters in Table II to (15), C_P should be larger than 90 nF in this article, as illustrated in Fig. 7. To ensure ZVS operation, the energy stored in $L_{\rm lkg}$ should be greater than that stored in the output capacitors of lagging-leg switches C_{OSS}. Thus, the following equation should be satisfied:

$$\frac{1}{2}L_{\rm lkg}{i_{\rm pri}(t_c)}^2 \ge C_{\rm OSS}{V_S}^2 \tag{16}$$

where

$$i_{\rm pri}(t_c) = \left(\frac{I_O}{n} + i_{Lm,\rm peak}\right)\cos\omega\left(\frac{1}{2} - D_{\rm eff}\right)T_S - v_{Cp}(t_b)\sqrt{\frac{C_P}{L_{\rm lkg}}}\sin\omega\left(\frac{1}{2} - D_{\rm eff}\right)T_S.$$

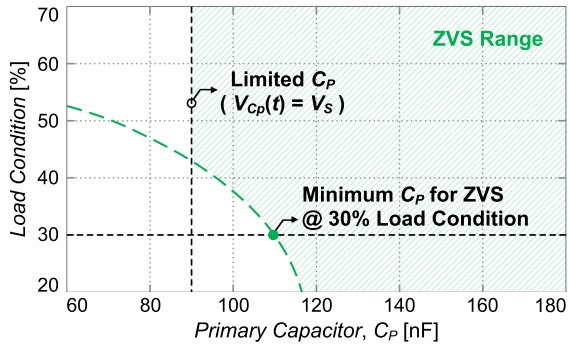

Fig. 7. Limited C_P and ZVS range of lagging-leg switches according to C_P at $V_S = 400$ V.

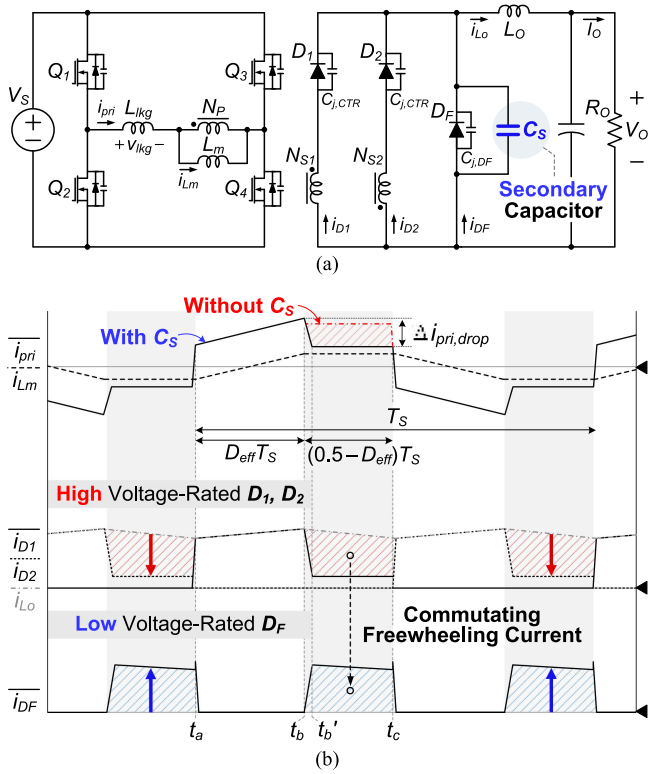

Fig. 8. PSFB converter with D_F and C_S. (a) Circuit diagram. (b) Key waveforms.

Fig. 7 shows the ZVS range for the lagging-leg switches according to C_P, indicated by the green-shaded area. When C_P is employed, $i_{\rm pri}$ is reduced according to the rate of $v_{Cp}/L_{\rm lkg}$, where v_{Cp} is inversely proportional to C_P. Consequently, the ZVS range becomes narrower as C_P decreases. In this article, the PSFB converter with C_P is designed to achieve ZVS operation under a 30% load condition as an example. Therefore, as illustrated in Fig. 7, the minimum C_P that satisfies the ZVS condition—i.e., 110 nF—is selected to maximize the overall efficiency.

B. *Secondary Capacitor* $C_{\rm S}$

1) Effect of Secondary Capacitor $C_{\rm S}$*:* As illustrated in Fig. 8(a), by employing C_S in parallel with D_F in the secondary

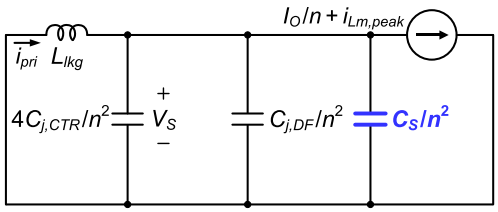

Fig. 9. Equivalent circuit of PSFB converter with D_F and C_S during t_b–t_b' when C_{OSS} is fully discharged.

side, the circulating current and i_{DF} can be further decreased and increased, respectively, compared to those when C_P is applied. As mentioned in mode 2 of Section II, after the leading-leg switches are turned OFF, i_{pri} is reduced about $\Delta i_{\mathrm{pri,drop}}$ which is proportional to the sum of the secondary junction capacitances. Consequently, a larger secondary junction capacitance makes the circulating current in the primary side to be lower and i_{DF} to be higher. Therefore, in the PSFB converter without C_S, the circulating current is only slightly reduced due to the small secondary junction capacitance, leading to slight improvement in efficiency, as shown in Fig. 8(b).

Meanwhile, by using C_S, the total secondary capacitance increases, which makes $\Delta i_{\mathrm{pri,drop}}$ larger. Hence, the circulating and turn-OFF currents are reduced. This also induces i_{DF} to be higher and i_{D1} or i_{D2} to be lower, resulting in low conduction losses. However, this approach causes a narrow ZVS capability.

2) Freewheeling Current Commutated to $\mathrm{D_F}$*:* After the leading-leg switch is turned OFF, i_{pri} discharges C_{OSS} and secondary capacitors, i.e., $C_{j,\mathrm{CTR}}$, $C_{j,\ DF}$, and C_S. Assuming that C_{OSS} is discharged much faster than the secondary capacitors, the body diode of leading-leg switch is conducted, as described in Fig. 9 [19]. Since the voltage across secondary capacitors is reflected to L_{lkg}, i_{pri} is reduced until t_b'. Thus, after C_{OSS} is discharged, i_{pri} is as follows:

$$i_{\mathrm{pri}}(t) \simeq \frac{I_O}{n} + i_{Lm,\mathrm{peak}} - V_S\sqrt{\frac{4C_{j,\mathrm{CTR}} + C_{j,\mathrm{DF}} + C_S}{n^2 L_{\mathrm{lkg}}}} \sin(\omega(t - t_b)) \tag{17}$$

where $\omega = 1/[L_{\mathrm{lkg}}(4C_{j,\mathrm{CTR}} + C_{j,\mathrm{DF}} + C_S)]^{1/2}$. From (17), i_{pri} at t_b' is as follows:

$$i_{\mathrm{pri}}(t_b{}') \simeq \frac{I_O}{n} + i_{Lm,\mathrm{peak}} - V_S\sqrt{\frac{4C_{j,\mathrm{CTR}} + C_{j,\mathrm{DF}} + C_S}{n^2 L_{\mathrm{lkg}}}}. \tag{18}$$

From (18), $\Delta i_{\mathrm{pri,drop}}$ is derived as follows:

$$\Delta i_{\mathrm{pri,drop}} = V_S\sqrt{\frac{4C_{j,\mathrm{CTR}} + C_{j,\mathrm{DF}} + C_S}{n^2 L_{\mathrm{lkg}}}}. \tag{19}$$

The current i_{pri} is reduced about $\Delta i_{\mathrm{pri,drop}}$ until t_b', and it does not changed during t_b'–t_c assuming that v_{lkg} is zero. Hence, from (6) and (18), i_{DF} is obtained as follows because the difference between i_{pri} and i_{Lm} is reflected to i_{D1} or i_{D2}. It can be approximated assuming that output inductor L_O is large enough:

$$\begin{aligned} i_{\mathrm{DF}}(t) &= i_{Lo}(t) - n\,|i_{\mathrm{pri}}(t) - i_{Lm,peak}| \\ &\simeq V_S\sqrt{\frac{4C_{j,\mathrm{CTR}} + C_{j,\mathrm{DF}} + C_S}{L_{\mathrm{lkg}}}}. \end{aligned} \tag{20}$$

Based on (20), when C_S is adopted, $<i_{\mathrm{DF}}>$ is given as follows:

$$\langle i_{\mathrm{DF}}\rangle \simeq V_S\sqrt{\frac{4C_{j,\mathrm{CTR}} + C_{j,\mathrm{DF}} + C_S}{L_{\mathrm{lkg}}}}\,(1 - 2D_{\mathrm{eff}})\,. \tag{21}$$

Consequently, as C_S increases, $\Delta i_{\mathrm{pri,drop}}$ increases. Thus, the circulating and turn-OFF currents are reduced and $<i_{DF}>$ is increased, resulting in low conduction losses.

3) Secondary Capacitor $\mathrm{C_S}$ *Design:* To maximize i_{DF} and guarantee the ZVS operation of lagging-leg switches, an appropriate C_S should be selected. All the freewheeling current flows through D_F when the difference between i_{pri} and i_{Lm} is zero because the difference of them flows through D_1 or D_2. Thus, i_{DF} can be maximized when $i_{\mathrm{pri}}(t_b{}')$ is equal to $i_{Lm,\mathrm{peak}}$ as follows:

$$i_{\mathrm{pri}}(t_b{}') = i_{Lm,\mathrm{peak}} = i_{\mathrm{pri}}(t_b) - \Delta i_{\mathrm{pri,drop}}. \tag{22}$$

From (19) and (22), C_S for maximum i_{DF}, i.e., $C_{S,\max}$, is as follows:

$$C_{S,\max} = \frac{L_{\mathrm{lkg}}{I_O}^2}{{V_S}^2} - 4C_{j,\mathrm{CTR}} - C_{j,\mathrm{DF}}. \tag{23}$$

To ensure the ZVS operation, the energy stored in L_{lkg} should be greater than that stored in C_{OSS}. Hence, the following equation should be satisfied for ZVS operation of lagging-leg switches:

$$\frac{1}{2}L_{\mathrm{lkg}}{i_{\mathrm{pri}}(t_c)}^2 \geq C_{\mathrm{OSS}}{V_S}^2 \tag{24}$$

where $i_{\mathrm{pri}}(t_c) = i_{\mathrm{pri}}(t_b{}') = i_{\mathrm{pri}}(t_b) - V_S\sqrt{\frac{4C_{j,\mathrm{CTR}}+C_{j,\mathrm{DF}}+C_S}{n^2 L_{\mathrm{lkg}}}}$.

Fig. 10 shows the ZVS range for the lagging-leg switches according to C_S, indicated by the blue-shaded area. When C_S is adopted, i_{pri} is reduced about $\Delta i_{\mathrm{pri,drop}}$ which is proportional to C_S. Thus, the ZVS range becomes narrower as C_S increases. In this article, the PSFB converter with C_S is designed to achieve ZVS operation under a 30% load condition as an example.

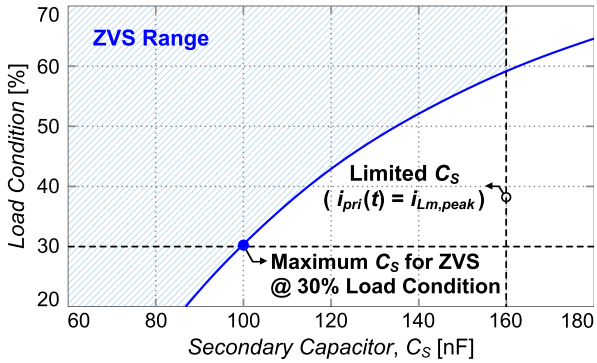

Fig. 10. Limited C_S and ZVS range of lagging-leg switches according to C_S at $V_S = 400$ V.

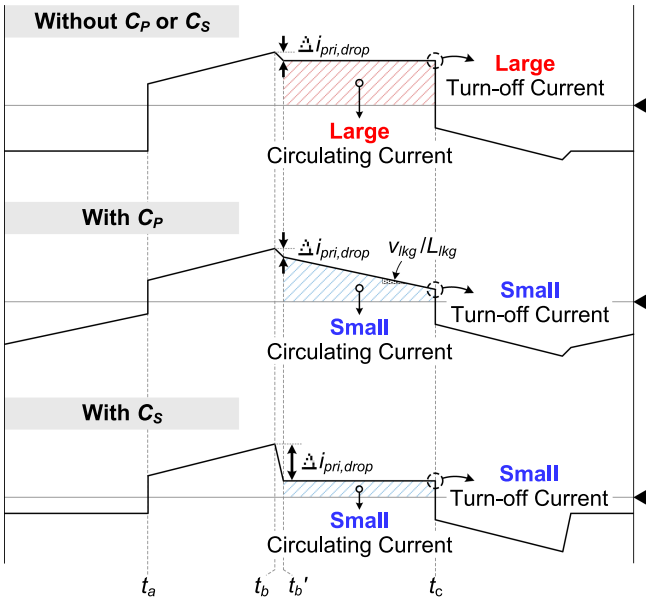

Fig. 11. Comparison of $i_{\rm pri}$ during freewheeling interval.

Therefore, as illustrated in Fig. 10, the maximum C_S that satisfies the ZVS condition—i.e., 100 nF—is selected to maximize the overall efficiency.

IV. Comparisons

A. Comparisons Between Two Methods: C_P and C_S

In this section, the PSFB converters with C_P and C_S are compared. These comparisons are conducted based on the same specifications and parameter values defined in Table II.

1) Circulating and Turn-off Currents in Primary Side: Fig. 11 illustrates the comparisons of primary currents during the freewheeling interval. The currents in each method are explained as follows.

1) Without C_P or C_S: $i_{\rm pri}$ is slightly reduced about $\Delta i_{\rm pri,drop}$ during t_b–t_b'. After then, it does not changed during t_b'–t_c.
2) With C_P: $i_{\rm pri}$ is slightly reduced during t_b–t_b'. It linearly decreases with a slope of $v_{Cp}/L_{\rm lkg}$ during t_b'–t_c.
3) With C_S: During t_b–t_b', $i_{\rm pri}$ is significantly reduced due to the large $\Delta i_{\rm pri,drop}$, which is proportional to the sum of secondary capacitances. After t_b', $i_{\rm pri}$ maintains its value of $i_{\rm pri}(t_b')$ until t_c.

Consequently, by adopting C_P or C_S, the circulating and turn-OFF currents are reduced, resulting in lower primary conduction and switching losses compared to that without C_P or C_S. Moreover, the circulating current can be further reduced when C_S is employed compared to adopting C_P, assuming that $i_{\rm pri}$ with C_P and $i_{\rm pri}$ with C_S reach the same value at t_c, as described in Fig. 11.

2) Freewheeling Current Commutated to $\rm D_F$*:* Based on (6) in Section II, the reduced $i_{\rm pri}$ makes $i_{\rm DF}$ to be higher. Hence, by adopting C_P or C_S, $i_{\rm DF}$ is increased, causing the reduced conduction loss compared to without C_P or C_S. As shown in Fig. 11, assuming that $i_{\rm pri}$ with C_P and $i_{\rm pri}$ with C_S reach the same value at t_c, $i_{\rm DF}$ can be further increased when C_S is used compared to using C_P.

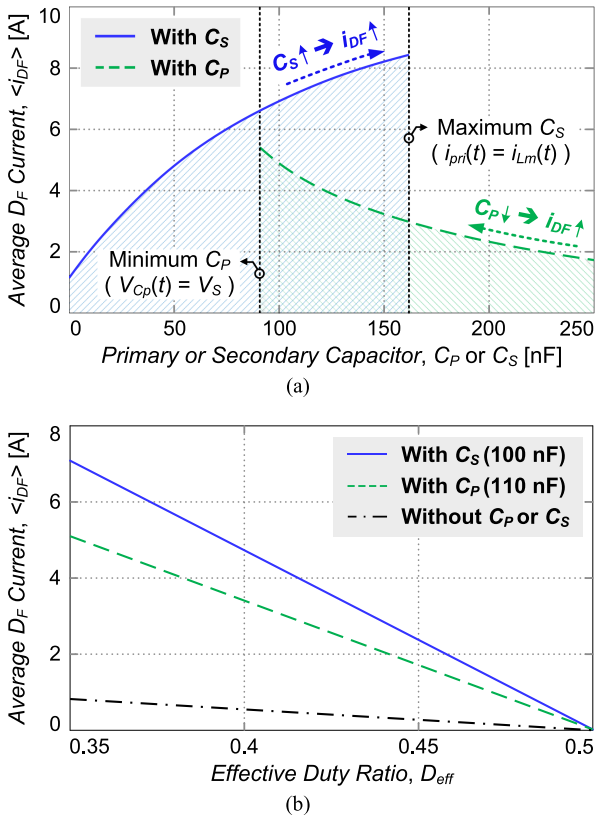

Fig. 12. Average freewheeling current commutated to D_F, i.e., $<i_{\rm DF}>$. (a) According to C_P or C_S at $V_S = 400$ V. (b) According to $D_{\rm eff}$.

Meanwhile, as described in Fig. 12(a), $<i_{\rm DF}>$ increases as C_P decreases and C_S increases. In addition, the minimum value of C_P and maximum value of C_S are determined by (15) and (23), respectively. Fig. 12(b) illustrates $<i_{\rm DF}>$ according to $D_{\rm eff}$. As $D_{\rm eff}$ increases, the freewheeling interval becomes shorter, which decreases $<i_{\rm DF}>$. Consequently, the efficiency improvement of the PSFB converter adopting C_P or C_S is maximized compared to that without C_P or C_S at the minimum $D_{\rm eff}$.

B. Comparisons With Existing Studies

Table I compares the additional component count, voltage stresses on rectifier diodes, control complexity, and power density among existing studies and the converter employing C_P or C_S. In [5], a rectifier with a low voltage charging technique was proposed. It reduced voltage stresses on rectifier components because the two capacitors were alternatively charged. However, this technique required additional active switches, increasing the control complexity and overall system volume. In [6], a hybrid dual full-bridge converter was introduced, which mitigated the output current ripple and voltage stresses on rectifier diodes due to the hybrid connection of secondary diodes. The circulating current and duty-cycle losses were also reduced because the primary current decayed to zero during the freewheeling interval. However, four switches and one transformer were added, leading to high control complexity and low power density. In [7], [8], and [9], rectifiers using coupled inductor and low voltage-rated components were described. The circulating current was eliminated in [7] and [8]. However, in

TABLE I
COMPARISONS WITH PREVIOUS STUDIES

	Topology	Additional components	Rectifier diodes* voltage stresses	Control complexity	Power density
Conv.	PSFB	–	$\frac{2V_S}{n}$	Simple	Extremely High
Kim et al. [5]	PSFB	Two switches, two diodes, two capacitors	$\frac{V_S}{n}$	Complicated	Low
Zhou et al. [6]	Dual-Full Bridge	Four switches, one transformer, four diodes	$\frac{V_S}{2n}$	Complicated	Low
Kim et al. [7]	Three-Level DC/DC	Two transformer, two diodes, two capacitors	$\frac{(n_c-1)V_S}{2nn_c(n_c+1)} - \frac{V_O}{n_c}$**	Simple	Medium
Han and Moon [8]	PSFB	Two diodes	V_O	Simple	High
Ahn et al. [9]	PSFB	Four diodes	V_O	Simple	Medium
Jeong et al. [10]	PSFB	One transformer, One diode	$\frac{V_S}{n} - V_O$	Simple	Medium
Lee et al. [11]	PSFB	Two capacitors	V_O	Simple	Extremely High
Prop.	**PSFB**	**One diode, One capacitor**	$\frac{V_S}{n}$	**Simple**	**High**

* The lowest voltage stress among rectifier diodes is presented.
** n_c is turns ratio of coupled inductor.
Bold to emphasize the characteristics of the proposed converter.

[7], two additional diodes and capacitors were demanded. In [8], although the voltage stresses on specific diodes were reduced, other diodes experienced higher voltage stresses compared to the conventional PSFB converter. In [9], only half of the circulating current was reduced. Furthermore, the rectifiers in [7], [8], [9] required a complex magnetic design process due to the coupled inductors. In [10], a two-transformer PSFB converter with eliminated circulating current and low voltage-rated diode was discussed, but two transformer were inevitably used, resulting in low power density. In [11], a voltage doubler rectifier was discussed, which clamped the voltage across secondary diodes to the output voltage and eliminated the circulating current. For this configuration, the output inductor was eliminated, which increased the secondary RMS and peak currents.

Compared to abovementioned studies, the converters adopting two methods require only a low voltage-rated diode D_F and a capacitor C_P or C_S without the addition of active switches or magnetic components. By adopting C_P or C_S, the circulating current can be eliminated or linearly reduced, respectively, which increases the freewheeling current commutated to the low voltage-rated diode. Therefore, two methods effectively improve the overall efficiency while maintaining the simple control and high power density.

V. TOPOLOGICAL EXTENSIONS ADOPTING D_F

In this section, topological extensions adopting D_F for a full-bridge rectifier (FBR) and a current doubler rectifier (CDR) are proposed, as illustrated in Fig. 13. The diode D_F in the FBR and CDR function as in the CTR by changing the freewheeling path, which reduces the conduction losses during the freewheeling interval. The brief explanations of the operation principles and characteristics of each rectifier are presented as follows.

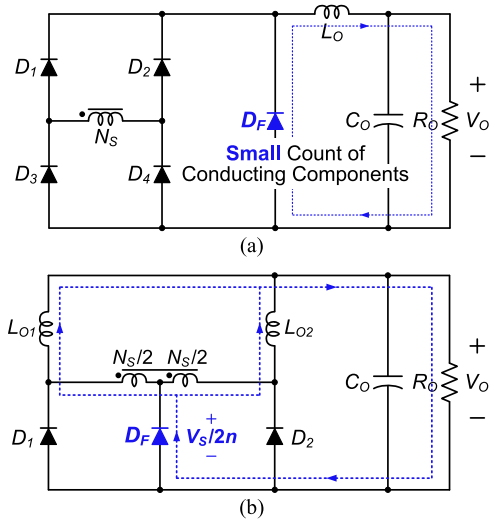

Fig. 13. Topological extensions adopting D_F and simplified freewheeling current path for small conduction losses. (a) Full-bridge rectifier. (b) Current doubler rectifier.

1) *Full-Bridge Rectifier*: In the conventional FBR, all the diodes D_1–D_4 are conducted during the freewheeling interval. However, by adopting D_F, only three diodes are conducted because the freewheeling current in the secondary side is commutated to D_F instead of the two diodes, as shown in Fig. 13(a). Consequently, the number of conducting components to make freewheeling path is reduced, resulting in low conduction losses.
2) *Current Doubler Rectifier*: In the conventional CDR, high voltage-rated diodes D_1 and D_2 are inevitably used due to the high voltage stresses on rectifier diodes, i.e., V_S/n. Thus, total freewheeling current in the secondary side flows through high voltage-rated diodes. To reduce the conduction losses, D_F with a center-tapped transformer

TABLE II
EXPERIMENTAL SPECIFICATIONS AND COMPONENTS

Parameter		Without D_F	With D_F [see Fig.1(a)]
Input		300−400 V	
Output		12 V / 250 W	
Switching Frequency, f_S		70 kHz	
Primary Side	Switch Q_1-Q_4	IPP60R160P7 (V_{DS} = 650 V / $R_{ds(on)}$ = 0.16 Ω / C_{OSS} = 43 pF)	
Transformer	Turns Ratio	23 : 1 : 1	
	Inductance	L_m = 800 μH / L_{lkg} = 30 μH	
	Core	PQ3230S (PL-9)	
Secondary Side	Rectifier Diode D_1, D_2	FERD40H100S (V_{RRM} = 100 V / V_F = 0.47 V / C_j = 330 pF)	
	Freewheeling Diode D_F	–	FERD20M60 (V_{RRM} = 60 V / V_F = 0.26 V / C_j = 390 pF)
	Output Inductor	L_O = 5 μH (Core : CH270125)	

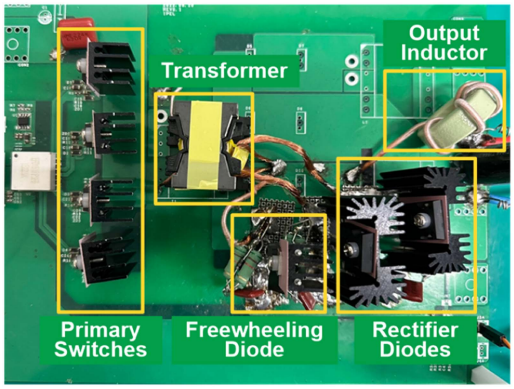

Fig. 14. Prototype of PSFB converter with D_F.

is adopted, as illustrated in Fig. 13(b). Since D_F has low voltage stress, i.e., $V_S/2n$, the low voltage-rated diode can be used for D_F. Hence, the overall efficiency is improved by commutating the freewheeling current to D_F instead of the high voltage-rated diodes.

VI. EXPERIMENTAL RESULTS

To verify the effects C_P and C_S with D_F, a 250 W prototype was implemented with the following specifications: $V_S = 300$–400 V; $V_O = 12$ V; and $f_S = 70$ kHz. As shown in Table II and Fig. 14, a low voltage-rated freewheeling diode with low V_F was employed to reduce the conduction losses in the rectifier diodes.

Fig. 15(a) and (b) displays the key waveforms of the PSFB converter using CTR without D_F and with D_F, respectively. As shown in Fig. 15(a), the diodes D_1 and D_2 experience high voltage stresses, i.e., $2V_S/n$. In contrast, D_F has a low voltage stress, i.e., V_S/n, as displayed in Fig. 15(b). Thus, the PSFB converter using CTR with D_F has lower conduction losses compared to using CTR without D_F because the freewheeling current in the secondary side is commutated to D_F instead of D_1 or D_2. However, actually, when only D_F is adopted, a small portion of the freewheeling current flows through D_F, and most of it still flows through D_1 or D_2, as displayed in Fig. 15(b).

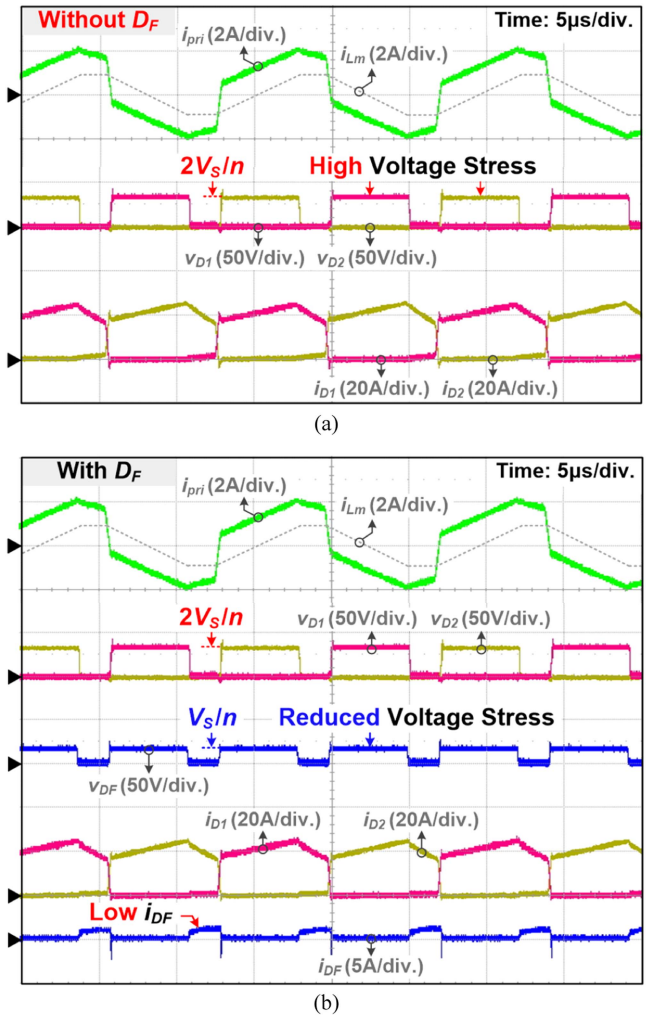

Fig. 15. Key waveforms of PSFB converter under full-load condition at $V_S = 400$ V. (a) CTR without D_F. (b) CTR with D_F.

Therefore, the addition of D_F alone has a limited impact on overall efficiency.

To improve efficiency by increasing the freewheeling current commutated to D_F, i.e., i_{DF}, C_P or C_S can be employed. Figs. 16 and 17 display the key waveforms of the PSFB converter with D_F according to C_P and C_S, respectively. As displayed in Fig. 16, by reducing C_P from 200 to 110 nF, the capacitor voltage ripple Δv_{Cp} is increased from 60 to 85 V. During the freewheeling interval, since i_{pri} decreases at the rate of v_{Cp}/L_{lkg}, it decreases more rapidly when 110 nF is used than when 200 nF is employed. Therefore, a smaller C_P, i.e., 110 nF, leads to higher i_{DF} and lower freewheeling current flowing through D_1 or D_2 i.e., i_{D1} or i_{D2}, resulting in low conduction losses. Similarly, Fig. 17 shows that increasing C_S from 20 to 100 nF increases $\Delta i_{\mathrm{pri,drop}}$ because $\Delta i_{\mathrm{pri,drop}}$ is proportional to the sum of the secondary capacitances. Thus, a larger C_S, i.e., 100 nF, allows higher i_{DF} and lower i_{D1} or i_{D2}, reducing conduction losses. However, during the powering interval, L_{lkg} resonates with the junction capacitors of diodes, i.e., $C_{j,CTR}$ and $C_{j,DF}$, and the secondary capacitor C_S, as illustrated in Fig. 18. Based on Fig. 18, the voltage across D_F, i.e., v_{DF}, and current flowing through C_S,

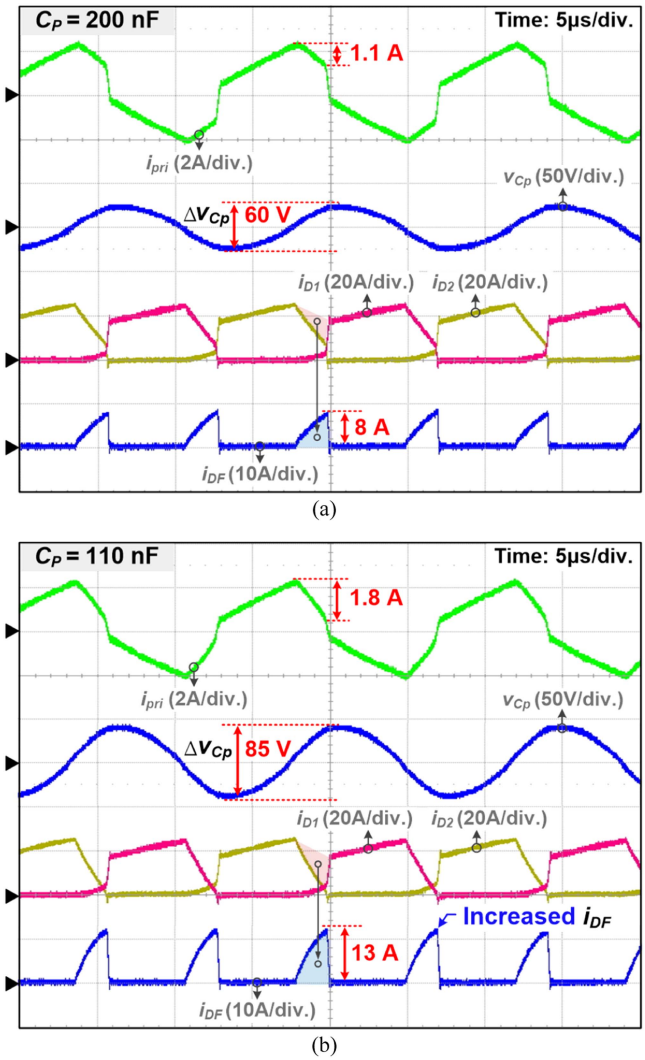

Fig. 16. Key waveforms of PSFB converter with D_F and C_P under full-load condition at $V_S = 400$ V. (a) $C_P = 200$ nF. (b) $C_P = 110$ nF.

i.e., i_{Cs}, are as follows assuming that C_S is sufficiently larger than $C_{j,\mathrm{CTR}}$ and $C_{j,\mathrm{DF}}$:

$$v_{\mathrm{DF}}(t) = \frac{V_S}{n} - \frac{V_S}{n}\cos\omega t \tag{25}$$

$$i_{Cs}(t) \simeq V_S\sqrt{\frac{4C_{j,\mathrm{CTR}} + C_{j,\mathrm{DF}} + C_S}{L_{\mathrm{lkg}}}}\sin\omega t \tag{26}$$

where $\omega = 1/[L_{\mathrm{lkg}}(4C_{j,\mathrm{CTR}} + C_{j,\mathrm{DF}} + C_S)]^{1/2}$. From (25), considering the voltage oscillation without snubber, v_{DF} can increase up to $2V_S/n$, and C_S does not affect the amplitude of the voltage oscillation. However, as C_S increases, the current required to charge C_S up to $2V_S/n$ increases. Therefore, the amplitude of the current oscillation increases as C_S increases, which is demonstrated in Fig. 17 and (26).

Fig. 19 shows the ZVS waveforms under 30% load condition at $V_S = 400$ V where v_{Q3} and $v_{gs,Q3}$ represent the drain-source and gate-source voltages of Q_3. As depicted in Fig. 19(a), when neither C_P nor C_S is employed, the lagging-leg switch

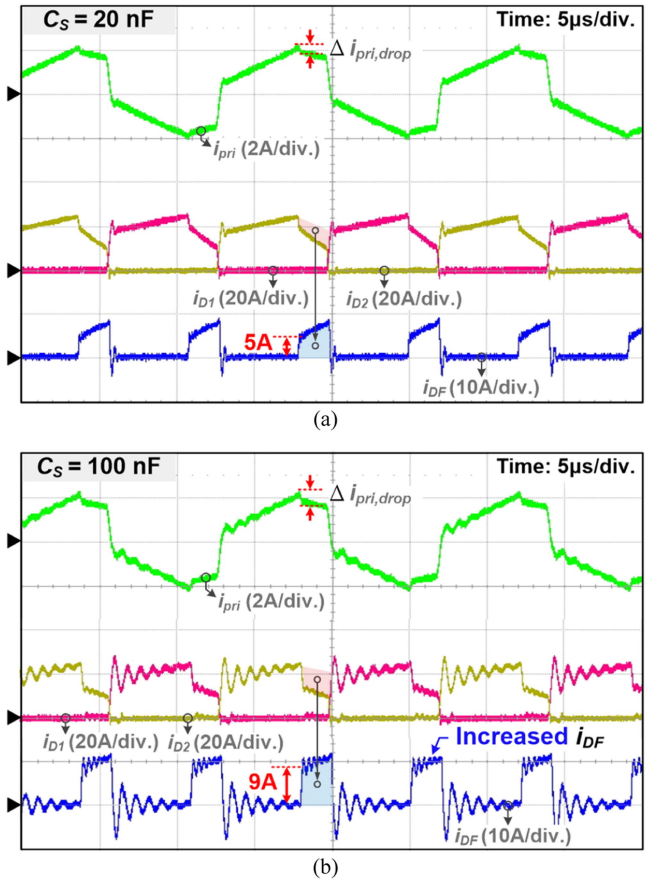

Fig. 17. Key waveforms of PSFB converter with D_F and C_S under full-load condition at $V_S = 400$ V. (a) $C_S = 20$ nF. (b) $C_S = 100$ nF.

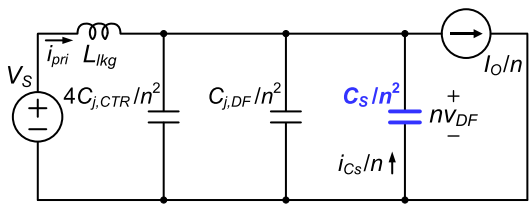

Fig. 18. Equivalent circuit of PSFB converter with D_F and C_S during powering interval.

achieves ZVS operation due to sufficient ZVS energy. However, as presented in Fig. 19(b) and (c), adopting a capacitor of 100 nF for C_P or 120 nF for C_S reduces ZVS energy due to the decreased i_{pri}. Thus, the lagging-leg switch operates with hard switching.

To evaluate the input voltage and load transient performance of the PSFB converter with D_F, digital control was implemented using the TMS320F28069M, as shown in Figs. 20 and 21. The input voltage transient experiment was conducted with a 50% load condition, where the input voltage was increased from 300 to 400 V and then decreased back to 300 V. The load transient experiment was conducted with a slew rate of 0.2 A/μs, where the load condition was increased from 20 to 80% and then decreased back to 20%. As described in Figs. 20 and 21, the output voltages are well regulated to 12 V and varies within 2.2 V and 1 V during the input voltage and load steps, respectively.

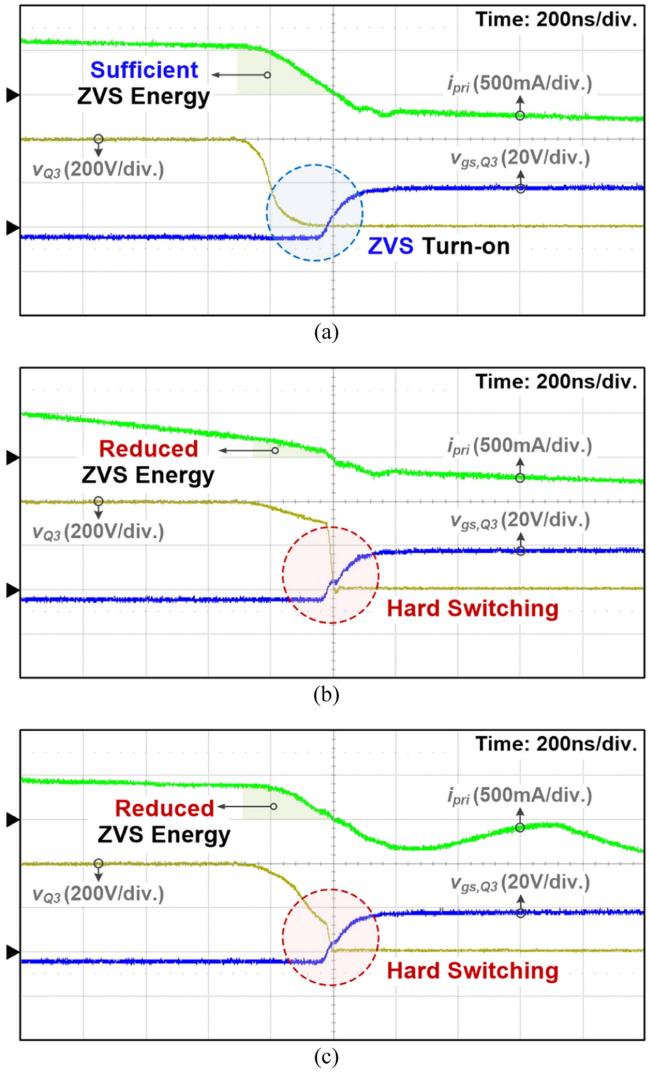

Fig. 19. ZVS waveforms under 30% load condition at $V_S = 400$ V. (a) Without C_P or C_S. (b) With C_P (= 100 nF). (c) With C_S (= 120 nF).

Fig. 22 presents the thermal pictures of the prototype under full-load condition. As shown in Fig. 22(a), in the converter without D_F, the temperature at the rectifier diodes D_1 and D_2 reaches 49.5 °C. Meanwhile, as presented in Fig. 22(b), the rectifier diodes in the converter with D_F and C_S reach only 44.3 °C, which is approximately 5.2 °C lower than that without D_F. This reduction occurs as some of freewheeling current flows through D_F with a lower V_F instead of D_1 or D_2. Thus, the converter with D_F and C_S exhibits lower power losses in the rectifier diodes compared to that without D_F, resulting in higher efficiency.

Fig. 23(a) presents the measured efficiency based on the load variations. As demonstrated in Fig. 23(a), the PSFB converter with D_F achieves higher efficiency compared to that without D_F. However, when only D_F is used, most of freewheeling current still flows through D_1 or D_2. Thus, the addition of D_F alone has a limited impact on overall efficiency. By adopting C_P or C_S, the efficiency is improved compared to employing D_F without C_P or C_S due to the reduced circulating current and increased

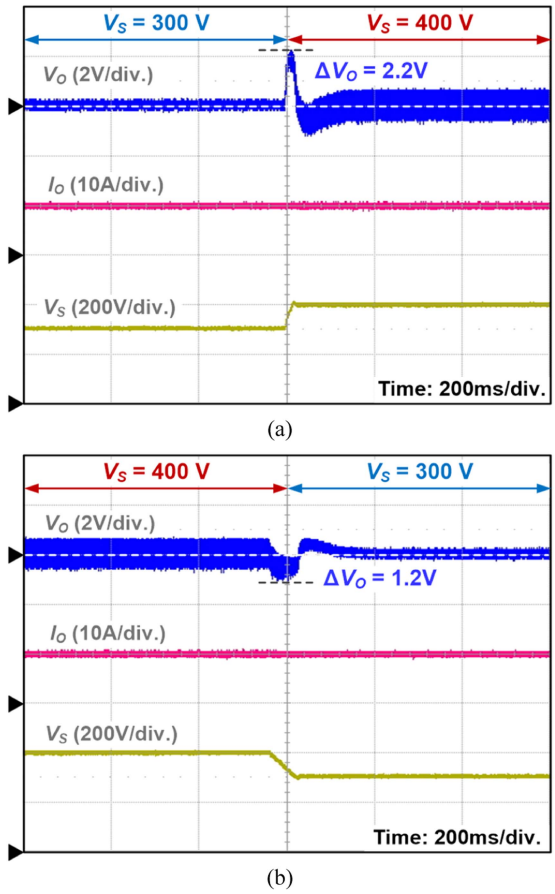

Fig. 20. Input voltage transient waveforms. (a) From 300 V to 400 V. (b) From 400 V to 300 V.

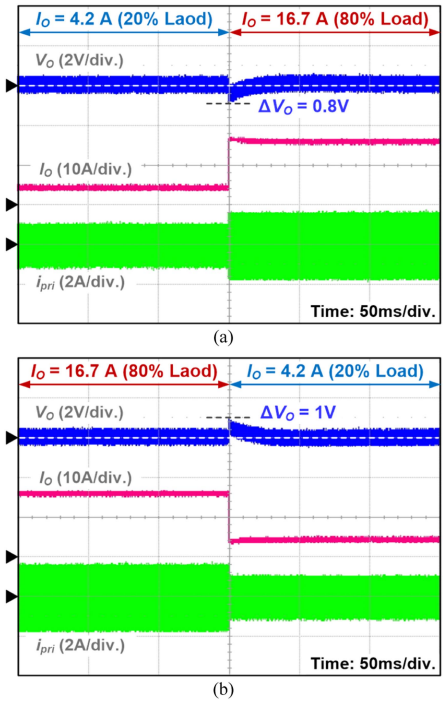

Fig. 21. Load transient waveforms. (a) From 20% to 80%. (b) From 80% to 20%.

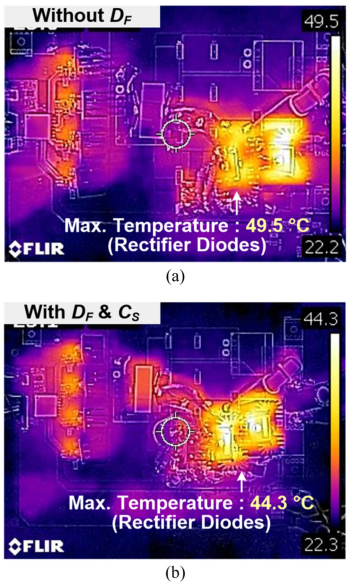

Fig. 22. Thermal picture under full-load condition. (a) Without D_F. (b) With D_F and C_S.

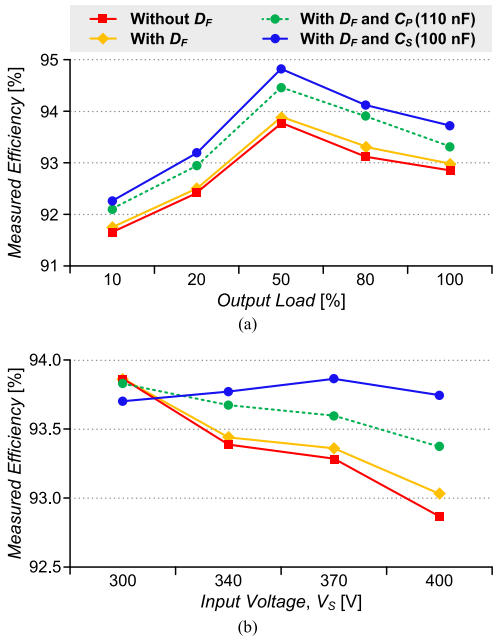

Fig. 23. Measured efficiency. (a) Load variation at $V_S = 400$ V. (b) Input voltage variation under full-load condition.

i_{DF}. Assuming the same peak current flowing through D_F when using C_P or C_S, as shown in Figs. 16(b) and 17(b), i_{DF} can be further increased by using C_S than C_P. Therefore, the overall efficiency is further improved when C_S is used compared to employing C_P.

Fig. 23(b) displays measured efficiency based on input voltage variations. The PSFB converter has a longer freewheeling interval as input voltage increases because the maximum D_{eff} is determined at the minimum input voltage [20]. Therefore, at 400 V input voltage, the PSFB converter with D_F using C_P or C_S achieves higher efficiency than that without D_F because the long freewheeling interval leads to an increase in $<i_{\mathrm{DF}}>$. As input

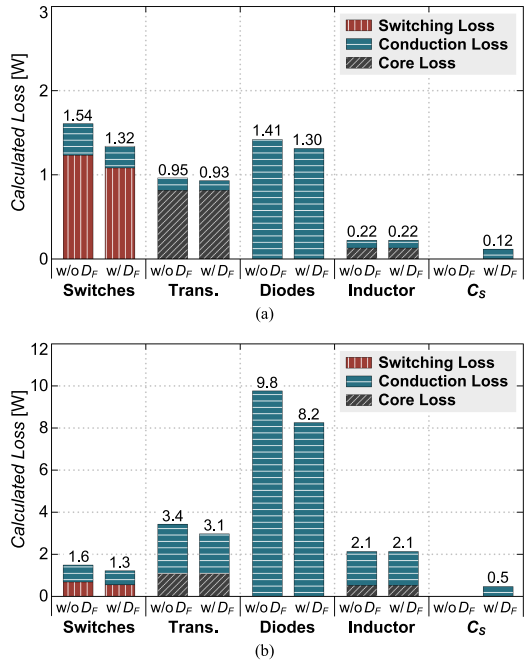

Fig. 24. Power loss distribution of converter without D_F and with D_F and C_S ($= 100$ nF) at $V_S = 400$ V. (a) 20% load condition. (b) Full-load condition.

voltage decreases, the difference in efficiency between without D_F and others is reduced. Moreover, slight efficiency degradation is observed at 300 V input voltage because additional power loss occurs to charge and discharge the additional capacitor C_P or C_S.

The two methods with D_F slightly increase cost and reduce system reliability due to additional components. However, since only passive components—one low voltage-rated diode and one capacitor—are added without any active switches or magnetic components, these methods effectively increase overall efficiency while minimizing cost and reliability degradation, as shown in Fig. 24.

VII. Conclusion

In the PSFB converter with CTR, the rectifier diodes suffered from high voltage stresses. To solve this problem, a low voltage-rated diode D_F was employed to make freewheeling path for output inductor current in previous studies [12], [13], [14]. However, the detailed commutation process and the impact of i_{DF} on the entire system were not addressed. Actually, when D_F was adopted alone, only a small portion of the total freewheeling current flowed through D_F, and most of it flowed through high voltage-rated diodes. Thus, the addition of D_F alone could not have a significant impact on overall efficiency. This article provided the operation principle during the freewheeling interval in detail. In addition, two simple methods for increasing i_{DF} were analyzed and the guidelines and characteristics of each method were offered. Furthermore, topological extensions adopting D_F for FBR and CDR were proposed for various applications. By adopting two methods, the converter achieved higher efficiency under most operating conditions due to the reduced circulating and turn-OFF currents and increased i_{DF}, despite the narrowed ZVS range and slight efficiency degradation under minimum

input voltage condition. Consequently, the PSFB converter with two methods is expected to be useful for high output current applications that required high efficiency and a simple design process.

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