

An Enhanced Carrier-Based Discontinuous PWM Strategy for Leakage Current Suppression in T-Type Three-Level Inverters

Xin Zhang, *Student Member, IEEE*, Zeng Liu , *Senior Member, IEEE*, Xujie Wang, and Jinjun Liu , *Fellow, IEEE*

Abstract—In nonisolated three-level inverter applications, common-mode voltage (CMV) and the leakage current resulting from it will lead to potential safety hazards, and a decrease in system efficiency. Existing research on carrier-based modulation is generally featured by the tradeoff between CMV suppression and switching loss reduction. To address this limitation, an enhanced carrier-based discontinuous pulsewidth modulation (DPWM) strategy is proposed for three-level inverters, using the T-type three-level inverter as an example. The proposed strategy further reduces the CMV variation within each clamping region of DPWM to suppress leakage current. On this basis, the sector division is optimized, which introduces a novel clamping mode and incorporates transition regions to avoid abrupt CMV variation when switching between clamping regions. Meanwhile, the mechanism by which the proposed method achieves this suppression is revealed through a double Fourier decomposition of CMV. Finally, the feasibility and superiority of the proposed modulation strategy are validated through experimental results.

Index Terms—Carrier-based discontinuous pulsewidth modulation (DPWM), common-mode voltage (CMV), leakage current suppression, switching loss, T-type three-level inverter (T²LI).

I. INTRODUCTION

MULTILEVEL inverters are employed to facilitate large-scale energy consumption while achieving higher power levels [1], [2], [3]. Three-level inverters demonstrate particular advantages over traditional two-level designs in medium and high voltage applications, owing to their reduced output harmonics and enhanced efficiency [4], [5], [6]. Among these, the T-type three-level inverter (T²LI) is distinguished by its elimination of additional diode requirements and its balanced switching loss distribution [7], [8], [9]. In grid systems, nonisolated inverters are predominantly utilized for distributed energy generation

because of their compact size, cost-effectiveness, and reduced losses [10], [11]. However, their inherent leakage currents, resulting from parasitic capacitance loops, adversely affect system efficiency, accelerate insulation degradation, and pose significant safety risks [12], [13], [14]. Furthermore, common-mode voltage (CMV), as the primary excitation source of leakage currents, not only compromises motor longevity but also jeopardizes winding insulation integrity [15], [16], [17], necessitating stringent CMV suppression measures.

Extensive research has been conducted to better suppress leakage current. The method of improving the topology can substantially enhance leakage current suppression capabilities [18], [19], [20], [21]. However, it is accompanied by compromised system stability, increased power losses and costs, and greater control complexity. Closed-loop control methods can effectively suppress leakage current by adjusting small vector duty cycles [18], [22], [23]. Nevertheless, this approach becomes unstable under varying operating conditions, resulting in inconsistent performance. In contrast, the reduction of CMV provides a more straightforward solution, as it eliminates additional power losses while simultaneously mitigating both CMV-induced effects and leakage current damage [24], [25], [26], [27]. Thus, this article focuses on optimizing CMV suppression for leakage current reduction.

CMV suppression can be realized by adjusting the modulation strategy. Two primary modulation strategies are employed: space vector pulsewidth modulation (SVPWM) and carrier-based modulation [28]. SVPWM can precisely control each link of modulation through detailed sector division and calculation [29], [30], [31], but it requires more extensive computations and exhibits higher control complexity. In contrast, carrier-based modulation simply requires injection of an appropriate zero-sequence voltage into the three-phase modulation wave, followed by comparison with the carrier wave to generate switching pulses [32], [33], [34]. Consequently, considering the convenience of practical engineering applications, this article concentrates on carrier-based modulation strategies for CMV suppression.

Currently, the most widely used modulation strategy in the industry is seven-segment pulsewidth modulation (7S-PWM), which has 12 switching actions and a CMV variation of $U_{dc}/2$ in each switching cycle, where U_{dc} denotes the dc-side voltage. To eliminate leakage current, the zero-leakage current modulation method has been proposed [35]. This approach effectively

Received 8 June 2025; revised 17 September 2025; accepted 20 October 2025. Date of publication 7 November 2025; date of current version 19 January 2026. This work was supported by the National Key Research and Development Program of China under Grant 2023YFB2604600. This paper was presented in part at the 16th IEEE Energy Conversion Congress and Exposition, Phoenix, USA, October 2024 [DOI: 10.1109/ECCE55643.2024.10860992]. Recommended for publication by Associate Editor Y. Siwakoti. (*Corresponding author: Zeng Liu.*)

The authors are with the State Key Laboratory of Electrical Insulation and Power Equipment, School of Electrical Engineering, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: zhangxin9@stu.xjtu.edu.cn; zeng liu@mail.xjtu.edu.cn; wangxujie@stu.xjtu.edu.cn; jliu@mail.xjtu.edu.cn).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TPEL.2025.3630479>.

Digital Object Identifier 10.1109/TPEL.2025.3630479

eliminates leakage current by maintaining a constant CMV while simultaneously balancing the dc-side neutral-point voltage (NPV) through transitions between different constant CMV values. However, the dc voltage utilization of this method is reduced to 86.6% of 7S-PWM. Furthermore, simultaneous multiphase switching takes place during state transitions, involving up to 16 switching actions per cycle, which considerably increases switching losses.

To minimize switching losses, zero-averaged CMV modulation has been implemented to maintain zero average CMV over each switching cycle, thereby eliminating the third harmonic component of the leakage current [36], [37], [38]. The additional switching loss generated during sector switching is also suppressed by adjusting the carrier wave [39]. Nevertheless, the dc voltage utilization of this method remains only 86.6% of 7S-PWM. Furthermore, the elimination of the third harmonic component is relatively ineffective since the primary harmonic component in the leakage current is at the switching frequency or its multiples. Additionally, each switching cycle still consists of 12 switching actions, which is equivalent to 7S-PWM. By discarding small vectors, the CMV variation is restricted to $\pm U_{dc}/6 - 0$, thereby suppressing leakage current [40]. However, this method still requires 12 switching operations per cycle.

Discontinuous pulsewidth modulation (DPWM) ensures that each phase bridge does not switch over one-third of a fundamental cycle, thus reducing the number of switching actions and improving overall system efficiency [41], [42], [43]. Therefore, to further reduce system switching losses, a discontinuous pulse width modulation strategy with reduced CMV (RCMV-DPWM) was proposed in [44] and [45]. This approach limits the range of CMV to between $-U_{dc}/6$ and $U_{dc}/6$ by discarding switching vectors with CMV values greater than $U_{dc}/6$, and reduces the number of switching actions within a switching cycle to 8 by employing DPWM. However, this approach still results in a CMV variation of $U_{dc}/3$ within one switching cycle, which hinders further suppression of system leakage current. Moreover, the primary unresolved issue lies in how further reducing the CMV variation within a switching cycle contributes to leakage current suppression. No existing study provides a reasonable physical explanation or mathematical derivation for this phenomenon.

Aiming at the issue that the existing carrier-based modulation studies fail to further suppress the leakage current on the basis of five-segment sequence, this article proposes an enhanced carrier-based discontinuous pulse width modulation (ECB-DPWM) strategy for the T²LI, and the contribution can be highlighted as follows.

The basic idea of the proposed ECB-DPWM strategy is that the CMV variation within each fundamental cycle is not constrained any more, meanwhile the CMV variation within each clamping region is limited to $U_{dc}/6$ for further suppressing leakage current. To ensure that the CMV variation of all clamping regions are confined within $U_{dc}/6$, the sector division is optimized, and a novel clamping mode is proposed. Furthermore, a transition region is introduced to avoid sudden change in CMV when shifting between clamping regions. Finally, based on double Fourier decomposition, CMV harmonics are analyzed

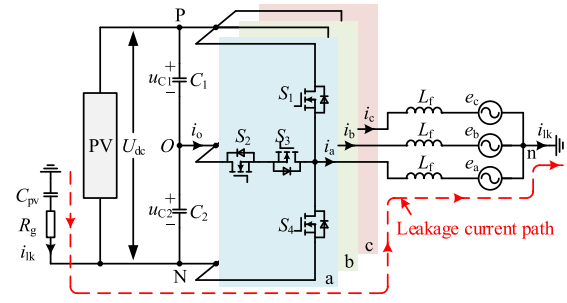


Fig. 1. Typical topology of the grid-tied system based on a T²LI.

TABLE I
RELATIONSHIP BETWEEN SWITCHING STATUS AND BRIDGE STATUS

Switching status				Bridge status	Output voltage
S_1	S_2	S_3	S_4		
ON	ON	OFF	OFF	P	$U_{dc}/2$
OFF	ON	ON	OFF	O	0
OFF	OFF	ON	ON	N	$-U_{dc}/2$

to fundamentally reveal the mechanism underlying the effectiveness of the proposed method.

The rest of this article is organized as follows. Section II outlines the fundamental operating principles of T²LI, and examines the mechanism underlying leakage current generation. Section III provides a detailed explanation of the working principles of the proposed methodology, as well as the implementation design. Section IV elucidates the fundamental principle of the proposed method for further suppression of leakage current, and provides a comprehensive performance comparison with existing methods. The feasibility of the proposed method and its superiority over existing methods are experimentally validated in Section V. Finally, Section VI concludes this article.

II. OPERATING PRINCIPLE OF T²LI AND ITS LEAKAGE CURRENT ANALYSIS

A. T²LI Topology and Basic Operation Principle

The T²LI is shown in Fig. 1, where R_g and C_{pv} denote the parasitic resistance and parasitic capacitance to ground of the dc source, such as the photovoltaic (PV) panel, respectively, and i_{lk} is the leakage current. C_1 and C_2 denote the dc-side equalizing capacitors, u_{C1} and u_{C2} correspond to the voltage values across C_1 and C_2 . i_o refers to the neutral-point current, i_a , i_b , and i_c represent the three-phase inductor currents, L_f is the filter inductor, and e_a , e_b , and e_c are the three-phase grid voltages.

There are four switching devices in each bridge. The switching states of S_1 and S_3 are complementary, as are the switching states of S_2 and S_4 . To prevent dc-side short-circuit faults, S_1 and S_4 cannot conduct simultaneously. Therefore, each bridge has three switch combinations corresponding to bridge states P, O, and N, as given in Table I.

There are 27 switch combinations for the three-phase bridge, which correspond to 19 switching vectors in the $\alpha\beta$ coordinate system. These vectors consist of 3 zero vectors, 6 medium vectors, 6 large vectors, and 12 small vectors. The small vectors

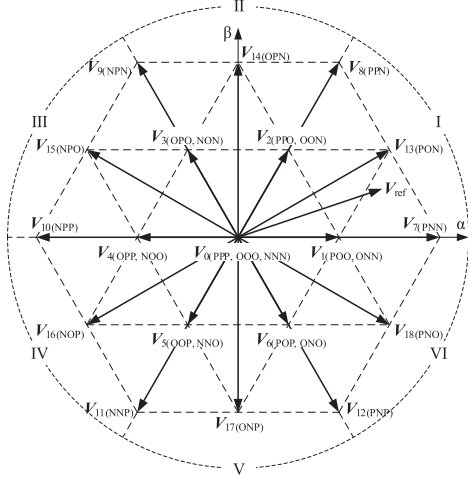


Fig. 2 Switching vector distribution of three-level inverters.

are further categorized into positive and negative types according to their effect on the NPV. Fig. 2 illustrates the distribution of these vectors.

B. Leakage Current Analysis

As illustrated in Fig. 1, there is a leakage current path in the inverter system. The voltage between the three-phase ac output and the negative bus on the dc side is

$$\begin{cases} u_{aN} = L_f \frac{di_a}{dt} + e_a + u_{nN} \\ u_{bN} = L_f \frac{di_b}{dt} + e_b + u_{nN} \\ u_{cN} = L_f \frac{di_c}{dt} + e_c + u_{nN} \end{cases} \quad (1)$$

The voltage between the ac-side neutral point n and the dc-side negative bus N can be expressed as follows:

$$u_{nN} = \frac{1}{C_{pv}} \int i_{lk} dt + R_g i_{lk}. \quad (2)$$

The relationship between leakage current and three-phase current can be derived from Fig. 1

$$i_{lk} = i_a + i_b + i_c. \quad (3)$$

Define the value of CMV as

$$u_{cm} = \frac{u_{aO} + u_{bO} + u_{cO}}{3}. \quad (4)$$

Assuming NPV is balanced, the u_{cm} values corresponding to all vectors can be obtained through (4), as given in Table II. Equations (1) through (4) can be integrated to obtain

$$u_{cm} = \frac{L_f}{3} \frac{di_{lk}}{dt} + \frac{1}{C_{pv}} \int i_{lk} dt + R_g i_{lk} - \frac{1}{2} U_{dc}. \quad (5)$$

The equivalent circuit diagram can be obtained by (5) as shown in Fig. 3.

As illustrated in Fig. 3, when the NPV is balanced, u_{cm} serves as the sole excitation source in the entire circuit, thus variations in u_{cm} induce leakage current. As shown in (4) and Table I, u_{cm} is related to the three-phase output voltage, which

TABLE II
CMV VALUES FOR DIFFERENT SWITCHING VECTORS

Switching vector type	Switching vectors	u_{cm}	Switching vectors	u_{cm}
Zero vectors	$V_0(PPP)$	$U_{dc}/2$	$V_0(OOO)$	0
	$V_0(NNN)$	$-U_{dc}/2$		
Small vectors	$V_1(ONN)$	$-U_{dc}/3$	$V_1(POO)$	$U_{dc}/6$
	$V_2(PPO)$	$U_{dc}/3$	$V_2(OON)$	$-U_{dc}/6$
	$V_3(NON)$	$-U_{dc}/3$	$V_3(OPO)$	$U_{dc}/6$
	$V_4(OPP)$	$U_{dc}/3$	$V_4(NOO)$	$-U_{dc}/6$
	$V_5(NNO)$	$-U_{dc}/3$	$V_5(OOP)$	$U_{dc}/6$
	$V_6(POP)$	$U_{dc}/3$	$V_6(ONO)$	$-U_{dc}/6$
Large vectors	$V_7(PNN)$	$-U_{dc}/6$	$V_8(PPN)$	$U_{dc}/6$
	$V_9(NPN)$	$-U_{dc}/6$	$V_{10}(NPP)$	$U_{dc}/6$
	$V_{11}(NNP)$	$-U_{dc}/6$	$V_{12}(PNP)$	$U_{dc}/6$
Medium vectors	$V_{13}(PON)$	0	$V_{14}(OPN)$	0
	$V_{15}(NPO)$	0	$V_{16}(NOP)$	0
	$V_{17}(ONP)$	0	$V_{18}(PNO)$	0

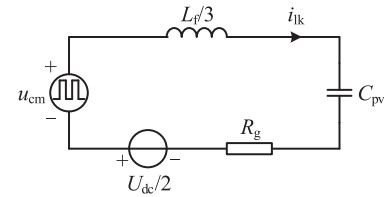


Fig. 3. Equivalent circuit of leakage current.

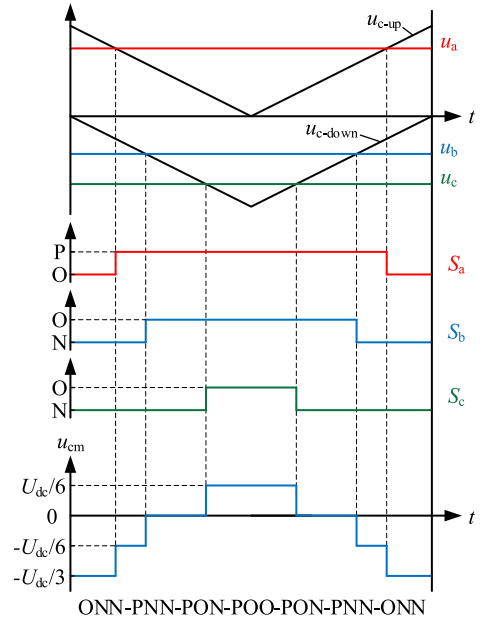


Fig. 4. Switching sequence and variation of u_{cm} in 7S-PWM.

is determined by the bridge status. The bridge status, in turn, changes with the switching sequence. Since different switching vectors correspond to different u_{cm} values, when the switching vector changes, the resulting variations in u_{cm} induce leakage current. Fig. 4 shows a switching sequence for 7S-PWM, where u_{c-up} and u_{c-down} represent the upper carrier and lower carrier, respectively, S_a , S_b and S_c denote the three-phase bridge status, respectively. As shown in the figure, as the switching vector changes, the u_{cm} value also varies accordingly, thereby inducing

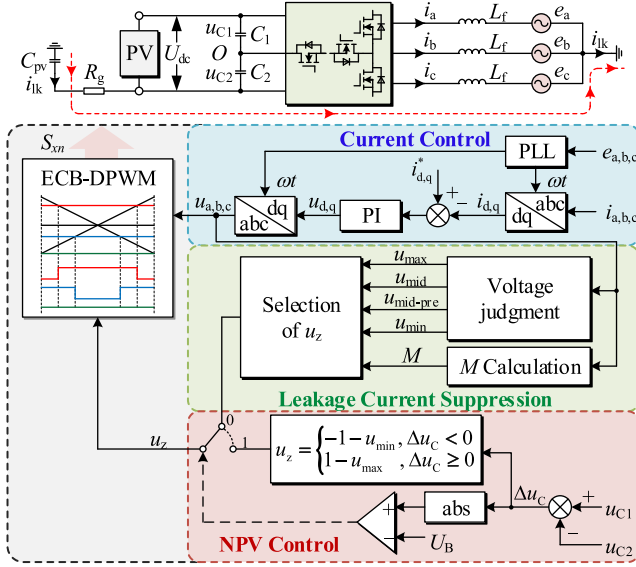


Fig. 5. Control block diagram of the carrier-based modulation.

leakage current. Therefore, from the modulation perspective, leakage current can be effectively suppressed by reducing CMV.

Numerous existing studies have been conducted to reduce the CMV variation by adjusting the modulation strategy, which in turn suppresses the leakage current. However, the relationship between CMV suppression and leakage current reduction is not purely linear, and current research has failed to provide a reasonable theoretical explanation for this phenomenon. Fundamentally, the effect of CMV suppression on leakage current should be analyzed from a harmonic perspective. Through harmonic analysis of CMV waveforms under different modulation strategies, the harmonic distribution characteristics of leakage current can be obtained, which fundamentally explains the underlying mechanism of leakage current suppression.

III. PROPOSED ECB-DPWM STRATEGY

The control block diagram of the carrier-based modulation is illustrated in Fig. 5, where $u_{a,b,c}$ is the three-phase reference voltage obtained from current control, u_{max} , u_{mid} , and u_{min} denote the maximum, intermediate and minimum values of $u_{a,b,c}$, respectively, $u_{mid-pre}$ is the value of u_{mid} from the previous switching cycle. M represents the system modulation index, as expressed in (6), U_{gm} is the grid voltage amplitude

$$M = U_{gm} / (U_{dc}/2). \quad (6)$$

The control block diagram is primarily divided into three functional components. During grid-connected operation, grid-following control is implemented via phase-locked loop and current control loop. Simultaneously, a boundary value U_B is established for NPV offset. When an excessive NPV offset is detected, compensation adjustment is achieved by selecting the u_{max} clamp in the P state or the u_{min} clamp in the N state. Otherwise, the control scheme focuses exclusively on leakage current suppression. The system modulation index and three-phase voltage are determined to select an appropriate zero

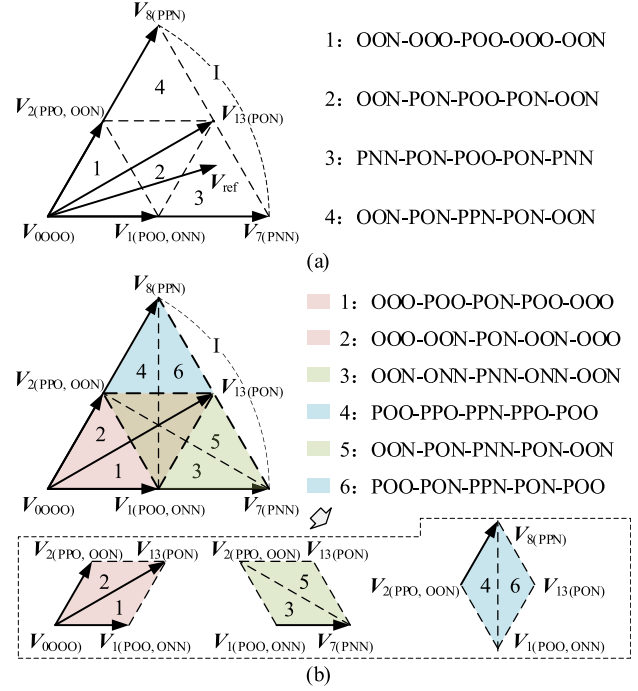


Fig. 6. Small sector division and available sequences corresponding to different regions with different modulation strategies in sector I. (a) RCMV-DPWM. (b) ECB-DPWM.

sequence voltage u_z , thereby enabling the implementation of a novel clamping mode, which provides additional suppression of the leakage current.

A. Principle of Leakage Current Further Suppression

According to the analysis, the variation in the CMV is identified as the fundamental cause of leakage current generation. Theoretically, if the CMV variation period is long enough, the leakage current will oscillate and attenuate to zero before the next excitation. However, in practice, the CMV varies with the switching states at a frequency exceeding the switching frequency, which prevents complete attenuation of the leakage current before the next CMV excitation. Therefore, from a modulation perspective, reducing the magnitude of CMV variations and extending the duration of CMV changes are fundamental methods for mitigating leakage current.

Taking sector I as an example, Fig. 6(a) illustrates the small sector division and switching sequence selection method in sector I for RCMV-DPWM. Each region corresponds to a specific sequence. All sequences adopt a five-segment structure, while discarding switching vectors with absolute CMV values exceeding $U_{dc}/6$, resulting in a total CMV variation of $U_{dc}/3$ per switching cycle. To simultaneously reduce switching losses, ECB-DPWM also adopts a five-segment sequence, further reducing the CMV variation to $U_{dc}/6$ within each switching cycle. Fig. 6(b) presents all six candidate sequences that fulfill the above requirements. Each sequence corresponds to specific operational regions, with some regions offering only one viable sequence while others provide three alternatives.

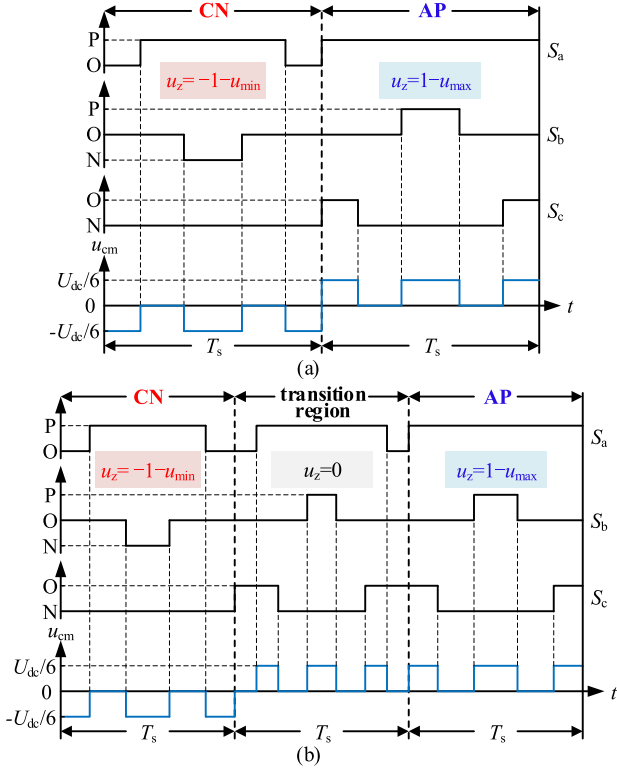


Fig. 11. Design of the clamping-mode switching transition region. (a) Without transition region. (b) With transition region.

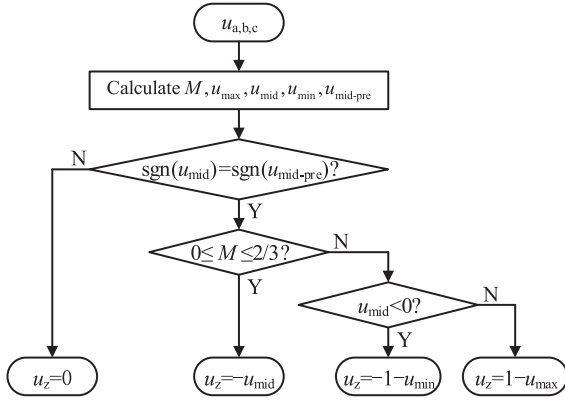


Fig. 12. Selection process of u_z .

The precise clamping of different regions is achieved by injecting u_z into the three-phase modulation waves. The design of u_z is illustrated in Fig. 12, where $\text{sgn}()$ is the sign function. When a change in the polarity of u_{mid} is detected, it corresponds to the switching moment of the clamping mode, during which u_z is adjusted to 0 to facilitate a smooth transition of the clamping mode. When the next switching cycle comes, the polarities of u_{mid} and $u_{\text{mid-pre}}$ become identical again, and normal clamping mode operation is restored. It can be noted that u_z is only related to M and the polarity of u_{mid} .

ECB-DPWM is achieved simply by changing the u_z injected into the three-phase modulation waves. This essentially alters the switching sequence and is independent of the topology. Therefore, the proposed method is applicable to all three-level

TABLE III
HARMONIC DISTRIBUTION COMPARISON OF CMV

	$M \leq 2/3$				$M > 2/3$			
	$m=0$ $n=0$	$m=0$ $n \neq 0$	$m \neq 0$ $n=0$	$m \neq 0$ $n \neq 0$	$m=0$ $n=0$	$m=0$ $n \neq 0$	$m \neq 0$ $n=0$	$m \neq 0$ $n \neq 0$
$u_{\text{cm}E}$	0	A_{0n}	0	A_{mn}	0	A_{0n}	0	A_{mn}
$u_{\text{cm}R}$	0	B_{0n}	B_{m0}	B_{mn}	0	A_{0n}	B_{m0}	B_{mn}

topologies such as NPC, ANPC, and CHB. Furthermore, the approach of suppressing system leakage current by reducing the CMV variation within a switching cycle can also be extended to multilevel topologies.

IV. PERFORMANCE ANALYSIS

A. CMV and Leakage Current

To validate the effectiveness of the proposed method, the CMV harmonic components of both ECB-DPWM and RCMV-DPWM under various operating conditions were derived using double Fourier decomposition, as presented in (7) and (8), where $u_{\text{cm}E}$ denotes the harmonic composition of ECB-DPWM; $u_{\text{cm}R}$ denotes the harmonic composition of RCMV-DPWM; $\omega_s t$ is the switching frequency subharmonic component; $\omega_0 t$ is the fundamental frequency subharmonic component; m and n are the harmonic orders of the switching frequency subharmonic component and the fundamental frequency subharmonic component, respectively; and $A_{0n}, A_{mn}, B_{0n}, B_{m0}, B_{mn1}, B_{mn2}$ are the amplitude coefficients of different harmonics for different modulation methods. The expressions of which are shown in the Appendix. Notably, unlike RCMV-DPWM, the CMV of ECB-DPWM contains no switching frequency subharmonic components

$$\begin{aligned}
 u_{\text{cm}E}(\omega_s t, \omega_0 t) &= \sum_{n=3,9,15,\dots}^{\infty} A_{0n} \cos(n\omega_0 t) \\
 &+ \sum_{m=1}^{\infty} \sum_{n=-\infty, n=\pm 3, \pm 9, \pm 15, \dots}^{\infty} A_{mn} \cos(m\omega_s t + n\omega_0 t) \quad (7) \\
 u_{\text{cm}R}(\omega_s t, \omega_0 t) &= \sum_{n=3,9,15,\dots}^{\infty} B_{0n} \cos(n\omega_0 t) \\
 &+ \sum_{m=1, m=\text{odd}}^{\infty} B_{m0} \cos(m\omega_s t) \\
 &+ \sum_{m=1, m=\text{even}}^{\infty} \sum_{n=-\infty, n=\pm 3, \pm 9, \pm 15, \dots}^{\infty} B_{mn1} \cos(m\omega_s t + n\omega_0 t) \\
 &+ \sum_{m=1, m=\text{odd}}^{\infty} \sum_{n=-\infty, n=\pm 6, \pm 12, \pm 18, \dots}^{\infty} B_{mn2} \cos(m\omega_s t + n\omega_0 t). \quad (8)
 \end{aligned}$$

The specific harmonic distribution of the two modulation strategies are given in Table III, where B_{mn} represents the sum of B_{mn1} and B_{mn2} . By combining (7) and (8), it can be more clearly observed that, compared with $u_{\text{cm}E}$, $u_{\text{cm}R}$ contains

TABLE IV
SYSTEM PARAMETERS

Description	Parameter	Value
DC Side Voltage	U_{dc}	200 V
DC Side Capacitance	C_1, C_2	2.24 mF
Inverter Side Filter Inductor	L_f	1 mH
Parasitic capacitance	C_{pv}	100 nF
Parasitic resistance	R_g	1 Ω
Rated current amplitude	I_{nmax}	10 A
Fundamental frequency	f_1	50 Hz
Switching frequency	f_s	20 kHz

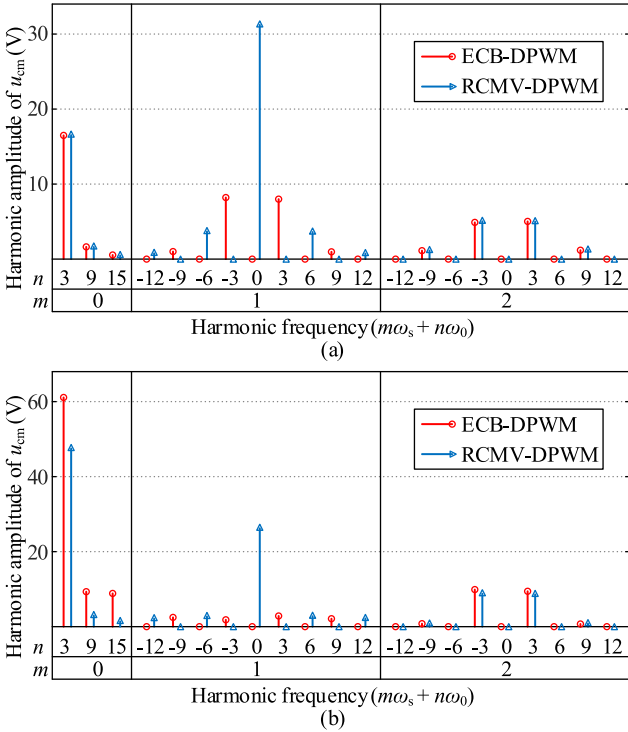


Fig. 13. Comparison of CMV harmonic distribution between ECB-DPWM and RCMV-DPWM. (a) $M = 0.4$. (b) $M = 0.8$.

odd-order switching frequency harmonic components, which exert a significant influence on leakage current.

The system parameters given in Table IV are substituted into (7) and (8) to determine the magnitude and distribution of each CMV subharmonic for the two modulation methods, as illustrated in Fig. 13. Based on the equivalent circuit shown in Fig. 3, the harmonic magnitudes and distributions of the leakage currents are derived, as shown in Fig. 14.

It is clearly demonstrated that the harmonic components of the ECB-DPWM are predominantly concentrated in the low-frequency range, with no spectral content at the switching frequency or its integer multiples. Due to the substantially higher associated leakage current loop impedance at these low frequencies, the resulting leakage currents become negligible. Conversely, the RCMV-DPWM contains larger harmonic components of odd-order switching frequency subharmonics, and the impedance of the leakage current loop is relatively small, resulting in significantly higher leakage currents. In summary,

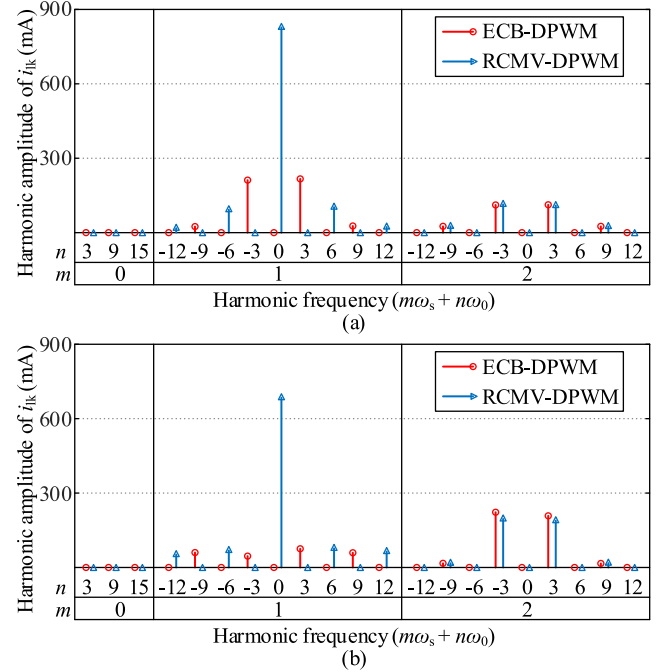


Fig. 14. Comparison of leakage current harmonic distribution between ECB-DPWM and RCMV-DPWM. (a) $M = 0.4$. (b) $M = 0.8$.

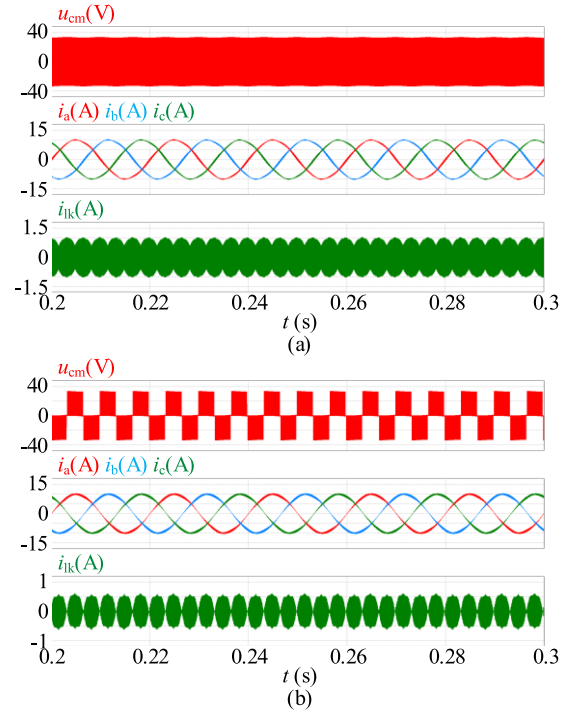


Fig. 15. Comparison of CMV and leakage current between ECB-DPWM and RCMV-DPWM at $M = 0.4$ and $\varphi = 0^\circ$. (a) RCMV-DPWM. (b) ECB-DPWM.

the fundamental mechanism enabling ECB-DPWM to achieve superior leakage current suppression lies in the elimination of switching frequency subharmonic components in the CMV.

By substituting the system parameters from Table III and taking $M = 0.4$ and $\varphi = 0^\circ$ as an example, the u_{cm} and i_{lk} waveforms of both modulation methods are compared in Fig. 15.

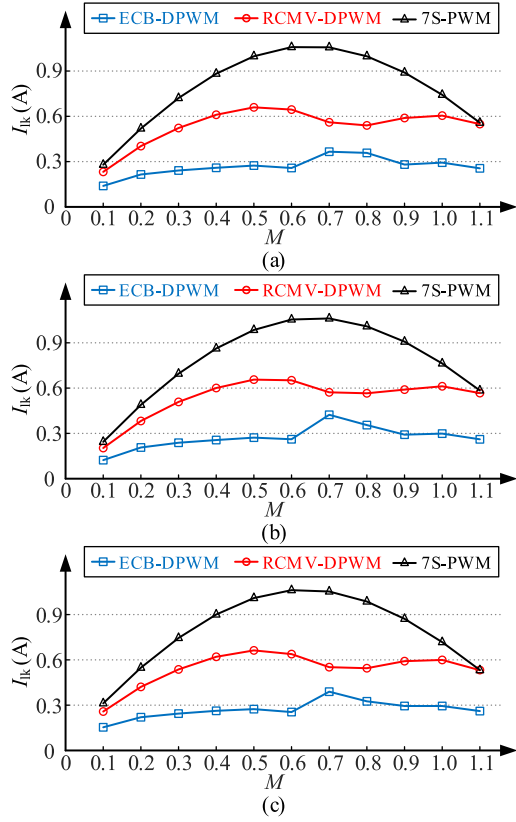


Fig. 16. RMS comparison of leakage current under different conditions. (a) $\varphi = 0^\circ$. (b) $\varphi = 60^\circ$. (c) $\varphi = -60^\circ$.

It is evident that during any given switching cycle, the CMV variation of the ECB-DPWM is limited to $U_{dc}/6$, whereas the CMV variation of the RCMV-DPWM is $U_{dc}/3$. The RMS values of the leakage current for ECB-DPWM and RCMV-DPWM are 0.259A and 0.613A, respectively. This indicates that the proposed method can suppress the leakage current to 42.2% of that in RCMV-DPWM.

To further validate the superiority of the proposed method under different operating conditions, the leakage current RMS values I_{ik} are compared for varying power factors and modulation indexes, as illustrated in Fig. 16. The results indicate that under varying power factors and modulation indexes, ECB-DPWM exhibits the lowest leakage current, while 7S-PWM yields the highest leakage current because it lacks suppression mechanisms.

B. Power Loss

In a nonisolated three-level inverter system, the total system loss comprises switching device turn-ON/turn-OFF losses, parasitic output capacitance losses, gate charge losses, diode reverse recovery losses, switching device conduction losses, and inductor losses [46]. Among these components, the modulation strategy primarily influences the switching device turn-ON/turn-OFF losses and conduction losses.

Fig. 17 illustrates loss model of the switching device over one switching cycle, where the power loss P_{Loss} consists of the switching loss P_{sw} and the conduction loss P_{con} . U_{sw}

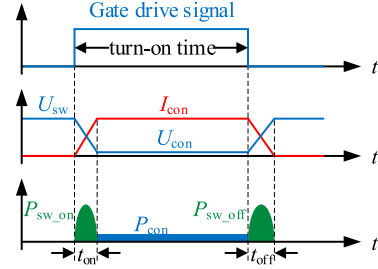


Fig. 17. Loss modeling of a switching device over one switching cycle.

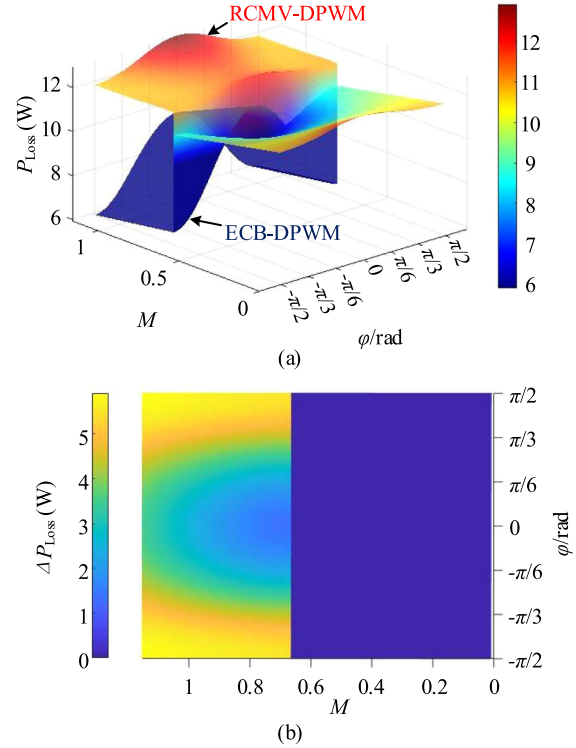


Fig. 18. Comparison of power losses for different modulation strategies. (a) Power losses of RCMV-DPWM and ECB-DPWM. (b) Difference in power losses between RCMV-DPWM and ECB-DPWM.

represents the blocking voltage across the switching device. I_{con} and U_{con} denote the conducting current and the forward voltage drop, respectively. t_{on} and t_{off} indicate the turn-ON and turn-OFF transition times, respectively. P_{sw_on} and P_{sw_off} denote the turn-ON and turn-OFF switching losses, respectively. Based on the analysis of Fig. 17, the P_{sw} and P_{con} can be derived as follows:

$$P_{sw} = \frac{1}{6} f_s U_{sw} I_{con} (t_{on} + t_{off}) \quad (9)$$

$$P_{con} = D I_{con}^2 R_{DS} \quad (10)$$

where D is the duty cycle of the current switching cycle, and R_{DS} denotes the ON-state resistance of the switching device. Thus, the P_{Loss} can be expressed as

$$P_{Loss} = P_{sw} + P_{con}. \quad (11)$$

As illustrated in Fig. 18(a), the P_{Loss} of ECB-DPWM and RCMV-DPWM is identical when $M \leq 2/3$. This is because both

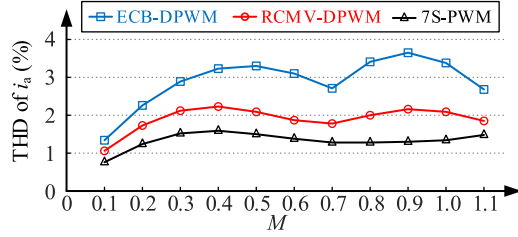


Fig. 19. Comparison of THD in grid-connected current under different modulation strategies.

TABLE V
COMPARISONS AMONG DIFFERENT MODULATION STRATEGIES

	7S-PWM	RCMV-DPWM	ECB-DPWM
Leakage current	Large	Medium	Small
Power loss	Large	Medium	Small
Current THD	Small	Medium	Large
Complexity	Simple	Complex	Moderate

modulation strategies employ the same clamping mode in this region, and the bridges corresponding to the intermediate phase voltage u_{mid} remain in the O state. The only difference is in the carrier modulation mode. When $M > 2/3$, ECB-DPWM exhibits a smaller P_{Loss} , since RCMV-DPWM still has some areas clamped in the O state when $M > 2/3$. Because S_2 and S_3 are MOSFET switches, the O state results in higher conduction losses, leading to a larger P_{Loss} for RCMV-DPWM. Fig. 18(b) shows the power loss difference between the two modulation strategies, where ΔP_{Loss} represents the difference between the power loss of RCMV-DPWM and ECB-DPWM. Through Fig. 18(b), the conclusions drawn from Fig. 18(a) can be more intuitively verified.

C. Waveform Quality

Compared to the 7S-PWM sequence, the five-segment sequence exhibits a larger inductance current ripple, resulting in higher total harmonic distortion (THD) [47]. Compared with RCMV-DPWM, ECB-DPWM violates the nearest three-vector (NTV) switching vector selection principle in certain regions [48], which leads to higher THD.

To ensure a rigorous comparison, the grid-connected current THD was tested under identical simulation conditions, with only the modulation strategy varied. The simulation results in Fig. 19 indicate that 7S-PWM has the smallest THD, whereas ECB-DPWM exhibits the poorest waveform quality, consistent with the preceding analysis. Therefore, although ECB-DPWM can effectively suppress system leakage current, it results in increased THD in grid-connected current.

Table V gives a comprehensive comparison of performance metrics across different modulation methods.

V. EXPERIMENTAL RESULTS

To further validate the effectiveness and superiority of the proposed method, a T²LI experimental platform was constructed as shown in Fig. 20. The control strategy and modulation strategy are implemented by TMS320F28377D microcontroller

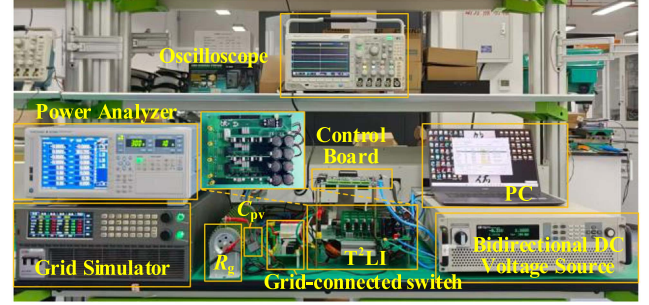


Fig. 20. Photograph of T²LI experimental platform.

TABLE VI
EXPERIMENTAL PARAMETERS

Description	Parameter	Value
DC Side Voltage	U_{dc}	200 V
DC Side Capacitance	C_1, C_2	2.24 mF
Inverter Side Filter Inductor	L_f	1 mH
Parasitic capacitance	C_{pv}	100 nF
Parasitic resistance	R	1 Ω
Rated current amplitude	I_{max}	5 A
Fundamental frequency	f_1	50 Hz
Switching frequency	f_s	20 kHz

(TI), while platform protection was realized through an FPGA chip 10M40SCE144C8G. The switching device is the MOSFET (IPW60R037CSFD) produced by Infineon, and the gate driver chip is the single-channel isolated gate driver (NSI6601C-DSWVR) produced by NOVOSENSE. In addition, Fig. 20 also gives the circuit design diagram. Detailed experimental parameters are given in Table VI.

A. Leakage Current Suppression

Fig. 21 shows the CMV comparison between RCMV-DPWM and ECB-DPWM under different modulation indexes, where k_{RE} indicates the modulation strategy switching signal, which signifies the switching of the modulation method from RCMV-DPWM to ECB-DPWM when it is switched to 1. Due to a twofold amplification in the control board circuitry, the waveform shows $k_{RE} = 2$ even though its actual value is 1.

The results demonstrate that ECB-DPWM maintains the CMV variation within $U_{dc}/6$ throughout each switching cycle, regardless of modulation index variations. Meanwhile, as illustrated in Fig. 22, when $M > 2/3$, the ac current ripple can be effectively suppressed by introducing a transition region of one switching cycle during clamping mode switching. Consequently, the leakage current is further reduced from 584 to 507 mA.

Fig. 23 shows the process of adding a transition region during clamping mode switching. Similar to the k_{RE} , the observed value of u_z appears doubled due to the two-fold amplification implemented in the control board circuitry. It is evident that u_z remains at 0 during the single switching cycle of the transition

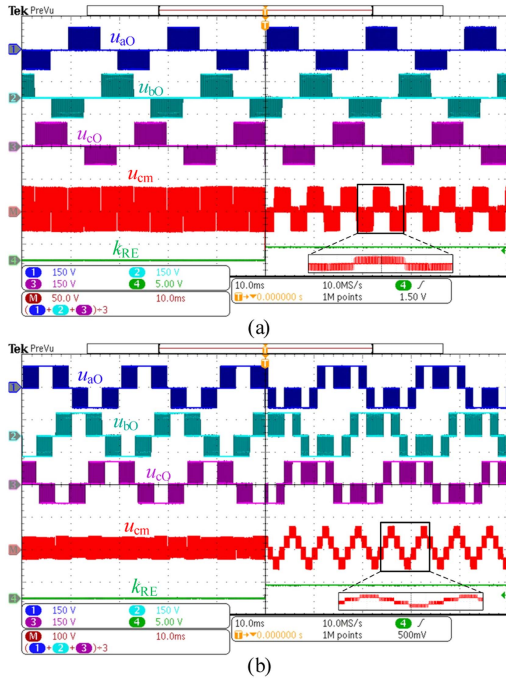


Fig. 21. Comparison of u_{cm} under different modulation methods. (a) $M = 0.4$. (b) $M = 1.0$.

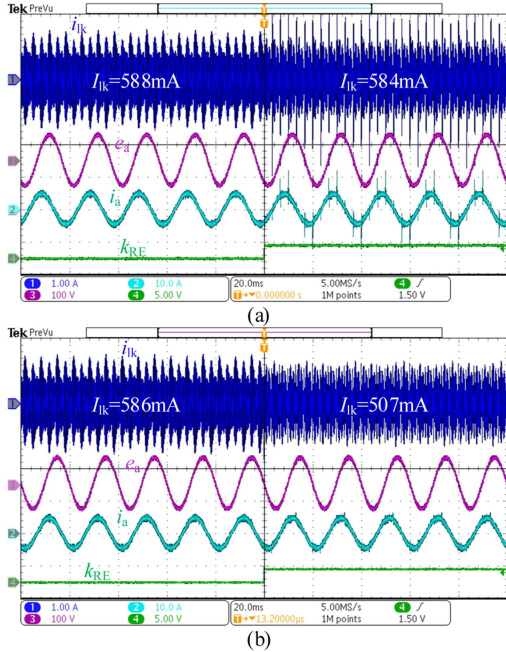


Fig. 22. Comparison of AC current and i_{lk} with/without transition region ($M = 0.8$, $\varphi = 60^\circ$). (a) Without transition region. (b) With transition region.

region, thereby facilitating a smooth transition between clamping modes.

Fig. 24 presents the leakage current characteristics of both RCMV-DPWM and ECB-DPWM across various modulation indexes and power factors. The results demonstrate that switching to ECB-DPWM modulation effectively reduces both the

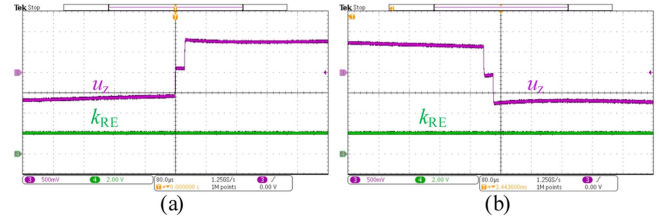


Fig. 23. Variation of u_z during clamping mode transitions. (a) Transition from N-clamping mode to P-clamping mode. (b) Transition from P-clamping mode to N-clamping mode.

amplitude and RMS value of leakage current under all tested operating conditions.

As a further validation, to provide a comprehensive evaluation of the proposed method's superiority, Fig. 25 compares the leakage current RMS values among RCMV-DPWM, ECB-DPWM, and 7S-PWM at three distinct power factors. The experimental data reveal that ECB-DPWM achieves the lowest leakage current RMS values in most operating conditions, confirming its superior leakage current suppression capability.

B. Comparison of System Efficiency

Given that system efficiency is a critical performance metric in industrial applications and that comprehensive verification of the proposed method is desirable, the system efficiency is also measured using a power analyzer. Fig. 26 presents a comparative analysis of system efficiency among RCMV-DPWM, ECB-DPWM, and 7S-PWM across three distinct power factors. The experimental results confirm that both RCMV-DPWM and ECB-DPWM exhibit higher efficiency than 7S-PWM under all operating conditions. This improvement is attributed to their five-segment switching sequence, which minimizes switching operations and consequently reduces switching losses.

Furthermore, ECB-DPWM shows the best system efficiency under all operating conditions. On the one hand, when $M > 2/3$, ECB-DPWM has smaller switching losses, thus achieving better system efficiency. On the other hand, effective suppression of system leakage current further reduces system losses. Consequently, even when $M \leq 2/3$, it continues to achieve superior system efficiency.

C. Waveform Quality Analysis

Fig. 27 presents a comparison of grid-connected current THD among ECB-DPWM, RCMV-DPWM, and 7S-PWM under identical test conditions. It can be observed that, owing to the reduced inductive current ripple of the seven-segment sequence, the 7S-PWM achieves the lowest grid-connected current THD. Compared to RCMV-DPWM, ECB-DPWM violates the NTV principle of switching vector selection in certain regions, which leads to the largest grid-connected current THD.

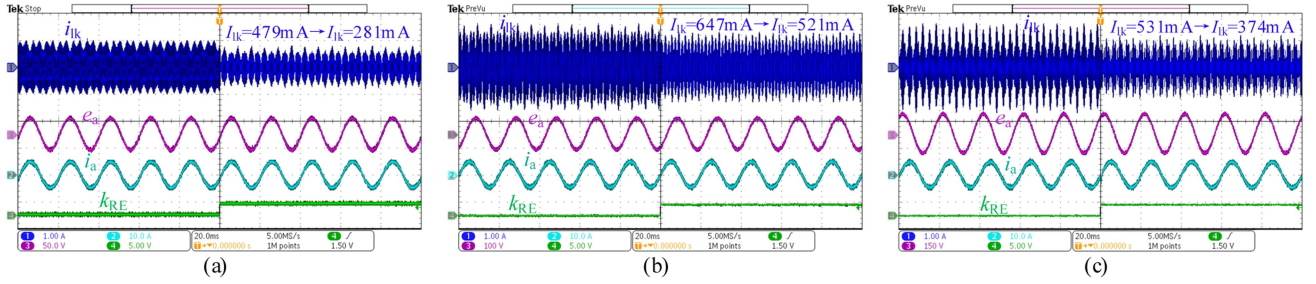


Fig. 24. Comparison of i_{ik} under different conditions. (a) $M = 0.3$; $\varphi = 0^\circ$. (b) $M = 0.6$; $\varphi = 60^\circ$. (c) $M = 1.1$; $\varphi = -60^\circ$.

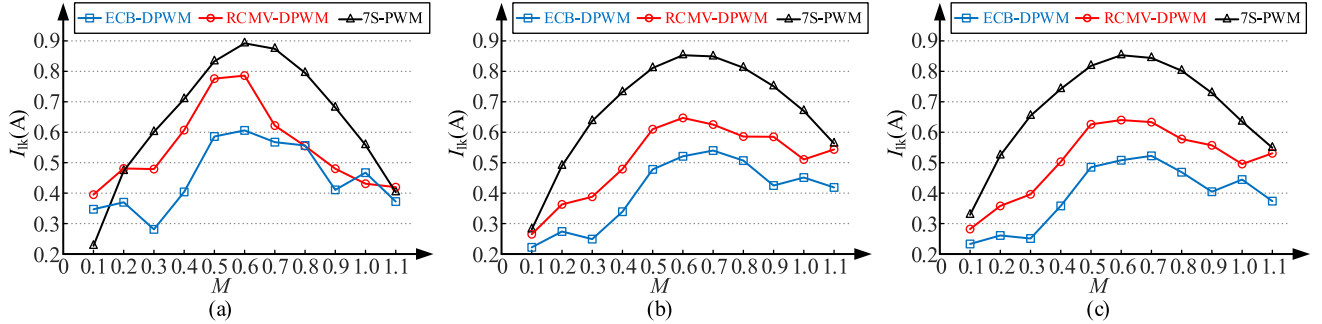


Fig. 25. RMS comparison of i_{ik} under different conditions. (a) $\varphi = 0^\circ$. (b) $\varphi = 60^\circ$. (c) $\varphi = -60^\circ$.

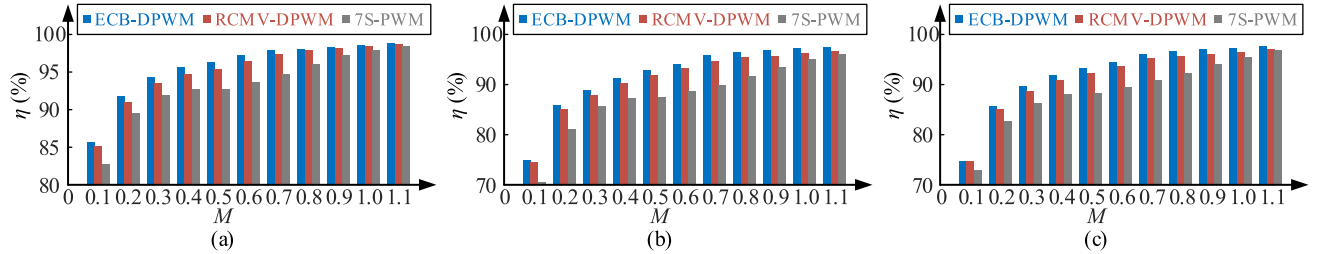


Fig. 26. Comparison of system efficiency under different conditions. (a) $\varphi = 0^\circ$. (b) $\varphi = 60^\circ$. (c) $\varphi = -60^\circ$.

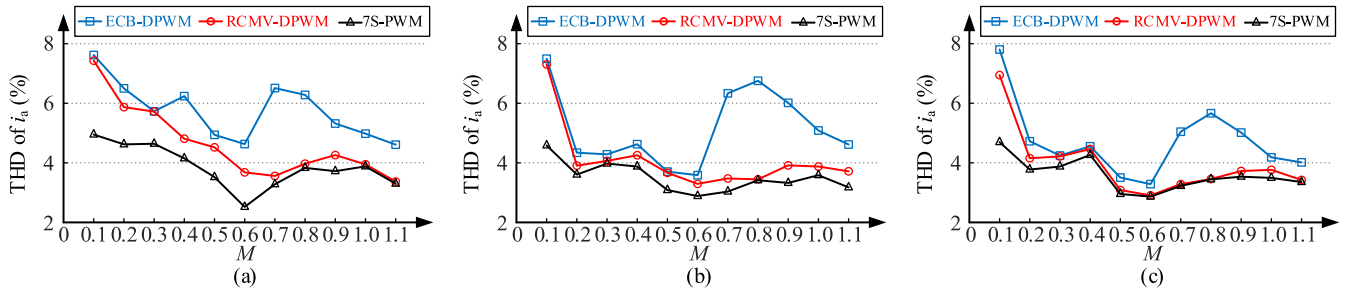


Fig. 27. Comparison of THD in grid-connected current under different modulation strategies. (a) $\varphi = 0^\circ$. (b) $\varphi = 60^\circ$. (c) $\varphi = -60^\circ$.

VI. CONCLUSION

This article focuses on the tradeoff between switching loss reduction and further suppression of leakage current in existing carrier modulation strategies, and proposes an enhanced carrier-based DPWM strategy to address these challenges. Further suppression of leakage current is achieved by reducing the CMV variation within each clamping region to $U_{dc}/6$ and by introducing a transition region to avoid sudden CMV changes. Moreover, double Fourier analysis reveals that the proposed

method can further suppress leakage current by effectively eliminating the switching frequency subharmonic components in CMV and leakage current. The experimental results prove that, compared with existing methods, not only is the system leakage current reduced under all operating conditions, but the system efficiency is also improved. Furthermore, analysis indicates that the proposed method is topology-independent and applicable to all three-level topologies. Additionally, the approach of reducing the CMV variation within a switching cycle to suppress system leakage current can also be generalized to multi-level topologies.

$$\begin{cases} A_{0n} = \frac{3\sqrt{3}MU_{dc}}{(n^2-1)\pi} \\ A_{mn} = \frac{4U_{dc}}{m\pi^2} \left[\sum_{k=0, k \neq \frac{n-1}{2}}^{\infty} (-1)^k J_{2k+1}(\xi) \cdot \left\{ \frac{1}{2k+1-n} \sin\left((2k+1-n)\frac{\pi}{6}\right) \cos\left((2k+1-n)\frac{\pi}{3} + \frac{n\pi}{6}\right) \right\} \right. \\ \left. + \sum_{k=0, k \neq \frac{-n-1}{2}}^{\infty} (-1)^k J_{2k+1}(\xi) \cdot \left\{ \frac{1}{2k+1+n} \sin\left((2k+1+n)\frac{\pi}{6}\right) \cos\left((2k+1+n)\frac{\pi}{3} - \frac{n\pi}{6}\right) \right\} \right] \end{cases} \quad (\text{A1})$$

$$\begin{cases} A_{0n} = \frac{U_{dc}}{\pi} \cdot \left(\frac{3\sqrt{3}M}{1-(-1)^{\frac{n+3}{6}n}} + (-1)^{\frac{n+3}{6}} \cdot \frac{6}{n} \right) \\ A_{mn} = \frac{8U_{dc}}{m\pi^2} \left[\sum_{k=0, k \neq \frac{n-1}{2}}^{\infty} (-1)^k J_{2k+1}(\xi) \cdot \frac{1}{2k+1-n} \cdot \left\{ \cos^2\left((2k+1-n)\frac{\pi}{4}\right) \sin\left((2k+1-n)\frac{\pi}{12}\right) \cos\left((2k+1-n)\frac{\pi}{12} + \frac{n\pi}{6}\right) \right\} \right. \\ \left. + \sum_{k=0, k \neq \frac{-n-1}{2}}^{\infty} (-1)^k J_{2k+1}(\xi) \cdot \frac{1}{2k+1+n} \cdot \left\{ \cos^2\left((2k+1+n)\frac{\pi}{4}\right) \sin\left((2k+1+n)\frac{\pi}{12}\right) \cos\left((2k+1+n)\frac{\pi}{12} - \frac{n\pi}{6}\right) \right\} \right] \end{cases} \quad (\text{A2})$$

$$\begin{cases} B_{0n} = \frac{3\sqrt{3}MU_{dc}}{(n^2-1)\pi} \\ B_{m0} = -\frac{8U_{dc}}{m\pi^2} \sum_{k=0}^{\infty} (-1)^k J_{2k+1}(\xi) \cdot \frac{1}{2k+1} \sin\left((2k+1)\frac{\pi}{6}\right) \cos\left((2k+1)\frac{\pi}{3}\right) \\ B_{mn1} = \frac{4U_{dc}}{m\pi^2} \\ \left[\sum_{k=0, k \neq \frac{n-1}{2}}^{\infty} (-1)^k J_{2k+1}(\xi) \cdot \left\{ \frac{1}{2k+1-n} \left[\sin\left((2k+1-n)\frac{\pi}{6}\right) \cos\left((2k+1-n)\frac{\pi}{3} + \frac{n\pi}{6}\right) \right] \right\} \right. \\ \left. + \sum_{k=0, k \neq \frac{-n-1}{2}}^{\infty} (-1)^k J_{2k+1}(\xi) \cdot \left\{ \frac{1}{2k+1+n} \left[\sin\left((2k+1+n)\frac{\pi}{6}\right) \cos\left((2k+1-n)\frac{\pi}{3} + \frac{n\pi}{6}\right) \right] \right\} \right] \\ B_{mn2} = -\frac{4U_{dc}}{m\pi^2} \sum_{k=0}^{\infty} (-1)^k J_{2k+1}(\xi) \cdot \left\{ \frac{1}{2k+1-n} \left[\sin\left((2k+1-n)\frac{\pi}{6}\right) \cos\left((2k+1-n)\frac{\pi}{3} + \frac{n\pi}{6}\right) \right] \right. \\ \left. + \frac{1}{2k+1+n} \left[\sin\left((2k+1+n)\frac{\pi}{6}\right) \cos\left((2k+1-n)\frac{\pi}{3} + \frac{n\pi}{6}\right) \right] \right\} \end{cases} \quad (\text{A3})$$

$$\begin{cases} B_{0n} = \left\{ \frac{3\sqrt{3}MU_{dc}}{\pi} \left[\frac{1}{1-n} \cos((1-n)\theta'_2) + \frac{1}{1+n} \cos((1+n)\theta'_2) \right] + \frac{3U_{dc}}{n\pi} [\sin(n\theta'_2) + \sin(n\theta'_1)] \right\} \\ B_{m0} = \frac{8U_{dc}}{m\pi^2} \sum_{k=0}^{\infty} (-1)^k J_{2k+1}(\xi) \\ \cdot \frac{1}{2k+1} \left[-\cos\left((2k+1)\frac{\pi}{3}\right) \sin\left((2k+1)\left(-\frac{\pi}{6} + \theta'_2\right)\right) + \sin\left((2k+1)\frac{\pi}{2}\right) \cos\left((2k+1)\frac{\pi}{6}\right) \cos\left((2k+1)\left(\frac{\pi}{6} + \theta'_2\right)\right) \right] \\ B_{mn1} = -\frac{8U_{dc}}{m\pi^2} \\ \left[\sum_{k=0, k \neq \frac{n-1}{2}}^{\infty} (-1)^k J_{2k+1}(\xi) \cdot \frac{1}{2k+1-n} \cdot \left\{ \cos\left((2k+1-n)\frac{\pi}{3} + \frac{n\pi}{6}\right) \sin\left((2k+1-n)\frac{\pi}{6}\right) \cos\left((2k+1-n)\theta'_2\right) \right\} \right. \\ \left. + \sum_{k=0, k \neq \frac{-n-1}{2}}^{\infty} (-1)^k J_{2k+1}(\xi) \cdot \frac{1}{2k+1+n} \cdot \left\{ \cos\left((2k+1+n)\frac{\pi}{3} - \frac{n\pi}{6}\right) \sin\left((2k+1+n)\frac{\pi}{6}\right) \cos\left((2k+1+n)\theta'_2\right) \right\} \right] \\ B_{mn2} = \frac{4U_{dc}}{m\pi^2} \sum_{k=0}^{\infty} (-1)^k J_{2k+1}(\xi) \\ \cdot \left\{ \frac{1}{2k+1-n} \left[\sin\left((2k+1-n)\frac{\pi}{2} - \frac{n\pi}{6}\right) \cos\left((2k+1-n)\theta'_2\right) - \cos\left((2k+1-n)\frac{\pi}{6} + \frac{n\pi}{6}\right) \sin\left((2k+1-n)\theta'_2\right) \right] \right. \\ \left. + \frac{1}{2k+1+n} \left[\sin\left((2k+1+n)\frac{\pi}{2} + \frac{n\pi}{6}\right) \cos\left((2k+1+n)\theta'_2\right) - \cos\left((2k+1+n)\frac{\pi}{6} - \frac{n\pi}{6}\right) \sin\left((2k+1+n)\theta'_2\right) \right] \right\} \end{cases} \quad (\text{A4})$$

$$\begin{cases} \theta'_1 = \frac{\pi}{3} - \arcsin\left(\frac{1}{\sqrt{3}M}\right) \\ \theta'_2 = \arcsin\left(\frac{1}{\sqrt{3}M}\right) \end{cases} \quad (\text{A5})$$

$$\xi = \sqrt{3}mM\pi. \quad (\text{A6})$$

APPENDIX

The clamping modes vary among different modulation methods and across various modulation indexes, with corresponding differences in their double Fourier decomposition expressions. (A1) and (A2) present the Fourier coefficient expressions for ECB-DPWM at modulation indexes $M \leq 2/3$ and $M > 2/3$, respectively. (A3) and (A4) provide the corresponding expressions for RCMV-DPWM under the same modulation index conditions. The expressions for θ'_1 and θ'_2 are given in (A5), and the expression for ξ is presented in (A6), shown at the top of this page.

REFERENCES

- [1] B. Gutierrez, S. Baek, and J.-S. Lai, "Space vector pulsewidth modulation based on a novel digital coordinate transformation for multilevel inverters eliminating common-mode voltages," *IEEE Trans. Ind. Electron.*, vol. 71, no. 10, pp. 11732–11742, Oct. 2024.
- [2] R. Goel, D. Eitta, R. V. Chavali, and A. Dey, "A fault tolerant modulation scheme for a hybrid multilevel inverter in the event of open-switch fault," *IEEE Trans. Power Electron.*, vol. 40, no. 3, pp. 3861–3872, Mar. 2025.
- [3] M. Wu, J. Pang, Z. Ma, K. Wang, K. Yang, and Y. Li, "A unified fault tolerant control and neutral-point voltage balance strategy for three-level T-type inverters under double signal PWM," *IEEE Trans. Power Electron.*, vol. 39, no. 11, pp. 14204–14215, Nov. 2024.

- [4] S. Xu et al., "A simultaneous diagnosis method for power switch and current sensor faults in grid-connected three-level NPC inverters," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 1104–1118, Jan. 2023.
- [5] Y. Wang et al., "An improved model predictive voltage control with reduced computational burden for T-type three-phase three-level inverters," *IEEE Trans. Power Electron.*, vol. 39, no. 2, pp. 2115–2127, Feb. 2024.
- [6] J. Chen, J. Deng, L. Ming, Z. Xin, W. Yin, and P. Wang, "A variable switching frequency control for ZVS three-phase three-level T-type inverter using hybrid discontinuous PWM," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 13456–13466, Nov. 2023.
- [7] W. Zhang, Y. He, X. Wang, and J. Chen, "A comprehensive method for online switch fault diagnosis and capacitor condition monitoring of three-level T-type inverters," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 10183–10195, Aug. 2023.
- [8] H.-P. N. Le, K. D. Pham, and N.-V. Nguyen, "Analyses, modeling, and SVPWM control of a three-level T-NPC inverter to reduce common-mode voltage under open-circuit fault in a neutral-point switch," *IEEE Access*, vol. 12, pp. 104708–104727, 2024, doi: [10.1109/ACCESS.2024.3434696](https://doi.org/10.1109/ACCESS.2024.3434696).
- [9] Q. Yan et al., "Optimization of the symmetrical SVPWM for three-level T-type inverters with unbalanced and oscillated neutral-point voltages," *IEEE Trans. Ind. Electron.*, vol. 71, no. 4, pp. 4026–4037, Apr. 2024.
- [10] J.-H. Kim, S.-H. Park, J. Lee, J.-H. Cho, G.-H. Cho, and H.-S. Kim, "A floating voltage source-based turn-off snubber for a non-isolated multi-level SiC DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 72, no. 1, pp. 390–400, Jan. 2025.
- [11] S. Pourfarrokhi, J. Adabi, and F. Zare, "A new grid-connected asymmetrical multilevel converter for PV application," *IEEE Trans. Power Electron.*, vol. 39, no. 9, pp. 11256–11265, Sep. 2024.
- [12] H. Le, A. Dekka, and D. Ronanki, "Model predictive control with inherent CMV reduction capability for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 71, no. 7, pp. 6730–6737, Jul. 2024.
- [13] Z. Zhang et al., "Common-mode voltage reduction modulation strategy based on nearest four voltage vectors optimization for Vienna rectifier," *IEEE Trans. Power Electron.*, vol. 39, no. 3, pp. 2954–2965, Mar. 2024.
- [14] Z. Wang et al., "Common-mode voltage suppression strategy for CHB-based motor drive based on topology and modulation optimization," *IEEE Trans. Power Electron.*, vol. 40, no. 1, pp. 1697–1716, Jan. 2025.
- [15] Y. Zou et al., "An optimized DPWM with reduced leakage current for three-phase three-level inverters with unbalanced neutral-point voltage," *IEEE Trans. Power Electron.*, vol. 39, no. 12, pp. 1697–1716, Dec. 2024.
- [16] Q. Yan, H. Chen, T. Zhao, X. Yuan, L. Zhang, and R. Zhao, "A carrier-based discontinuous space-vector PWM for common-mode voltage reduction in dual-input three-level T-type inverters with unbalanced neutral-point voltages," *IEEE Trans. Power Electron.*, vol. 39, no. 9, pp. 11020–11033, Sep. 2024.
- [17] Z. Li, X. Xing, C. Du, X. Li, C. Liu, and R. Zhang, "Leakage current suppression for dual-DC-port DC-AC converter in PV-battery hybrid system," *IEEE Trans. Power Electron.*, vol. 40, no. 5, pp. 7315–7328, May 2025.
- [18] Z. Hu, X. Xing, C. Liu, R. Zhang, and F. Blaabjerg, "A modified discontinuous PWM method for three-level inverters with the improved LCL filter," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 5498–5505, May 2024.
- [19] C. Zhang, Y. Jiang, X. Xing, X. Li, C. Qin, and B. Zhang, "Passivity-based control method for three-level photovoltaic inverter to mitigate common-mode resonant current," *IEEE Trans. Ind. Informat.*, vol. 19, no. 9, pp. 9733–9744, Sep. 2023.
- [20] J. Wang, X. Liu, Y. Xun, and S. Yu, "Common mode noise reduction of three-level active neutral point clamped inverters with uncertain parasitic capacitance of photovoltaic panels," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6974–6988, Jul. 2020.
- [21] Z. Shen, M. Chen, H. Wang, X. Wang, and F. Blaabjerg, "EMI filter robustness in three-level active neutral-point-clamped inverter," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4641–4657, Apr. 2022.
- [22] Z. Lin, H. Zhang, P. Zhang, and Y. Li, "Analysis and reduction of zero-sequence LC-resonant current in DPWM-modulated 3 Φ LCL-type grid-connected inverter with neutral line," *IEEE Trans. Ind. Electron.*, vol. 71, no. 9, pp. 11721–11725, Sep. 2024.
- [23] X. Li, X. Xing, C. Zhang, A. Chen, C. Qin, and G. Zhang, "Simultaneous common-mode resonance circulating current and leakage current suppression for transformerless three-level T-type PV inverter system," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4457–4467, Jun. 2019.
- [24] T. Yu, W. Wan, and S. Duan, "A modulation method to eliminate leakage current and balance neutral-point voltage for three-level inverters in photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 70, no. 2, pp. 1635–1645, Feb. 2023.
- [25] F. Guo et al., "Hybrid active modulation strategy for three-level neutral-point-clamped converters in high-speed aerospace drives," *IEEE Trans. Ind. Electron.*, vol. 70, no. 4, pp. 3449–3460, Apr. 2023.
- [26] R. Phukan, X. Zhao, P. Asfaux, D. Dong, and R. Burgos, "Investigation of staggered PWM scheme for AC common mode current minimization in SiC-based three-phase inverters," *IEEE Trans. Transp. Electrification*, vol. 8, no. 4, pp. 4378–4390, Dec. 2022.
- [27] H. Du, Y. He, J. Qiu, and J. Liu, "Research on SVPWM method for leakage current suppression and switching loss reduction in nonisolated three-level inverters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 12, no. 3, pp. 2960–2971, Jun. 2024.
- [28] K. L. Zhou and D. W. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis three-phase inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 1, pp. 186–196, Feb. 2002.
- [29] Z. Li and C. Wang, "Novel synchronized three-level SVPWM algorithms with boundary sampling methods," *IEEE Trans. Power Electron.*, vol. 40, no. 10, pp. 15718–15729, Oct. 2025.
- [30] M. Zhao, Q. Ge, J. Zhu, K. Wang, B. Zhang, and L. Zhao, "Improved synchronized SVPWM strategy for high-power three-level active neutral point clamped traction inverter," *IEEE Trans. Power Electron.*, vol. 40, no. 2, pp. 3189–3209, Feb. 2025.
- [31] Y. Shen, Z. Chen, H. Huang, Q. Wang, and Y. Liu, "Asymmetric space vector pulse width modulation for the phase current reconstruction in three-phase inverters," *IEEE Trans. Power Electron.*, vol. 40, no. 1, pp. 1686–1696, Jan. 2025.
- [32] R. Sarker, A. Bhattacharya, S. Debnath, A. Castillo-Atoche, and A. Datta, "A novel FPGA-driven HD-SPWM architecture with zero-sequence voltage insertion strategy for three-level NPC inverter," *IEEE Trans. Ind. Informat.*, vol. 20, no. 9, pp. 10814–10824, Sep. 2024.
- [33] A. Lewicki, D. Kondratenko, and C. I. Odeh, "Hybridized PWM strategy for three- and multiphase three-level NPC inverters," *IEEE Trans. Ind. Electron.*, vol. 71, no. 8, pp. 8279–8290, Aug. 2024.
- [34] Y. Zou et al., "Enhanced carrier-based discontinuous PWM for three-level inverters with unbalanced neutral-point voltage," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 12, no. 2, pp. 2176–2187, Apr. 2024.
- [35] M. Lak, Y.-T. Tsai, B.-R. Chuang, T.-L. Lee, and M. H. Moradi, "A hybrid method to eliminate leakage current and balance neutral point voltage for photovoltaic three-level T-type inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 12070–12089, Oct. 2021.
- [36] K. D. Pham and N. V. Nguyen, "A reduced common-mode-voltage pulsewidth modulation method with output harmonic distortion minimization for three-level neutral-point-clamped inverters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6944–6962, Jul. 2020.
- [37] K. D. Pham, M.-V. Doi, and N. V. Nguyen, "Hybrid pulse-width modulation strategy with reduced high-frequency common-mode voltage to lower RMS motor leakage current for a three-level neutral point clamped converter," *IEEE Access*, vol. 11, pp. 131302–131318, 2023, doi: [10.1109/ACCESS.2023.3336767](https://doi.org/10.1109/ACCESS.2023.3336767).
- [38] K. D. Pham and N.-V. Nguyen, "A hybrid asymmetric average zero CMV PWM strategy with four nearest vectors to optimize harmonic distortion for a three-level NPC converter," *IEEE Trans. Ind. Electron.*, vol. 72, no. 2, pp. 1091–1100, Feb. 2025.
- [39] K. D. Pham and N. V. Nguyen, "Switching loss optimization for a pulse width modulation strategy with reduced CMV and improved output harmonic distortion for a three-level NPC converter," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12118–12133, Oct. 2022.
- [40] S. S. Hakami, L. M. Halabi, and K.-B. Lee, "Dual-carrier-based PWM method for DC-link capacitor lifetime extension in three-level hybrid ANPC inverters," *IEEE Trans. Ind. Electron.*, vol. 70, no. 4, pp. 3303–3314, Apr. 2023.
- [41] H.-J. Cho, K.-H. Sui, K.-H. Kim, J.-J. Jung, and H.-S. Kim, "Carrier-based minimum-loss discontinuous PWM with neutral-point voltage balancing for three-level NPC inverters," *IEEE Trans. Power Electron.*, vol. 40, no. 9, pp. 13895–13906, Sep. 2025.
- [42] J. Kucera, O. Lipcak, and J. Bauer, "Efficient modulation strategies to minimize switching losses in dual-inverter systems," *IEEE Trans. Transp. Electrification*, vol. 11, no. 4, pp. 9764–9777, Aug. 2025.
- [43] D.-J. Lee, J.-H. Choi, and U.-M. Choi, "Reliability improved discontinuous pulse width modulation for NPC inverters operated at high modulation index," *IEEE Trans. Power Electron.*, vol. 40, no. 7, pp. 9876–9888, Jul. 2025.
- [44] W. Jiang, H. Jiang, S. Liu, S. Ji, and J. Wang, "A carrier-based discontinuous PWM strategy for T-type three-level converter with reduced common mode voltage, switching loss, and neutral point voltage control," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1761–1771, Feb. 2022.

- [45] J. Wang et al., "A novel discontinuous modulation strategy with reduced common-mode voltage and removed DC offset on neutral-point voltage for neutral-point-clamped three-level converter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7637–7649, Aug. 2019.
- [46] X. Pan, H. Li, Y. Liu, T. Zhao, C. Ju, and A. K. Rathore, "An overview and comprehensive comparative evaluation of current-fed-isolated-bidirectional DC/DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2737–2763, Mar. 2020.
- [47] Q. Li, D. Jiang, and Y. Zhang, "Analysis and calculation of current ripple considering inductance saturation and its application to variable switching frequency PWM," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12273–12275, Dec. 2019.
- [48] L. M. K. Johny, J. Mathew, and K. Gopakumar, "Improved trans-Z-source active-neutral-point-clamped multilevel inverter with continuous input current for induction motor drives," *IEEE Trans. Ind. Electron.*, vol. 72, no. 2, pp. 1281–1291, Feb. 2025.



Xin Zhang (Student Member, IEEE) received the B.S. degree in electrical engineering from Northeast Electric Power University, Jilin, China, in 2019, and the M.S. degree in electrical engineering in 2022 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His current research interests include modulation strategy optimization and performance enhancement for three-level inverters.



Zeng Liu (Senior Member, IEEE) received the B.S. degree from Hunan University, Changsha, China, and the M.S. and the Ph.D. degrees from Xi'an Jiaotong University (XJTU), Xi'an, China, in 2006, 2009, and 2013, respectively, all in electrical engineering.

He was the Faculty Member in electrical engineering with joined XJTU, where he is currently a Full Professor. From 2015 to 2017, he was with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, as a Visiting Scholar. His research interests include

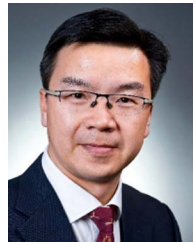
modulation, control and stability of power converters for renewable energy and energy storage applications.

Dr. Liu was the recipient of two Prize Paper Awards in IEEE TRANSACTIONS ON POWER ELECTRONICS, and the CPSS Science and Technology Progress Award. He is currently an Associate Editor FOR IEEE OPEN JOURNAL OF POWER ELECTRONICS and on the Editorial Board for the Energies, and served as Secretary-General for 2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems and 2020 The 4th International Conference on HVDC.



Xujie Wang received the B.S. and M.S. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2022 and 2025, respectively.

His research interests include the key technology and optimization design of three-phase four-wire converters.



Jinjun Liu (Fellow, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University (XJTU), Xi'an, China, in 1992 and 1997, respectively.

After that, he was the Faculty Member with the XJTU Electrical Engineering School. From 1999 to 2002, he was a Visiting Scholar with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. In 2002, he was promoted to a Full Professor and then the Head of the Power Electronics and Renewable

Energy Center, XJTU, which now comprises nearly 30 faculty members and around 300 graduate students and carries one of the leading power electronics programs in China. From 2005 to 2010, he was the Associate Dean of the Electrical Engineering School, XJTU. From 2009 to 2015, he was the Dean for Undergraduate Education with XJTU, where he is currently a Distinguished Professor of Power Electronics. He has coauthored three books (including one textbook), has published more than 500 technical papers in peer-reviewed journals and conference proceedings, holds more than 70 invention patents (China/US/EU), and has delivered many times plenary keynote speeches and tutorials at IEEE conferences or China national conferences. His research interests include modeling, control, and design methods for power converters and electronic power systems, power quality control and utility applications of power electronics, and microgrids for sustainable energy and distributed generation.

Dr. Liu was the IEEE Power Electronics Society Region 10 Liaison and then China Liaison for 10 years. He has been an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS since 2006. He was the 2015–2021 Vice President of IEEE PELS. He was on the Board of the China Electrotechnical Society during 2012–2020 and was elected the Vice President in 2013 and the Secretary-General in 2018 for the CES Power Electronics Society. He was 2013–2021 Vice President for International Affairs of the China Power Supply Society (CPSS). Since 2013, he has been the Vice Chair of the Chinese National Steering Committee for College Electric Power Engineering Education Programs. Since 2016, he has been the inaugural Editor-in-Chief of CPSS Transactions on Power Electronics and Applications. He was elected the President of CPSS in November 2021. He was the recipient of many times governmental awards at the national level or provincial/ministerial level for scientific research/teaching achievements. He was also the recipient of the 2006 Delta Scholar Award, the 2014 Chang Jiang Scholar Award, the 2014 Outstanding Sci-Tech Worker of the Nation Award, the 2016 State Council Special Subsidy Award, the IEEE Transactions on Power Electronics 2016 and 2021 Prize Paper Awards, the Nomination Award for the Grand Prize of 2020 Bao Steel Outstanding Teacher Award, and the 2022 Fok Ying Tung Education and Teaching Award.