Letters

A Wide-Frequency-Range GaN Half-Bridge Driver With Reconfigurable High-Voltage Charge Sharing Path

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***Abstract*—To address the challenges of narrow operating frequency range and insufficient high-side supply rail voltage at high frequencies in gallium nitride half-bridge drivers, this article proposes a driver capable of operating at 1–10 MHz switching frequency with a high-side driving voltage of 4.99 V. The proposed driver incorporates two novel techniques: reconfigurable charge sharing path (RCSP) and high-voltage charge sharing. By modulating the resistance of the charge sharing path through RCSP, the charging rate of the sharing path can be regulated, thereby enabling the driver to operate over a wider switching frequency range. The high-voltage charge sharing technique enhances the charging rate of the bootstrap path, thereby ensuring sufficient high-side driving voltage even at elevated switching frequencies. This design was fabricated and verified using a 0.18-μm bipolar-CMOS-DMOS process. It achieves a high-side driving voltage ranging from 4.02 to 4.99 V at switching frequencies of 1–10 MHz, demonstrating a 28.8% enhancement in the high-side driving voltage at 10 MHz.**

***Index Terms*—Gallium nitride (GaN), half-bridge driver, high-voltage charge sharing, reconfigurable, wide frequency range.**

I. Introduction

OWING to their excellent figure of merit ($R_{ON} \times Q_G$), gallium nitride (GaN) devices are extensively employed in half-bridge switching power converters operating at MHz frequencies [1].

However, in high-frequency applications, conventional bootstrap (CB)-based half-bridge drivers suffer from insufficient high-side supply rail voltage due to limitations in bootstrap charging speed. While increasing the driving voltage can enhance bootstrap charging speed and ensure adequate high-side supply rail voltage at high frequencies, this approach leads to an overshoot of the high-side supply rail voltage during low-frequency operation, potentially causing power device breakdown, as illustrated in Fig. 1(a). Insufficient high-side supply rail voltage increases the on-resistance of the power switch, as shown in Fig. 1(b), thereby reducing conversion efficiency. Furthermore, most existing GaN half-bridge drivers are efficient only within a relatively fixed frequency range [2], [3], which restricts the design flexibility of half-bridge converter control circuits and results in poor versatility.

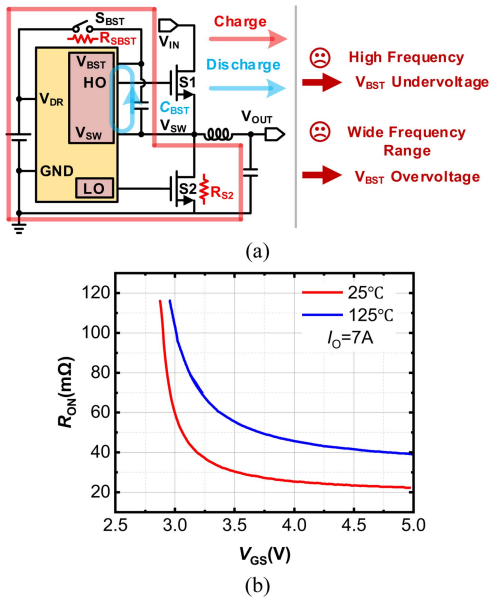

Fig. 1. (a) Schematic diagram of the bootstrap-based half-bridge driver operating principle. (b) Relationship between the on-resistance of EPC2019 and its gate-driving voltage.

In response to the challenges of narrow switching frequency range and insufficient high-side supply rail voltage in GaN half-bridge drivers, numerous solutions have been proposed by researchers. Chen et al. [4] employed a high-voltage charge-sharing scheme to enhance the charging speed of the bootstrap path, ensuring sufficient high-side supply rail voltage at high frequencies. However, this approach only operates effectively at a fixed frequency of 10 MHz. Yan et al. [5] utilized a bandgap comparator to monitor the bootstrap capacitor voltage in real time, controlling the switching of the bootstrap transistor. This

Received 15 October 2025; revised 25 November 2025; accepted 15 December 2025. Date of publication 18 December 2025; date of current version 19 January 2026. This work was supported by the Joint Funds of the National Natural Science Foundation of China under Grant U23A20367. *(Corresponding authors: Zhuoqi Guo; Zhongming Xue; Li Geng.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3645788.

Digital Object Identifier 10.1109/TPEL.2025.3645788

method achieves sufficient high-side supply rail voltage within 2–10 MHz, but the voltage consistently exceeds 5 V and increases with frequency, raising the risk of GaN gate breakdown and compromising robustness. Ming et al. [6] adopted a synchronous bootstrap method. At 10 MHz with a duty cycle of 0.825, the high-side supply rail voltage was only 3.9 V, resulting in significant power loss. In [7], during the bootstrap charging phase, the bootstrap capacitor acquires only a limited amount of charge. While using a smaller bootstrap capacitor helps maintain sufficient high-side supply rail voltage, it consequently restricts the size of the power switches that can be driven. Therefore, achieving a wide operating frequency range along with sufficient and safe high-side supply rail voltage at high frequencies has become a primary design challenge for GaN half-bridge drivers [8].

To address the limitations of narrow switching frequency range and insufficient high-side supply rail voltage in GaN half-bridge drivers, the following two innovative approaches are adopted in this work.

1) *Reconfigurable charge sharing path (RCSP):* By adjusting the resistance of the charge sharing path through configurable switches, the charging speed of the path can be regulated, thereby enabling the driver to operate over a wider frequency range.
2) *High-voltage charge sharing:* The high-voltage charge sharing technique enhances the maximum charging speed of the bootstrap path, ensuring sufficient high-side driving voltage even at high frequencies, thereby improving the efficiency of the half-bridge topology.

Experimental results demonstrate that the proposed GaN half-bridge driver achieves a high-side driving voltage ranging from 4.02 to 4.99 V across a switching frequency range of 1–0 MHz. Notably, it exhibits a 28.8% improvement in high-side driving voltage at 10 MHz, effectively validating the significant efficacy of both RCSP and the high-voltage charge sharing technique in ensuring sufficient high-side supply rail voltage across varying operating frequencies.

II. Proposed Half-Bridge Driver

A. Analysis of the Bootstrap Circuit Under High-Frequency Operation

A schematic diagram of the bootstrap circuit principle is shown in Fig. 1(a). When the low-side power transistor is turned ON, V_{SW} is pulled to ground. The bootstrap capacitor C_{BST} is charged through the path formed by the parasitic resistance R_{SBST} of the bootstrap switch and the parasitic resistance R_{S2} of the low-side power transistor, with V_{DR} as the supply voltage. When V_{SW} is pulled to V_{IN} by the high-side power transistor, the voltage across C_{BST} is bootstrapped to supply the high-side rail.

When the bootstrap switch and the low-side power transistor are turned ON,the bootstrap charging process begins. The variation of V_{BST} over charging time can be expressed as

$$V_{BST}(t) = V_{DR} + (V_{BST0} - V_{DR})\, e^{-\frac{t}{(R_{SBST}+R_{S2})C_{BST}}} \quad (1)$$

where V_{DR} is the driving supply voltage, V_{BST0} is the initial voltage of the bootstrap capacitor, R_{SBST} is the parasitic resistance of the bootstrap switch, R_{S2} is the parasitic resistance of the low-side power transistor, and C_{BST} is the bootstrap capacitance.

When the high-side transistor is turned ON, the bootstrap capacitor discharges through the power transistor. At this time, C_{BST} acts as the power source for the entire floating supply rail and must provide charge to the entire driver module.

During the bootstrap charging process, the following relationship holds:

$$\frac{dV_{BST}(t)}{dt} = \frac{V_{DR} - V_{BST0}}{C_{BST}\,(R_{SBST} + R_{S2})} e^{-\frac{t}{\tau_1}}. \quad (2)$$

Defining the time constant $\tau_1 = (R_{SBST} + R_{S2})\, C_{BST}$. At high frequencies, the charging time per cycle for the bootstrap circuit is much shorter than τ_1, allowing (2) to be simplified as

$$\frac{dV_{BST}}{dt} = \frac{V_{DR} - V_{BST0}}{C_{BST}\,(R_{SBST} + R_{S2})}. \quad (3)$$

According to (3), the charging rate of the bootstrap capacitor remains constant and is proportional to the difference between the driving voltage and the initial voltage of the bootstrap capacitor, while being inversely proportional to the total parasitic resistance along the bootstrap path.

The charge injected into the bootstrap capacitor C_{BST} per switching cycle is given by

$$Q_{CH} = \frac{V_{DR} - V_{BST0}}{R_{S2} + R_{BST}} \cdot \frac{1 - D}{f_{SW}} \quad (4)$$

where D is the duty cycle of the control signal, and f_{SW} is the frequency of the control signal.

According to (4), at higher switching frequencies, the amount of charge acquired by the bootstrap capacitor per cycle decreases. When Q_{CH} becomes less than the charge required to drive the high-side power transistor per cycle, the high-side supply rail voltage drops until Q_{CH} equals the charge demand, reaching an equilibrium state. In other words, the high-side supply rail voltage decreases as the operating frequency of the half-bridge converter increases. This reduction can lead to degraded power stage efficiency and may even trigger undervoltage lockout protection in the control circuitry.

B. Circuit Implementation

The schematic of the proposed wide switching frequency range GaN half-bridge driver with RCSP is illustrated in Fig. 2. The circuit comprises a high-side power transistor driver circuit, a low-side power transistor driver circuit, a low-voltage bootstrap circuit, a high-voltage bootstrap circuit, and the configurable switches along with their corresponding driver circuits within the RCSP. The design employs two bootstrap capacitors to form the high-side supply rail: a low-voltage capacitor charged by V_{DR}, and a high-voltage capacitor directly charged from V_{IN}. These two capacitors share charge through the RCSP. This approach not only ensures sufficient high-side supply rail voltage at high frequencies but also regulates the charge sharing rate by reconfiguring the path resistance, preventing excessive high-side voltage at low frequencies that could cause power device breakdown. Consequently, the proposed GaN half-bridge

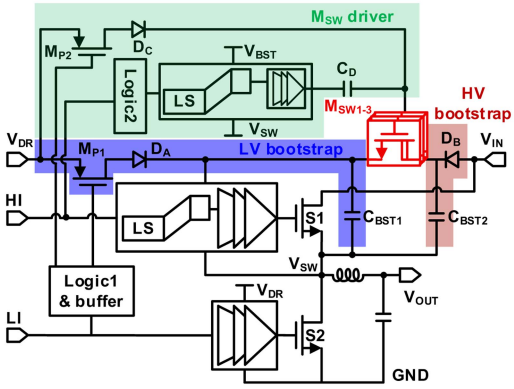
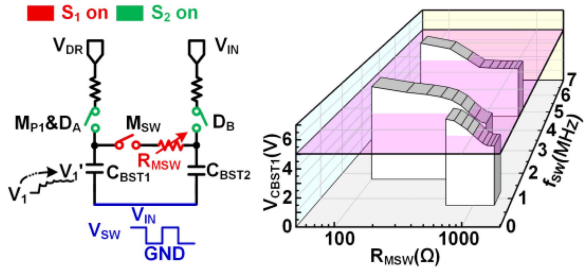


Fig. 2. Schematic diagram of proposed half-bridge driver circuit.



(a) (b)

Fig. 3. (a) Equivalent model of proposed RCSP technology. (b) Simulation diagrams of C_{BST1} and R_{MSW} at different frequencies.

driver achieves adequate high-side supply rail voltage across a wide operating frequency range.

When the low-side power transistor is turned ON, V_{SW} is pulled down to near ground potential. During this phase: C_{BST1} is charged by V_{DR} through switch transistor M_{P1} and diode D_A; C_{BST2} is charged by V_{IN} through diode D_B; C_D (10 nF) is charged by V_{DR} through switch transistor M_{P2} and diode D_C.

When the high-side power transistor is turned ON, the bootstrapped supply rail powers the high-side driver. At this time, the size-tunable transistor M_{SW} is driven by C_D and fully turned ON, enabling charge sharing between C_{BST1} and C_{BST2} to elevate the V_{BST} voltage, thereby meeting the driving voltage requirement of the power transistor. In addition, to prevent transient noise from interfering with the high-voltage domain logic signals, we have adopted the level shifter presented in [9].

During the dead time, V_{SW} may drop to a range of -3 to -2 V depending on the load current. At this point, switch transistors M_{P1} and M_{P2} are turned OFF to stop charging capacitor C_{BST1}, thereby preventing overcharging phenomena.

During the charge sharing phase, it is critical to ensure that the bootstrapped voltage rail provides sufficient drive voltage for the power transistor while preventing excessive voltage that could cause gate breakdown. The RCSP technique ensures a sufficient and safe high-side rail voltage by regulating the on-resistance of M_{SW}.

Equivalent model of the proposed RCSP technology is shown in Fig. 3(a). When the high-side power transistor S_1 is turned

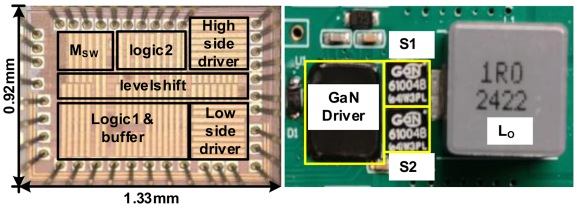


Fig. 4. Die micrograph of the fabricated chip and test PCB for proposed GaN half-bridge driver.

ON, the following condition must be satisfied:

$$V_1(t) = \frac{C_{BST1}V_1 + C_{BST2}V_2}{C_{BST1} + C_{BST2}} - \frac{C_{BST2}(V_2 - V_1)}{C_{BST1} + C_{BST2}} e^{-\frac{t}{\tau_2}} \quad (5)$$

where V_1 is the initial voltage of C_{BST1} and V_2 is the initial voltage of C_{BST2}. The time constant is defined as $\tau_2 = (R_{MSW}C_{BST1}\ C_{BST2})/\ (C_{BST1} + C_{BST2})$, where R_{MSW} is the parasitic resistance of M_{SW}. Due to the relatively small parasitic capacitance of the power transistor gate, which rapidly reaches charge sharing equilibrium with C_{BST1}, $V_1(t)$ can be regarded as the gate voltage of the high-side power transistor.

Under high-frequency operation, the turn-ON time of the high-side power transistor is much shorter than τ_2. Applying a first-order Taylor expansion to (5), it can be simplified to

$$V_1(t) = V_1 + \frac{(V_2 - V_1)t}{RC_{BST1}}. \quad (6)$$

Then, when the high-side power transistor is turned OFF, the following relationship holds:

$$V_1' = V_1 + \frac{(V_2 - V_1)D}{f_{SW}RC_{BST1}}. \quad (7)$$

where f_{SW} is the operating frequency of the switching converter and D is the duty cycle of the control signal.

As can be observed from (7), the speed of high-voltage charge sharing can be regulated by adjusting the resistance of the charge sharing path, thereby enabling this design to operate over a wider frequency range. Fig. 3(b) shows the simulation results of V_{CBST1} versus the on-resistance of M_{SW} (R_{MSW}) under different frequencies in the application scenario with duty cycle of 0.5. Furthermore, the proposed design ensures a sufficient and safe high-side rail voltage across input voltages (V_{IN}) of 6, 12, 24, 36, and 48 V, as well as under different duty cycles.

III. Measurement Results

The GaN gate driver was designed and fabricated with 0.18 μm high voltage (HV) bipolar-CMOS-DMOS (BCD) technology. A die micrograph is shown on the left side of Fig. 4, with a total chip area of 1.22 mm^2. The test printed circuit board (PCB) for the half-bridge converter is shown on the right-hand side of Fig. 4, employing two enhancement-mode GaN devices (GS61004B) as power transistors to validate the driver's performance under high-frequency conditions. The inductor and output capacitor values are 1 μH and 4.7 μF, respectively.

Under the condition of a half-bridge converter input voltage of 12 V and an output voltage of 6 V, the switching frequencies were set to 1, 5, and 10 MHz (The dead time is set to 10% of the cycle

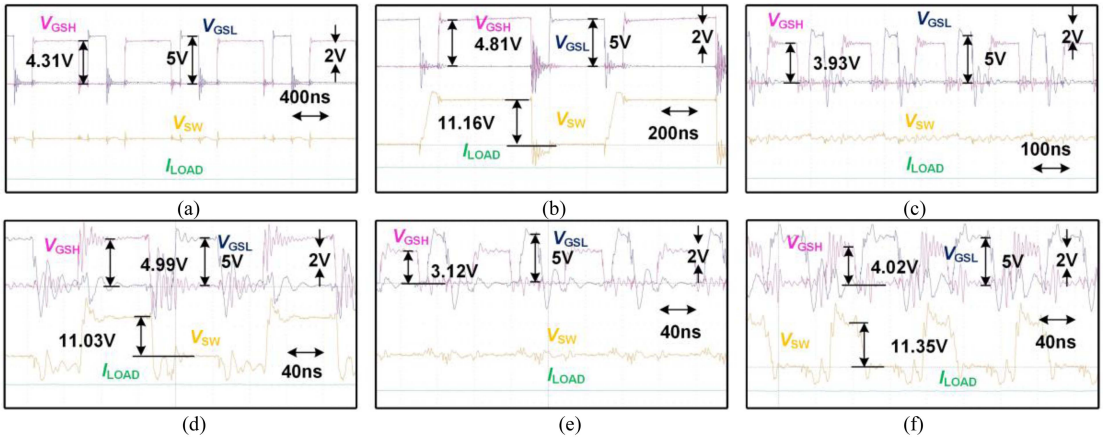


Fig. 5. Comparative measured waveforms of conventional and proposed drivers across frequencies. (a) CB at 1 MHz. (b) Proposed bootstrap at 1 MHz. (c) CB at 5 MHz. (d) Proposed bootstrap at 5 MHz. (e) CB at 10 MHz. (f) Proposed bootstrap at 10 MHz. (Since V_{IN} has minimal impact on high-side rail voltage, test results of the CB scheme were obtained by setting V_{IN} to zero.)

period), with the reconfigurable switches configured as $\mathrm{M_{SW1}}$, $\mathrm{M_{SW2}}$, and $\mathrm{M_{SW3}}$, respectively. The corresponding measurement waveforms of the conventional and proposed drivers are shown in Fig. 5. Measurement results show that the proposed driver improves the high-side supply rail voltage by 11.6% , 27.0% , and 28.8% at 1, 5, and 10 MHz, respectively, compared to a CB driver. Moreover, it maintains a safe operating voltage even when negative voltage spikes occur during the dead time.

In order to demonstrate the advantages of proposed RCSP technology over traditional control method, an analysis and comparison of their efficiency and losses were conducted through postsimulation. As shown in Fig. 6(a), at 1 and 5 MHz under relatively light loads, the efficiency of the RCSP technique is slightly lower than that of the CB scheme. This is because, at 1 and 5 MHz with a 50% duty cycle, the high-side rail voltage does not drop significantly, and conduction losses are not the dominant factor under light-load conditions. However, the RCSP technique introduces additional losses P_{RCSP} due to high-voltage charge sharing, resulting in a marginal efficiency reduction. Under heavy loads, conduction losses become dominant, and the RCSP technique demonstrates a clear improvement in system efficiency compared to CB approach. In 10 MHz applications, CB scheme fails to provide an adequate high-side rail voltage, preventing proper turning-ON of the high-side power transistor and leading to low efficiency. In contrast, the proposed RCSP technology, via its reconfigurable high-voltage charge-sharing path, continues to deliver sufficient drive voltage, significantly enhancing system efficiency.

Under the application scenario of 12–6 V conversion with $I_{\mathrm{LOAD}} = 6$ A, the simulated loss breakdown of the proposed RCSP technique and CB scheme at 1 and 5 MHz is shown in Fig. 6(b). It mainly includes four types of losses: driving loss (P_{DR}), conduction loss and switching loss (P_{DR} and P_{SW}), inductor direct current resistance loss (P_{DCR}), and RCSP loss (P_{RCSP}). Although the RCSP technique introduces additional P_{RCSP}, it significantly reduces P_{CON}, resulting in a net efficiency improvement and enhanced system performance. At 10 MHz, CB scheme fails to provide sufficient high-side rail voltage, preventing the high-side power transistor from turning ON completely and causing the power stage to malfunction. Therefore, a detailed analysis at 10 MHz is not provided.

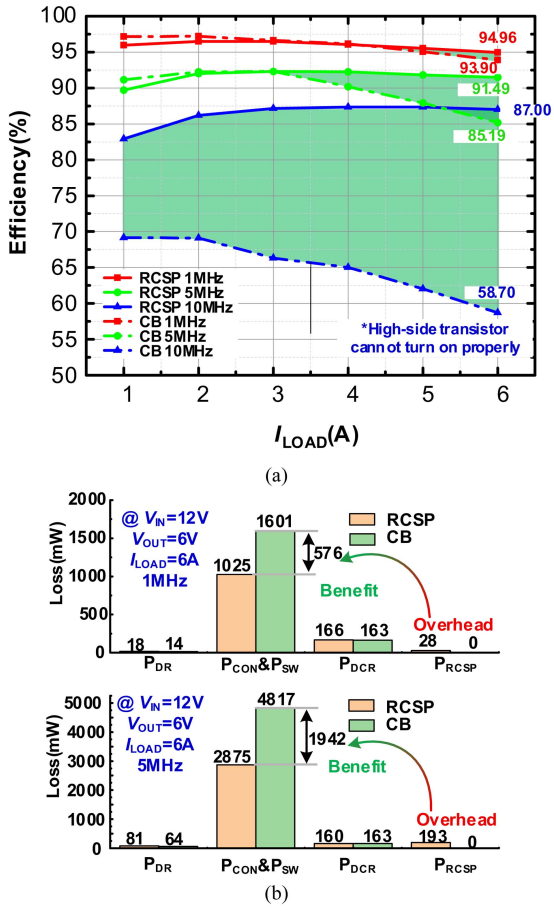


Fig. 6. (a) Postsimulation results of efficiency comparison between proposed driver and CB driver under different conditions. (b) Comparison diagram of detailed losses between the proposed driver and CB driver.

TABLE I
COMPARISON WITH PREVIOUS WORKS

Design	TPE' 22[4]	TIE' 20[5]	CICC' 22[6]	ISSCC' 16[7]	This work
Process	0.25 μm BCD	0.18 μm BCD	0.5 μm HV	0.35 μm HV	0.18 μm BCD
F_{SW} [MHz]	10	2–10	0.5–10	10–30	1–10
V_{IN} [V]	12	3–18	3–48	3–40	12
V_{OUT} [V]	6	3.3	3.3/5	5	6
$I_{O,MAX}$ [A]	0.65	5	5	1.2	5.1
$P_{OUT,MAX}$ [W]	3.25	16.5	13	6	30.6
V_{BST} [V]	4.365	4.92–5.44	3.9–5.1	5.1	4.02–4.99
V_{BST}/ Charge time [V/ns][#]	4.365/ 58	5.44/ 73	3.9/ 73	5.1/ 32	4.99/ 50
Techniques for Wide-Frequency V_{BST}	Without	BGRCC	DMSB	ABB	RCSP
Peak EFF [%]	89.9	91.58	90.1	90.7	91.91
Active area [mm^2]	1.5	2.72	2.045	0.48	1.22

[#]Maximum Achievable Values

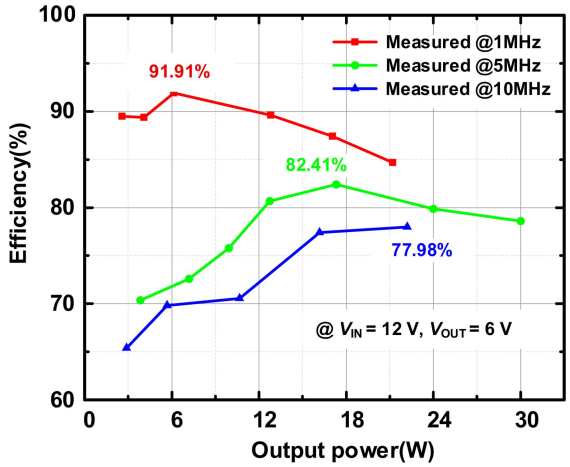


Fig. 7. Efficiency curves of the half-bridge converter employing the proposed RCSP half-bridge driver at 1–10 MHz.

The measured efficiency curve of the half-bridge converter under operating frequencies of 1–10 MHz, with an input voltage of 12 V and an output voltage of 6 V, is shown in Fig. 7. The maximum output current is 5.1 A, and the maximum output power is 30.6 W. Due to increased switching and driving losses at high frequencies, along with exacerbated gate oscillations, the measured maximum output power at 5 and 10 MHz is relatively low. The peak efficiency (Peak EFF) of 91.91% is achieved at 1 MHz with an output power of 6 W.

A performance comparison between this work and other state-of-the-art GaN half-bridge drivers is summarized in Table I. By employing the high-voltage charge sharing technique and RCSP, the proposed driver achieves a high-side driving voltage ranging from 4.02 to 4.99 V over a switching frequency range of 1–10 MHz. Compared to the designs in [5], [6], and [7], this work eliminates the need for a high-precision detection circuit, thereby enhancing robustness. In addition, unlike the design in [4], it avoids the issue of high-side rail overvoltage at low frequencies. Furthermore, thanks to the use of off-chip bootstrap capacitors and the high-voltage charge sharing strategy, the driver is capable of driving larger power transistors, enabling the half-bridge converter to deliver higher output power. Consequently, the output power achieved by the half-bridge converter in this work is also the highest among state-of-the-art implementations.

IV. CONCLUSION

This letter presents a high-frequency gate driver designed for GaN half-bridge applications. By incorporating high-voltage charge sharing and RCSP, the proposed half-bridge driver ensures sufficient high-side driving voltage at high frequencies while supporting operation over a wide frequency range. Within a switching frequency range of 1–10 MHz, the driver maintains a high-side supply rail voltage between 4.02 and 4.99 V. At 10 MHz, it achieves a 28.8% improvement in high-side driving voltage compared to CB drivers. Due to its insensitivity to instantaneous control signals, this design is well-suited for both steady-state and transient operation under pulsewidth modulation and constant on-time control schemes. Furthermore, the use of off-chip capacitors and the high-voltage charge sharing strategy allows the driver to drive larger power transistors, demonstrating its potential for high-frequency and high-power applications.

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