A Novel Single-Phase Common-Ground Rectifier With Active Power Decoupling for DC Microgrids

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***Abstract*—To suppress the leakage current in non-isolated rectifiers and reduce dc-link capacitance, this article proposes a novel single-phase common-ground rectifier with active power decoupling as the interface between an ac power supply system and a dc load. Leakage current is minimized by connecting the ground on the ac side to the negative terminal on the dc side. By transferring dual-frequency power fluctuations to decoupling capacitors without any additional switches, the dc-link capacitance is significantly reduced, thereby decreasing the size of the rectifier. The topology derivation and the operating principle is described, the voltage across the semiconductors and decoupling capacitor, state space model and constraint are analyzed respectively. The mathematical model of the proposed rectifier is built and a voltage-current dual closed-loop controller is designed to regulate the output dc voltage. The passive component parameters are also designed. The principle and performance of the proposed rectifier are demonstrated through static and dynamic experiments. A comparison with other step-up and step-down rectifiers is discussed, which reveals that the proposed rectifier offers better performance in terms of higher efficiency and lower dc-side capacitance.**

***Index Terms*—Active power decoupling (APD), common-ground rectifier, leakage current suppression, step-up and step-down.**

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I. Introduction

With the increasing number of distributed renewable energy sources and dc loads in power systems, research on low-voltage direct current (LVDC) microgrids has also grown significantly [1]. Compared with traditional ac microgrids, LVDC microgrids have advantages such as high efficiency, high cost-effectiveness, and simplified control design [2]. In addition, LVDC microgrids have significant advantages in power distribution, resilience, and load optimization, especially in applications such as data centers, all-electric aircraft, and ship power distribution [3]. AC–DC converters, also known as rectifiers, are essential components of LVDC microgrids, serving to convert the AC power supplied by the grid into dc power [4], [5].

Single-phase rectifiers can be categorized into two types: isolated rectifiers [4], and nonisolated rectifiers [5]. Isolated rectifiers use either a high-frequency (HF) compact transformer on the dc side [6] or a line-frequency transformer on the ac grid side [7], which eliminates common-mode (CM) leakage current. However, isolated rectifiers are associated with several limitations, including low power density, reduced efficiency, high cost, elevated noise levels, and bulky form factors.

In contrast, non-isolated rectifiers, which lack transformers, offer advantages in efficiency, cost, size, and installation convenience, making them more suitable for home application. However, nonisolated rectifiers may simultaneously present HF CM voltage and parasitic capacitors, which generate the leakage current. When the leakage current exceeds a specified threshold, it can affect the operation of dc equipment, pose safety risks, and reduce system efficiency as well [8].

To suppress leakage current in non-isolated rectifiers, the most common approach is to add EMI filters on either the ac or dc side. This process usually requires first predicting or measuring the CM noise in the circuit and then designing the corresponding EMI filter [9]. However, adding these extra components reduces the advantages of nonisolated rectifiers in terms of cost and size. Furthermore, due to the uncertainty associated with parasitic parameters in nonisolated rectifiers, a large safety margin is usually incorporated during the EMI filter design to ensure compliance with CM voltage noise requirements, thereby further reducing the benefits of nonisolated rectifiers [10].

Various modulation methods, which avoid adding additional components, have been proposed to suppress leakage current through minimizing CM voltage fluctuations. For instance, using bipolar sinusoidal PWM modulation in H-bridge topology [11]

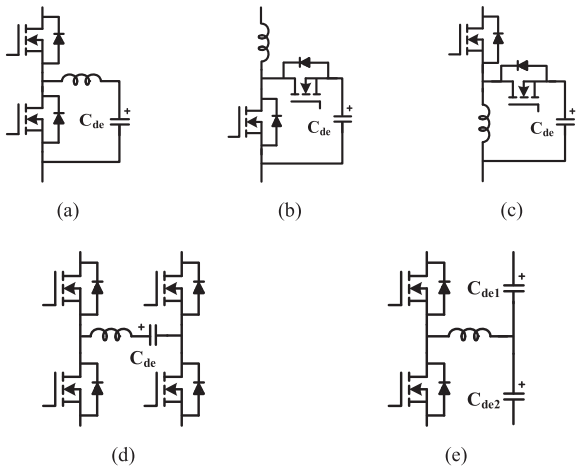


Fig. 1. Basic decoupling cell. (a) Buck type. (b) Boost type. (c) Buck-Boost type. (d) Full-bridge type. (e) Split-capacitor types.

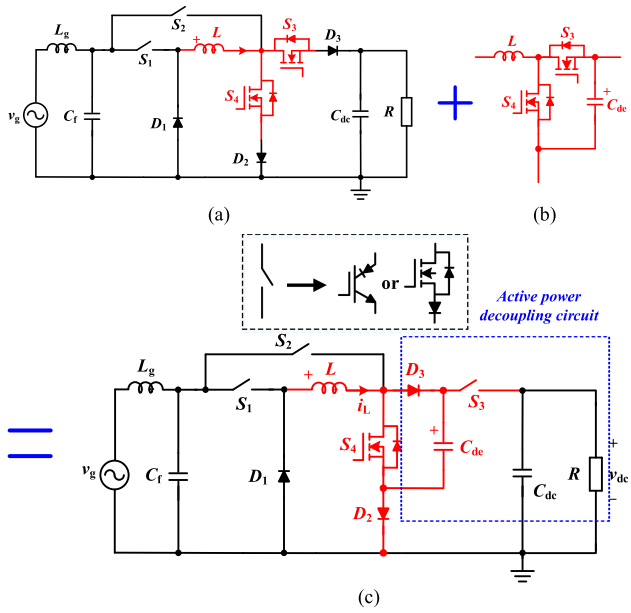


Fig. 2. Topology derivation. (a) Step-up and step-down common-ground rectifier circuit. (b) Boost-type decoupling circuit. (c) Proposed common-ground rectifier with active power decoupling capability.

can achieve CMV $= v_{dc}/2$. Alternatively, unipolar sinusoidal PWM modulation can be applied in improved H-bridge topologies, such as H5-type [12], and H6-type [13], to disconnect the dc side from the ac side during the freewheeling period. However, compared to unipolar sinusoidal PWM modulation, bipolar modulation results in higher switching losses and a significant amount of harmonic currents, necessitating additional filters. Moreover, improved H-bridge topologies using unipolar sinusoidal PWM modulation require additional switches, leading to increased losses and control complexity. Additionally, leakage current cannot be completely eliminated [14]. As an effective method for suppressing leakage current, a large number of common-ground topologies have been proposed and analyzed recently [5]. By connecting the N terminal of the ac side to the negative terminal of the dc side, the parasitic capacitor of the dc side equipment to ground is bypassed, thereby completely suppressing the CM leakage current [15].

Due to the instantaneous power mismatch between the ac and dc sides, power decoupling technology is required to reduce the secondary ripple. Large electrolytic capacitors are often used as a passive power decoupling method due to their low cost and the fact that no additional control technology is required [16]. However, electrolytic capacitors are large in size and their lifespan is inconsistent with that of other components, which affects the reliability of LVDC microgrids. Active power decoupling (APD) is considered another effective solution to this issue. The ripple power is transferred through an active switching circuit to a specific energy storage component, such as a film capacitor, which is relatively small in size and has a long lifespan. As shown in Fig. 1, basic APD cells can be divided into buck type [see Fig. 1(a)] [17], boost type [see Fig. 1(b)] [18], buck-boost type [see Fig. 1(c)], full-bridge type [see Fig. 1(d)] [19], [20] and discrete capacitor type [see Fig. 1(e)] [21]. However, this approach increases the number of switches and diodes, potentially increasing the cost and size of the system. Therefore, the topological structure of the composite of main circuit and power decoupling circuit is being actively explored [22], [23].

Based on the work presented in [24], a novel single-phase non-isolated common-ground rectifier with APD capability is proposed in this article, where new contributions can be summarized as follows:

1) To facilitate a deeper understanding of the proposed rectifier principle, a comprehensive introduction and rigorous mathematical analysis are provided.
2) A method for the passive device parameters of the proposed rectifier is presented to enhance the practical application of this topology.
3) A prototype was built and the performance of the proposed rectifier was experimentally verified.
4) A comparison between the proposed rectifier and existing rectifiers has been added.

The rest of this article is organized as follows: In Section II, the topology derivation, working principle, voltage across the semiconductor and decoupling capacitor, state-space model, and constraints of the proposed rectifier are described and analyzed. In Section III, the mathematical model of the proposed rectifier is analyzed, and a voltage-current dual closed-loop controller is designed to regulate the output DC voltage. Section IV provides a detailed analysis and design of the main passive component parameters in the rectifier. In Section V, various experiments are conducted based on a prototype, and the results verify the validity of the rectifier's working principle and passive component design. Section VI compares the proposed rectifier with other step-up and step-down rectifiers in terms of number of devices, decoupling function, structure, and performance. Finally, Section VII concludes this article.

II. Description and Analysis of the Proposed Rectifier With APD Capability

A. Topology Derivation

As shown in Fig. 2(a), a step-up and step-down rectifier circuit with common ground structure is firstly proposed in article. The

grid-side inductor L_g, and capacitor C_f, form an LC filter. $C_{\rm dc}$ is the dc-link capacitor, L is the dc energy storage inductor, R is the dc load, S_1-S_4 are fully controlled switches, and D_1-D_3 are diodes Since the voltage across parasitic capacitors is clamped to a constant value by connecting the ground of the grid and dc load, the CM leakage current can be completely eliminated.

By comparing with the Boost-type decoupling circuit shown in Fig. 2(b), it can be observed that the rectifier with decoupling capability depicted in Fig. 2(c) can be derived by adding a decoupling capacitor ($C_{\rm de}$), which can effectively reduce the dc-link capacitor. The inductor (L) and two switches (S_3 and S_4) are shared between the rectifier circuit and the power decoupling circuit. To prevent the voltage across the decoupling capacitor $C_{\rm de}$ from following the changes in the voltage across the dc-bus capacitor $C_{\rm dc}$, the positions of the active switch S_3 and the diode D_3 in the decoupling circuit are interchanged.

To facilitate the subsequent description and analysis of the circuit, the relevant variables are defined as follows, i_L represents the current through the inductor L, $|v_g|$ denotes the absolute value of the grid voltage, $v_{\rm dc}$ is the voltage across the output load R, and v_c is the voltage across the decoupling capacitor $C_{\rm de}$. The variables d_{S1}-d_{S4} represent the duty cycles of switches S_1-S_4.

B. Operating Principle

Assuming the circuit operates in continuous conduction mode (CCM), the equivalent circuits of the proposed step-up and step-down rectifier operating in various states are depicted in Fig. 3. States 1–3 and states 4–6 correspond to the current flow loop in the rectifier during the positive and negative half-cycles of the grid voltage, respectively. The working principle of the proposed rectifier with a decoupling capability is described in detail as follows.

State 1: Switches S_1 and S_4 are turned ON, while S_2 and S_3 are turned OFF. The grid voltage v_g charges inductor L through S_1 and S_4, resulting in an increase in the inductor current i_L. During this period, there is no power exchange between the decoupling circuit and the original rectifier circuit. Simultaneously, the output voltage $v_{\rm dc}$ starts to decrease linearly since the energy stored in the dc capacitor is consumed by the dc load.

State 2: All switches S_1–S_4 are turned OFF. The energy stored in the inductor L is discharged to the decoupling capacitor $C_{\rm de}$. Therefore, the instantaneous power of $C_{\rm de}$ is positive. Meanwhile, the output voltage $v_{\rm dc}$ continues to decrease during this stage.

State 3: S_3 and S_4 are turned ON, while S_1 and S_2 are turned OFF. The decoupling capacitor $C_{\rm de}$ is supplying energy to the dc side through inductor L. The instantaneous power of $C_{\rm de}$ is negative, and both the inductor current i_L and the output voltage $v_{\rm dc}$ are increasing.

State 4: S_2 is turned ON, while S_1, S_3 and S_4 are turned OFF. The inductor L is charged by the grid voltage v_g. Similar to state 1, the dc voltage decreases linearly.

Note that **states 2** and **5**, and **states 3** and **6** work exactly the same, the only difference is the polarity of the grid. The states of the inductor L, capacitors $C_{\rm de}$ and $C_{\rm dc}$ in different cases are given in Table I.

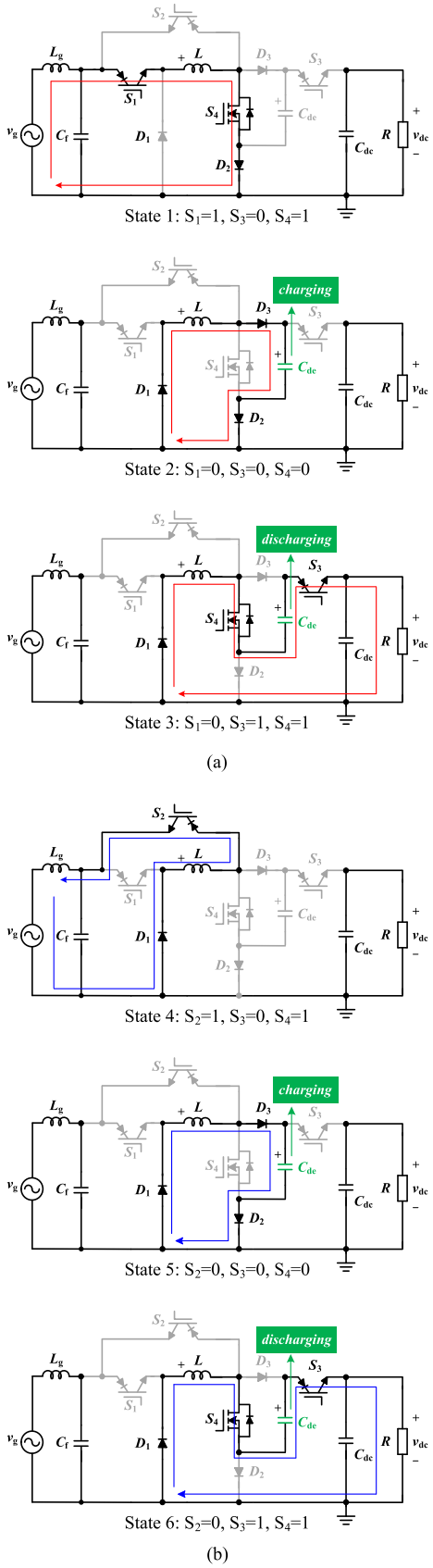


Fig. 3. Equivalent circuits of the proposed rectifier at (a) positive and (b) negative half-line cycles.

TABLE I
SUMMARY OF DIFFERENT OPERATING STATES

States	S_1	S_2	S_3	S_4	L	C_{de}	C_{dc}
State 1	1	0	0	1	Charge	Idle	Discharge
State 2	0	0	0	0	Discharge	Charge	Discharge
State 3	0	0	1	1	Charge	Discharge	Charge
State 4	0	1	0	1	Charge	Idle	Discharge
State 5	0	0	0	0	Discharge	Charge	Discharge
State 6	0	0	1	1	Charge	Discharge	Charge

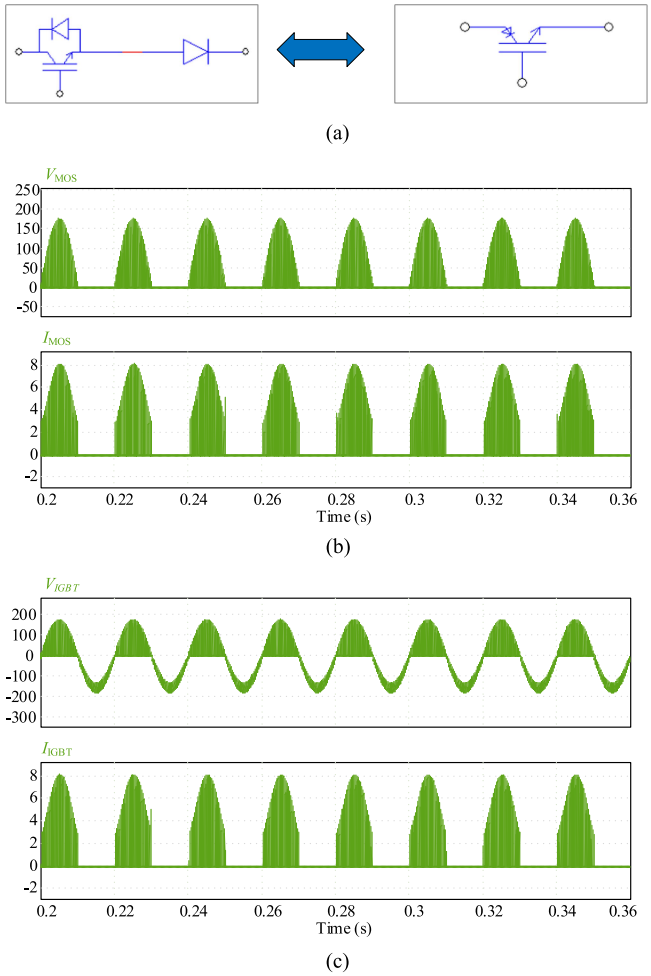


Fig. 4. (a) MOSFET with series-connected diode and RB-IGBT module in PSIM. Simulation results of different switching device modules in the circuit. (b) V_{MOS} and I_{MOS}. (c) V_{IGBT} and I_{IGBT}.

As shown in Fig. 4(a), the switches S_1, S_2, and S_3 can be MOSFET and diode connected in series, or the reverse-blocking IGBT (RB-IGBT). Fig. 4(b) and (c) displays the comparative waveforms of forward voltage and conduction current for both the MOSFET and RB-IGBT devices based on PSIM. Simulation results confirm that both configurations have reverse blocking capabilities and validate the principle of the proposed rectifier.

However, MOSFETs with series diodes and RB-IGBTs exhibit significant differences in performance, cost, and application suitability. MOSFETs are well-suited for HF, low-power applications due to their fast-switching speeds, low conduction losses, and relatively low manufacturing costs. However, they may experience higher losses under high-current conditions. In contrast, RB-IGBTs are more appropriate for medium- to high-power applications, offering lower on-state voltage drops and improved reverse recovery characteristics, which contribute to higher efficiency at elevated power levels.

Given that the prototype developed in this article operates at high frequency with low power and low current, MOSFETs with series diodes were selected for switches S_1, S_2, and S_3.

TABLE II
VOLTAGE/CURRENT STRESS OF THE DEVICES

Dev.	State1	State2	State3	State4	State5	State6
S_1	$0/i_L$	$v_g/0$	$v_g/0$	$v_g/0$	$v_g/0$	$v_g/0$
S_2	$v_g/0$	$(v_g-v_c)/0$	$(v_c+v_g-v_{dc})/0$	$0/i_L$	$(v_g+v_c)/0$	$(v_c+v_g-v_{dc})/0$
S_3	$(v_c-v_{dc})/0$	$(v_c-v_{dc})/0$	$0/i_L$	$(v_c-v_{dc})/0$	$(v_c-v_{dc})/0$	$0/i_L$
S_4	$0/i_L$	$v_c/0$	$0/i_L$	$0/i_L$	$v_c/0$	$0/i_L$
D_1	$v_g/0$	$0/i_L$	$0/i_L$	$0/i_L$	$0/i_L$	$0/i_L$
D_2	$0/i_L$	$0/i_L$	$(v_c-v_{dc})/0$	$v_g/0$	$0/i_L$	$(v_c-v_{dc})/0$
D_3	$v_c/0$	$0/i_L$	$v_c/0$	$v_c/0$	$0/i_L$	$v_c/0$

Note: Voltage stress / Current stress

C. Voltage/Current Analysis Across the Switches and Diodes

Based on the operating principle of the proposed rectifier, the voltages across the switches and diodes are summarized in Table II. It can be observed that the switches S_1, S_3, and S_4, along with all the diodes, experience relatively low voltage stress.

Additionally, the voltage stress on S_2 is relatively higher than that on the other switches, with the highest instantaneous voltage reaching $v_c+|v_g|$, which can be mitigated by selecting an appropriate dc bias voltage $\bar{V}_{\mathrm{d}}$ and decoupling capacitor C_{de} to reduce the instantaneous value of v_c and enhance the reliability of S_2. The current stress of all devices is i_L, and the peak value of i_L affects the selection of devices.

D. Voltage Analysis Across the Decoupling Capacitor

When the proposed rectifier operates under unity power factor (PF) correction, neglecting losses in the inductors and active devices, the grid instantaneous power should satisfy

$$P_{\mathrm{ac}} = \underbrace{\frac{1}{2}V_m I_m}_{P_{\mathrm{dc}}} \underbrace{-\frac{1}{2}V_m I_m \cos(2\omega t)}_{P_r} \tag{1}$$

where P_{dc} represents the constant term in the instantaneous power, while P_r represents the second harmonic term. V_m and I_m denote the amplitude of the grid voltage v_g and grid current i_g respectively, while ω represents the grid angular frequency.

Since the operating principle of the decoupling capacitor is similar during both the positive and negative half-cycles of the

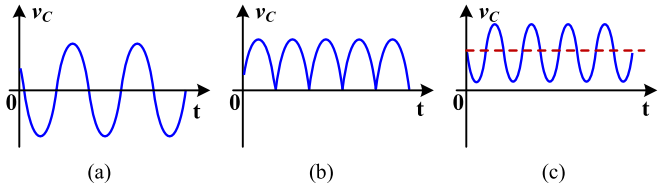


Fig. 5. Voltage waveforms of decoupling capacitor (v_c). (a) Pure sine wave. (b) Rectified sine wave. (c) Sine wave with dc bias.

line frequency, we will use the voltage across the decoupling capacitor during the positive half-cycles as an example here.

Through the charging and discharging process of state 2 and state 3, the second harmonic power P_r should be absorbed by $C_{\rm de}$. At this time, the output power should correspond to the constant term $P_{\rm dc}$. Thus, the voltage across the decoupling capacitor can be expressed as

$$\mathrm{v}_c^2 = \bar{\mathrm{V}}_d^2 + \mathrm{A} - \frac{\mathrm{P}_{dc}}{\omega \mathrm{C}_{de}} \cdot \sin(2\omega \mathrm{t}) \tag{2}$$

where $\bar{\mathrm{V}}_{\rm d}$ represents the dc bias voltage of the decoupling capacitor, A is a constant term. From (2), the voltage across the decoupling capacitor v_c can be calculated as (3) and the waveforms of v_c in three conditions are described separately in Fig. 5

$$v_C = \begin{cases} (\mathrm{a}): \sqrt{\frac{2P_{\rm dc}}{\omega C_{\rm de}}} \cdot \sin\left(\omega t + \frac{3}{4}\pi\right), \overline{V_d} = 0, A = \frac{P_{\rm dc}}{\omega C_{\rm de}} \\ (b): \sqrt{\frac{2P_{\rm dc}}{\omega C_{\rm de}}} \cdot \left|\sin\left(\omega t + \frac{3}{4}\pi\right)\right|, \overline{V_d} = 0, A = \frac{P_{\rm dc}}{\omega C_{\rm de}} \\ (c): \sqrt{\overline{V_{\rm d}}^2 - \frac{P_{\rm dc}}{\omega C_{\rm de}} \sin(2\omega t)}, \overline{V_d} > \sqrt{\frac{P_{\rm dc}}{\omega C_{\rm de}}}, A = 0. \end{cases} \tag{3}$$

Similarly, according to the law of power conservation, the reference value of the grid current can be derived as follows:

$$i_{g\_\rm ref}(t) = \frac{2 \cdot P_{\rm dc}}{V_m} \sin(\omega t). \tag{4}$$

E. State Space Model Analysis

Taking the positive half-cycle of the grid as an example, the durations of state 1 to state 3 within one switching cycle are designated as $d_1 T_s$, $d_2 T_s$, and $d_3 T_s$, respectively, where

$$d_1 + d_2 + d_3 = 1. \tag{5}$$

The relationship between the duty cycles of S_1-S_4 can be obtained from Fig. 3 as follows:

$$\begin{cases} d_{S4} = d_1 + d_3 \\ d_{S3} = d_3 \end{cases}. \tag{6}$$

By averaging the circuit states over one switching cycle the state space model can be derived as

$$\begin{cases} L \cdot \frac{di_{\rm L}}{dt} = d_{S4} \cdot (|v_g| + v_C) + d_{\rm S3} \cdot (v_C - v_{\rm dc} - |v_g|) - v_C \\ C_b \cdot \frac{dv_C}{dt} = (1 - d_{S4} - d_{\rm S3}) \cdot i_L \\ C_{\rm dc} \cdot \frac{dv_{\rm dc}}{dt} = d_{S3} \cdot i_L - \frac{v_{\rm dc}}{R} \end{cases}. \tag{7}$$

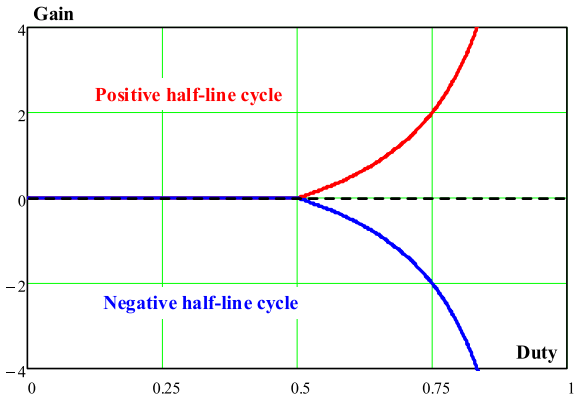


Fig. 6. Voltage gains of the proposed rectifier.

Since the circuit operating status is consistent during the positive and negative half cycles of the grid, the above state space model is applicable to states 1–6.

Through analyzing the variables in (7) at the large-signal steady-state operating point, the voltage gain of the proposed converter can be yielded as

$$Gain = \frac{\mathrm{v}_{dc}}{\mathrm{V}_{\rm g}} = \frac{2\mathrm{D}_{\rm S4} - 1}{1 - \mathrm{D}_{\rm S4}} \tag{8}$$

where D_{S4} and $|V_g|$, respectively, represent the steady-state average values of d_{S4} and $|v_g|$.

Similarly, during the negative half-line cycle, the gain of the rectifier can be expressed in terms of the duty cycle of switch S_2

$$Gain = \frac{\mathrm{v}_{dc}}{\mathrm{V}_{\rm g}} = -\frac{2\mathrm{D}_{\rm S2} - 1}{1 - \mathrm{D}_{\rm S2}}. \tag{9}$$

Fig. 6 depicts the voltage gain in a line cycle and it can be found that the proposed rectifier can achieve a wide voltage regulation range.

F. Constraint Analysis

Based on Fig. 3, the average value of $|i_g|$, $i_{\rm dc}$, and i_c within one switching cycle can be represented as

$$\begin{cases} |i_g| = (d_{S4} - d_{S3}) \cdot i_L \\ i_{\rm dc} = d_{S3} \cdot i_L \\ i_c = (1 - d_{S3} - d_{S4}) \cdot i_L \end{cases}. \tag{10}$$

Solving (10), the reference current for dc inductor i_L can be exhibited as

$$i_{L\_\rm ref} = i_g + 2i_{\rm dc} + i_c \tag{11}$$

where the dc bias component in (11) can compensate for the decoupling losses of $C_{\rm de}$ when v_g crosses zero. Meanwhile, expressions for $d_{\rm S3}$ and $d_{\rm S4}$ can also be derived from (10)

$$\begin{cases} d_{S3} = \frac{i_{\rm dc}}{2i_{\rm dc} + |i_g| + i_c} \\ d_{S4} = \frac{i_{\rm dc} + |i_g|}{2i_{\rm dc} + |i_g| + i_c} \end{cases}. \tag{12}$$

From (12), the constraints for d_{S3} and d_{S4} can be found as follows:

$$d_{S3} \le d_{S4}. \tag{13}$$

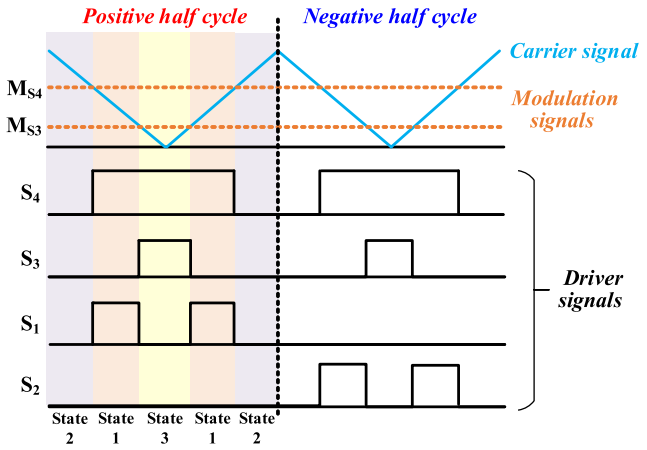


Fig. 7. Switching states of the proposed circuit.

Therefore, the two in-phase triangular carriers shown in Fig. 7 are utilized to modulate d_{S3} and d_{S4}, ensuring that the rectifier operates in the six modes mentioned in Fig. 3.

Additionally, d_{S3} and d_{S4} should also fall within the range of 0 to 1, yielding the following constraint

$$i_{\mathrm{dc}} + i_c > 0 \tag{14}$$

where

$$i_c = -\frac{P_{\mathrm{dc}} \cdot \cos(2\omega t)}{v_c}. \tag{15}$$

By solving (14), (15), another constraint for the circuit can be obtained as

$$v_c > v_{dc}. \tag{16}$$

If (16) is not satisfied, D_2 will conduct in state 3 and state 6, causing v_c to follow v_{dc}.

III. Control System Design

According to (1), controlling the power of any two ports (i.e., the ac port, the decoupling port, or the dc port) is sufficient to control the power of the remaining ports. Thus, the secondary harmonic power can be compensated by controlling the decoupling power or the dc-side power. Typically, the power control structure on the dc side is preferred because its voltage or current reference values are usually fixed.

To achieve better dynamic performance, this article adopts a voltage-current dual closed-loop control method to regulate the ac current. The detail control block diagram is drawn in Fig. 8, which is divided into a reference generation part and a controller design part.

In the reference generation part, the voltage outer loop utilizes a notch filter to extract the dc component of v_c, working in conjunction with the inner loop ac current control. This filtering approach, compared to computing reference values, relies only on sampling accuracy and is unaffected by parameter variations. Since the output is a purely resistive load, the power control design for the dc side is a simple voltage single-loop system.

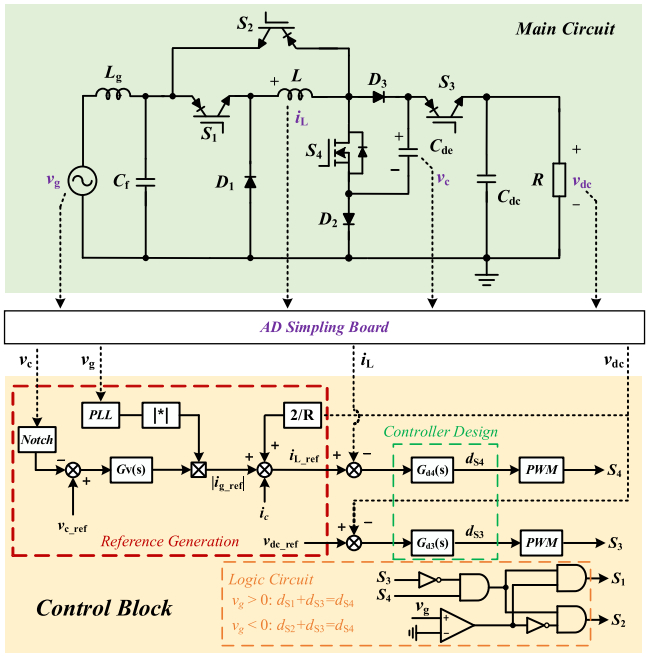


Fig. 8. Control block diagram of the proposed circuit.

Neglecting the dynamic equation of v_c, (8) can be rewritten as

$$\dot{x} = f(\mathrm{x}) + g(x) \cdot d \tag{17}$$

where $x = \begin{bmatrix} i_L \\ v_{\mathrm{dc}} \end{bmatrix}$ is the state variable, $d = \begin{bmatrix} d_{S3} \\ d_{S4} \end{bmatrix}$ is the control input, $f(x) = \begin{bmatrix} -v_C \\ -\frac{v_{\mathrm{dc}}}{R} \end{bmatrix}$ is the smooth vector field, $g(x) = \begin{bmatrix} v_C - v_{\mathrm{dc}} - |v_g| & v_C + |v_g| \\ i_L & 0 \end{bmatrix}$ is the smooth matrix.

From (17), it can be seen that the proposed rectifier is a highly nonlinear (multiplication of d with x) and highly coupled (between d and x) system. In order to reduce the control complexity, the nonlinear feedback linearization technology suitable for single-phase power systems is proposed by referring to the decoupling measures in motor drive theory in [25] and [26]. The basic idea is to construct a new control input to transform the complex system into multiple independent, decoupled single-input and single-output linear systems. First, the control output is selected as

$$\begin{cases} y_1 = L \cdot i_L \\ y_2 = C_{\mathrm{dc}} \cdot v_{\mathrm{dc}} \end{cases}. \tag{18}$$

Given that the differential expression of (18) contains the control input d, to linearize the system, let the new control input be the derivative of the control output

$$\begin{cases} u_A = \dot{y}_1 \\ u_B = \dot{y}_2 \end{cases}. \tag{19}$$

Since there is no coupling relationship between the new control inputs, the dynamic system in (17) is transformed into a decoupled linear system. By solving (17)–(19), the relationship between the original control input and the new control input can

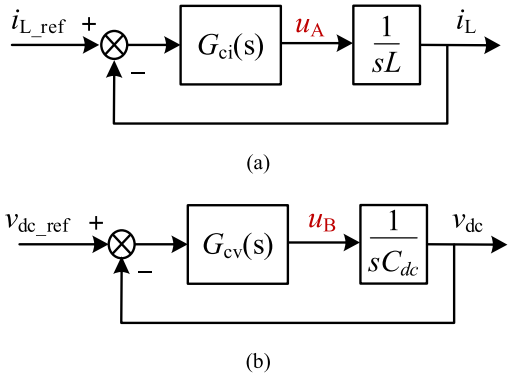


Fig. 9. Closed-loop control structure of the proposed circuit.

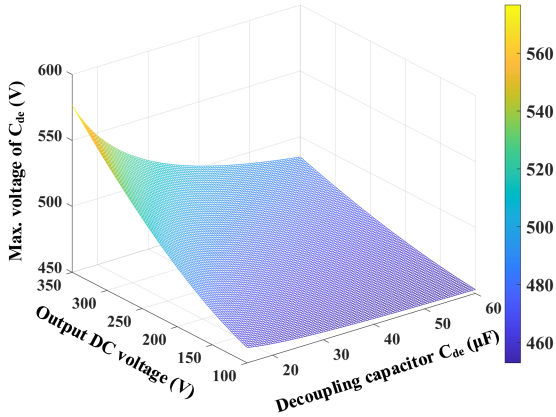


Fig. 10. Relationship between C_{de} and associated voltages when $R = 200\ \Omega$.

be derived as

$$\begin{cases} d_{S3} = \frac{u_B}{i_L} \\ d_{S4} = \frac{u_A + v_c + d_{S3}\cdot(v_{dc} + |v_g| - v_c)}{v_c + |v_g|} \end{cases}. \tag{20}$$

Regarding the compensator design, the closed-loop transfer function concerning the state variable x can be derived as

$$\begin{cases} \frac{v_{\mathrm{dc}}}{u_B} = \frac{1}{sC_{\mathrm{dc}}} \\ \frac{i_L}{u_A} = \frac{1}{sL} \end{cases}. \tag{21}$$

The closed loop of the state variable is depicted in Fig. 9, offering various options for compensator selection. A straightforward choice is to employ a proportional controller, which transforms the closed-loop system into a simple first-order inertial element.

Interestingly, for the decoupled system, the discrete form of (20) is consistent with the algorithm used in deadbeat predictive control, which is a proportional control with a feedforward compensation term, i.e.,

$$\begin{cases} d_{S3}(k+1) = \frac{C_{\mathrm{dc}}\cdot R\cdot[v_{\mathrm{dc}}{}^*(k) - v_{\mathrm{dc}}(k)] + T_s\cdot v_{\mathrm{dc}}(k)}{i_L(k)\cdot R\cdot T_s} \\ d_{S4}(k+1) = \frac{L\cdot[i_L{}^*(k) - i_L(k)] + d_C(k+1)\cdot T_s\cdot|v_g(k)|}{[v_C(k) + |v_g(k)|]\cdot T_s} \\ \quad + \frac{d_C(k+1)\cdot T_s\cdot[v_{\mathrm{dc}}(k) - v_C(k)] + v_C(k)\cdot T_s}{[v_C(k) + |v_g(k)|]\cdot T_s} \end{cases} \tag{22}$$

Therefore, deadbeat predictive control can be considered, to some extent, a special case of feedback linearization control.

IV. Parameter Design of the Main Components

A. Decoupling Capacitor Design

The choice of C_{de} should be a compromise between device stress and system power density. Combining (3) and (16), C_{de} should satisfy the following condition:

$$C_{\mathrm{de}} \geq \max\{C_{\mathrm{de1}}, C_{\mathrm{de2}}\} \tag{23}$$

where

$$C_{\mathrm{de1}} = \max_{\omega t \in (0, \frac{\pi}{2})} \left(\frac{v_{\mathrm{dc}}^2 \sin(2\omega t)}{\omega R\left(\bar{V}_d^2 - v_{\mathrm{dc}}^2\right)} \right) \tag{24}$$

$$C_{\mathrm{de2}} = \max_{\omega t \in (\frac{\pi}{4}, \frac{\pi}{2})} \left(\frac{P_{\mathrm{dc}} \sin(2\omega t)}{\omega\left(\bar{V}_d^2 - v_{\mathrm{dc}}^2 \cos^2(2\omega t)\right)} \right). \tag{25}$$

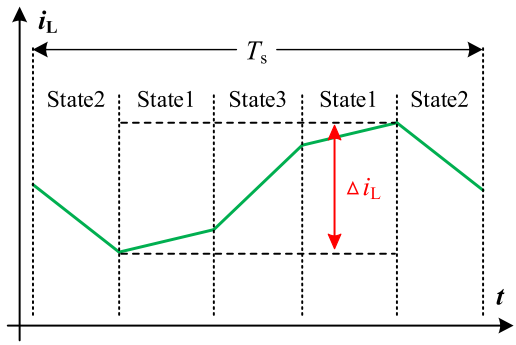


Fig. 11. Variation trend of i_L within one switching cycle.

Given $v_{\mathrm{dc}} \in (150, 300)\mathrm{V}$, $R = 200\ \Omega$, and $\overline{V_d} = 450\mathrm{V}$, C_{de1} and C_{de2} can be calculated to be 12.74 and 7.07 μF respectively.

Fig. 10 illustrates the maximum value of v_c versus C_{de} and v_{dc} under the aforementioned conditions. To minimize device voltage stress, C_{de} should not be too small. In this article, C_{de} is selected as 40 μF. Then, based on (3), the voltage fluctuation range of 420–477 V across the decoupling capacitor can be estimated when the output power is 320 W.

B. DC Inductor Design

The design of L should ensure that the peak-to-peak ripple of i_L, denoted as Δi_L, is less than the rated value. In this article, the proposed circuit operates in CCM and follows the relationship

$$\frac{\Delta i_L}{2} < r_i \cdot i_L \tag{26}$$

where r_i is current ripple rate of dc inductor. By solving (5), (6), and (12), d_1 to d_3 can be expressed as

$$\begin{cases} d_1 = \frac{|i_g|}{2i_{\mathrm{dc}} + |i_g| + i_c} \\ d_2 = \frac{i_{\mathrm{dc}}}{2i_{\mathrm{dc}} + |i_g| + i_c} \\ d_3 = \frac{i_{\mathrm{dc}} + i_c}{2i_{\mathrm{dc}} + |i_g| + i_c} \end{cases}. \tag{27}$$

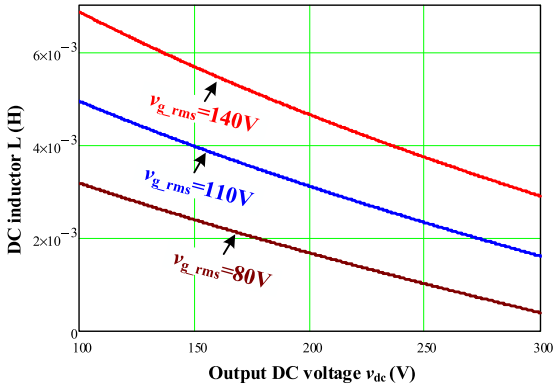


Fig. 12. Relationship between DC inductor L and output DC voltage $v_{\rm dc}$ when $R = 200\ \Omega$, $P_{\rm dc} = 320$ W, and $r_i = 20\%$.

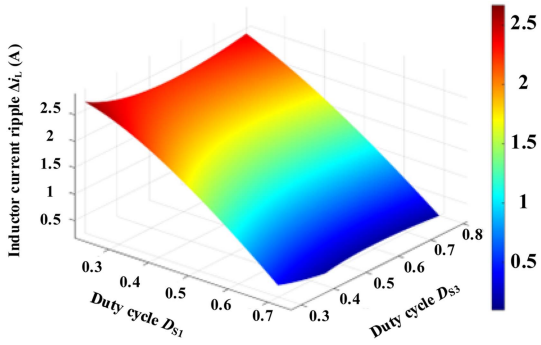


Fig. 13. Relationship between inductor current ripple and duty cycle, when $P_{\rm dc} = 320$ W, $v_g = 110$ V, $v_{\rm dc} = 250$ V, $v_c = 450$ V, and $L = 4$ mH.

The waveform of the inductor current within one switching cycle is shown in Fig. 11. At this time, Δi_L can be expressed as

$$\Delta i_L = \frac{2\,|v_g|}{L} \cdot d_1 T_s + \frac{v_c - v_{\rm dc}}{L} \cdot d_3 T_s. \tag{28}$$

Thus, the inductance of dc inductor can be determined as follows:

$$L = \frac{T_s}{\Delta i_L}[2\,|v_g| \cdot d_1 + (v_c - v_{\rm dc}) \cdot d_3]. \tag{29}$$

Assuming an output dc voltage range of 150–300 V, with $R = 200\ \Omega$, $P_{\rm dc} = 320$ W, and $r_i = 20\%$, the relationship between the minimum inductance of the dc inductor and the output dc voltage, as derived from (26)–(29), is illustrated in Fig. 12. When the grid voltage is 110 V and the dc output voltage is 150 V, the calculated c inductor inductance is 3.95 mH. To address this, we incorporated a design margin of 20%, resulting in a revised calculated value of 4.74 mH. Consequently, we selected a 4.8 mH inductor to ensure adequate performance [5], [27]. According to (28), the relationship between the current ripple in the dc inductor and the duty cycles of switches S_1 and S_3 is illustrated in Fig. 13, with parameters set to $P_{\rm dc} = 320$ W, $v_g = 110$ V, $v_{\rm dc} = 250$ V, and $v_c = 450$ V.

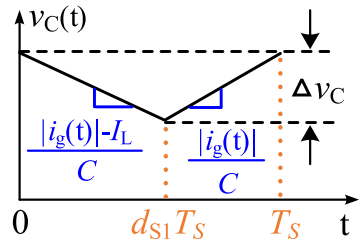


Fig. 14. Steady-state input voltage waveform $v_C(t)$ during the switching cycle in the positive half-line cycle.

C. DC-link Capacitor Design

When a decoupling capacitor is used for ac–dc power decoupling, the capacitor on the dc side primarily serves to establish the dc voltage and prevent fluctuations in the dc voltage caused by the slow response of the power supply during sudden load changes. Assuming that during a sudden change in load power, the time available for the power supply to respond can be expressed as

$$\Delta t_{\rm dc} = \frac{C_{\rm dc} \times [{v_{\rm dc}}^2(t) - {v_{\rm dc}}^2(t_0)]}{2 \times P_{\rm delt}} \tag{30}$$

where $v_{\rm dc}$(t) is the voltage at time t, $v_{\rm dc}(t_0)$ is the voltage at time t_0, $P_{\rm delt}$ is the changing power, and $C_{\rm dc}$ is the dc side support capacitor.

According to (30), the dc-link capacitance value can be obtained as

$$C_{\rm dc} = \frac{2 \times \Delta P \cdot \Delta t_{\rm dc}}{{v_{\rm dc}}^2(t) - {v_{\rm dc}}^2(t_0)}. \tag{31}$$

This article assumes that the maximum permissible power change within 1 ms is 100 W and that the maximum allowable drop in dc voltage is 5% of the rated dc voltage (250 V). The calculated dc-link capacitance value is 32.8 μF. Considering capacitor aging and safety margins, the final selected dc-link capacitance value is 40 μF.

D. Filter Capacitor Design

To calculate the voltage ripple across the filter capacitor, the following definition can be used

$$i_C\,(\mathrm{t}) = C\frac{dv_C\,(\mathrm{t})}{dt}. \tag{32}$$

Based on this formula, the expression for the ripple amplitude Δv_c across the filter capacitor can be derived, and the voltage waveform across the filter capacitor can be plotted. When the proposed rectifier operates during the positive half-line cycle, the filter capacitor voltage waveform during one switching cycle is shown in Fig. 14. During the dc inductor charging period, as illustrated in state 1 of Fig. 3, the slope of the filter capacitor voltage waveform v_C(t) is

$$\frac{dv_C(t)}{dt} = \frac{i_{Cf}(t)}{C_f} = \frac{i_g(t) - I_L}{C_f}. \tag{33}$$

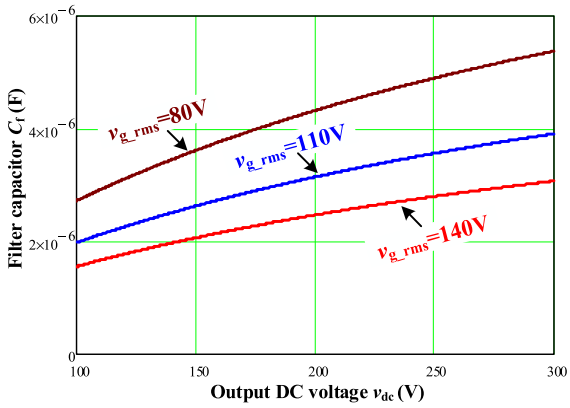


Fig. 15. Relationship between filter capacitor C_f and output DC voltage vdc when $R = 200\ \Omega$, $P_{\rm dc} = 320$ W, and $r_v = 3\%$.

During the dc inductor discharge period, as shown in states 2 and 3 of Fig. 3, the slope of the filter capacitor voltage waveform v_C(t) is

$$\frac{dv_C(t)}{dt} = \frac{i_{Cf}(t)}{C_f} = \frac{i_g(t)}{C_f}. \tag{34}$$

According to the Fig. 14, the ripple voltage of filter capacitor can be derived as

$$\Delta v_C(t) = \frac{i_g(t)}{C_f} \cdot (1 - d_1) \cdot T_S. \tag{35}$$

Then, the capacitance of the filter capacitor will be calculated as

$$C_f = \frac{i_g(t)}{\Delta v_C(t)} \cdot (1 - d_{S1}) \cdot T_S. \tag{36}$$

To better represent the voltage ripple, the voltage ripple rate is defined as follows:

$$r_v = \frac{\Delta v_{C\_\max}}{2v_{C\_\text{peak}}}. \tag{37}$$

Similarly, the parameters used to calculate the dc inductor value—an output dc voltage range of 150–300 V, with $R = 200\ \Omega$, $P_{\rm dc} = 320$ W, and a voltage ripple rate $r_v = 3\%$—are also used to calculate the filter capacitor value. Based on the (27), (36) and (37), the relationship between the minimum capacitance of the filter capacitor and the output dc voltage is drawn in Fig. 15. When the grid voltage is 110 V and the dc output voltage is 300 V, the calculated capacitance of the filter capacitor is 3.93 μF. Considering ac voltage fluctuations and potential margin, the capacitance value of filter capacitor is selected as 5 μF.

E. Grid-side Inductor Design

To ensure that the grid current contains less harmonics, the resonant frequency of the *LCL* filter is typically designed to fall between 10 times the line frequency and 0.5 times the switching frequency, that is,

$$10 f_0 < f_{\rm res} < 0.5 f_S. \tag{38}$$

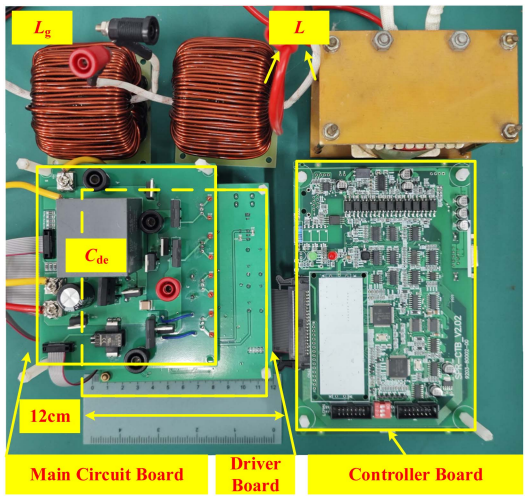


Fig. 16. Experimental platform for the proposed rectifier.

TABLE III
SYSTEM PARAMETERS

Device	Symbol	Value	Unit
Grid voltage (rms)	v_g	110	V
Grid frequency	f_0	50	Hz
Switching frequency	f_s	20	kHz
Output voltage	$v_{\rm dc}$	250	V
Grid-side inductor	L_g	3.6	mH
	R_{g_dc}	0.074	Ω
Filter capacitor	C_f	5	μF
DC inductor	L	4.8	mH
	R_{L_dc}/ R_{L_ac}	0.085/0.6	Ω
DC load	R	200	Ω
DC-link capacitor	$C_{\rm dc}$	40	μF
Decoupling capacitor	$C_{\rm de}$	40	μF

The resonant frequency of the *LCL* filter in the system is given by

$$f_{\rm res} = \frac{1}{2\pi}\sqrt{\frac{L + L_g}{LL_gC_f}}. \tag{39}$$

Furthermore, to achieve a larger stability margin and control bandwidth, the value of grid-side inductance should not exceed that of the dc inductance [28]. The grid-side inductance is selected as 3.6 mH, resulting in a resonant frequency of 1635 Hz.

V. EXPERIMENTAL RESULTS

To verify the feasibility of the proposed rectifier and control strategy, various experiments have been implemented based on a 320 W experimental prototype shown in Fig. 16. The Texas Instruments TMS320F28035 digital signal processor is used as the controller. Due to the large voltage ripple across the decoupling capacitor, a film capacitor is preferred. In contrast, the voltage ripple across the dc-link capacitor is small, so an electrolytic capacitor is chosen to minimize size. The main parameters of the system are given in Table III.

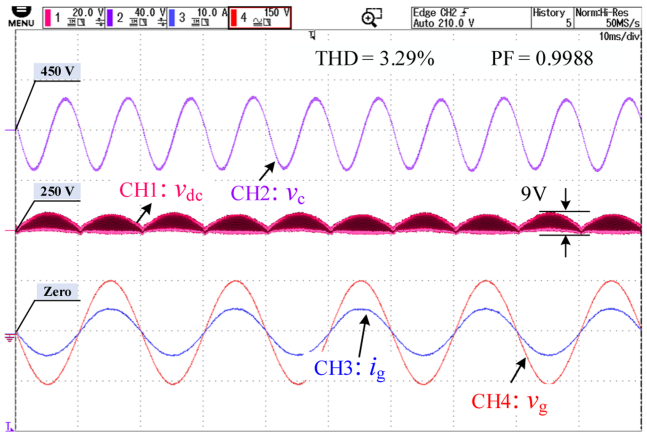


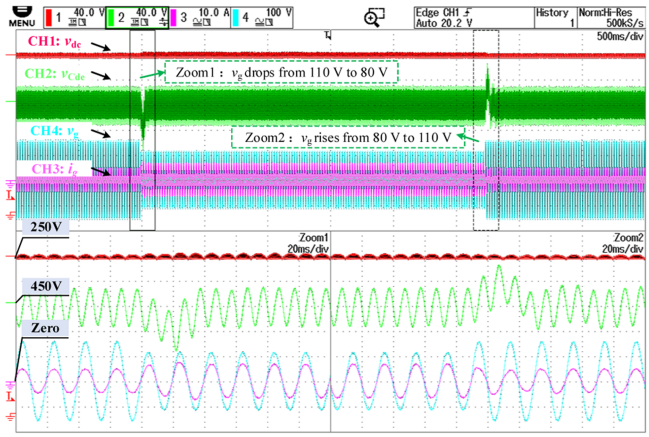
Fig. 17. Steady-state waveforms of the rectifier.

When the proposed rectifier operates in steady state, the experimental waveforms are described in Fig. 17. The voltage across the decoupling capacitor, v_c, fluctuates at 100 Hz, twice the grid frequency, with a range of 417–477 V, which is very close to the calculated value of 420–477 V in Section IV-A. The output dc voltage, $v_{\rm dc}$, is 250 V, with the maximum fluctuation of 9 V. Additionally, the grid current i_g can accurately follow the reference given in (4), with a low total harmonic distortion (THD) of only 3.29% and a high PF of 0.9988. The static test results indicate that the proposed rectifier with a decoupling function exhibits good performance of power conversion. Furthermore, regarding the buck-boost operation mode of the circuit, Fig. 19 presents the steady-state waveforms when the dc output voltage is set to 130 V. The results demonstrate a maximum voltage fluctuation of 4 V in $v_{\rm dc}$ and a THD of 3.07%, which further verifies the circuit's buck-boost capability.

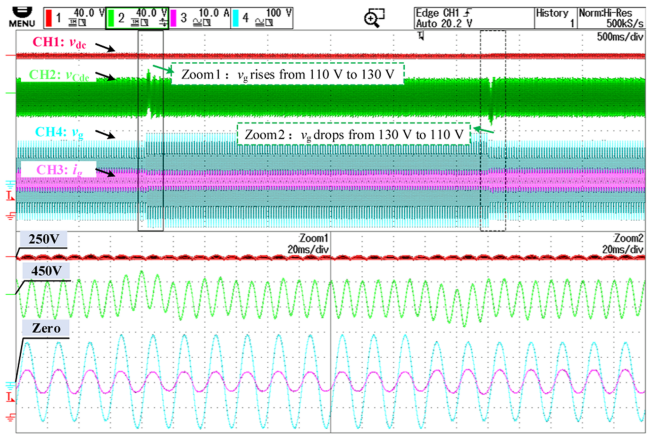
To demonstrate the good dynamic performance of the proposed rectifier and the designed controller, experiments involving grid voltage $v_{\rm g}$ and dc voltage $v_{\rm dc}$ step changes were conducted. The experimental results are shown in Figs. 18 –21.

Fig. 18(a) shows the dynamic experimental waveform of the grid voltage $v_{\rm g}$ suddenly dropping from 110 to 80 V (a drop of about 27%), and then rising from 80 V back to 110 V. Fig. 18(b) shows the dynamic experimental waveform of the grid voltage $v_{\rm g}$ suddenly increasing from 110 to 130 V (an increase of about 18%), and then dropping from 130 V back to 110 V. It can be observed from Fig. 18 that the dc output voltage $v_{\rm dc}$ and the input grid current i_g have no obvious fluctuations, and the decoupling capacitor voltage $v_{\rm de}$ quickly returns to stability.

Figs. 19 and 20 respectively present the dynamic experimental waveforms when $v_{\rm dc} = 130$ V, showing the grid voltage $v_{\rm g}$ rises from 110 to 130V and back down to 110V, the dynamic recovery time is maintained below 10 ms. When the dc output voltage drops from 250 to 200 V, holds for 2 s, and then returns to 250 V, the test results are shown in Fig. 21. During the dc voltage transient, the dc output voltage $v_{\rm dc}$ quickly and accurately tracks the reference voltage, and the system stabilizes again after 90 ms. The dynamic test results in Fig. 18 through Fig. 21 demonstrate that the proposed rectifier and the designed control system exhibit excellent dynamic performance.



(a)



(b)

Fig. 18. Dynamic waveforms of the rectifier when (a) v_g first drops from 110 to 80 V, and then returns to 110 V and (b) v_g first rises from 110 to 130 V and then returns to 110 V.

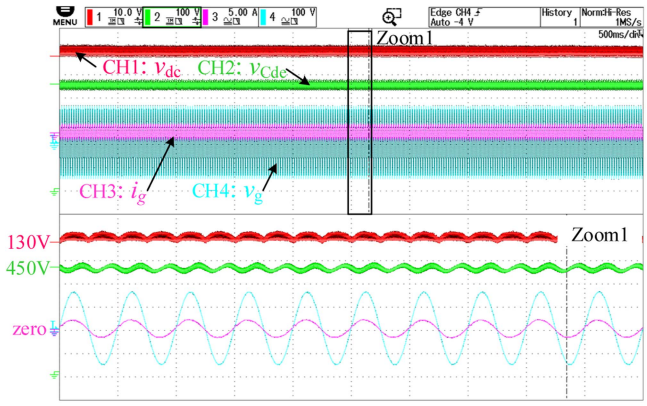


Fig. 19. Steady-state waveforms of the rectifier when $v_{\rm dc} = 130$ V.

When the grid voltage is 110 V and the output dc voltage is 250 V, based on the device parameters provided in Tables III and IV, the rectifier's efficiency curve at various input power levels is plotted in Fig. 22. The maximum experimental efficiency of the proposed rectifier is 94.4%, and the maximum estimated

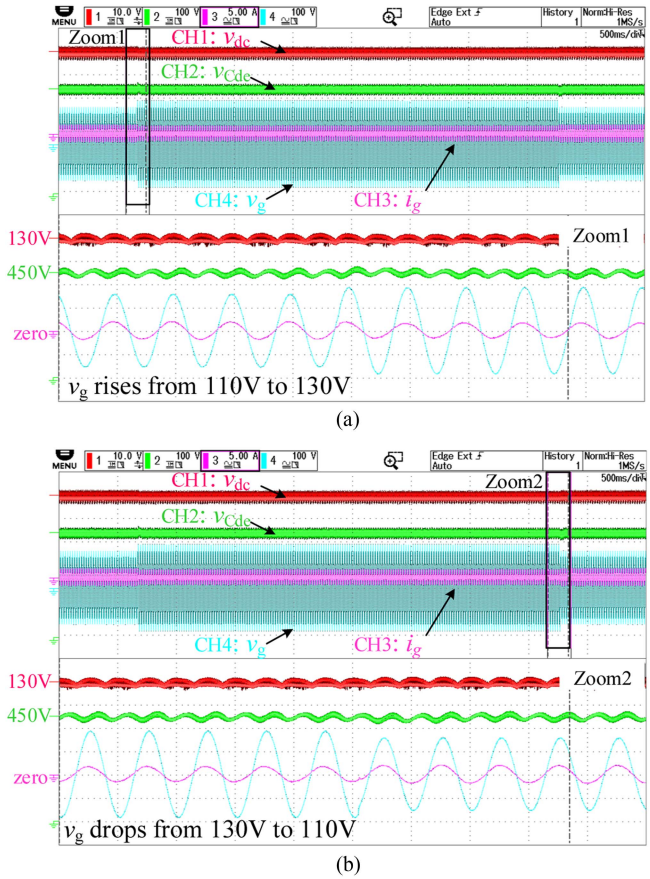


Fig. 20. Dynamic waveforms of the rectifier when (a) $v_{dc} = 130$V, v_g rises from 110 to 130 V and (b) v_g drops from 130 to 110 V.

TABLE IV
TYPE OF THE MAIN COMPONENTS

Device	Symbol	Type
*Switch	S	IPZ65R019C7
Diode	D	STTH30R06
Filter capacitor	C_f	FS55X105K631EHG
DC-link capacitor	C_{dc}	UCY2V470MHD
Decoupling capacitor	C_{de}	C4AQOEW5400M3CJ

* Switches $S_{1\text{-}3}$ are equivalent to a MOSFET connected in series with a diode, respectively, and switch S_4 is a MOSFET

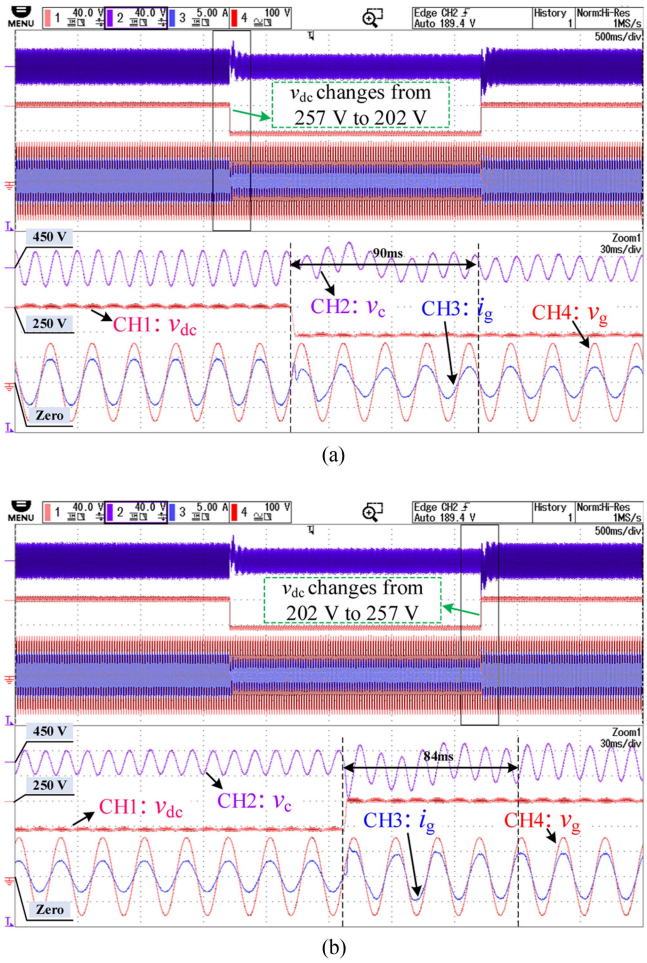


Fig. 21. Dynamic waveforms of the rectifier when (a) v_{dc} drops from 257 to 202 V and (b) v_{dc} rises from 202 to 257 V.

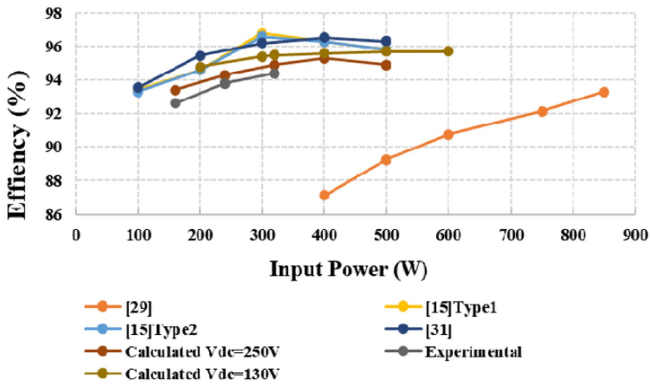


Fig. 22. Efficiency curves at different input powers.

efficiency is 95.3%. Furthermore, when the output dc voltage is set to 130 V for step-down operation, the theoretically calculated maximum efficiency of the rectifier reaches 95.7%. Although the efficiency of the proposed rectifier is not the highest, it is still acceptable.

Fig. 23(a) illustrates the power loss distribution among the main components when $v_g = 110$ V, $v_{dc} = 250$ V, and $P_{in} = 320$ W. The diode power losses represent the largest portion of the total power losses, accounting for 42%, with diode D_2 contributing the most at 21%. Switch power losses account for 29% of the total, with switch S_4 having the smallest share at 4%. The power losses of switches S_1 and S_2 are almost equal, respectively contributing 9% and 10% of the total. The total inductor power loss makes up 29%, with the dc inductor power loss being 9% higher than that of the grid-side inductor, which results from the AC losses and the larger inductance value of the dc inductor.

Fig. 23(a) illustrates that semiconductor losses constitute 71% of the total losses, amounting to approximately 14.2 W. Fig. 23(b)–(d) presents the distributions of total losses, conduction losses, and switching losses for the semiconductor devices,

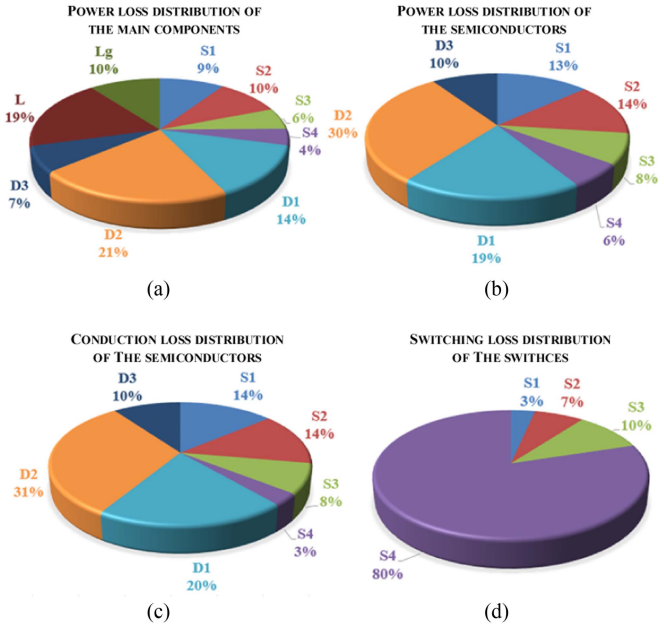


Fig. 23. Power loss distribution of the main components when $v_{\rm g} = 110$ V, $v_{\rm dc} = 250$ V and $P_{\rm in} = 320$ W.

TABLE V
POWER LOSS IN THE MAIN COMPONENTS OF THE RECTIFIER AT INPUT POWER LEVELS OF 50, 320, AND 600 W, RESPECTIVELY

Device	Condition 1 $P_{\rm in}$= 50 W	Condition 2 $P_{\rm in}$= 320 W	Condition 3 $P_{\rm in}$= 600 W
S_1	0.85 W	1.901 W	3.083 W
S_2	0.853 W	1.924 W	3.153 W
S_3	1.087 W	1.123 W	1.182 W
S_4	0.517 W	0.873 W	1.474 W
D_1	2.214 W	2.725 W	3.259 W
D_2	1.825 W	4.256 W	6.777 W
D_3	0.839 W	1.35 W	1.884 W
L	1.15 W	3.76 W	8.187 W
L_g	0.638 W	2.086 W	4.542 W
Total losses	9.973 W	19.998 W	33.541 W

respectively. It is observed that diode D_1 has the highest conduction loss, followed by D_2, with switches S_2 and S_1 coming next. Additionally, Fig. 23(d) indicates that switch S_4 experiences the greatest switching loss. Therefore, to enhance system efficiency, it is recommended to select diodes with a low on-state voltage drop for D_1 and D_2, choose switches with low on-state resistance for S_2 and S_1, and opt for a switch with superior switching performance for S_4.

Table V and Fig. 24 illustrates the comparison of the power loss distribution among the main components of the rectifier, expressed as a percentage of the total loss, at input power levels

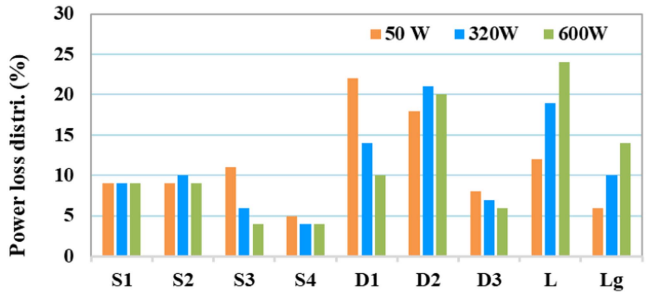


Fig. 24. Comparison of the power loss distribution among the main components of the rectifier, expressed as a percentage of the total loss, at input power levels of 50, 320, and 600 W when $v_g = 110$ V, $v_{\rm dc} = 250$ V.

of 50, 320, and 600 W when $v_g = 110$ V, $v_{\rm dc} = 250$ V. As the power increases, the loss percentages of switch S_3 and diodes D_1 and D_3 significantly decrease. In contrast, the loss percentages of inductors L and L_g show a noticeable increase. Meanwhile, the loss percentages of switches S_1, S_2, S_4, and D_2 change little. This indicates that, with increasing power, the loss characteristics of different components vary significantly, suggesting a need to pay attention to the loss issues related to inductors in the design.

VI. COMPARISON WITH EXISTING SINGLE-PHASE COMMON-GROUND RECTIFIERS

In this section, the proposed rectifier is compared with the existing single-phase common-ground rectifier, as given in Table VI. Generally, the number and stress of active components are directly related to the system's complexity and cost, whereas the quantity and size of passive components influence the system's overall size and cost [5], [27]. Through APD technology, small-capacity film capacitors can be used to replace large-capacity electrolytic capacitors. In addition, switching frequency, efficiency, THD, transition time, operating mode, power level of the test prototype, output voltage ripples etc. are used to evaluate the performance of the rectifier. It is worth noting that the output type affects the application scenario of the rectifier.

For instance, Maghsoudi and Farzanehfard [29] proposed a bridgeless rectifier using a single-core coupled inductor that achieved high efficiency through full soft-switching technology, it experienced significant output voltage fluctuations and high THD. The operating voltage and power levels of [15] and [30] are comparable to our proposed rectifier, but both [30] and [31] exhibit lower efficiency, with [31] designed for only 40 W. In contrast, Pourmahdi et al. [15] introduced a common-ground rectifier with positive and negative outputs, which offers higher efficiency but lacks APD capabilities and still requires large electrolytic capacitors, leading to low power density.

Moreover, Tian et al. [22], Yang et al. [32], and Tian et al. [33] presented rectifiers with APD capabilities. However, the application scenarios for the rectifiers in [22] and [33] are primarily limited to low-power LED applications with medium power density, operating in current source mode. Building upon the wide input voltage capability demonstrated in [22], theoretical analysis confirms that the proposed circuit when

TABLE VI
COMPARISON WITH EXISTING COMMON GROUND RECTIFIERS

Topology		Maghsoudi and HFarzanehfard [29]	Li et al. [30]	Malekanehrad and Adib [31]	Pourmahdi et al. [15]	Tian et al. [22]	Yang et al. [32]	Tian et al. [33]	Proposed
Number of	*HFS*	3	3	2	2	4	3	3	3
	D	4	5	4	4	3	2	2	3
	L (mH)	4 (0.5)	2 (0.6+1.2)	4 (2+ 2*25uH+ 0.5uH)	3 (1.5+0.2+ 0.2)	2 (1+0.4)	2 (3+2)	3 (3uH+ 0.1+0.5)	2 (3.6+4.8)
	C	2	2	3	3	1	2	2	3
Max. number of semiconductors in power loop		3	2	2	2	3	3	3	3
APD Capacitor		None	None	None	None	6 uF	57 uF	8.8 uF	40 uF
DC-Link Capacitor		1700 uF	5600 uF	2200 uF	20000 uF	None	20 uF	None	40 uF
Switches voltage stress		$\max(V_{ac}+V_{dc})$	n/a (S:650V/ 68.5A D:650V/ 30A)	n/a (S:500V/ 13A D:600V/ 8A)	$V_{ac}+V_{dc}$	$S_{PFC1\text{-}2}$: $(V_{ac}+V_c)/2$ $S_{1\text{-}2}$: $\lvert V_o-V_c \rvert$	$V_{ac}+V_{dc}$	n/a (*S*:600V/ 1.9A *D*:600V/ 4A)	S_1:V_{ac} S_2:$V_{ac}+V_c$ S_3:V_c-V_{dc} S_4: V_c
Switches current stress		$\max(I_{Lm})$			$I_{ac}+I_{dc}$	$S_{PFC1\text{-}2}$:I_{ac} S_1:I_{ac} S_2:I_o	$I_{ac}+I_{dc}$		I_L
V_{ac}→V_{dc} (V)		110→48	110→200	110→24	110→200	90~240→80	100→72–150	220→65	110→250
f_s (kHz)		100	40	50	50	50	50	25	20
$T_{transition}$		≈0.1s	≈0.2s	n/a	≈0.35s	n/a	0.9s	≈0.2s	0.09s
Output Voltage ripple rate		≈10%	<5%	<5%	<5%	n/a	2.53% (V_o=150 V)	n/a	3.6%
Efficiency		96.20%	90.53%	93.30%	96.80%	≈92.30% (V_{ac}=120V)	96.54%	96.80%	94.4%
THD		4.0%	n/a	3.5%	2.6%	≈3%	3.1%	4.59%	2.7%
Operation		DCM	CCM	DCM	DCM	DCM	CCM	DCM	CCM
Rated power		120 W	360 W	40 W	500 W	50 W	400 W	100 W	320 W
Modulation		Unipolar PWM	Unipolar PWM	Unipolar PWM	Unipolar PWM	Unipolar PWM	Unipolar PWM	Unipolar PWM	Unipolar PWM
Power density		Low	Low	Low	Low	Medium	High	Medium	High
Output Type		Constant Voltage	Constant Voltage	Constant Voltage	Constant Voltage	Constant Current	Constant Voltage	Constant Current	Constant Voltage

Note: *HFS*: High frequency switch, *L*: Inductor, *C*: Capacitor, *D*: Diode, n/a: Not reported, $T_{transition}$: Transition time, f_s=Switching frequency.

implemented with properly rated voltage-tolerant devices can effectively operate across a 100-240V input range. Although, Yang et al. [32] proposed a three-switch common ground rectifier with enhanced efficiency and fewer components, resulting in high power density, it demonstrated a 25% output voltage fluctuation (from 100 to 125 V) when power changes by 50% (from 400 to 200 W), indicating that complete power decoupling was not achieved. Additionally, its transition time is relatively long, at 0.9 s, with larger current stress on the power switches.

Based on the comprehensive analysis provided, our proposed rectifier demonstrates acceptable efficiency, high power density and commendable dynamic performance, making it a competitive option in its application space.

VII. CONCLUSION

Compared to isolated rectifiers, non-isolated rectifiers, particularly those with step-up and step-down functionality, are more suitable as interfaces between traditional ac systems and dc loads due to their advantages in efficiency, cost, size, and installation ease. However, non-isolated rectifiers often face challenges such as CM voltage and parasitic capacitance to ground, which can generate leakage current, adversely affecting the safety and performance of electrical equipment. Furthermore, these rectifiers typically require large dc-link capacitors on the dc side for effective power decoupling.

To address these issues, this article proposes a novel single-phase common-ground rectifier with APD, which offers the following advantages.

1) The common-ground structure ensures complete leakage current suppression.
2) The APD capability allows the use of small-capacity, long-life film capacitors, replacing the need for large-capacity, short-life electrolytic capacitors.
3) The step-up and step-down functionality facilitates a wide output voltage range.

This article provides a detailed analysis of the proposed rectifier, introduces the control strategy, derives the design method for passive components, and validates the performance through experimental results.

Future work will focus on the modularization of the proposed rectifier, as well as enhancing efficiency and increasing power levels.

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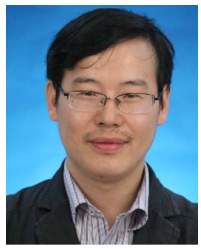

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