A Novel Scalable Multilevel PFC Rectifier Based on Full Binary-Tree Structure

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***Abstract*—This article presents a novel scalable multilevel power factor correction rectifier topology, termed the multilevel topology based on the full binary tree (MT-FBT). Through the utilization of new clamping units, the MT-FBT constructs the multilevel network by successively binary partitioning the root node and extending it with branch nodes. Therefore, more voltage levels can be obtained due to a multiplying effect. Moreover, a computationally efficient carrier-overlapping pulsewidth modulation strategy has also been employed to maintain the voltage balance of the dc-link capacitors. A four-level implementation is presented to demonstrate the operation principle, modulation method, and control scheme of the proposed topology. Finally, experimental results from a 1 kW prototype confirm that the MT-FBT meets the design criteria for both steady-state and dynamic performance.**

***Index Terms*—Active rectifiers, bridgeless converters, full binary tree, multilevel converters, multilevel topology, power factor correction, single-phase ac-dc converters.**

I. Introduction

MULTILEVEL rectifiers have attracted significant attention in power conversion systems due to their advantages, including reduced voltage stress across power switches, lower harmonic distortion, and enhanced fault-tolerant capability. These features are particularly valuable in applications such as renewable generation inverters, electric transportation systems, large motor drives and electric vehicle charging [1], [2], [3], [4]. Representative topologies, such as the neutral-point-clamped (NPC) [5], flying-capacitor (FC) [6], cascaded H-bridge [7], and active-neutral-point-clamped (ANPC) converters have been extensively adopted in industrial practice.

However, the proliferation of auxiliary components, such as diodes, capacitors, and independent power sources, makes it difficult to achieve more output voltage levels for these topologies and significantly complicates system scaling [8], [9]. Typically, obtaining a higher number of output voltage levels necessitates the development of entirely new topologies. This process involves redesigning control strategies and capacitor voltage balancing mechanisms, while addressing challenges such as minimizing switching losses, managing voltage stress on power switches, and enhancing power density [10]. Furthermore, most multilevel converters require balanced voltage on the dc-link capacitors. This challenge is also prevalent in nonmultilevel Buck-derived topologies with split dc bus [11], [12], [13]. Current mitigation strategies predominantly concentrate on advanced control algorithms and balancing circuits [14], [15], [16], [17]. However, specialized balancing algorithms often lead to higher computational complexity and greater memory requirements. Furthermore, dedicated balancing circuits often compromise power density, increase cost, and elevate electromagnetic interference emission, collectively limiting the practical industrial adoption of highly scalable topologies [18], [19], [20], [21].

While some recent works have proposed modular units or embedded-switch approaches, they often suffer from issues such as excessive switching loss, low scalability, limited voltage gain, or bulky passive components. Two diodes and two power switches are combined as a basic unit to obtain more voltage levels [22], [23]. While this configuration increases the number of current paths, it incurs higher switching losses due to the additional switches. Similarly, the topology in [24] employs a unit composed of four diodes and one power switch. This configuration reduces the number of required active switches but does not further increase the output voltage levels. Three circuit topologies are proposed in [25], but scalability issues remain unresolved. Additionally, each topology demands four separate inductors, which compromises both power density and overall efficiency. The work in [26] introduces a topology that extends output voltage levels by combining basic power cells. However, it requires many capacitors as the number of output levels increases. The complexity of the basic power cell adversely affects system stability and power density.

Notably, some studies have proposed unified design criteria or systematic derivation methodologies. These approaches may prove beneficial for the development of new topologies [27], [28], [29]. A family of three-level power factor correction (PFC) rectifier topologies is proposed in [30] with the idea of embedded power switches. By replacing the bridge arms with different types of bidirectional switches, these topologies achieve multilevel operation with fewer switches and capacitors. However, the scalability of the voltage levels was not further investigated. Recent work on Buck rectifiers has focused on component reduction and modulation optimization, especially for low-THD applications in aviation and data centers, but the

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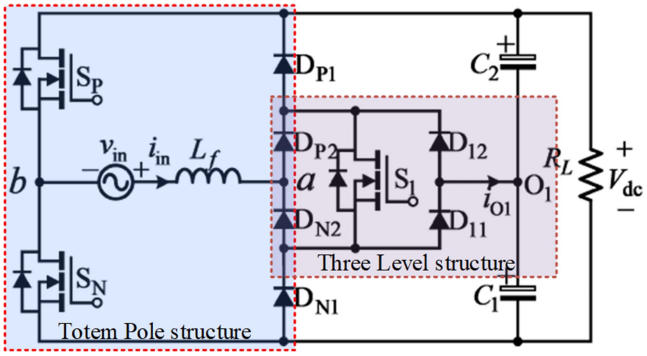

Fig. 1. Obtained three-level PFC.

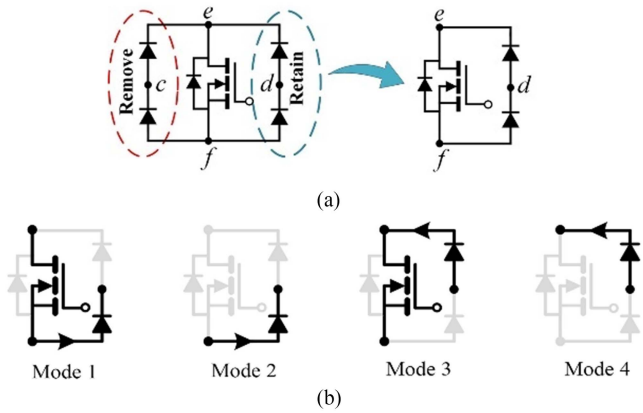

Fig. 2. (a) Obtaining the new clamping unit. (b) Different current paths of the new clamping unit.

scalability remains constrained by the nature of single-stage conversion [31], [32]. Achieving a higher number of voltage levels with good scalability, reduced component count, and an efficient capacitor voltage balancing strategy remains a major research focus for multilevel PFC rectifiers [33], [34].

Despite numerous developments in multilevel converter designs, achieving higher output voltage levels with good scalability, minimal component count, and efficient capacitor voltage balancing remains a challenge. This article proposes a multilevel topology based on the full binary tree (FBT) as an effective solution. The topology targets low-voltage, grid-connected single-phase rectifier applications, including on-board chargers, residential converters, and communication power supplies. It inherently supports scalability, allowing the generation of more voltage levels within a unified circuit structure. A compact control algorithm is also presented to enhance its applicability in commercial contexts.

The rest of this article is organized as follows: Section II introduces the derivation of the MT-FBT topology and its scaling methodology. Section III presents the implementation of the derived four-level PFC example FT-MBT-4 and its operating principle. The modulation scheme, capacitor voltage balancing algorithm, and control strategy are discussed in Section IV. Section V provides experimental results and a comparative study. Finally, Section VI concludes the article.

II. Derivation of the Proposed Multilevel Topology and Scaling Method

As illustrated in Fig. 1, the three-level PFC converter is obtained by embedding the three-level structure into the totem pole circuit. The clamping unit (CU) shown in Fig. 2(a) consists of one switch and four diodes. By removing the diodes on one side, the new clamping unit (NCU) is obtained. Current paths between any two nodes can be established by controlling the power switch, as illustrated in Fig. 2(b). Based on the circuit in Fig. 1, the three-level topology is further improved by as follows:

1) Adding a capacitor in series with the original two capacitors in the dc bus.
2) Connecting node *d* of the original CU to nodes *e* and *f* of the two newly added NCUs.
3) Connecting the *d* nodes of the two newly added NCUs to the center nodes of the series-connected dc-link capacitors.

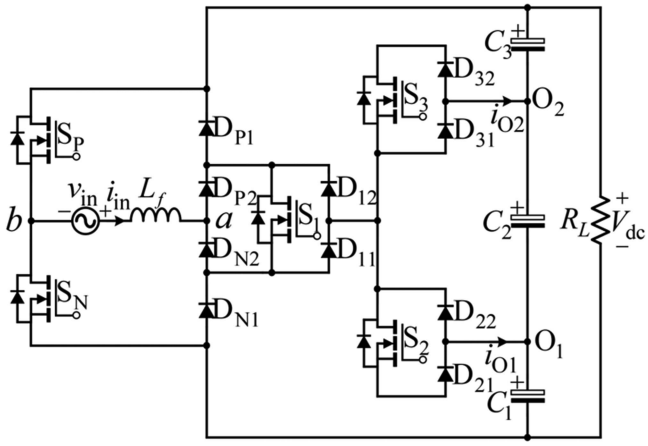

Fig. 3. Four-level PFC example of the MT-FBT.

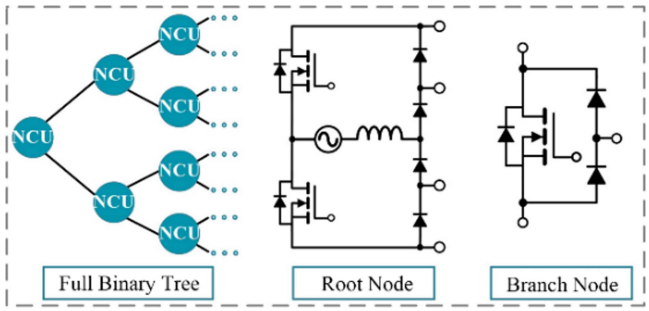

Fig. 4. Structure of the full binary tree and basic modules of FT-MBT.

Therefore, the four-level rectifier topology example shown in Fig. 3 is obtained. To increase the number of output voltage levels, NCUs are employed as branch nodes. Fig. 4 illustrates the basic modules in the proposed multilevel topology, the root node and the branch node. The multilevel rectifier topology is constructed by successively binary partitioning the root node and extending it with more branch nodes. While the root node retains part of the totem pole PFC structure, the branch nodes allow the bidirectional current flow and therefore assure multilevel operation. The generalized structure of the proposed multilevel

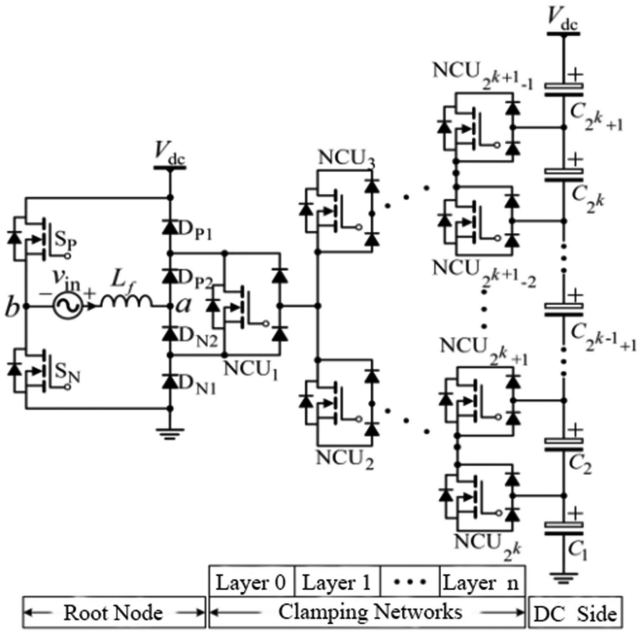

Fig. 5. Generalized structure of MT-FBT.

TABLE I
OVERALL COMPONENT QUANTITY OF THE MT-FBT TOPOLOGY

Clamping layer	0	1	…	k
V_{ab} level	3	4	…	2^k+2
Root nodes	1	1	…	1
Branch nodes	1	3	…	$2^{k+1}-1$
Switches	3	5	…	$2^{k+1}+1$
Diodes	6	10	…	$2^{k+2}+2$
DC-link capacitors	2	3	…	2^k+1
Inductors	1	1	…	1
Total	12	19	…	$7\times2^k+5$

topology is illustrated in Fig. 5. It is observed that the proposed MT-FBT topology exhibits structural similarities to an FBT in computer science, as summarized follows:

1) The number of nodes on layer i is 2^{i-1}.
2) The number of nodes in each layer follows a geometric progression with a first term of 1 and a common ratio of 2.
3) The total number of nodes in a k-layer FBT is 2^{k-1}.

To further evaluate the advantages of the proposed MT-FBT topology in terms of component count, a comparative analysis is conducted against several well-established multilevel topologies. Table II gives the component quantities required by several different topologies to generate $2h$+1 output voltage levels, where h is a positive integer. It should be clarified that the MT-FBT topology inherently produces even-numbered voltage levels. Therefore, the component counts shown for MT-FBT in Table II correspond to the components required to generate $2h$+2 levels. Given a specified layer number k, the voltage level count and the number of auxiliary components of the MT-FBT topology can be derived, as given in Table I. The relationship between k and the output voltage levels exhibits an exponential scaling, offering a more compact configuration compared to

TABLE II
COMPONENT REQUIREMENTS FOR GENERATING ($2H$+1) LEVELS IN DIFFERENT TOPOLOGIES

Topology	DC-link Capacitor	Flying Capacitor	Diode	Switch	Total
NPC	$2h$	0	$2h(2h$-1)	$4h$	$4h(h$+1)
FC	$2h$	$h(2h$-1)	0	$4h$	$h(2h$+5)
SMC	$2h$	$h(h$-1)	0	$4h$	$h(h$+7)
ANPC	$2h$	$h(h$-1)/2	0	$6h$	$h(h$+15)/2
MT-FBT	2^h+1	0	$2^{h+2}+2$	2^{h+1}+1	4+7*2^h

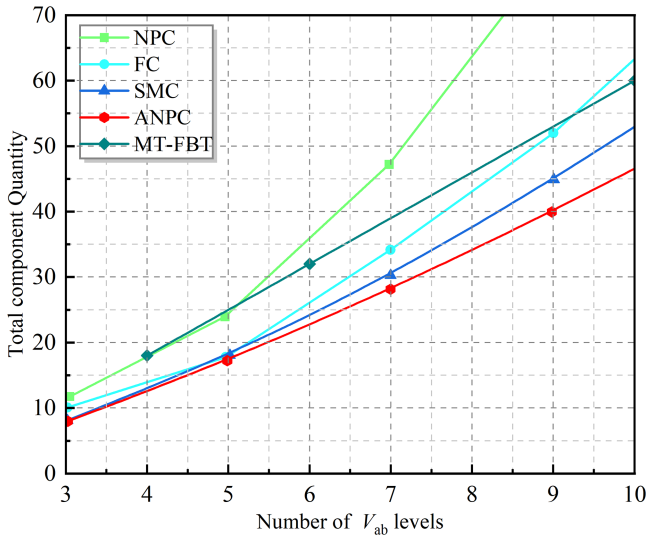

Fig. 6. Component quantity comparison between MT-FBT and other multilevel topologies.

conventional topologies. As illustrated in Fig. 6, the data from Tables I and II are compared up to ten levels. Therefore, the proposed MT-FBT topology demonstrates clear advantages in terms of system cost and control strategy complexity.

III. OPERATING PRINCIPLE OF MT-FBT-4

The switching behaviors of the MT-FBT-4 during an entire line cycle are listed in Table III. The OFF and ON states of the switches are represented by "0" and "1," respectively. The equivalent circuits illustrating each operation modes are illustrated in Fig. 7. The proposed multilevel topology shows a symmetrical behavior in the negative half of the line cycle. Therefore, only the operation modes during the positive half cycle is explained in this section.

Mode-1: S_N is gated, D_{P1} and D_{P2} are forward-biased at the start of this mode. The voltage between a and b satisfies $V_{ab} = V_{C1}+V_{C2}+V_{C3}$. The inductor charges C_1, C_2, and C_3 at a current of i_{in}-i_{dcp}, with the current path shown in Fig. 7(a). The relation between inductor current and dc-link voltage during this mode can be described as

$$L_f \frac{di_{\text{in}}}{dt} = v_{\text{in}} - V_{\text{dc}}. \tag{1}$$

TABLE III
KEY OPERATING STATES OF THE MT-FBT-4 FOR DIFFERENT MODES

Mode	S_P	S_N	S_1	S_2	S_3	V_{AB}	A	B	C	D	C_1	C_2	C_3
1	0	1	0	0	0	V_{dc}	1	1	1	1	Charge	Charge	Charge
2	0	1	1	0	0	$2/3V_{dc}$	1	0	1	1	Charge	Charge	Discharge
3	0	1	1	1	0	$1/3V_{dc}$	1	0	0	1	Charge	Discharge	Discharge
4	1	0	0	0	0	0	1	0	0	0	Discharge	Discharge	Discharge
5	0	1	0	0	0	0	0	0	0	0	Discharge	Discharge	Discharge
6	1	0	1	0	1	$-1/3V_{dc}$	0	0	0	1	Discharge	Discharge	Charge
7	1	0	1	0	0	$-2/3V_{dc}$	0	0	1	1	Discharge	Charge	Charge
8	1	0	0	0	0	$-V_{dc}$	0	1	1	1	Charge	Charge	Charge

Mode-2: The ON state of S_1 denotes the completion of mode-1 and the beginning of mode-2. S_N is gated, accompanied by the conduction of D_{P2}, D_{11}, and D_{31}. According to the relative value of v_{in} and V_{dc}, inductor L_f has two different states:

1) If $v_{in} < 2/3V_{dc}$, C_3 discharges at a current of i_{dcp} to supply the load, while C_1 and C_2 charge at a current of i_{in}-i_{dcp}. Energy stored in L_f is transferred into C_1 and C_2.
2) If $v_{in} > 2/3V_{dc}$, C_3 discharges, C_1, C_2, and L_f charges. With the linear increase of the inductor current, energy is now gradually stored in C_1, C_2, and L_f.

Although inductor current i_{in} has two states in this mode, a single equation can be employed because of the unaltered circuit structure

$$L_f \frac{di_{in}}{dt} = v_{in} - \frac{2}{3}V_{dc}. \tag{2}$$

The current path in this mode is shown in Fig. 7(b).

Mode-3: The end of Mode-2 is characterized by the gating of S_2 and the conduction of S_1 and S_N. Diodes D_{P2}, D_{11}, and D_{21} are forward-biased, while all other semiconductor components remain nonconductive. $V_{ab} = V_{C1}$ is obtained because of the commutation path provided by the lower branch node. Similar to mode-2, inductor L_f in this mode also has two different states according to the relative value of v_{in} and V_{dc}.

1) If $v_{in} < 1/3V_{dc}$, L_f charges C_1 at a current of i_{in}-i_{dcp}. C_3 and C_2 discharge at a current of i_{dcp} to supply the load.
2) If $v_{in} > 1/3V_{dc}$, C_1 charges, C_2, and C_3 discharges. L_f is gradually storing energy.

A unified equation applies to both states owing to the consistent circuit configuration.:

$$L_f \frac{di_{in}}{dt} = v_{in} - \frac{1}{3}V_{dc}. \tag{3}$$

The current path in this mode is shown in Fig. 7(c).

Mode-4: Fig. 7(d) illustrates the corresponding operating state for this mode. Turn-OFF of S_N after mode-3 triggers the beginning of mode-4. During this mode, S_P is turned ON, D_{P2} and D_{P1} are brought into conduction. All capacitors of C_1, C_2, and C_3 discharge, inductor L_f charges up with a linearly rising current i_{in}. The mathematical model of this mode is given as follows:

$$L_f \frac{di_{in}}{dt} = v_{in}. \tag{4}$$

IV. SYSTEM CONTROL AND COMPREHENSIVE ANALYSIS

A. Modulation Strategy

The proposed MT-FBT-4 employs a triple-carrier overlapping modulation strategy, as illustrated in Fig. 8. The gating signals are generated based on logical operation. In the proposed strategy, the carriers v_1, v_2, and v_3 are of the same frequency and phase but differ in amplitude, with $v_1(t) = v_3(t) + 1.5$ and $v_2(t) = 2v_3(t)$. Four logic values A, B, C, and D are defined as follows to obtain the gating signals

$$A = \begin{cases} 1, v_{ref} > 0 \\ 0, v_{ref} < 0 \end{cases} \tag{5}$$

$$B = \begin{cases} 1, |v_{ref}| > v_1 \\ 0, |v_{ref}| < v_1 \end{cases} \tag{6}$$

$$C = \begin{cases} 1, |v_{ref}| > v_2 \\ 0, |v_{ref}| < v_2 \end{cases} \tag{7}$$

$$D = \begin{cases} 1, |v_{ref}| > v_3 \\ 0, |v_{ref}| < v_3 \end{cases}. \tag{8}$$

B. Control Scheme and Analysis

As shown in Fig. 9, the MT-FBT-4 employs a dual-loop control scheme. The voltage loop stabilizes the output voltage, and the current loop tracks the line phase in real-time. The difference between reference voltage $V_{dc}*$ and actual value V_{dc} is regulated by a proportional-integral (PI) controller. After multiplying with the phase angle provided by the phase-locked loop, the current reference $i_{in}*$ for the current loop is obtained. Inside the current loop, the difference between $i_{in}*$ and actual line current i_{in} is processed by another PI controller to achieve phase synchronization of the input current.

In the proposed PFC topology, the capacitors are connected in series across the dc bus. Topologies of this type typically experience unbalanced capacitor voltages, resulting in uneven component aging and potential early system failure. By employing the carrier overlapping modulation, the voltage control of the three dc-link capacitors can be decoupled [35]. The

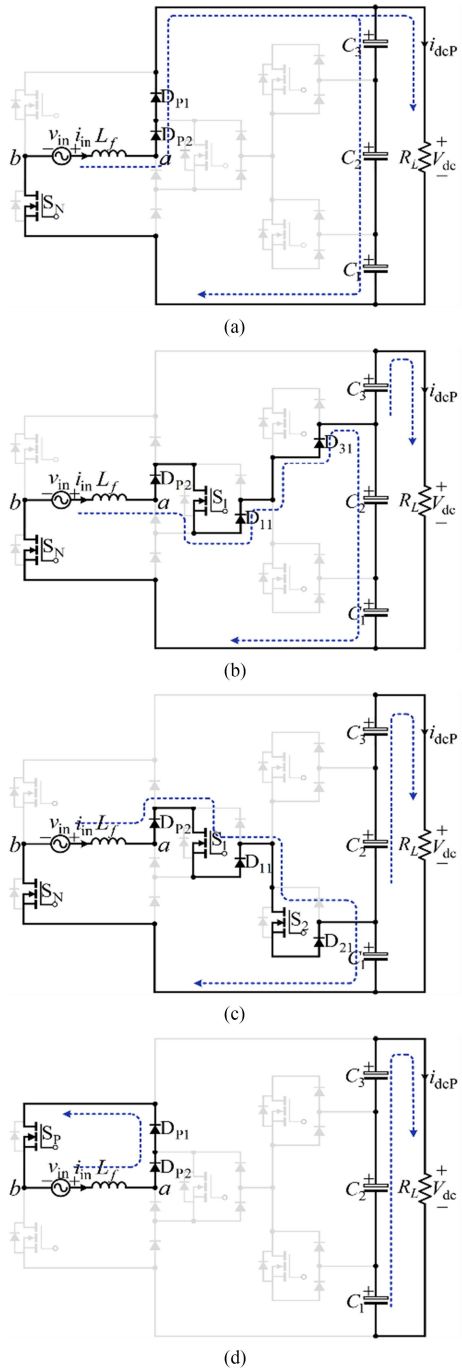

Fig. 7. Operation modes of the FT-MBT-4 during positive line cycle. (a) Mode-1. (b) Mode-2. (c) Mode-3. (d) Mode-4.

corresponding expressions are given as

$$\Delta u_{C1} - \Delta u_{C3} = \Delta u = \frac{(i_{o1} + i_{o2})T_s}{C} \tag{9}$$

$$\Delta u_{C2} = \frac{-(d_1 + d_3 - 2d_2)i_{\text{in}}T_s}{3C} \tag{10}$$

where Δu_{C1}, Δu_{C2}, and Δu_{C3} are the voltage fluctuations of capacitors C_1, C_2, and C_3, respectively. i_{O1} and i_{O2} are the currents flowing into nodes O_1 and O_2., d_1, d_2 and d_3 correspond to the duty cycles of B, C, and D in one carrier period, respectively.

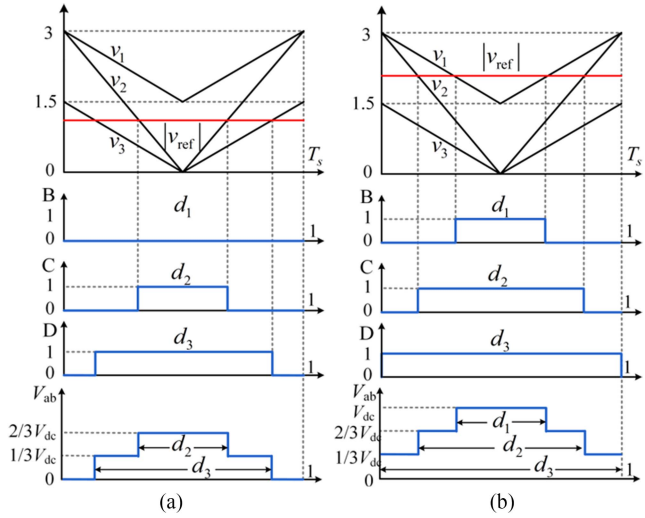

Fig. 8. Triple carrier overlapping modulation strategy in MT-FBT-4. (a) $0 \le |v_{\text{ref}}| < 1.5$. (b) $1.5 \le |v_{\text{ref}}| < 3$.

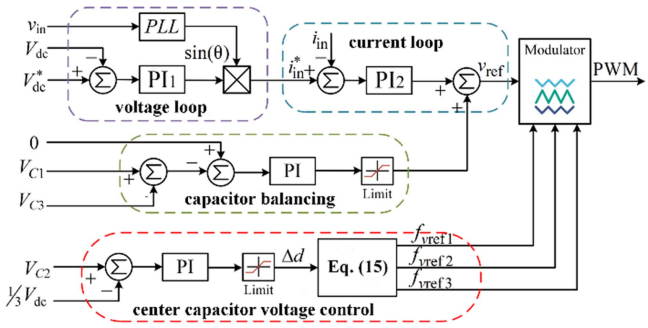

Fig. 9. Control scheme of the proposed MT-FBT-4.

The voltage difference between V_{C1} and V_{C3} is first compared to a reference value of zero. After processing through a PI controller, the resulting signal is added to the output of the current loop. As a result, balanced voltages across the upper and lower capacitors are obtained by adjusting the reference signal v_{ref} of the modulator.

To design the loop parameter, consider the basic dual loop of MT-FBT-4. Assume that G_{PI1} is the PI transfer function of the voltage loop, G_{PI2} is the PI transfer function of the current loop. The open-loop transfer function of the current loop, denoted as $G_{\text{io}}(s)$, can be expressed as

$$G_{io}(s) = \frac{G_{\text{PI2}}(s) * K_{PWM}}{L_S} \tag{11}$$

where K_{PWM} is the effective gain of the power stage.

Therefore, the closed loop transfer function of the current loop $G_{\text{ic}}(s)$ is obtained as:

$$G_{ic}(s) = \frac{1}{1 + L_S/(K_{PWM}G_{PI2}(s))}. \tag{12}$$

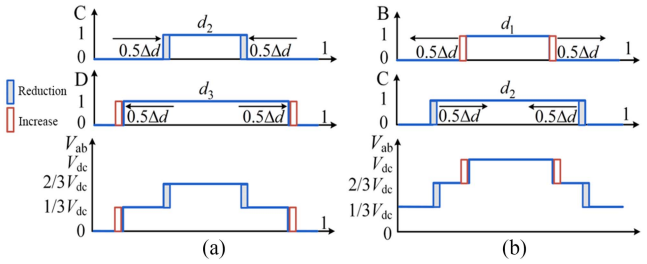

Fig. 10. Duty cycle fine-tuning to balance the middle capacitor. (a) $0 \le |v_{\rm ref}| < 1.5$. (b) $1.5 \le |v_{\rm ref}| < 3$.

TABLE IV
VOLTAGE BALANCING OF THE MIDDLE CAPACITOR

$1/3V_{dc}$-V_{C2}	$\lvert v_{ref}\rvert$	d_1	d_2	d_3
>0	$1.5 \le \lvert v_{\rm ref}\rvert \le 3$	$-\Delta d$	Δd	0
	$0 \le \lvert v_{\rm ref}\rvert < 1.5$	0	Δd	$-\Delta d$
<0	$1.5 \le \lvert v_{\rm ref}\rvert \le 3$	Δd	$-\Delta d$	0
	$0 \le \lvert v_{\rm ref}\rvert < 1.5$	0	$-\Delta d$	Δd

The transfer function of output dc voltage to input current can be written as

$$G_{ui}(s) = \frac{V_{\rm dc}}{i_{\rm in}} = \frac{kR_L}{1 + R_L C_S} \tag{13}$$

where k is the scaling factor of input current.

The open loop transfer function of the control loop is therefore derived as

$$G_{\rm op}(s) = \frac{G_{\rm PI1}(s) \cdot kR_L/(1 + R_L C_S)}{1 + L_S/(K_{PWM} G_{\rm PI2}(s))}. \tag{14}$$

The bandwidth of the voltage loop is chosen as 5 Hz, which is 10% of the line frequency. The current loop is designed with a relatively high bandwidth, with the parameters selected to achieve a fast dynamic response with minimal overshoot and undershoot.

C. Middle Capacitor Balancing

To achieve a balanced voltage of the middle capacitor, Δu_{C2} can be reduced by increasing d_1+d_3-2d_2 when $V_{C2} > 1/3V_{\rm dc}$, as illustrated in (10). If $0 \le |v_{\rm ref}| < 1.5$, keep d_1 constant, and reduce d_2 by Δd. To maintain the constant voltage on the bridge arms, increase d_3 by Δd, as is shown in Fig. 10(a). However, if $1.5 \le |v_{\rm ref}| < 3$, keep d_3 constant, reduce d_2 by Δd. At the same time, increase d_1 by Δd to maintain the same voltage on the bridge arms, as shown in Fig. 10(b).

Similar situations when $V_{C2} < 1/3V_{\rm dc}$ are listed in Table IV. Consider the case where $V_{C2} > 1/3V_{\rm dc}$ and $0 \le |v_{\rm ref}| < 1.5$. To obtain Δd, the difference of V_{C2} and $1/3V_{\rm dc}$ is first processed through a PI controller. Subsequently, the balancing factors $f_{v\rm ref1}$, $f_{v\rm ref2}$, and $f_{v\rm ref3}$ are calculated using (15). After adding $|v_{\rm ref}|$ to each balancing factor, the three resulting sums are compared with the carriers v_1, v_2, and v_3, respectively, as illustrated in Fig. 11. The duty cycles d_1, d_2, and d_3 are then adjusted accordingly to balance the middle capacitor voltage

$$\begin{cases} f_{v\rm ref1} = d_1 - |v_{\rm ref}| \\ f_{v\rm ref2} = 3(d_2 - \Delta d) - |v_{\rm ref}| \\ f_{v\rm ref3} = 1.5(d_3 + \Delta d) - |v_{\rm ref}| \end{cases}. \tag{15}$$

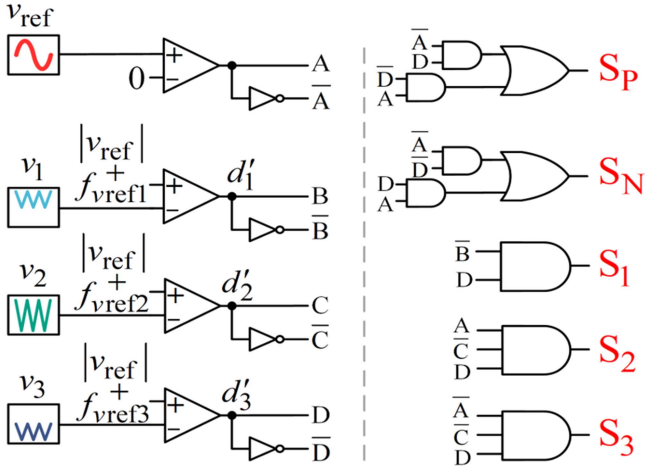

Fig. 11. Synthesis of gating signals.

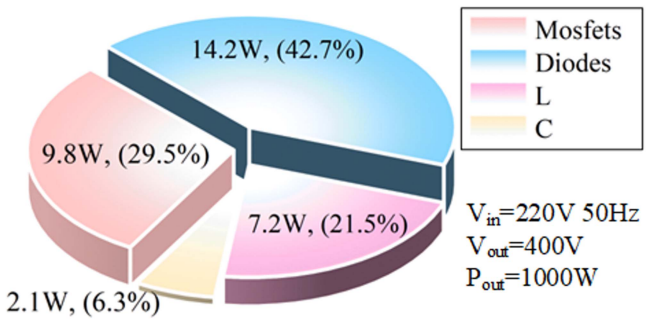

Fig. 12. Power loss analysis of the MT-FBT-4.

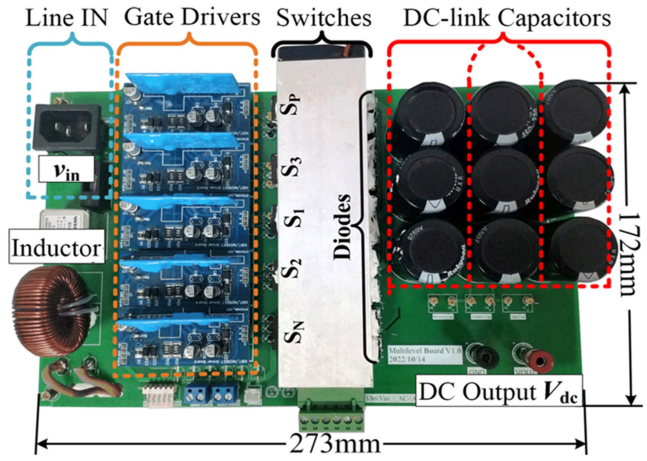

Fig. 13. Photo of the MT-FBT-4 prototype.

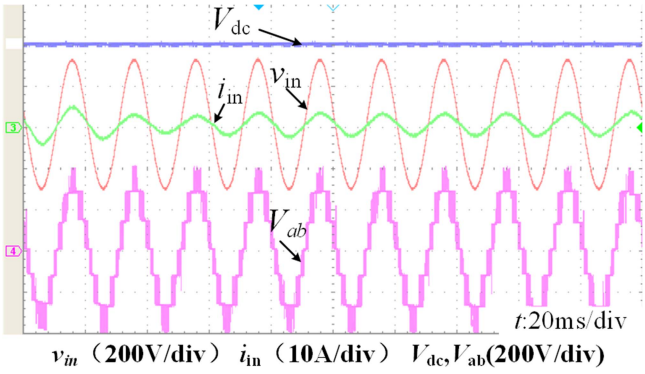

Fig. 14. Voltage and current waveforms of MT-FBT-4.

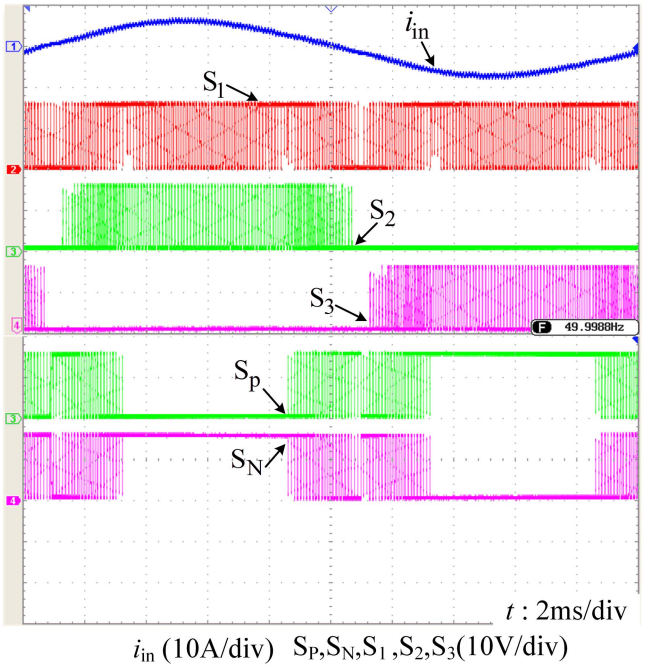

Fig. 15. Gating signals with input current of MT-FBT-4.

The capacitor voltage balancing strategy is also applicable to MT-FBT rectifiers with more output voltage levels. Additional carrier signals and logic values are introduced to support more switching states according to the specific circuit configuration. While the balancing principle for the outer capacitors remains unchanged, duty cycles corresponding to each logic value are dynamically adjusted to control the currents flowing into the center capacitors.

D. Loss Analysis

The power loss of the MT-FBT-4 include conduction losses and switching losses on power switches, ripple losses on capacitors, and core losses on the inductor. Conduction losses in MOSFETs and diodes were calculated using datasheet parameters and actual measured values, which is then calculated through

$$P_{\text{cond}} = {i_s}^2(t) * R_{\text{cond}} \tag{16}$$

$$P_d = i_d(t) * V_{\text{FD}} \tag{17}$$

where P_{cond} and P_d are the conduction losses on the MOSFETs and diodes, i_s and i_d are the currents passing through, R_{cond} is the conduction resistance of the MOSFETs, V_{FD} is the forward voltage drop of the power diodes.

Switching losses (P_{sw}) were evaluated based on the energy consumption generated during switch transitions [36]

$$E_{\text{off}} = \int_0^{t_{\text{off}}} \left[\left(\frac{v_{\text{off}}}{t_{\text{off}}} t \right) \left(-\frac{I_{\text{off}}}{t_{\text{off}}} (t - t_{\text{off}}) \right) \right] \tag{18}$$

$$E_{\text{on}} = \int_0^{t_{\text{on}}} \left[\left(\frac{v_{\text{on}}}{t_{\text{on}}} t \right) \left(-\frac{I_{\text{on}}}{t_{\text{on}}} (t - t_{\text{on}}) \right) \right] \tag{19}$$

$$P_{\text{sw}} = f_s \left[\sum_{k=1}^{N_{\text{sw}}} \left(\sum_{i=1}^{N_{\text{on}}} E_{\text{on}} + \sum_{i=1}^{N_{\text{off}}} E_{\text{on}} \right) \right] \tag{20}$$

where t_{off}, v_{off}, I_{off} are the turn-OFF time, voltage, current of a switch, respectively. And t_{on}, v_{on}, I_{on} are the corresponding parameters during turn-on time of a switch. N_{sw} is the number of switches, f_s is the switching frequency, and N_{on} and N_{off} are the numbers of switching transitions during a complete line cycle.

The ripple losses in each dc-link capacitor P_{cap} can be calculated as

$$P_{\text{cap}} = \frac{1}{2} C f_{\text{sw}} \Delta V_C^2 \tag{21}$$

where f_{sw} is the switching frequency, ΔV_C is the voltage ripple across the capacitor, and C is the capacitance.

The inductor core loss is evaluated using the general form of the core loss from the improved Generalized Steinmetz equation [37], [42]

$$P_{\text{core}} = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} dt \tag{22}$$

the coefficient k_i is calculated as

$$k_{\text{i}} = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha}} \tag{23}$$

where coefficients α, β, and k are manufacturer-provided constants, ΔB is the peak-to-peak value of magnetic flux density of the core, which is defined as

$$\Delta B = \frac{L \Delta I}{nA}. \tag{24}$$

The calculated total losses at rated output power are summarized in Fig. 12, where total MOSFET losses account for 29.5%, diode losses for 42.7%, and inductor plus capacitor losses for the remaining 27.8%.

V. Experimental Performance of MT-FBT-4

A laboratory-scaled prototype of the MT-FBT-4 has been developed to validate the proposed topology. The structure of the prototype is illustrated in Fig. 13. Other parameters of the prototype are given in Table V.

The steady-state performance of the MT-FBT-4 prototype under rated operating condition is presented in Fig. 14. The results demonstrate that the prototype achieves near-unity power

TABLE V
PARAMETERS OF MT-FBT-4 PROTOTYPE

Parameter	Value
Nominal input voltage	220 V/50 Hz
Rated output voltage	400 VDC
Rated output power	1 kW
Inductor L_f	2 mH/10 A
Capacitor C_1, C_2, C_3	3*680 μF/450 V
Diodes	SDUR1040
MOSFET	IRFP460PBF
Controller	TMS320F28335

factor operation at the grid, featuring four V_{ab} levels: $|\pm V_{\rm dc}|$; $|\pm 2/3V_{\rm dc}|$; $|\pm 1/3V_{\rm dc}|$, and 0. A stable 400 V dc-link voltage and low distortion in the line current are also observed. It is also observed that the pulse distribution aligns well with the results presented in Table III and Fig. 15.

To assess the dynamic performance of the converter, the dc voltage reference step-change and load-stepping experiment were conducted. Fig. 16(a) illustrates the output voltage response during the $V_{\rm dc}*$ step change. At $t = 0.1$s, $V_{\rm dc}*$ is increased from 400 to 450 V. The output voltage $V_{\rm dc}$ closely tracks the reference within 60ms, while V_{C1}, V_{C2}, and V_{C3} remain balanced. Fig. 16(b) and (c) depicts the load-stepping waveforms of the MT-FBT-4. The resistive load is switched from 100% to 50%, then back to 100%. During both changes, V_{C1}, V_{C2}, V_{C3}, and i_{in} are quickly stabilized within three-line cycles without significant overshoot or sudden transitions.

Fig. 17(a) presents the harmonic distribution of the line current under full load. The measured THD of the line current is 3.4%, which complies with the IEC 61000-3-2 standard of maintaining harmonic content below 5%. Fig. 17(b) presents the power factor of the prototype with distorted input voltage. It can be observed that the current THD still complies with the IEC 61000-3-2 standard requirements with the input voltage THD of 2.8%. Under rated operating condition, the measured power data are shown in Fig. 17(c).

Fig. 18 presents a comparison of the efficiency of the proposed MT-FBT-4 prototype against other similar prototypes. To ensure a fair comparison across converters with different rated output powers, the horizontal axis is defined as the loading ratio, i.e., the ratio of load power to each prototype's rated output power. The MT-FBT-4 prototype reaches a peak efficiency of 97.3% at 40% load and maintains an efficiency of 96.6% at full-load. The prototype exhibits higher efficiency than the similar topology in [40] across 10% - 85% of the rated load range, and outperforms the topology in [39] and [42] near 10% load. As shown in the efficiency curve, the MT-FBT-4 prototype sustains above 96.5% efficiency across a wide load range. The slight drop in efficiency beyond 40% load primarily results from increased semiconductor losses and resistive losses in the input protective components under high-current conditions.

To provide a more comprehensive understanding of the proposed MT-FBT topology, Table VI gives a quantitative comparison with several representative multilevel converter structures,

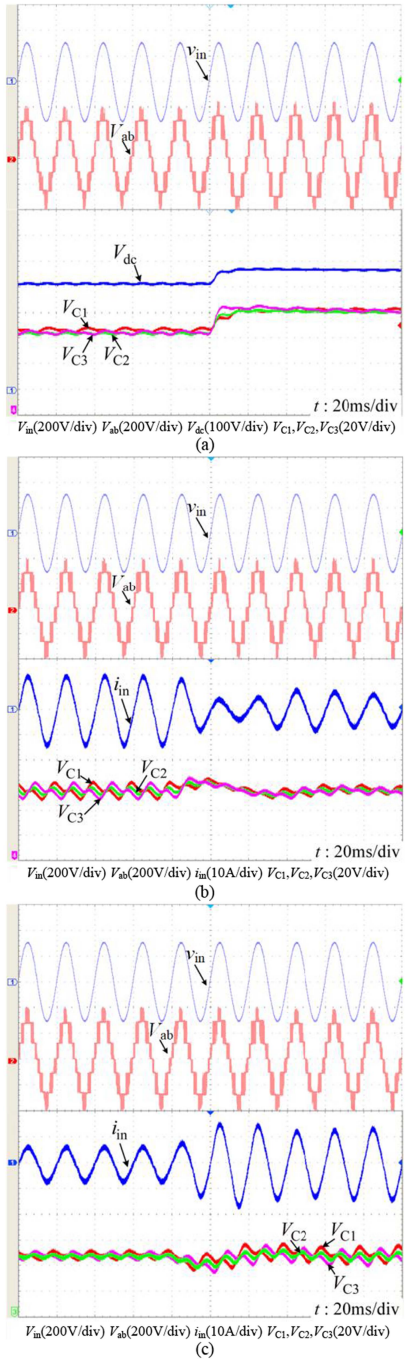

Fig. 16. Dynamic performance of proposed MT-FBT-4. (a) $V_{\rm dc}*$ step change. (b) Load-stepping from 100% to 50%. (c) Load-stepping from 50% to 100%.

including ANPC, hybrid-ANPC, and flying capacitor multilevel (FCML) topologies. The classification of control complexity is based on the complexity of control strategy, the modulation method, and the associated computational burden. Moreover, the gain is defined as the ratio of the dc output voltage to the peak value of the ac input voltage. It is observed that the proposed MT-FBT topology demonstrates several key advantages, including efficient component utilization, good scalability, low output ripple, balanced performance, and simple control. Utilizing only five switches, ten diodes, and three capacitors, the proposed

TABLE VI
COMPARATIVE EVALUATION OF MULTILEVEL TOPOLOGIES

Reference	Type	Components	THD	Peak Efficiency	Gain	Control Complexity	TVS	Output Ripple	Scalability
Proposed	MMC	5S 10D 3C[a]	3.4%	97.3%	1.29	Simple	V_{dc}	1.9 V_{p-p}	High
Chen [38]	ANPC	6S 3C	2.94%	99.54%	0.16	Complex	2/3 V_{dc}	2 V_{p-p}	Low
Huang et al. [39]	FCML	6S 6D 3C	3.9%	98.8%	1.79	Moderate	V_{dc}	13.9 V_{p-p}	Low
Chung et al. [40]	FCML	8S 3C	/	96.8%	1.25	Moderate	V_{dc}	1.5 V_{p-p}	Medium
Deng and Ma [41]	Hybrid-ANPC	12S 2D 5C	/	85.67%	1.29	Moderate	V_{dc}	2 V_{p-p}	Low
Ishraq and Mallik [42]	FCML	14S 5C	4.33%	99.14%	1.29	Complex	V_{dc}	11 V_{p-p}	Medium

[a] S = switches, D = diodes, C = capacitors.

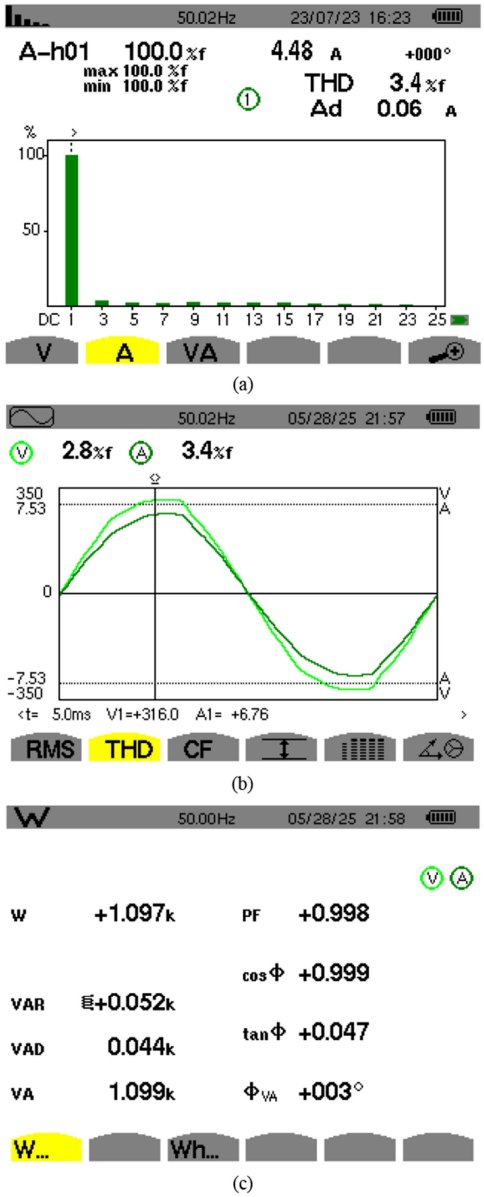

Fig. 17. Measured power data. (a) Input current harmonic. (b) Waveform of input current and distorted input voltage. (c) Power factor and other data.

topology achieves comparable output performance to more complex alternatives, while reducing overall component count and implementation cost. In contrast to many conventional topologies that become increasingly complex and hardware-intensive

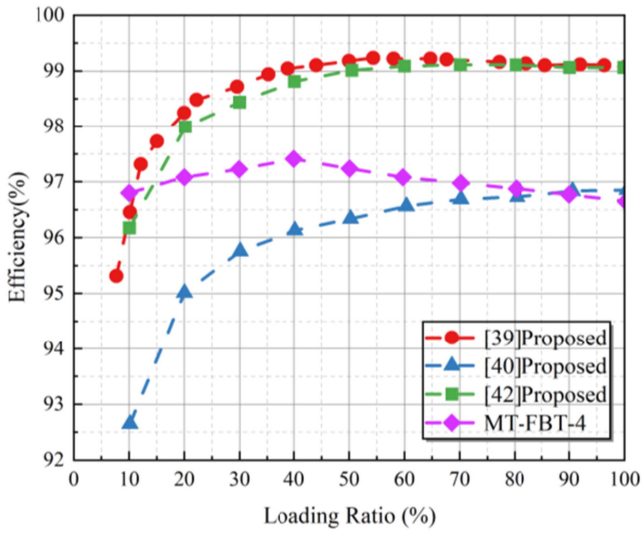

Fig. 18. Efficiency comparison between the proposed MT-FBT-4 and similar works.

as voltage level number increase, the proposed structure enables linear and predictable expansion with minimal control overhead.

The proposed topology achieves a favorable tradeoff between THD and efficiency, with a moderate voltage gain suitable for single-phase PFC applications. Moreover, its compact control strategy can be implemented on low-cost controllers, enhancing practicality in resource-constrained scenarios. Compared with the ANPC topology in [38], which yields higher efficiency (99.57%) but a significantly lower voltage gain (0.16), the proposed approach delivers a more balanced performance profile. FCML-based converters in [39] and [42] provide higher gain or lower THD, but at the cost of increased component count and design complexity. The MT-FBT topology offers a middle ground, making it attractive for practical and scalable applications.

VI. CONCLUSION

This article introduces a novel multilevel PFC rectifier topology based on the full binary-tree structure, demonstrating superior voltage level scalability compared to conventional topologies. Capacitor voltage balancing is achieved through an efficiency-improving PWM strategy. Experimental verification using the MT-FBT-4 prototype confirms the applicability of the proposed topology for medium- and small-scale converter designs. The following conclusions can be drawn.

1) The number of voltage levels generated by the MT-FBT topology increases exponentially with the number of clamping network layers. Compared with conventional multilevel topologies, the MT-FBT offers significant advantages in achieving more output voltage levels without the requirement of major modifications to the overall control scheme or modulation strategy.
2) For large-scale applications, the CUs can be integrated into independent modules by manufacturers. This modular design improves thermal management and facilitates periodic maintenance.
3) By keeping the external characteristics of the root and branch nodes unchanged, these modules can be substituted with alternative designs. This flexibility enables the development of new multilevel structures within the same framework.

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