A Novel Active Temperature Management Strategy for SiC MOSFETs

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***Abstract*—A major factor limiting the reliability of SiC MOSFETs is junction temperature fluctuation under nonstationary conditions. This article proposes an equivalent gate resistance control method to dynamically regulate switching loss, enabling active thermal management (ATM) of individual devices. Unlike conventional multiplexer-based approaches, the proposed method uses only two discrete resistors, reducing circuit complexity while achieving continuous control via delay modulation. Experimental results show that the proposed ATM method can effectively suppress temperature fluctuations (from 18.83 to 9.85 K), and the lifetime model estimation indicates a potential improvement of up to 2.18 times. To address the tradeoff between reliability and efficiency, this article further introduces the concepts of temperature control operating space and junction temperature control coefficient, enabling coordinated lifetime improvement with minimal additional power loss.**

***Index Terms*—Active thermal management, equivalent gate resistance control, junction temperature fluctuations, lifetime, SiC MOSFET.**

I. Introduction

POWER electronics technology is constantly being applied and developed in various fields [1], [2], [3]. Power electronic devices are critical in converting, transmitting, and controlling electric energy, and they will impact power network expansion and performance in the future. The wide band-gap semiconductor devices represented by SiC devices are widely used in producing high-temperature, high-frequency, and high-power electronic devices because of their advantages of high-temperature resistance, fast switching speed, and high efficiency. Its performance is better than that of traditional Si devices. However, for SiC devices, junction temperature fluctuation is one of the critical factors affecting reliability [4]. Numerous factors limit SiC MOSFET dependability. Temperature accounts for around 55% [5]. Studying how to increase the reliability of power devices and consequently improve the safety of power electronic systems is of practical value and significance.

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The superior electro-thermal properties of SiC power devices permit higher temperatures of operation and enable higher power density compared with silicon devices. Despite the superior electrical properties mentioned above, the limited reliability of SiC power devices hinders their application in the application fields [6]. Due to the direct contact of materials with different thermal expansion coefficients, the packaged components are subjected to thermal stress caused by the temperature variation during system operation. Thermal stress will deteriorate the weaker components in the encased device, resulting in device failure [7]. Converters generally work in nonstationary situations, creating random power fluctuations in the SiC MOSFETs. Increased thermal conductivity and Young's modulus of SiC [8] may create higher stress in the molded solder layer during power variation. In addition, power fluctuations generate temperature fluctuations in SiC MOSFETs [9], [10], resulting in welding fatigue [11], [12], [13]. Experimental results from different samples reveal that the shear stress in a SiC die-attach is higher than that in a Si device [14], and strain energy density tends to concentrate at the chip edge where the difference is 1.5 times between the SiC and Si devices under comparable conditions. It is considered that the in-service lifetime of the SiC solder layer is only a third of the benchmark Si device [15]. This means that SiC devices are more susceptible to temperature fluctuations. Although the SiC device is suitable for higher temperatures, the power variation in the actual application scenario results in a constant junction temperature variation. Therefore, compared with the challenges of continuous high temperature, junction temperature fluctuations have a more significant impact on the life of the SiC device.

The active thermal management (ATM) technique for SiC MOSFETs is critical for lowering thermal stress shock and delaying the aging rate of power devices [16]. ATM is mainly used to control the heat produced by limiting the amplitude of junction temperature changes, such as "Peak-clipping and valley filling." Internal loss is reduced while the junction temperature is at its peak and significantly enhanced when the junction temperature is at its trough.

As high-power SiC devices become more widely utilized in the industrial sphere, their reliability issues become more significant, and relevant research is gradually carried out. In study [17], a three-level parallel converter junction temperature management technique based on reactive power regulation was proposed, which adjusted the switching loss by managing the reactive current cycle. It was only suited for parallel converter systems, and the diode's heat load increased significantly. In

TABLE I
REQUIREMENT AND REASON

Requirement	Reason
Low hardware complexity	Ensures scalability in multi-device/multi-phase systems
Thermal tunability (ΔR_G)	Allows real-time junction temperature shaping
Safe fail-state behavior	Avoids catastrophic overvoltage in case of auxiliary gate path failure
Fast modulation	Compatible with junction temperature feedback update intervals

study [18], a temperature management mechanism based on power distribution was reported to limit the converter's power and temperature. The disadvantage of this approach was that the converters must be utilized in tandem, with each converter operating at a lower frequency, lowering the power density. In study [19], a modulation approach with discontinuous pulsewidth was proposed to alter the power device's average junction temperature. However, the inverter's output quality was severely lowered. The maximum power point tracking method was proposed to reduce the thermal load on power devices [20] and to solve the frequent junction temperature variations induced by fast changes in solar inverter illumination circumstances. Currently, the standard method for junction temperature management is to change the switching loss of power devices by varying the switching frequency [21], [22], [23]. However, when the switching frequency is changed to smooth the junction temperature, the decrease in switching frequency will increase the harmonics of the system. The disadvantage is that the junction temperature of each power device cannot be controlled separately. In some applications, such as modular multilevel converters, different power devices may withstand different thermal stresses [24], which requires separate temperature control.

Unlike traditional active gate driver (AGD) studies, which focus on optimizing the following:

1) dv/dt or di/dt shaping;
2) switching loss minimization;
3) EMI suppression;
4) fault protection.

This article aims to use active gate modulation to control junction temperature variation, serving a reliability-driven function rather than switching optimization alone. To achieve this, a gate driving scheme that satisfies in Table I is needed.

Junction temperature fluctuations in power semiconductor devices can be classified into the following three categories shown in Fig. 1.

1) High-frequency fluctuations: These are induced by turn-ON and turn-OFF events within each switching cycle, with time scales in the microsecond-to-millisecond range. Such rapid dynamics require ultrafast measurement methods to capture accurately.
2) Fundamental-frequency fluctuations: In sinusoidal power converters, devices conduct only during half of the fundamental cycle, producing temperature swings that follow the line frequency, typically in the millisecond-to-second range.

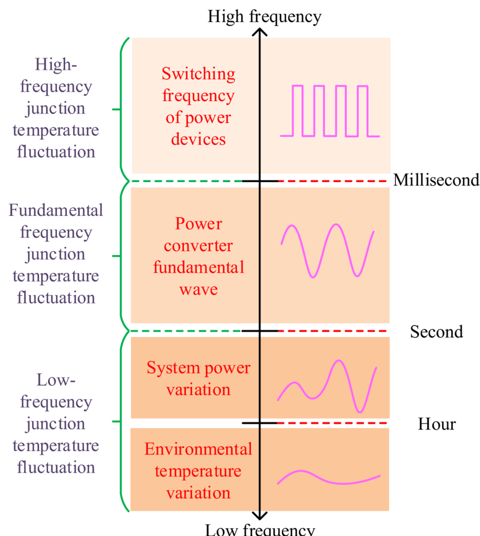

Fig. 1. Types of temperature fluctuation.

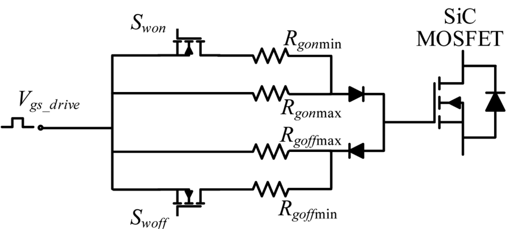

Fig. 2. Proposed EGRC method.

3) Low-frequency fluctuations: These are triggered by load and ambient variations, such as switching between light-load and heavy-load operation. Their time scale is typically in the order of seconds or longer.

The present work specifically targets low-frequency junction temperature fluctuations, which are the most critical from a reliability perspective because they drive thermo-mechanical fatigue of packaging materials. Unlike high-frequency fluctuations, these do not require cycle-by-cycle temperature detection, which significantly reduces the speed requirements on the sensing method.

Therefore, this paper proposes an equivalent gate resistance control (EGRC)-based ATM for SiC MOSFETs, as shown in Fig. 2. The gate resistance can dynamically adjust switching loss. This approach requires only two discrete resistors, a significant simplification compared to conventional multiplexer-based systems, and achieves continuous regulation through precise control of the delay time. Changing the delay time of the auxiliary switch achieves continuous drive resistance adjustment while reducing system cost.

A full-bridge inverter prototype shows the practicality and superiority of the suggested technique, which reduces temperature fluctuations. Although the literature [25] proposed a resistor-less approach that focuses on high-speed gate modulation, our method emphasizes continuous thermal regulation with low circuit complexity, making it suitable for industrial adoption. Regarding the adjustment of dynamic gate resistance, Choo and Pfost also proposed a relatively concise circuit structure [26].

TABLE II
COMPARISON WITH OTHER GATE DRIVER TYPES

Gate Driver Type	Key Features & Advantages	Limitations for Our Thermal Management Focus	Suitability for ATM
Multilevel voltage-source drivers [28]	Offers fast dv/dt control and overshoot suppression with multiple V_{GS} levels	Requires complex bias rails and controller logic	Complex
Adaptive current-source gate drivers [29]	Real-time gate current shaping for precise switching loss control	Analog feedback loop design; not temperature-feedback integrated	Not thermal-focused
Digitally controlled RG arrays [30]	Discrete tunability with digital logic or FPGA	Requires multiple MOSFETs/resistors; area and BOM cost	High cost
This work	Simple dual-resistor time-modulated gate path with low cost and feedback-friendly structure	Quasi-continuous RG control; not designed for high-speed switching shaping	☺ Yes

They explore variable gate resistance techniques to mitigate voltage overshoot and parasitic ringing during switching transitions. Therefore, they emphasize overshoot and EMI suppression, our method targets real-time, temperature-dependent adaptation of gate resistance to dynamically balance switching loss and thermal performance. Although gate resistance manipulation has been previously implemented in Si IGBTs [27], our proposed EGRC method specifically targets SiC MOSFETs that fundamentally differ from Si IGBTs in their switching characteristics, thermal stress behavior, and di/dt sensitivity. It enables continuous resistance adjustment using only two physical resistors, eliminating the need for large resistor arrays. Furthermore, this article integrate this mechanism into a real-time ATM framework and analyze its impact not only on thermal cycling but also on system efficiency and expected lifetime under dynamic power conditions.

As shown in Table II, several advanced gate driver concepts for SiC MOSFETs have been proposed in recent years, including multilevel voltage-source drivers [28], adaptive current-source gate drivers [29], and digitally controlled R_G arrays [30]. However, these techniques often emphasize switching performance, EMI suppression, or fault protection. In contrast, our EGRC approach is specifically designed for device-level thermal fluctuation regulation (ΔT_j) with minimal hardware complexity, enabling scalable real-time junction temperature shaping in a closed-loop feedback system.

The novelty of this study lies in proposing a gate-resistance–controlled active thermal management (EGRC-based ATM) strategy for SiC MOSFETs, aimed at directly addressing the challenge of junction temperature fluctuation, which is a key driver of device reliability degradation. In contrast to conventional methods such as switching-frequency modulation or adaptive gate drivers, the proposed approach enables independent, fine-grained temperature regulation at the device level while maintaining a simple and low-cost hardware structure. By integrating real-time junction temperature tracking with dynamic resistance modulation, this strategy provides a practical and effective pathway for enhancing the reliability of SiC-based power converters.

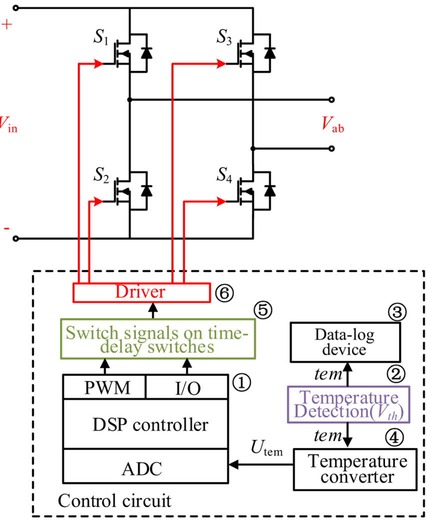

Fig. 3. System architecture.

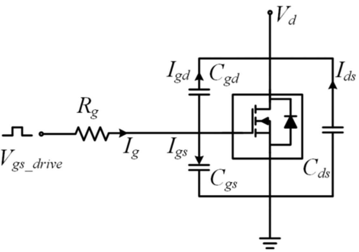

Fig. 4. Simplified model of SiC MOSFET.

This article details the system architecture and basic principle in Section II, briefly discussing the control structure in Section III. Then, the experimental prototype and experimental results are presented in Section IV. Finally, optimization of allocation rules are considered in ATM before concluding this article in Section VII.

II. Architecture and Basic Principle

A. System Architecture

The control circuit based on a full-bridge inverter is built to validate the effectiveness, as shown in Fig. 3. A temperature detection (①) collects the SiC MOSFET's temperature tem, and a data-log device (②) records the real-time temperature. Then, a temperature transmitter module (③) obtains the voltage signal U_{tem}. U_{tem} is gathered by the DSP controller (④), the auxiliary switch's delay switch signal (⑤), and the SiC MOSFET's gate drive signal (⑥) are generated after operation.

B. Mathematical Model

To exclude the influence of external factors, the gate circuit of SiC MOSFET is simplified in this article, as shown in Fig. 4. Where $V_{\text{gs_drive}}$ represents the driving voltage, R_{g} represents the driving resistance, I_{g} represents the gate driving current, C_{gd} and C_{gs} represent the parasitic capacitance of the gate–drain and the

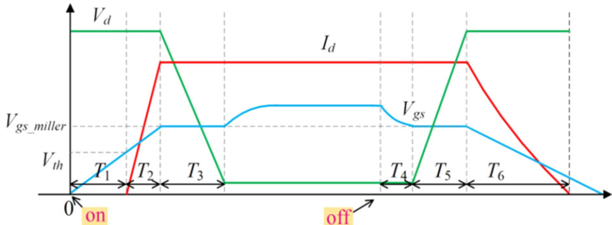

Fig. 5. Dynamic modeling of the switching process for SiC MOSFET.

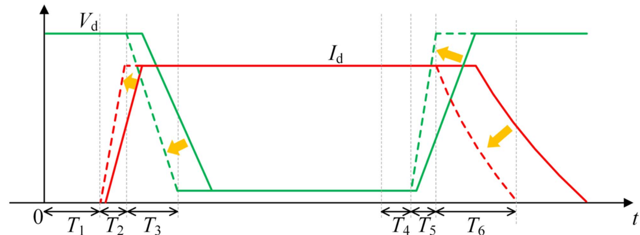

Fig. 6. Schematic diagram of adjustment.

gate–source, respectively. The current flowing through them are $I_{\rm gd}$ and $I_{\rm gs}$, and the voltage is $V_{\rm gd}$ and $V_{\rm gs}$, respectively. $V_{\rm d}$ represents the drain voltage.

Then, the six switching processes of the SiC MOSFET are dynamically modeled [4], as shown in Fig. 5

$$T_1 = (C_{\rm gs} + C_{\rm gd}) \times R_{\rm g} \times \ln\left(\frac{V_{\rm gs_drive}}{V_{\rm gs_drive} - V_{\rm th}}\right) \quad (1)$$

$$T_2 = (C_{\rm gs} + C_{\rm gd}) \times R_{\rm g} \times \ln\left(\frac{V_{\rm gs_drive}}{V_{\rm gs_drive} - V_{\rm gs_miller}}\right) \quad (2)$$

$$T_3 = \frac{Q_{\rm gd} \times R_{\rm g}}{V_{\rm gs_drive} - V_{\rm gs_miller}} \quad (3)$$

$$T_4 = (C_{\rm gd} + C_{\rm gs}) \times R_g \times \ln\left(\frac{V_{\rm gs_drive}}{V_{\rm gs_miller}}\right) \quad (4)$$

$$T_5 = \frac{Q_{\rm gd} \times R_{\rm g}}{V_{\rm gs_miller}} \quad (5)$$

$$T_6 = (C_{\rm gd} + C_{\rm gs}) \times R_g \times \ln\left(\frac{V_{\rm gs_miller}}{V_{\rm th}}\right). \quad (6)$$

Switching loss is expressed as follows:

$$\begin{aligned} E_{\rm on} &= E_{\rm on1} + E_{\rm on2} \\ &= \int_{t_1}^{t_2} V_{\rm d} \frac{I_{\rm d}}{t_2 - t_1}(t - t_1)dt + \int_{t_2}^{t_3} I_{\rm d} \frac{V_{\rm d}}{t_3 - t_2}(t - t_2)dt \\ &= \frac{I_{\rm d} V_{\rm d}(T_2 + T_3)}{2} \end{aligned} \quad (7)$$

$$\begin{aligned} E_{\rm off} &= E_{\rm off1} + E_{\rm off2} \\ &= \int_{t_5}^{t_6} I_{\rm d} \frac{V_{\rm d}}{t_6 - t_5}(t - t_5)dt + \int_{t_6}^{t_7} V_{\rm d} \frac{I_{\rm d}}{t_7 - t_6}(t - t_6)dt \\ &= \frac{I_{\rm d} V_{\rm d}(T_5 + T_6)}{2} \end{aligned} \quad (8)$$

then the switching energy consumption $E_{\rm sw}$ can be obtained

$$E_{\rm sw} = E_{\rm on} + E_{\rm off} \approx \frac{I_d V_d}{2}(T_2 + T_3 + T_5 + T_6). \quad (9)$$

The gate charge and gate current of SiC MOSFET are expressed as $Q_{\rm sw}$ and $I_{\rm g}$, respectively. Set in a minimal period, the gate current is certain, rewrite the definite integral into the form of component segment sum

$$T_2 + T_3 + T_5 + T_6 = \frac{Q_{\rm sw2}}{I_{g2}} + \frac{Q_{\rm sw3}}{I_{g3}} + \frac{Q_{\rm sw5}}{I_{g5}} + \frac{Q_{\rm sw6}}{I_{g6}} \quad (10)$$

where $Q_{\rm sw2}$, $Q_{\rm sw3}$, $Q_{\rm sw5}$ and $Q_{\rm sw6}$ respectively represent the gate charges of T_2, T_3, T_5 and T_6. $I_{\rm g2}$, $I_{\rm g3}$, $I_{\rm g5,}$ and $I_{\rm g6,}$ respectively, represent the gate current of the four stages, then

$$E_{\rm sw} \approx \frac{I_d V_d}{2}\left(\frac{Q_{\rm sw2}}{I_{g2}} + \frac{Q_{\rm sw3}}{I_{g3}} + \frac{Q_{\rm sw5}}{I_{g5}} + \frac{Q_{\rm sw6}}{I_{g6}}\right). \quad (11)$$

The $E_{\rm sw}$ is inversely correlated with the gate current $I_{\rm g}$ and

$$I_g = \frac{V_{\rm gs_drive} - V_{\rm gs}}{R_g}. \quad (12)$$

Since excessively high gate-drive voltage may exceed the device ratings, this work regulates the gate current $I_{\rm g}$ by adjusting the external gate resistance $R_{\rm g}$, thereby controlling the switching time and ultimately the switching energy $E_{\rm sw}$, as shown in Fig. 6.

Furthermore, the switching loss $P_{\rm sw}$ of the SiC MOSFET can be expressed as follows:

$$\begin{aligned} P_{\rm sw} &= f_{\rm sw} k_{\rm I} k_{\rm U} E_{\rm sw} = \frac{f_{\rm sw} I_{\rm d} V_{\rm d}}{I_{\rm ref} V_{\rm ref}} E_{\rm sw} \\ &= \frac{f_{\rm sw} {I_{\rm d}}^2 {V^2}_{\rm d}}{2 I_{\rm ref} V_{\rm ref}}(T_2 + T_3 + T_5 + T_6) \end{aligned} \quad (13)$$

where $f_{\rm sw}$ is the switching frequency, $k_{\rm I}$ and $k_{\rm U}$ are the conversion coefficients of voltage and current, respectively, $I_{\rm d}$ is the current when the SiC MOSFET is fully turned ON, $V_{\rm d}$ is the voltage when the SiC MOSFET is completely turned OFF, and $I_{\rm ref}$ and $V_{\rm ref}$ are the reference values, which can be obtained through the datasheet.

Through (2), (3), (5), and (6), $T_{\rm i}$ can be regarded as a function $f(R_{\rm g})$ of $R_{\rm g}$, which can be obtained

$$\begin{cases} P_{\rm sw} = \frac{f_{\rm sw} {I_{\rm d}}^2 {V^2}_{\rm d}}{2 I_{\rm ref} V_{\rm ref}} f(R_{\rm g}) = P_{\rm sw}(R_{\rm g}) \\ f(R_{\rm g}) = \Big[(C_{\rm gs} + C_{\rm gd}) \ln\left(\frac{V_{\rm gs_drive}}{V_{\rm gs_drive} - V_{\rm gs_miller}}\right) + \frac{Q_{\rm gd}}{V_{\rm gs_drive} - V_{\rm gs_miller}} \\ \quad + \frac{Q_{\rm gd}}{V_{\rm gs_miller}} + (C_{\rm gd} + C_{\rm gs}) \ln\left(\frac{V_{\rm gs_miller}}{V_{\rm th}}\right)\Big] R_{\rm g} \end{cases} \quad (14)$$

therefore

$$\begin{cases} tem_{\rm j_sw}(R_g) = P_{\rm sw}(R_g) \cdot \theta_{\rm jc} \\ \Delta tem_{\rm j_sw}(R_g) = [P_{\rm sw}(R_{g1}) - P_{\rm sw}(R_{g2})] \cdot \theta_{\rm jc} \end{cases} \quad (15)$$

where $\mathrm{tem}_{\rm j_sw}(R_{\rm g})$ is the junction temperature corresponding to the switching loss part under the driving resistance $R_{\rm g}$,

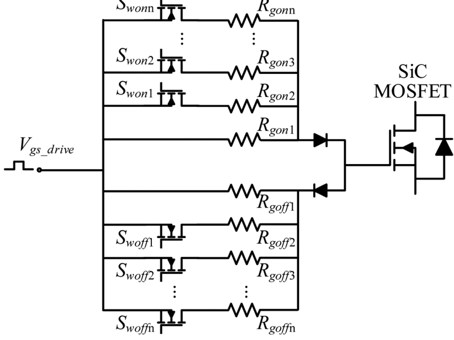

Fig. 7. Conventional method.

$\Delta\text{tem}_{\text{j_sw}}(R_g)$ is the adjustment change of junction temperature when the driving resistance changes from R_{g1} and R_{g2}, and θ_{jc} is the thermal resistance between junction and case. In combination with (14) and (15), the range of temperature regulation $\Delta\text{tem}_{\text{j_sw}}(R_g)$that can be realized by changing R_{g} under different load I_{d} can be calculated, which will be verified explicitly in Section IV.

III. ATM Method Based on EGRC

A. Basic Principles

In this article, junction temperature fluctuation refers to the cyclic variation of T_j between peak and valley values during repetitive power cycling. These fluctuations are driven by power variations, such as when the converter alternates between heavy-load and light-load conditions. Although this may appear as a shift around a medium-load equilibrium, it fundamentally represents cyclic thermal fluctuations. This is distinct from a one-time temperature excursion or random thermal drift. The proposed EGRC-based ATM specifically targets the suppression of such cyclic temperature fluctuations, thereby mitigating thermomechanical stress and improving device lifetime.

As seen above, the junction temperature may be varied by altering the gate resistance. This method simply adjusts resistors quantitatively. For example, in Fig. 7, six auxiliary switches and six driving resistors are required to cover all resistance values within the range of these six resistors [26]. This approach requires more devices and has poor continuous online regulating capacity. As a result, this work presents the delay switch concept, as seen in Fig. 1. Reducing drive resistance increases drive current, modifying the rise or fall time of current and voltage, and reducing SiC MOSFET switching loss. The proposed EGRC scheme offers several advantages over conventional multiresistor gate control approaches. By employing only two resistors and modulating the effective resistance through time-domain delay control, it achieves quasi-continuous adjustment with analog-like resolution. This design significantly simplifies circuitry, reduces cost and PCB complexity, and enhances real-time responsiveness to thermal dynamics. Moreover, it inherently supports fault tolerance—defaulting to safe resistance states under switch failures—making it a robust and scalable solution for industrial thermal management applications. The SiC MOSFET's turn-ON stage is depicted in Fig. 8(a). The solid yellow line represents

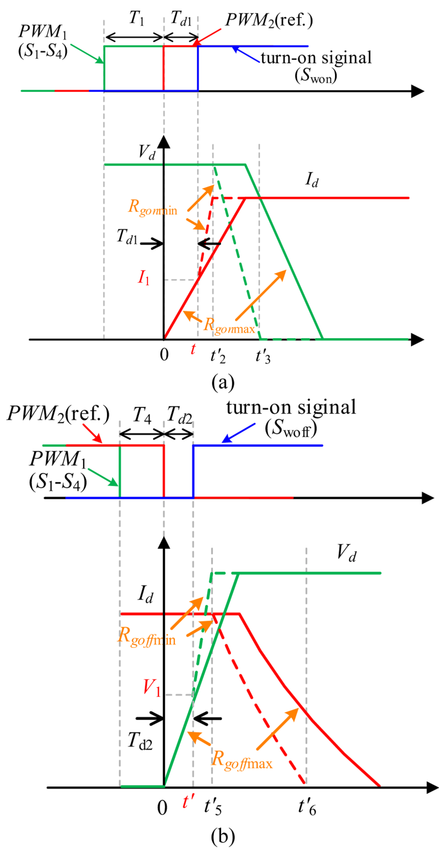

Fig. 8. Schematic diagram of voltage and current after using EGRC.

the SiC MOSFET turn-ON signal PWM_1. The solid red line is the reference signal PWM_2, lagging behind PWM1, and the lag time is T_1. Use PWM_2 as the benchmark, the driving signal of the auxiliary switch S_{won} will turn to a high level after the delay time T_{d1}, S_{won} will turn ON, and the gate resistance will change. The switching point of the turn-ON track can be regulated by altering T_{d1}, realizing the corresponding adjustment of the gate resistance in the turn-ON stage at this moment when the current and voltage waveform of the SiC MOSFET changes from a solid line to a dashed line. The SiC MOSFET's turn-OFF stage is depicted in Fig. 8(b), and it operates on the same principles as the turn-ON stage. The auxiliary switch S_{woff} is switched ON based on the reference signal. Following the delay period T_{d2}, the gate resistance can be modified. The switching point of the turn-off track can be regulated by altering T_{d2}, realizing the corresponding adjustment of the gate resistance in the turn-off stage at this moment when the current and voltage waveform of the SiC MOSFET changes from a solid line to a dashed line. In this article, R_{gmax} is set to 30 Ω and R_{gmin} to 6 Ω. The equivalent driving resistance of the auxiliary switch before closure is 30 Ω, and the equivalent driving resistance after closure is 5 Ω. Adjusting the delay time allows the equivalent adjustment of the drive resistance between 5 and 30 Ω. Another advantage of this method is that when the auxiliary switch fails, the equivalent drive resistance is 5 Ω when the short circuit occurs. The equivalent drive resistance is 30 Ω when the circuit is broken, which will not destroy the regular operation of the primary circuit.

It needs to be clarified that the goal of our gate driver is to enable dynamic, real-time adjustment of switching behavior based on temperature feedback, not to provide a metrologically precise resistance value. This makes it well-suited for active thermal management in practical converters. Therefore, the EGRC-based gate driver is not intended as a replacement for precision gate drivers used in DPT. It should be noted that the EGRC-based ATM strategy primarily targets the switching loss component of total device losses. Conduction loss and diode conduction loss are mainly determined by device parameters and load conditions, making them difficult to manipulate dynamically during operation. In contrast, switching loss is highly sensitive to gate resistance and thus can be adjusted in real time through the gate driver. Although switching loss contributes only a portion of total loss, it plays a dominant role in driving dynamic junction temperature swings during load transients. Similar conclusions have been reported in recent literature, where switching-loss-oriented modulation is adopted as the main lever for active thermal management in SiC MOSFETs [31], [32], [33].

As shown in Fig. 8(a), re-establish the relationship between $E_{\rm on}$ and $T_{\rm d1}$

$$E_{\rm on}\left(T_{d1}\right) = \int_0^t V_d \frac{I_d}{T_2} t dt + \int_{t_1{'}}^{t_2{'}} V_d I_d dt - \frac{V_d}{2} \cdot I_1 \cdot T' + \frac{V_d I_d T_3'}{2}$$
$$= \frac{V_d I_d}{2{T_2}^2}\left(T_2 - T_2'\right) T_{d1}^2 + \frac{V_d I_d}{2}\left(T_2' + T_3'\right). \quad (16)$$

Then derivation

$$E_{\rm on}{'}\left(T_{d1}\right) = \frac{V_d I_d \left(T_2 - T_2'\right) T_{d1}}{{T_2}^2}. \quad (17)$$

And because of

$$\begin{cases} T_2 = \left(C_{\rm gs} + C_{\rm gd}\right) \times R_{g\max} \times \ln\left(\frac{V_{\rm gs_drive}}{V_{\rm gs_drive} - V_{\rm gs_miller}}\right) \\ T_2{'} = \left(C_{\rm gs} + C_{\rm gd}\right) \times R_{g\min} \times \ln\left(\frac{V_{\rm gs_drive}}{V_{\rm gs_drive} - V_{\rm gs_miller}}\right) \end{cases} \quad (18)$$

where $R_{\rm gmax} > R_{\rm gmin}$, therefore T_2-$T_2{'}$>0, means the turn-ON loss $E_{\rm on}$ is a monotone increment function with respect to $T_{\rm d1}$. The analysis of the turn-OFF stage is consistent with the turn-ON process, as shown in Fig. 8(b)

$$E_{\rm off}\left(T_{d2}\right) = \int_0^{t'} I_d \frac{V_d}{T_5} t dt + \int_{t_4{'}}^{t_5{'}} V_d I_d dt - \frac{I_d}{2} \cdot V_1 \cdot t' + \frac{V_d I_d T_6'}{2}$$
$$= \frac{V_d I_d}{2{T_5}^2}\left(T_5 - T_5'\right) T_{d2}^2 + \frac{V_d I_d}{2}\left(T_5' + T_6'\right). \quad (19)$$

Then derivation

$$E_{\rm off}{'}\left(T_{d2}\right) = \frac{V_d I_d \left(T_5 - T_5'\right) T_{d2}}{{T_5}^2}. \quad (20)$$

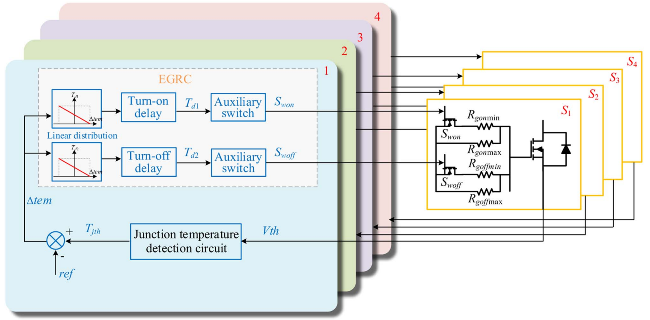

Fig. 9. Control block diagram.

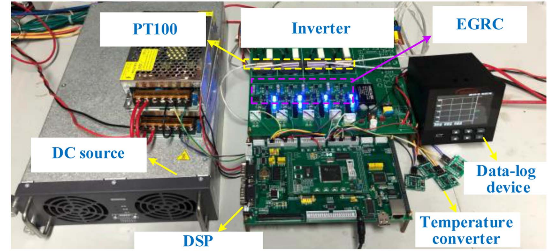

Fig. 10. Experiment platform.

And because of

$$\begin{cases} T_5 = \frac{Q_{\rm gd} \times R_{g\max}}{V_{\rm gs_miller}} \\ T_5{'} = \frac{Q_{\rm gd} \times R_{g\min}}{V_{\rm gs_miller}} \end{cases}. \quad (21)$$

$R_{\rm gmax} > R_{\rm gmin}$, therefore T_5-$T_5{'}$>0, means the turn-OFF loss $E_{\rm off}$ is a monotone increment function with respect to $T_{\rm d2}$. In conclusion, the junction temperature of SiC MOSFET can be controlled by the delay time $T_{\rm d}$.

B. Description of Control Strategy

Fig. 9 depicts the design of the ATC control system based on the EGRC suggested in this article. Because the full-bridge inverter architecture was chosen as the study object, the system includes four SiC MOSFETs (S_1, S_2, S_3, S_4). An online junction temperature detection circuit is used this paper. After comparing the reference temperature, the delay time $T_{\rm d}$ is calculated using linear distribution and amplitude limiting processing. The delay switch signals $S_{\rm won}$ and $S_{\rm woff}$ of the auxiliary switch in the EGRC circuit are obtained, and the drive resistance is equivalently regulated in real time.

IV. Experimental Verification

A. Experimental Prototype

As shown in Fig. 10, an experimental platform is developed to verify the feasibility and effectiveness of the proposed strategy. It primarily consists of a SiC MOSFET-based full-bridge inverter, a dc source, a rectifier bridge, and an electronic load. The dashed line frame is the designed EGRC, the SiC MOSFET used in this article is IXFN50N120SIC, and the auxiliary switch is BSC052N03LS. The driver chip of the primary power device (S_1–S_4) is ISO5852s, and the driver chip of the auxiliary

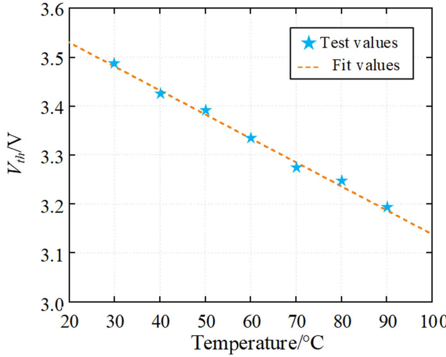

Fig. 11. Threshold voltage acquisition and fitting results.

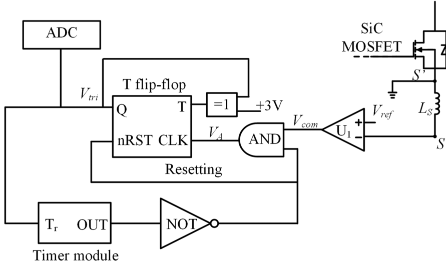

Fig. 12. Proposed online threshold voltage detection circuit based on a T flip-flop.

switch is IXDD604SI. The load is a programmable electronic load with the model CHROMA_63200A. To emulate power fluctuation under non-stationary conditions, the electronic load is programmed to change the system's power by switching different loads. In inverter mode, the variation of load current was realized by programming the electronic load to change its effective resistance. The current values reported in this paper are RMS values, unless otherwise specified. The actual load current was continuously monitored through the load resistance of the electronic load and used to represent the imposed power fluctuation conditions during testing.

In this work, the junction temperature estimation is based on a temperature-sensitive electrical parameter method, where the threshold voltage Vth of the SiC MOSFET is selected as the sensing parameter. As reported in study [34], a nearly linear relationship exists between $V_{\rm th}$ and the junction temperature $T_{\rm j}$, expressed as $V_{\rm th} = 3.6281 - 0.0049\,T_{\rm j}$.

With a sensitivity of approximately −5 mV/°C, as shown in Fig. 11. This correlation was experimentally validated using a heating platform, and importantly, it shows little dependence on the load current, making Vth particularly suitable for online junction temperature monitoring.

Furthermore, Ruoyin and Xiaoyong [34] proposed a practical detection circuit using Kelvin-source connections and a T-triggered measurement approach to minimize the influence of parasitic inductances, thereby enabling accurate capture of $V_{\rm th}$ during switching intervals, as shown in Fig. 12. Their experimental validation on a SiC inverter platform demonstrated that the measurement error can be maintained within 3 °C, confirming the feasibility of online $T_{\rm j}$ detection via $V_{\rm th}$ (shown in Fig. 13).

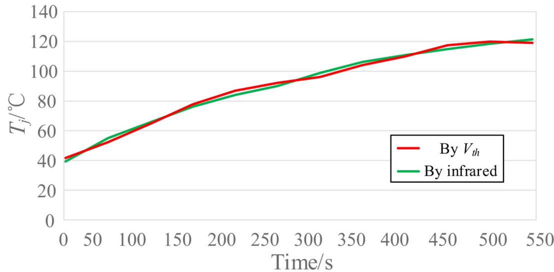

Fig. 13. Comparison of test results of T_j.

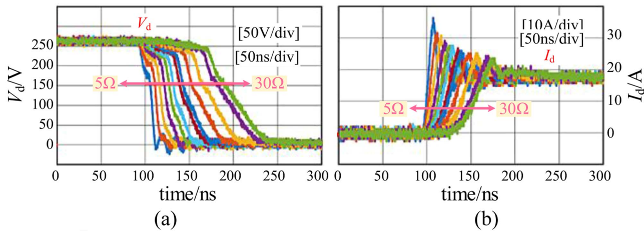

Fig. 14. (a) Voltage waveform. (b) Current waveform at the turn-ON stage.

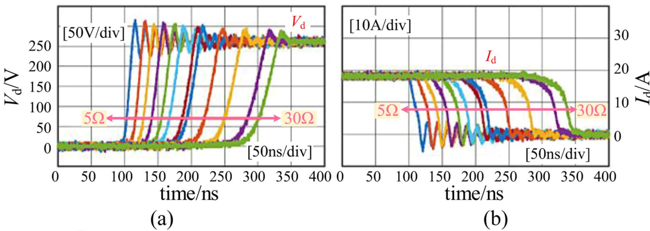

Fig. 15. (a) Voltage waveform. (b) Current waveform at the turn-OFF stage.

It is also noted in study [34] that long-term drift of $V_{\rm th}$, caused by mechanisms such as bias temperature instability and oxide trap charging, may introduce measurement deviations. Compensation strategies were suggested to recalibrate the detection circuit during maintenance or downtime. In our work, such drift effects are acknowledged and will be addressed in future studies to further improve the robustness of the proposed EGRC-based active thermal management.

B. Validation of EGRC

This article tests the turn-ON and OFF waveform of SiC MOSFETs under various driving resistances before verifying EGRC. The system's input dc voltage is set to 250 V. Fig. 14(a) and (b) present the voltage and current waveforms at the turn-ON stage.

Fig. 15(a) and (b) present the voltage and current waveforms at the turn-OFF stage. The larger the drive resistance at the turn-ON stage, the longer the rise time of $I_{\rm d}$ and the longer the drop time of $V_{\rm d}$, implying a higher switching loss. The stronger the drive resistance, the longer the rise time of $V_{\rm d}$ and the longer the decline time of $I_{\rm d}$ during the turn-OFF stage, which also means the more significant the switching loss. On the other hand, the lower the driving resistance, the lower the switching loss.

If the auxiliary switch's conducting time is too short, the auxiliary switch may have been turned OFF before the main switch's

TABLE III
SWITCHING LOSSES AND OVERSHOOT CHARACTERISTICS

R_G	E_{on} (mJ)	E_{off} (mJ)	I_D Overshoot (A)	V_D Overshoot (V)
5 Ω	2.2	1.8	59 (+12%)	280 (+12%)
10 Ω	2.6	2.2	56 (10%)	270 (+8%)
20 Ω	3.4	2.8	54 (6%)	260 (+4%)
30 Ω	4.2	3.5	52 (+2%)	255 (+2%)

turn-ON (or turn-OFF) stage is complete. The only remedy that can be offered is that the auxiliary switch's conducting duration should equal the main switch's longest turn-ON (or turn-OFF) period. After testing, SiC MOSFET with 30 Ω gate resistance has the longest turn-ON and turn-OFF time, which are 158 and 115 ns, respectively. In conclusion, the conducting time of the auxiliary switch in this study is fixed at 200 ns, which completely covers the SiC MOSFET's turn-ON or turn-OFF stage and prevents the auxiliary switch from being turned OFF too soon. Therefore, the EGRC method proposed in this work dynamically adjusts R_g within a predefined range (5 to 30 Ω). Within this range, even if an overshoot occurs, it is still within the rated value of the device. This range was chosen to ensure that the device operates safely within its rated limits while achieving effective thermal management. The relevant test results are shown in Figs. 14 and 15. Therefore, for the selection range of the gate resistance, we have actually made the selection after thorough consideration.

The voltage and current waveforms are shown in Fig. 16. Then, the auxiliary switches are tested under various $T_{\rm d}$. The ability of the auxiliary switch to vary the turn-ON and turn-OFF trajectories with different delay times is demonstrated. The PWM_2 is used as the reference signal when the SiC MOSFET is in the turn-ON stage [see Fig. 16(a)]. Following the delay $T_{\rm d2}$, the auxiliary switch's access causes $V_{\rm d}$ to climb rapidly, changing the trajectory of turn-ON voltage and current. For turn-OFF stage [see Fig. 16(b)], the auxiliary switch's access causes the $I_{\rm d}$ to rise rapidly after the delay $T_{\rm d1}$, changing the trajectory of the turn-OFF waveform. The voltage and current curves differ depending on the $T_{\rm d}$. As a result, the waveforms can be equivalently adjusted.

To further illustrate the trade-OFF between switching performance and device stress, Table III summarizes the measured switching losses and overshoot characteristics of the IXFN50N120SIC from Fig. 16 under different gate resistance values. The results show that increasing $R_{\rm g}$ suppresses current and voltage overshoots but at the expense of higher switching losses, confirming the effectiveness of EGRC in providing a tunable balance between efficiency and reliability.

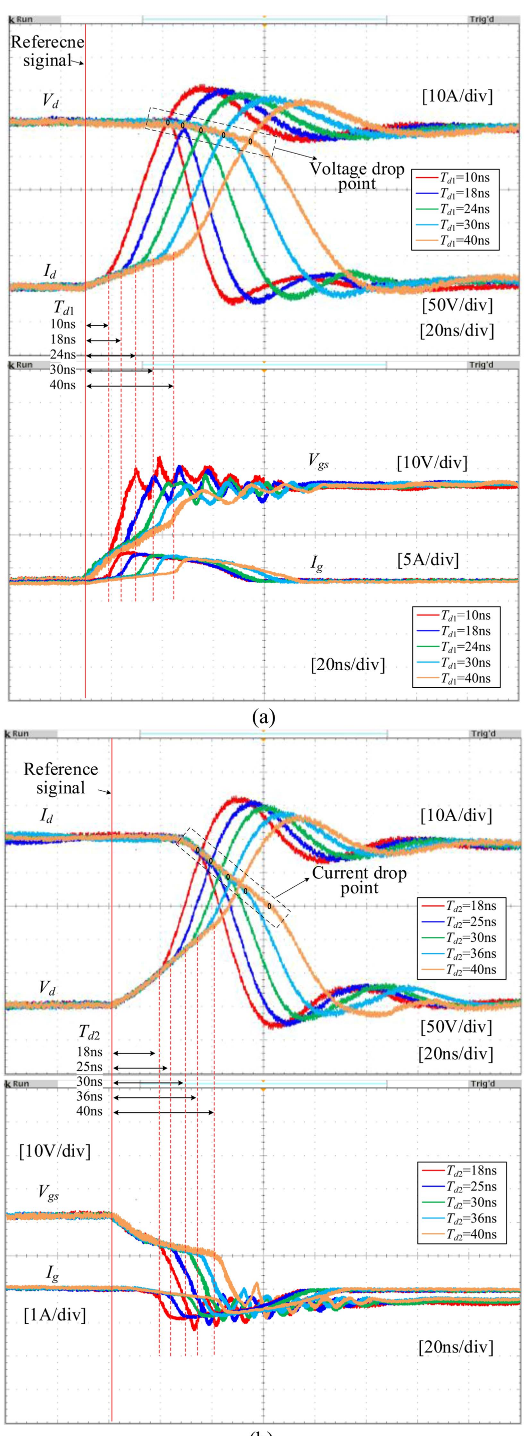

Fig. 16. Voltage and current waveforms at (a) turn-ON and (b) turn-OFF stages.

C. Verify ATM Method Based on EGRC

Before the experiment, planning and allocating the delay time $T_{\rm d}$ before the auxiliary switch is turned on is necessary. The basic principle is that when the junction temperature is higher than the reference temperature, $T_{\rm d}$ decreases with the increase of Δtem to reduce losses. When the junction temperature is lower than the reference temperature, $T_{\rm d}$ increases with the negative increase of Δtem to increase the loss. The maximum switching time of SiC MOSFET occurs at the maximum system current and maximum gate resistance. In contrast, the minimum value occurs near the minimum system current and minimum gate resistance. According to the rated current of SiC MOSFET, the effective operating range is set to 5–35 A. After testing, the turn-ON time of SiC MOSFET is about 158 ns, and the turn-OFF time is about 115 ns when the gate driving resistance value is 30 Ω and the junction temperature is 47 °C. When the gate driving resistance

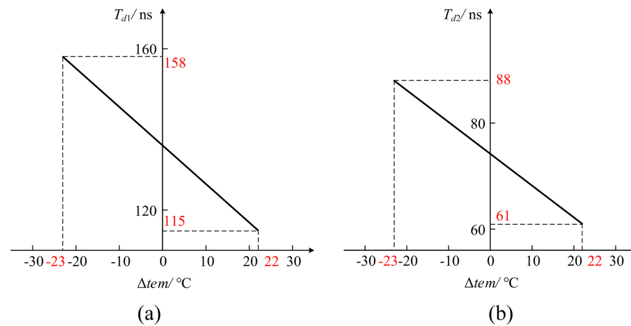

Fig. 17. Delay time allocation rule of the auxiliary switch. (a) T_{d1}. (b) T_{d2}.

TABLE IV
PARAMETERS OF INVERTER

Parameters	Value
V_{in}	250 V
f_{w}	20 kHz
tem_{a}	28°C
R_{gmin}	6 Ω
R_{gmax}	30 Ω

value is 5 Ω, the turn-ON time is about 88 ns, the turn-OFF time is about 61 ns, and the junction temperature is 92 °C. Using the junction temperature (70 °C) at 20 A as the reference temperature, subtract it from the real-time junction temperature to obtain Δtem. The reference temperature is generally set to the junction temperature of the SiC MOSFET when the high-frequency inverter operates at half load. Based on the rated current of the selected SiC MOSFET, the reference temperature in the experiment is set to the junction temperature corresponding to 20 A (tested to be 70 °C). When the junction temperature exceeds 70 °C, switching losses are reduced; conversely, switching losses are increased. In summary, the allocation rules for the delay time T_{d1} of S_{won} and the delay time T_{d2} of S_{woff} are shown in Fig. 17(a) and (b), respectively. Furthermore, the functional expressions for the delay time and temperature difference allocation rules can be obtained as follows:

$$T_{d1} = -0.96\Delta\text{tem} + 136.12 \tag{22}$$

$$T_{d2} = -0.6\Delta\text{tem} + 74.2. \tag{23}$$

The load is adjusted using a programmable electronic load to emulate power fluctuations. Table IV lists the system parameters. The power fluctuation is defined as 30, 25, 17, 30, 20, 17, 25 A.

The EGRC-based ATM method is tested in this article, and the experimental results are shown in Fig. 18. The red line is the result without any control strategy. As shown in Fig. 18, the maximum fluctuation reached 18.83 K without any control. The blue line shows that the ATM method significantly reduces the temperature fluctuation range, and the maximum fluctuation is reduced to 9.85 K. The adjustment range of junction temperature by adjusting switching loss under different current I_{d} is different. It should be noted that the junction temperature and current waveforms shown in Fig. 18 were recorded after the system had reached thermal steady-state, following repeated execution of the power fluctuation sequence. The baseline device temperature at time zero is therefore higher than room temperature, corresponding to the stabilized thermal operating point. The maximum junction temperature fluctuation amplitude is consistent both at startup and after many cycles, since it is determined by dynamic load variation and EGRC regulation rather than the absolute starting temperature. The device was mounted on an aluminum heatsink with forced-air cooling using a silicone-based thermal interface material (2.5 W/m·K). The estimated thermal resistances are R_{jc}≈0.29 K/W, R_{ch}≈0.15 K/W, and Rha≈0.6K/W, resulting in an overall junction-to-ambient thermal resistance of ∼1.0 K/W. The thermal capacitance of the heatsink was approximately 120 J/K, which explains the relatively slow junction temperature evolution compared with electrical transients.

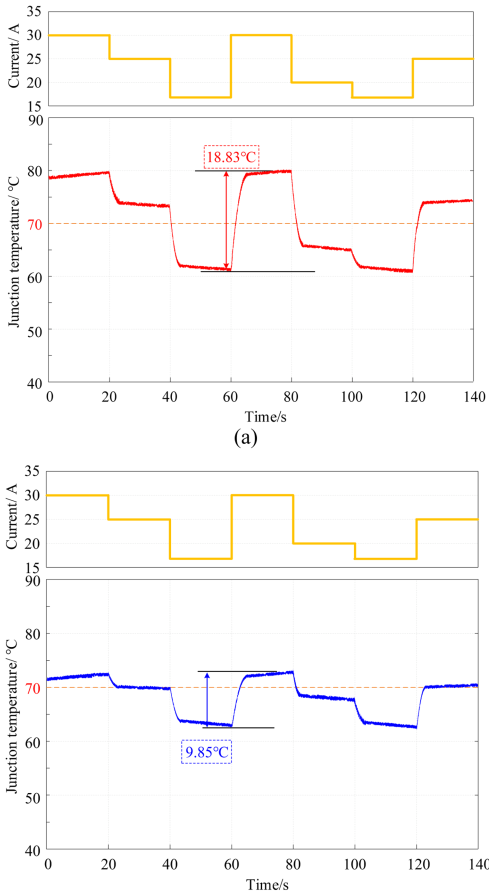

Fig. 18. Experimental results. (a) Uncontrolled. (b) EGRC-based ATM.

Finally, since this method reduces the junction temperature fluctuation of SiC MOSFET by changing switching loss, the calculation expression of the relationship between the driving resistance and the temperature adjustment range is given in Section II. The SiC MOSFET selected in this article is IXFN50N120SIC, and the relevant parameters can be obtained from the Datasheet, as shown in Table V. Finally, the calculated value of the temperature regulation range is obtained through (14) and (15), as shown in Fig. 19, to obtain the regulation range that can be realized by changing R_{g} under different load I_{d}.

TABLE V
KEY PARAMETERS

Parameters	Value
C_{iss}	1900 pF
C_{oss}	160 pF
C_{rss}	13 pF
C_{gd}	13 pF
C_{gs}	1890 pF
C_{ds}	147 pF
Q_{gd}	36 nC
V_{gs_drive}	20 V/-5 V
V_{th}	2.6 V
f_{sw}	85 kHz
I_{ref}	40 A
V_{ref}	400 V
V_d	250 V
g_{fs}	18

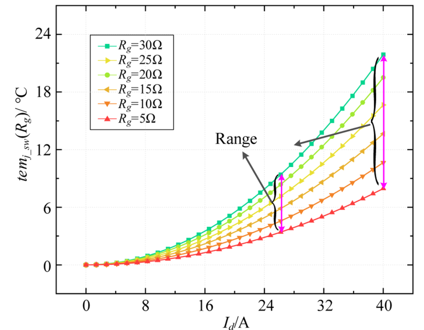

Fig. 19. Adjustable junction temperature range.

D. Life Assessment

A life assessment mechanism is introduced to better characterize the proposed method's effectiveness in improving SiC MOSFET's reliability. The complete life assessment process is as follows:

Step 1. Calculate the complete cycle of temperature loads: Establishing the life assessment model requires statistical analysis and extraction of temperature cycle loads based on the junction temperature curve of SiC MOSFETs [35], [36]. The commonly used methods for calculating fatigue life loads include peak counting, traversal analysis, and rain flow counting [37]. Among them, the basic principle of the rain flow counting method conforms to the fatigue damage law of materials and is widely used. The rain flow counting method simplifies the process of the device bearing temperature cyclic loads into the complete cycle and half cycle. It comprehensively considers the relationship between the mean temperature cyclic load, load amplitude, and frequency of occurrence in the thermal fatigue load cycle. This article uses the rain flow counting method to traverse all total cycle temperature fluctuations Δtem_{ji} in the junction temperature curve of SiC MOSFET and its frequency of occurrence n_i. As the rain flow counting method is a mature technology, the extraction process will not be elaborated further.

Step 2. Establish the lifetime model: The number of cycles N_f usually characterizes the lifetime of power semiconductor devices before failure, mainly divided into physical and mathematical models. Among them, the mathematical method is a lifetime model obtained through mathematical fitting using aging experimental test data, which is easy to implement. Therefore, the Coffin-Manson model [38] is chosen for the lifetime evaluation of SiC MOSFETs, as shown in (24). In our reliability tests, the observed failure mechanisms were packaging-related, mainly bond-wire fatigue and solder joint cracking, rather than intrinsic chip-level degradation. These thermo-mechanical failures are directly driven by junction temperature swings, making the Coffin–Manson model particularly suitable for lifetime estimation in this context. And The heating process during power cycling was realized by applying a controlled dc current to the device under test, producing self-heating due to conduction and switching losses. The devices then cooled naturally through the thermal path (junction–case–heatsink–ambient), ensuring that the stress conditions were representative of realistic converter operation. The use of the Coffin-Manson model in our study primarily serves as a relative lifetime indicator rather than an absolute prediction, especially when Δtem_j drops into the elastic regime [39]

$$N_f = a \cdot (\Delta\text{tem}_j)^b \tag{24}$$

where a and b represent the fitting coefficients, which need to be obtained through a power cycling experiment. Unlike TDDB, BTI, HTRB, or HTGB tests, which evaluate intrinsic device-level degradation under static bias stress, the Coffin–Manson model specifically captures thermo-mechanical fatigue caused by repeated junction temperature swings, and is thus more relevant for assessing the effectiveness of active thermal management. The SiC MOSFET model selected in this article is IXFN50N120SiC, and the manufacturer has provided the power cycle test result. When Δtem_j is 40K, the failure cycle of SiC MOSFET is about 34 6421 times, and when Δtem_j is 120K, the failure cycle is about 106 867. Put these two sets of data into (36) to obtain $a\approx 17972611$ and $b\approx 1.070501$ in the Coffin Manson model, as shown in (25). Meanwhile, the lifetime model is demonstrated by the orange line in Fig. 20

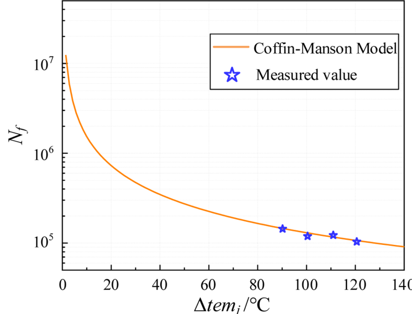

Fig. 20. Validation of the Coffin–Manson lifetime model.

$$N_f = 17\,972\,611 \cdot (\Delta\text{tem}_j)^{-1.070501}. \tag{25}$$

The SiC MOSFET is continuously heated and cooled in the experiment by changing system power. During the heating process, the fan is stopped to accelerate the heating, and during the cooling process, the fan is turned on to accelerate the cooling. The cycle continued until the SiC MOSFET failed. Complete four

TABLE VI
RESULT OF LIFETIME CALCULATION

	Uncontrolled		EGRC-based ATM	
Δtem_j	12.18 K	18.69 K	6.06 K	9.11 K
n_i	1	1	1	1
N_{fi}	1.2×10^6	7.8×10^5	2.6×10^6	1.7×10^6
D	2.1×10^{-6}		9.7×10^{-7}	
Life prediction	18383/h		40091/h	

sets of testing experiments, with junction temperature fluctuations Δtem_j of 90, 100, 110, and 120 K, respectively. After conducting power cycle aging tests. The number of failure cycles is shown by the star in Fig. 20, which verifies the correctness of the Coffin-Manson model. The yellow line denotes the predicted failure cycles calculated from the Coffin–Manson relation, while the pentagram markers indicate the experimentally measured failure cycles from temperature cycling tests. The good agreement between model and experiment demonstrates the accuracy of the adopted lifetime model for reliability assessment.

Step 3. Calculate the lifetime: By substituting the complete cycle temperature fluctuation Δtem_{ji} in Step 1 into the Coffin-Manson model established by (25), the number of cycles N_{fi} of SiC MOSFETs under each temperature load condition can be obtained. Then, life consumption is calculated using the damage accumulation theory. In this article, the Miner linear damage accumulation theory is used [28], and the mathematical expression is

$$D = \sum_{i=1}^{m} \frac{n_i}{N_{fi}} \tag{26}$$

where D is the accumulated damage degree, and the failure of SiC MOSFET is determined when $D = 1$, m is the number of thermal cycles that SiC MOSFET is subjected to. Finally, the lifetime can be evaluated using the steps above based on the temperature load curve shown in Fig. 20. The time scale is 140 s. The expected life L is obtained based on the cumulative degree of damage D, and the calculation process is shown in (27). The results are shown in Table VI. The ATM method proposed in this article has increased the expected lifetime of SiC MOSFETs by 218% compared to the technique without any thermal management strategy, confirming the proposed method's effectiveness. It should be emphasized that the lifetime predictions and comparisons in this study represent relative values rather than precise lifetime calculations. It should be noted that the accelerated tests do not directly replicate field operation but rather emulate equivalent thermal stress conditions, enabling estimation of lifetime according to the adopted model

$$L = \frac{140}{D}\,(\text{second}) = \frac{140/3600}{\sum_{i=1}^{m} \frac{n_i}{N_i}}\,(\text{hour})\,. \tag{27}$$

The lifetime prediction procedure adopted in this work follows the standard methodology commonly applied in semiconductor reliability studies. First, the complete junction temperature history obtained under power fluctuation conditions is analyzed using the rainflow counting algorithm, which decomposes the temperature sequence into equivalent thermal cycles of different amplitudes. Second, for each identified cycle, the Coffin–Manson model is used to establish the relationship between the junction temperature swing (ΔT_j) and the number of cycles to failure (N_f). Finally, the overall device lifetime is estimated by applying Miner's linear damage accumulation theory, which sums the damage contributions of individual cycles to determine the equivalent failure time under the applied load profile. This stepwise procedure is not limited to a particular operating condition but is applicable to arbitrary power variation scenarios, provided the junction temperature sequence is available. In this paper, the predicted lifetime is presented in terms of equivalent operating hours, which are obtained by multiplying the cycle-based estimation with the average period of the applied power fluctuation profile. This ensures that the lifetime results serve as a consistent and quantitative indicator of the effectiveness of the proposed EGRC-based active thermal management strategy.

E. Practical Considerations in Half-Bridge Operation

In half-bridge configurations, the EGRC-based ATM may lead to different switching speeds between the high-side and low-side MOSFETs due to variable gate resistance. In our implementation, however, the adjustment range of R_g (5–30 Ω) is carefully constrained within the safe switching envelope specified by the device datasheet. This ensures that the turn-ON and turn-OFF transitions remain safe and do not result in excessive overlap current. Furthermore, conventional dead-time control at the driver level inherently prevents cross-conduction (shoot-through), even if asymmetric switching occurs. Our double-pulse tests have verified that no abnormal overlap current or short-circuit event occurs under EGRC regulation. It is also important to emphasize that the EGRC-based ATM is designed for thermal management during normal converter operation. In the rare case of a short-circuit fault caused by load disturbance or gate driver malfunction, the junction temperature evolution is dominated by large fault currents within microseconds, which is beyond the regulation capability of EGRC. Under such fault conditions, conventional protection mechanisms, such as DESAT detection and soft turn-OFF, remain indispensable. Therefore, the proposed EGRC strategy should be considered as complementary to existing short-circuit protection schemes: EGRC reduces ΔT_j and extends device lifetime during normal operation, while dedicated protection ensures safety under abnormal conditions.

In this work, the experimental validation was carried out at a dc link voltage of 250 V, which was selected to ensure safe laboratory operation and facilitate repeated thermal cycling within the constraints of the available test platform. It should be emphasized that the effectiveness of the proposed EGRC-based ATM strategy is not dependent on the absolute bus voltage, but rather on the modulation of switching losses through gate resistance control. At higher dc link voltages (e.g., 400 or 800 V), the switching energy per event increases proportionally; however, the same principle of quasi-continuous resistance adjustment remains valid. In such cases, the effective R_g range may need to be adjusted within datasheet limits to ensure safe dv/dt and overvoltage margins. The present results

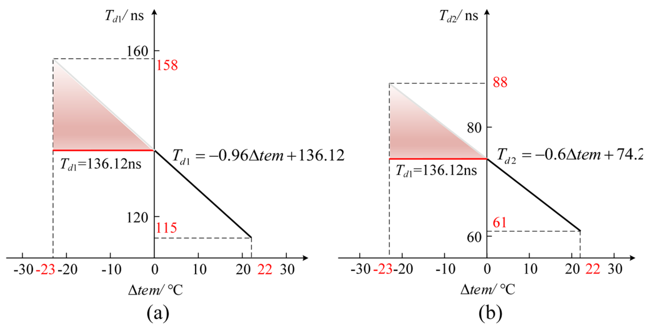

Fig. 21. Schematic diagram of distribution rule variation range of delay time (a) T_{d1};(b) T_{d2}.

therefore serve as a proof-of-concept demonstration, while ongoing work is extending the test platform to 800 V to further validate the method under conventional inverter operating voltages.

V. ATM Optimization Scheme Considering Efficiency

The traditional ATM strategy is reliability-oriented and dynamically adjusts the switching loss of SiC MOSFETs. And the EGRC-based method does not interfere with the inherent thermal balancing of parallel-connected SiC MOSFETs. Instead, it provides an additional degree of control to minimize ΔT_j cycling, further improving device lifetime. However, existing active control methods for junction temperature rarely consider efficiency factors, which, to some extent, limits their application and promotion. Therefore, this section further explores efficiency indicators for mitigating junction temperature fluctuations. As shown in Fig. 21, when using the ATM method proposed in this article, according to the linear allocation rule, ATM helps reduce switch loss when the junction temperature is higher than 70 °C, and the efficiency will increase in this stage. Therefore, it is not accurate to simply use the decrease in efficiency or increase in power consumption at a particular moment to illustrate that ATM strategies will reduce efficiency. This article proposes to use the concept of average power consumption P_{ave} to characterize the impact on system efficiency. The system operating conditions in Fig. 18 are divided into seven stages, and the switching loss of SiC MOSFET in each stage can be obtained through calculation and testing. Finally, P_{ave} of these seven operating conditions can be calculated.

After theoretical analysis, the EGRC-based ATM strategy helps to reduce switching loss when the junction temperature is higher than the reference temperature. At this point, the allocation rule for the delay time of the auxiliary switch corresponds to the positive half-axis of the horizontal axis in Fig. 18. The switching loss increases when the junction temperature is lower than the reference temperature, and precisely, these stages require optimization, namely the 17 and 20 A current stages in Fig. 18. The delay time allocation rule for auxiliary switches corresponds to the negative half-axis of the horizontal axis in Fig. 21. Changing the slope of the negative half-axis function can change the adjustment ability of switch loss. The limit situation is that the delay time remains fixed when the

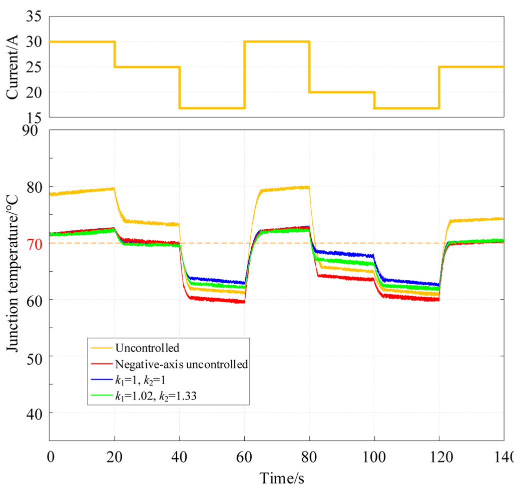

Fig. 22. Control of junction temperature with different allocation rules.

junction temperature is lower than the reference temperature, indicating that the ATM strategy is not performed. The slope of the function is –1. The horizontal half-axis remains unchanged in the allocation rules, while the red line in Fig. 21 shows the negative half-axis.

Changing the slope of the above allocation rules allows the junction temperature regulation ability to be controlled. This section defines this area as the temperature control operating space (TCOS), as shown in the red area in Fig. 21.

The junction temperature control coefficient (JTCC) is defined as k. By changing the JTCC, the function can change within the TCOS. Therefore, the negative half-axis allocation rule has been changed to

$$T_{d1} = -0.96\Delta T \cdot k_1 + 136.12 \qquad 1 \leq k_1 \leq \frac{25}{24} \tag{28}$$

$$T_{d2} = -0.6\Delta T \cdot k_2 + 74.2 \qquad 1 \leq k_2 \leq \frac{5}{3} \tag{29}$$

where k_1 and k_2 represent the JTCCs of SiC MOSFET during turn-ON and turn-OFF stages, respectively. The positive half-axis of the horizontal axis maintains the original allocation rule. After retesting with $k_1 = 1.02$ and $k_2 = 1.33$, the results are shown in Fig. 22. The yellow waveform represents the junction temperature curve of SiC MOSFET without any ATM strategy. The red waveform represents the junction temperature curve when the junction temperature is below the reference temperature without ATM. The blue waveform shows the junction temperature curve using the method proposed in this article, with $k_1 = 1$ and $k_2 = 1$. The green waveform represents the junction temperature curve when the junction temperature control coefficient $k_1 = 1.02$ and $k_2 = 1.33$. The allocation rule is shown in Fig. 23.

It can be seen that adjusting the JTCC can change the junction temperature regulation ability of the proposed active thermal management strategy. The switching loss of SiC MOSFET at each stage is measured using different control methods, as shown in Table VII.

Table VIII summarizes the expected lifetime, partial average power consumption and overall average power consumption

TABLE VII
SWITCH LOSS STATISTICS AT DIFFERENT STAGES WITH DIFFERENT ALLOCATION RULES

Current/A	30	25	17	30	20	17	25
Uncontrolled	27.2 W	17.4 W	6.26 W	27.2 W	9.77 W	6.26 W	17.4 W
k_1=1, k_2=1	18.1 W	15.2 W	8.57 W	18.2 W	13.6 W	8.59 W	15.2 W
Negative-axis uncontrolled	18.2 W	15.2 W	5.47 W	18.1 W	8.55 W	5.46 W	15.3 W
k_1=0.5, k_2=0.5	18.2 W	15.2 W	7.24 W	18.2 W	10.1 W	7.28 W	15.3 W

TABLE VIII
LIFETIME AND POWER CONSUMPTION STATISTICS FOR DIFFERENT ALLOCATION RULES

Strategy	Lifetime/h	Partial P_{ave}/W	Total P_{ave}/W
Uncontrolled	18383 (100%)	7.43 (100%)	15.93 (100%)
k_1=1, k_2=1	40091 (218%)	10.25 (138%)	13.92 (87.38%)
Negative-axis uncontrolled	26616 (145%)	6.49 (87.35%)	12.32 (77.34%)
k_1=0.5, k_2=0.5	35400 (193%)	8.21 (110%)	13.07 (82.05%)

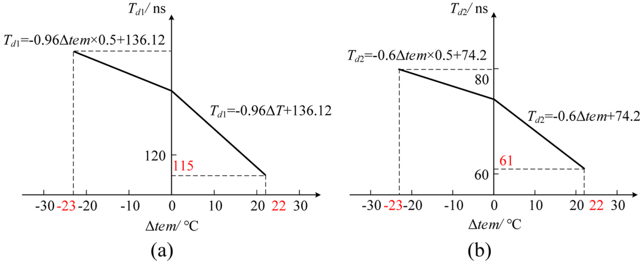

Fig. 23. Schematic diagram of allocation rules when using different JTCCS (a) allocation rules for T_{d1} when $k_1 = 1.02$, (b) allocation rules for T_{d2} when $k_2 = 1.33$.

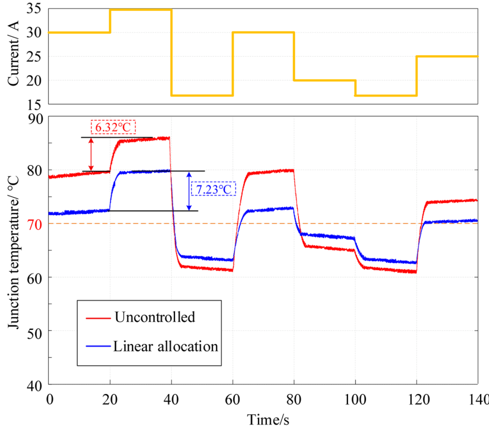

Fig. 24. Phenomenon of increased temperature fluctuations.

calculated under the 4 test scenarios mentioned above, all based on the measurement results without any control strategy conditions (100%) for easy comparison. When $k_1 = 1$ and $k_2 = 1$, the junction temperature fluctuation amplitude is the smallest, therefore, the expected lifetime is the longest. As analyzed earlier, when adopting an ATM strategy based on switching loss, the impact on efficiency cannot be solely evaluated by instantaneous power. Only when the system is in low-power operating conditions is it necessary to increase the switching loss to improve the junction temperature. The partial average power consumption in Table VII refers to the average power consumption of the two stages (17 and 20 A). It is undeniable that adopting the ATM strategy will slightly increase the loss. Still, the overall change is relatively small, mainly due to the relatively small system current at these two stages.

Overall, compared to the situation without any control, when using the ATM strategy based on the EGRC, the overall average power consumption P_{ave} is 13.92 W, which is reduced by 12.62%, and the expected lifetime is 40 091 h, which is increased by 218%, and the junction temperature fluctuation control effect is the best. After introducing the JTCC, when the temperature difference negative half axis is not controlled, the overall average power consumption significantly decreases to 12.32 W, a decrease of 22.66%, and the power performance is the best. In this case, the fluctuation of junction temperature increases, and the expected lifetime decreases to 26 616 h, which is still better than that without any thermal management strategy. After adjusting the JTCC, the fluctuation amplitude of the junction temperature decreases, and the expected lifetime increases to 35 400 h. However, the P_{ave} has increased to 13.07 W.

In summary, this section proposes the concepts and design methods of JTCC and TCOS. The average power consumption can be adjusted by constructing the JTCC and optimizing the allocation rule of delay time T_{d}. This method limits additional efficiency loss while extending the expected lifetime of SiC MOSFETs, providing researchers with a reasonable combination and selection between lifetime performance and power consumption performance.

VI. PRELIMINARY EXPLORATION OF GLOBAL ATM

In Section V, this article optimizes the allocation rules for the negative *X*-axis by considering efficiency factors. For the positive *X*-axis, due to the randomness of actual load power fluctuations, implementing junction temperature management strategies during certain phases where the load current I_{d} exceeds the load current corresponding to the reference temperature (20 A) in the test actually increases junction temperature fluctuations. As shown in Fig. 24, the junction temperature fluctuation increases from 6.32 to 7.23 °C. The primary reason for this phenomenon is that the actual load current has exceeded the upper limit of the junction temperature regulation capability, causing the delay turn-ON time T_{d} of the auxiliary switch to

maintain a fixed-value output. This implies that continuing to adopt the linear allocation rules of Fig. 17 (positive X-axis) may increases the junction temperature fluctuations shown in the dashed frame, which will adversely affect the service life of SiC MOSFETs.

Given the randomness of load power fluctuations in actual operating conditions, a new allocation rule needs to be discussed to ensure that junction temperature management does not adversely affect the expected service life of SiC MOSFETs under any load variations. Thus, this article further optimizes the linear allocation for the positive X-axis in Fig. 17. As a relatively simple allocation rule, the linear allocation currently distributes the delay time of the auxiliary switch according to (22) and (23). To facilitate the discussion on the phenomenon of increased junction temperature fluctuations in the positive X-axis, it is assumed that an arbitrary load current I_{d0} fluctuates upward to I_{d1}. Before implementing junction temperature management, the switching loss generated by the SiC MOSFET at load current I_{d0} is $P\mathrm{loss}(I_{\mathrm{d0}})$, and at load current I_{d1} is $P\mathrm{loss}(I_{\mathrm{d1}})$. The loss fluctuation ΔP_{loss} caused by load variations is then expressed as follows:

$$\Delta P_{\mathrm{loss}} = P_{\mathrm{loss}}\left(I_{d1}\right) - P_{\mathrm{loss}}\left(I_{d0}\right) \tag{30}$$

where $P_{\mathrm{loss}}(I_{\mathrm{d0}})$ and $P_{\mathrm{loss}}(I_{\mathrm{d1}})$ can be calculated according to formula (22).

The loss fluctuation $\Delta P_{\mathrm{loss_linear}}$ caused by load variations under the junction temperature management strategy with linear allocation is expressed as follows:

$$\Delta P_{\mathrm{loss_adj}} = P_{\mathrm{loss_linear}}\left(I_{d1}, \Delta\mathrm{tem}_1\right) - P_{\mathrm{loss_linear}}\left(I_{d0}, \Delta\mathrm{tem}_0\right) \tag{31}$$

where $P_{\mathrm{loss_linear}}(I_{\mathrm{d0}}, \Delta\mathrm{tem}_0)$ and $P_{\mathrm{loss_linear}}(I_{\mathrm{d1}}, \Delta\mathrm{tem}_1)$ can be calculated using (13), (16), (19), (22), and (23).

Let the change in loss fluctuation before and after junction temperature management be $\Delta P_{\mathrm{loss_diff}}$, as shown in the following:

$$\begin{aligned}\Delta P_{\mathrm{loss_diff}} &= \Delta P_{\mathrm{loss}} - \Delta P_{\mathrm{loss_adj}}\\ &= \Delta P_{\mathrm{loss}}\left(I_{d1}\right) - \Delta P_{\mathrm{loss}}\left(I_{d0}\right) - P_{\mathrm{loss_linear}}\left(I_{d1}, \Delta\mathrm{tem}_1\right)\\ &\quad + P_{\mathrm{loss_linear}}\left(I_{d0}, \Delta\mathrm{tem}_0\right).\end{aligned} \tag{32}$$

When $\Delta P_{\mathrm{loss_diff}}>0$, it indicates that when the load current fluctuates from I_{d0} to I_{d1}, the loss fluctuation after junction temperature management $\Delta P_{\mathrm{loss_adj}}$ is smaller than the loss fluctuation before management ΔP_{loss}, meaning that the junction temperature management reduces the loss fluctuation of the SiC MOSFET module. When $\Delta P_{\mathrm{loss_adj}} = 0$, the loss fluctuations of the SiC MOSFET remain unchanged before and after management. When $\Delta P_{\mathrm{loss_diff}}<0$, the junction temperature management actually increases the loss fluctuation of the SiC MOSFET. Thus, the global ATM strategy requires that during load current fluctuations, it must always satisfy the following:

$$\Delta P_{\mathrm{loss_diff}} \geq 0. \tag{33}$$

By introducing the evaluation function $\vartheta(\Delta\mathrm{tem})$, (33) can be expressed as follows:

$$\Delta P_{\mathrm{loss_diff}} = \vartheta\left(\Delta\mathrm{tem}_1\right) - \vartheta\left(\Delta\mathrm{tem}_0\right) \geq 0. \tag{34}$$

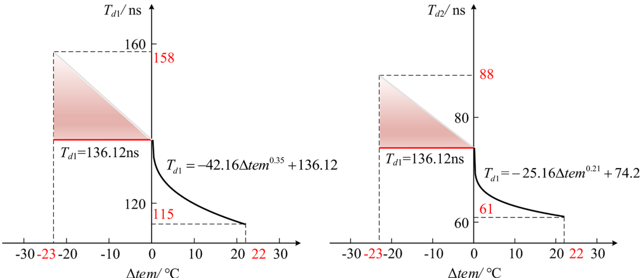

Fig. 25. Based on the distribution rule of power functions.

This transforms into solving the monotonicity problem of the evaluation function $\vartheta(\Delta\mathrm{tem})$. Through the above analysis, to ensure that the junction temperature management strategy always has a beneficial effect on the junction temperature of SiC MOSFETs under full-range load fluctuations, it is necessary to increase the compensation slope of the management strategy at low loads and decrease it at high loads. The linear junction temperature management strategy, which belongs to the uniform allocation rule with a fixed global compensation slope, fails to meet this requirement, leading to increased junction temperature fluctuations after management, as shown in the dashed box in Fig. 24. To achieve a larger compensation slope at low loads and a reduced slope at high loads, this correction method aligns with the characteristics of a power function. Therefore, a power function allocation rule for the delay time during the turn-ON phase of SiC MOSFETs is first constructed

$$T_{d1} = a\Delta\mathrm{tem}^b + c. \tag{35}$$

Combined with (30), the boundary conditions are as follows:

$$\begin{cases} T_{d1}\left(\Delta tem = 0\right) = 136.12\\ T_{d1}\left(\Delta tem = 22\right) = 115\\ \vartheta'\left(\Delta tem\right) > 0 \end{cases}. \tag{36}$$

The optimized allocation rule is obtained

$$T_{d1} = -42.16\Delta\mathrm{tem}^{0.35} + 136.12. \tag{37}$$

Using the same method, T_{d2} can be derived

$$T_{d2} = -25.16\Delta\mathrm{tem}^{0.21} + 74.2. \tag{38}$$

After reallocating the positive X-axis using a power function, as shown in Fig. 25, $\Delta P_{\mathrm{loss_diff}}>0$ always holds. The junction temperature regulation effect is illustrated in Fig. 26 where the amplitude of junction temperature fluctuations is smaller than that before optimization.

Table IX provides a comprehensive comparison of our proposed EGRC-based active thermal control with several recent ATM strategies for SiC MOSFETs. As shown, our method achieves precise ΔT_j regulation with minimal hardware complexity and real-time responsiveness. Unlike other methods that require additional sensing circuits, fuzzy logic controllers, or buffer energy modulation, our method integrates seamlessly with online Vth-based temperature estimation, offering an effective tradeoff between reliability enhancement and efficiency.

TABLE IX
COMPARISON OF ATM STRATEGIES FOR SIC MOSFETS

Strategy	Control Principle	Thermal Feedback	Complexity	Efficiency Factor Considered	Scalability	Real-Time Use	Reliability Enhancement	Global management capability
[40]	Buffer capacitance tuning to modulate loss	No	Moderate	No	Moderate	No	Moderate	No
[41]	Fuzzy rule adjusts frequency/duty	☑Yes	High	No	Low	No	Moderate	No
[42]	Monitors power degradation under cycling	☑Yes	High	No	Low	No	☑Yes	No
[43]	Transient thermal model & adaptive gate control	☑Yes	Moderate	No	Low	☑ Yes	☑Yes	No
[32]	Load/freq control for hybrid SiC/Si device	☑Yes	Moderate	No	Moderate	Moderate	Moderate	No
This work	EGRC	☑Yes	☑ Low	☑ Yes (JTCC)	☑ High	☑ Yes	☑ Yes and Quantified (TCOS)	☑ Yes

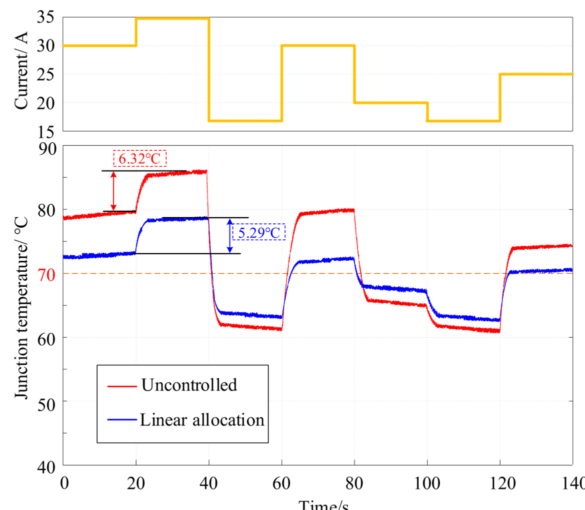

Fig. 26. Test results after applying the power function distribution rule.

Due to the limited length of this article, future work will further optimize the coefficients of the power function to bias it toward low-load compensation.

VII. Conclusion

In this article, we propose an EGRC-based ATM strategy for SiC MOSFETs. By modifying the gate driving resistance, the switching loss of SiC MOSFETs can be reduced, thereby enabling effective junction temperature regulation. A comparative switching mechanism is introduced to simplify the system design while maintaining performance. Additionally, this work establishes a temperature control range by dynamically adjusting switching losses. Using a full-bridge inverter as a case study, the proposed ATM system demonstrates a noticeable reduction in junction temperature fluctuations under varying power conditions, and the lifetime model suggests a possible improvement of up to 2.18 times. Furthermore, this study analyzes the impact of junction temperature control on system efficiency and presents a design methodology for optimizing the temperature control coefficient and operating range. As a result, the proposed approach not only enhances the longevity of SiC MOSFETs but also minimizes additional system power losses. Furthermore, to enhance the strategy's performance under dynamic or long-duration load cycles, a global temperature control method based on power-law distribution is further integrated.

The novelty and relevance of this work lie in showing that the proposed EGRC-based ATM strategy can effectively suppress low-frequency junction temperature fluctuations caused by load variations, thereby reducing thermo-mechanical stress in SiC MOSFETs. Experimental validation under different load scenarios (see Section V) and the integration of a global thermal management strategy (see Section VI) confirm the robustness and practicality of the approach. Compared with existing solutions, the proposed method offers a unique combination of device-level control precision, simple circuit implementation, and proven reliability benefit, making it directly relevant for real-world inverter applications.

In this work, lifetime prediction was introduced not as an absolute measure of field lifetime, but as a practical indicator to evaluate the effectiveness of the proposed ATM. By linking the reduction of junction temperature swings to estimated lifetime improvement through the Coffin–Manson model, the benefits of the control strategy can be expressed in a more intuitive and quantitative way. Furthermore, the adopted model was validated against our measured failure cycles, confirming its suitability. Therefore, the lifetime analysis complements the thermal results and provides a clearer demonstration of the overall effectiveness of the proposed method.

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