A Multiobjective Optimized Asymmetric Triple-Variable Modulation Strategy and Simplified Direct Duty Scheme for DAB Converters

Hao Li, Chonghui Song, *Member, IEEE*, Wenbing Hu, Guangdi Li, *Member, IEEE*, Dongsheng Yang, *Senior Member, IEEE*, Nie Hou, *Member, IEEE*, and Wei Xu, *Fellow, IEEE*

***Abstract*—To improve the efficiency of dual-active-bridge (DAB) converters under mismatched input and output voltages relative to the transformer ratio, a multiobjective optimized asymmetric triple-variable modulation (MOATVM) strategy is proposed in this article. Building on the asymmetric triple-variable modulation, this study introduces zero-voltage switching (ZVS) constraints to minimize the peak-to-valley current, thereby indirectly reducing the rms current and extending the ZVS range, which can enhance the efficiency of the DAB converter, especially under light-load conditions. Moreover, one simplified direct duty (SDD) scheme is further proposed based on the optimization results. The SDD scheme bypasses the need for power-based duty cycle calculations, which can reduce the computation with lower implementation complexity. Finally, experimental results demonstrate that the proposed MOATVM strategy, combined with the low-complexity SDD scheme, achieves a wide ZVS range and low rms current among several typical modulation methods, thereby significantly enhancing the efficiency of DAB converters at light loads.**

***Index Terms*—Dual-active-bridge (DAB) converter, efficiency, multiobjective asymmetric three-variable modulation (MOATVM), simplified direct duty (SDD) scheme, zero-voltage switching (ZVS).**

I. Introduction

OVER the past decade, advancements in power electronics technology have spurred the rapid development of dc power transmission, electric vehicles, energy storage, and other related fields [1], [2], [3]. As a key energy conversion device in these fields, the dual-active-bridge (DAB) converter has been widely and deeply studied due to its simple structure, wide zero-voltage switching (ZVS) range, galvanic isolation, and high efficiency [4], [5]. Single-phase-shift (SPS) modulation is widely used to maintain high efficiency in dc energy conversion. However, its efficiency declines significantly when input and output voltages are mismatched relative to the transformer ratio [5].

To overcome this limitation, advanced modulation methods with more control variables, such as dual-phase-shift (DPS) [6], extended-phase-shift (EPS) [7], and triple-phase-shift (TPS) [8], have been proposed. Among these, TPS modulation, with its three modulation variables, offers greater flexibility, enabling significant current reduction and efficiency improvement. Consequently, extensive research based on TPS modulation has been conducted [9], [10], [11], [12], [13], [14], [15], [16], [17], [18].

In the frequency-domain model of the DAB converter, transmission power and root-mean-square (rms) current are expressed as the sum of the fundamental component and higher order harmonics. Noroozi et al. [10] employed intelligent optimization algorithms to minimize rms current, reducing conduction losses. However, numerical solutions for higher order harmonics necessitate offline lookup tables, complicating implementation. To simplify optimization, fundamental component-based methods, such as fundamental duty modulation (FDM-TPS) [11] and fundamental harmonic analysis (FHA-TPS) [12], were proposed. These approaches provide analytical solutions by minimizing the fundamental rms current and achieving good ZVS performance at light loads. Unfortunately, neglecting higher order harmonics causes the optimization results to degenerate into an EPS form, leading to higher rms currents.

Apart from the frequency-domain approach, time-domain modeling is also commonly utilized in DAB converters, where transmission power and rms current expressions can be derived through piecewise integral calculations [13], [14], [15], [16]. Tong et al. [13] calculated and optimized the rms current using the time-domain model. However, the process involved complicated rms current calculations and optimization procedures. In addition, this approach resulted in a narrow ZVS range under light-load conditions. To address these complexities, simpler peak current optimization approaches have been proposed [14], [15], [16], indirectly reducing rms current and enhancing converter efficiency by minimizing peak current. For example, Huang et al. [14] introduced a unified TPS control method,

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Hao Li, Chonghui Song, Wenbing Hu, Guangdi Li, and Dongsheng Yang are with the State Key Laboratory of Synthetical Automation for Process Industries, College of Information Science and Engineering, Northeastern University, Shenyang 110004, China (e-mail: 2110259@stu.neu.edu.cn; songchonghui@mail.neu.edu.cn; 2310256@stu.neu.edu.cn; liguangdi@mail.neu.edu.cn; yangdongsheng@mail.neu.edu.cn).

Nie Hou is with the School of Electrical and Information Engineering, Tianjin University, Tianjin 300072, China (e-mail: nie_hou@tju.edu.cn).

Wei Xu is with the State Key Laboratory of High Density Electromagnetic Power and Systems, Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing 100190, China (e-mail: weixu@mail.iee.ac.cn).

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Shao et al. [15] optimized peak current indirectly through backflow power minimization, and Gu et al. [16] proposed current stress minimization (CSM-TPS) to reduce conduction losses and improve efficiency. However, similar to the rms current optimization result in [13], optimizing peak current typically encounters the issue of a limited ZVS range, with only two switches achieving ZVS under light-load conditions. Furthermore, some methods [17], [18] extended the ZVS range at light loads, further enhancing converter efficiency. Nevertheless, these methods lack precise analytical solutions and instead rely on empirical coefficients, limiting their scalability and adaptability.

Fortunately, asymmetric modulation strategies with non-50% switch duty cycles provide a promising solution compared to symmetric modulations, such as DPS, EPS, and TPS, which inherently operate at a 50% duty cycle. Due to the symmetry of current half-cycles, ZVS losses typically occur in pairs with TPS. In contrast, asymmetric modulation strategies can break this symmetry, enabling improved ZVS performance. Mou et al. [19] proposed an asymmetric modulation strategy, but its improvement in ZVS range is limited. Furthermore, a five-degree-of-freedom (5-DoF) modulation strategy has been proposed to further improve the light-load efficiency of DAB converters [20], achieving excellent performance. However, due to the high number of variables involved, optimizing and implementing 5-DoF strategies are complex, sometimes requiring offline lookup tables [21]. To reduce implementation complexity, two-variable asymmetric modulation methods have been proposed [22], [23], exhibiting good ZVS performance but encountering high rms current issues. Recently, unilateral asymmetric triple-phase-shift (UATPS) modulation was proposed [24] to reduce rms current compared to two-variable modulation, allowing four switches to achieve ZVS at light loads and improving efficiency significantly. Nevertheless, four switches still lack ZVS capability at light loads.

Therefore, it is necessary to develop a modulation strategy capable of enabling ZVS for more switches at light loads without the high rms current associated with two-variable modulation or the complexity of 5-DoF modulation. Consequently, this article proposes a multiobjective optimized asymmetric triple-variable modulation (MOATVM) strategy along with a simplified direct duty (SDD) scheme characterized by low computational complexity. The main contributions are summarized as follows.

1) The MOATVM strategy integrates ZVS constraints into the optimization of peak-to-valley current to indirectly reduce rms current and broaden the ZVS range, thus enhancing the DAB converter's efficiency at light loads.
2) By introducing two ZVS constraints, the MOATVM strategy enables ZVS for seven switches under light loads, balancing the complexity of optimization while avoiding significant rms current increases.
3) Based on optimization results, the SDD scheme, bypassing the need for power-based duty cycle calculations, is proposed to further decrease computational complexity. The combination of MOATVM and SDD achieves an excellent balance between efficiency enhancement and practical implementation feasibility.

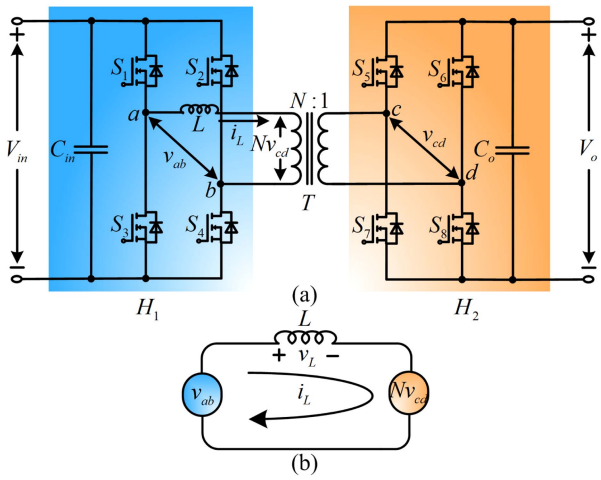

Fig. 1. Topology of the DAB converter. (a) Original topology. (b) Equivalent circuit.

4) Compared to the 5-DoF scheme, the proposed MOATVM and SDD scheme based on the 3-DoF framework not only slightly improve the light-load efficiency of the DAB converter but also effectively reduce the computational burden of modulation by over 40%.

The rest of this article is organized as follows. Section II introduces asymmetric three-variable modulation (ATVM) and its operating modes. Section III details the proposed MOATVM strategy with indirectly reduced rms current and extended ZVS range. Section IV presents the SDD scheme aimed at simplifying modulation implementation. Section V presents experimental validation results. Finally, Section VI concludes this article.

II. ATVM and Its Classification

The DAB converter shown in Fig. 1(a) consists of two full H-bridges (denoted as H_1 and H_2), an inductor L, and an ideal transformer T with a turns ratio of $N:1$. The SiC MOSFET switches in the circuit are labeled as S_1–S_8. The voltages across the primary and secondary sides of the transformer are defined as v_{ab} (voltage between points a and b) and v_{cd} (voltage between points c and d), respectively. The current flowing through the inductor L is denoted by i_L, with v_L representing the voltage across inductor L, as shown in Fig. 1(b). By controlling the switching states of S_1–S_8, the relative positions and duty cycles of v_{ab} and Nv_{cd} can be adjusted to regulate the converter operation.

In this article, the parameter k is used to characterize the mismatch between V_{in} and V_o, defined as the mismatch coefficient, i.e.,

$$k = \frac{V_{\text{in}}}{NV_o}. \tag{1}$$

To simplify the analysis, the condition $k \geq 1$ is discussed in detail. The proposed method in this article can also be applied to optimize systems when $k < 1$. The optimization solutions for $k < 1$ is provided in the Appendix rather than including detailed analysis in the article.

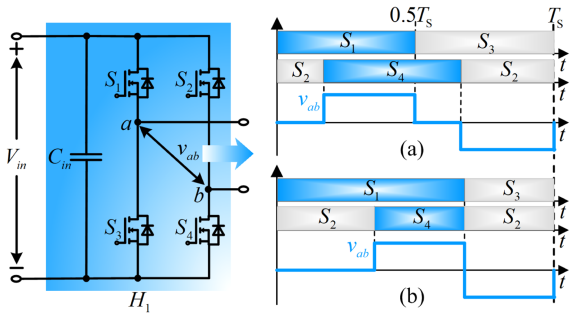

Fig. 2. Typical waveforms of switching signals and output. (a) Symmetric modulation. (b) Asymmetric modulation.

A. Symmetric Modulation and Asymmetric Modulation

Fig. 2 illustrates typical waveforms of the symmetric and asymmetric modulation methods with H_1 as an example. Fig. 2(a) shows the waveform of symmetric modulation, which features a 50% duty cycle per switching cycle, resulting in a symmetrical voltage sequence of "zero-high-zero-low." In contrast, asymmetric modulation allows a non-50% duty cycle. Specifically, switches S_1 and S_2 have duty cycles greater than 50%, while S_3 and S_4 have duty cycles less than 50%. S_1 switches ON first, followed by S_4. Then, S_1 and S_4 switch OFF simultaneously as S_2 and S_3 turn ON simultaneously. This switching sequence generates an output voltage sequence of "zero-high-low" within one switching period, distinguishing it from the symmetrical modulation method, as clearly depicted in Fig. 2(a) and (b).

B. ATVM Strategy and Mode Classification

The ATVM is a modulation strategy in which both H_1 and H_2 adopt asymmetric modulation, as shown in Fig. 3. The ON-time of S_3 and S_4 in H_1 is D_1T_s, while the ON-time of S_1 and S_2 is $(1-D_1)T_s$, resulting in a duty cycle of v_{ab} equal to D_1. Similarly, in H_2, the ON-time of S_7 and S_8 is D_2T_s, and the ON-time of S_5 and S_6 is $(1-D_2)T_s$, giving a duty cycle of Nv_{cd} as D_2. In addition, there is an on-time delay of D_3T_s between H_1 and H_2. Consequently, the DAB converter using the ATVM features three control variables, namely, D_1, D_2, and D_3. For the ATVM, v_{ab}, Nv_{cd}, and their relative positions differ, leading to variations in the inductor current i_L. This results in different operational modes (modes I–IV), corresponding to Fig. 3(a)–(d). The classification criterion is established as follows. Since power is transferred from H_1 to H_2, H_2 lags behind H_1, meaning the turn-ON instants of S_6 and S_7 lag behind those of S_2 and S_3. Based on this, the classification is determined by the permutation of relative positions between the voltage transition points of v_{cd} (purple and gray dots in Fig. 3) and the voltage transition points of v_{ab} (green and red dots in Fig. 3). This includes the following four scenarios. Both purple and gray dots of v_{cd} lie between the green and red dots of v_{ab} (Mode I); only the purple dot of v_{cd} lies between the red and green dots of v_{ab} (Mode II); both purple and gray dots of v_{cd} occur after the green and red dots of v_{ab} (Mode III); and the purple dot of v_{cd} occurs before the green and red dots, while the gray dot occurs after them (Mode IV).

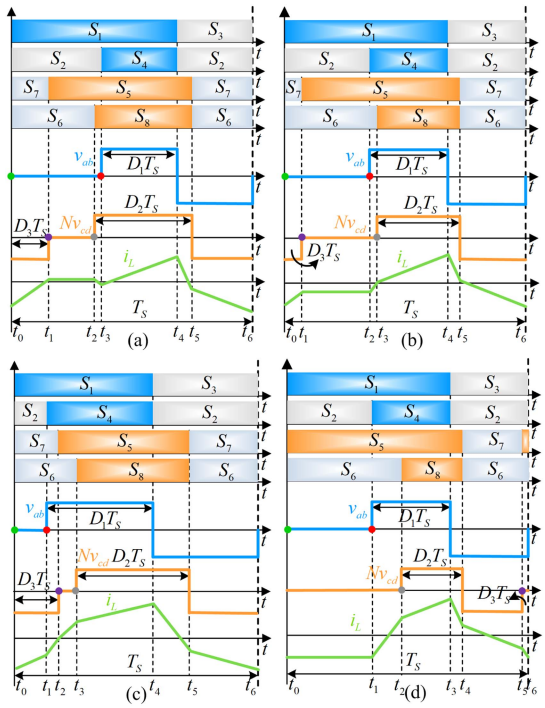

Fig. 3. Typical switching signals and outputs of the ATVM. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

TABLE I
MODE CLASSIFICATION

Mode	Inequality Constraints
Mode I	$1+D_3-2D_2 \le 1-2D_1,\ 1-D_1 \le 1+D_3-D_2$
Mode II	$D_3 \le 1-2D_1 \le 1+D_3-2D_2 \le 1-D_1 \le 1+D_3-D_2$
Mode III	$1-2D_1 \le D_3,\ 1+D_3-2D_2 \le 1-D_1 \le 1+D_3-D_2$
Mode IV	$1-2D_1 \le 1-D_3-2D_2 \le 1-D1 \le 1-D3-D2$

The characteristics of different modes can be described in terms of the relationship in sizes among D_1, D_2, and D_3, as given in Table I.

III. Proposed MOATVM With Indirectly Reduced RMS Current and Wide ZVS Range

A. Steady-State Characteristics

The steady-state characteristics define the mathematical relationships of power transmission P and inductor current i_L. While power transmission is essential for converter operation, inductor current influences efficiency by affecting conduction losses and ZVS. Since rms current directly impacts conduction losses but is complex to optimize, peak-to-valley current is used as a simpler alternative to indirectly reduce rms current.

Before solving the steady-state characteristics, the ZVS potentials for the three modes are analyzed to simplify subsequent discussions. The ZVS conditions for switches S_1–S_8 can be expressed as follows:

$$\begin{cases} S_1, S_4 : i_L(t_*) \le -I_{\text{ZVS1}},\ S_2, S_3 : i_L(t_*) \ge I_{\text{ZVS1}} \\ S_6, S_7 : i_L(t_*) \le -I_{\text{ZVS2}},\ S_5, S_8 : i_L(t_*) \ge I_{\text{ZVS2}} \end{cases} \tag{2}$$

where t_* represents the moment when each switch turns ON, and I_{ZVS1} and I_{ZVS2} denote the critical current values required to achieve the ZVS condition of H_1 and H_2 sides, respectively. According to (2) and as observed in Fig. 3(a) and (c), both modes I and III have the potential to achieve ZVS entirely. In the case of mode II, since $i_L(t_1)=i_L(t_2)$ (switch S_4 turns ON at time t_1 and switch S_5 turns ON at time t_2), and considering (2), the ZVS conditions for switches S_4 and S_5 have opposite current requirements. Therefore, in mode II, achieving ZVS for either switch S_4 or S_5 inevitably comes at the cost of hard switching for the other switch. For mode IV, since the ZVS conditions for S_5 and S_6/S_7 require opposite current polarities (S_5 requires positive current while S_6/S_7 require negative current), and since the applied voltage from t_4 to t_5 is negative in this mode, the current at the turn-ON instant of S_5 is smaller than that at the turn-ON of S_6/S_7. Consequently, in mode IV, at least one switch S_5 (or even two switches S_6/S_7) experiences complete hard switching due to the reversed current direction. In contrast, modes I and III do not encounter this issue. Even if a certain switch in mode I or mode III does not achieve complete ZVS, it may still attain quasi-ZVS due to the current direction potentially meeting the ZVS conditions. This scenario remains preferable to the complete hard switching observed in modes II and IV. Based on the above analysis, only modes I and III are discussed.

Taking mode I as an example for detailed derivation, the instantaneous value of inductance current in one T_s can be expressed as

$$i_L(t)=\begin{cases} i_L(t_0)+\frac{NV_o}{L}(t-t_0) & (t_0\le t\le t_1)\\ i_L(t_1) & (t_1\le t\le t_2)\\ i_L(t_2)-\frac{NV_o}{L}(t-t_2) & (t_2\le t\le t_3)\\ i_L(t_3)+\frac{V_{\text{in}}-NV_o}{L}(t-t_3) & (t_3\le t\le t_4)\\ i_L(t_4)-\frac{V_{\text{in}}+NV_o}{L}(t-t_4) & (t_4\le t\le t_5)\\ i_L(t_5)-\frac{V_{\text{in}}-NV_o}{L}(t-t_5) & (t_5\le t\le t_6) \end{cases} \tag{3}$$

where

$$\begin{cases} t_0=0, t_1=D_3T_s, t_2=(1+D_3-2D_2)T_s\\ t_3=(1-2D_1)T_s, t_4=(1-D_1)T_s, t_5=(1+D_3-D_2)T_s. \end{cases} \tag{4}$$

According to the volt–second principle, the integral of the current i_L flowing through the inductor L in one T_s is zero, i.e.,

$$\int_0^{T_s} i_L(t)dt=0. \tag{5}$$

TABLE II
p AND i_{p-V} OF MODES I AND III

Mode	p	i_{p-v}
Mode I	$8(D_1^2-D_2^2-D_3^2+2D_2D_3)$	$8[kD_1+D_1-2D_2+2D_3]$
Mode III	$8(-3D_1^2-3D_2^2-2D_3^2+4D_1D_2$ $-4D_1D_3+4D_2D_3+2D_1+D_3-\frac{1}{2})$	$8[kD_1+D_1-2D_2+2D_3]$

By solving (5), the inductor current values of $i_L(t_0)$–$i_L(t_6)$ can be obtained, i.e.,

$$\begin{cases} i_L(t_0)=\frac{V_{\text{in}}(-D_1^2)+NV_o(D_2^2-D_3)}{f_sL}\\ i_L(t_1)=\frac{V_{\text{in}}(-D_1^2)+NV_oD_2^2}{f_sL}\\ i_L(t_2)=\frac{V_{\text{in}}(-D_1^2)+NV_oD_2^2}{f_sL}\\ i_L(t_3)=\frac{V_{\text{in}}(-D_1^2)+NV_o(D_2^2+2D_1-2D_2+D_3)}{f_sL}\\ i_L(t_4)=\frac{V_{\text{in}}(-D_1^2+D_1)+NV_o(D_2^2+D_1-2D_2+D_3)}{f_sL}\\ i_L(t_5)=\frac{V_{\text{in}}(-D_1^2+D_2-D_3)+NV_o(D_2^2-D_2)}{f_sL}\\ i_L(t_6)=i_L(t_0). \end{cases} \tag{6}$$

Then, the peak-to-valley current I_{P-V} of i_L and the transmitted power P can be obtained, i.e.,

$$\begin{cases} I_{P-V}=i_L(t_4)-i_L(t_6)=\frac{V_{\text{in}}(D_1)+NV_o(D_1-2D_2+2D_3)}{f_sL}\\ P=\frac{1}{T_s}\int_0^{T_s}v_{ab}i_L(t)dt=\frac{NV_{\text{in}}V_o(D_1^2-D_2^2-D_3^2+2D_2D_3)}{f_sL}. \end{cases} \tag{7}$$

For the convenience of analysis, I_{P-V} and P can be normalized with I_N and P_N as the reference values, respectively, i.e.,

$$\begin{cases} i_{p-v}=\frac{I_{P-V}}{I_N}=8(kD_1+D_1-2D_2+2D_3)\\ p=\frac{P}{P_N}=8(D_1^2-D_2^2-D_3^2+2D_2D_3) \end{cases} \tag{8}$$

where i_{p-v} and p are the normalized peak-to-valley current and transmitted power, respectively, and

$$\begin{cases} I_N=\frac{NV_o}{8f_sL}\\ P_N=\frac{NV_{\text{in}}V_o}{8f_sL}. \end{cases} \tag{9}$$

According to the same analysis method, p and i_{p-v} for modes I and III are calculated and given in Table II.

B. MOATVM: Minimization of i_{p-V} With ZVS Constraints

In Table II, the values of p and i_{p-v} are determined by the free variables D_1, D_2, and D_3. Finding a set of D_1, D_2, and D_3 combinations that satisfy the power equality constraint and duty cycle inequality constraint while minimizing i_{p-v} can indirectly reduce the rms current. This optimization problem can be expressed as

$$\begin{aligned} &\min\ i_{p-v}(D_1,D_2,D_3)\\ &\text{s.t. } p(D_1,D_2,D_3)-p^*=0\\ &g_i(D_1,D_2,D_3)\le 0, i=1,2,\ldots,l \end{aligned} \tag{10}$$

where i_{p-v} is the optimization objective, p is the equality constraint, p^* is the desired unit power, g_i is the boundary condition for variables, and l is the number of boundary conditions.

In particular, the ZVS range of the DAB converter is narrow when operating at light loads and wide at heavy loads. Therefore, specific ZVS constraints must be incorporated when optimizing mode I to enhance efficiency at light loads. Two key factors should be considered when extending the ZVS range under light-load conditions.

1) Implementing full ZVS at light loads often introduces significant complexity to the optimization process, resulting in computationally expensive solutions that are less suitable for microcontroller implementations.
2) Increasing the number of ZVS-enabled switches generally leads to a larger duty cycle of ac voltage, which could lead to elevated core losses due to intensified magnetic flux density variations in the transformer.

Therefore, expanding the ZVS range requires balancing the tradeoff between the number of ZVS-enabled switches and the resulting increase in optimization complexity, analytical solution difficulty, and core losses. Fortunately, interesting insights can be gleaned from observing Fig. 3(a). Specifically, $i_L(t_1)$ and $i_L(t_2)$ represent the turn-ON moments of S_5 and S_8, respectively, and they are equal ($i_L(t_1) = i_L(t_2)$). Since both S_5 and S_8 belong to H_2, their ZVS current boundary values are identical. Therefore, achieving ZVS for both S_5 and S_8 simultaneously requires only one value of $i_L(t_2)$ to exceed the ZVS boundary. In addition, since both S_6 and S_7 are turned ON simultaneously, S_6 and S_7 can achieve ZVS as long as $i_L(t_5)$ exceeds the ZVS boundary value. In summary, it is necessary to add only two ZVS boundary conditions to enable ZVS for four switches (S_5–S_8). As a result, a total of seven switches can achieve ZVS, as S_1–S_3 naturally attain ZVS due to their turn-ON at the current peaks and valleys.

Remark 1 (The reason for not adding the ZVS constraint of S_4): For S_5/S_8, adding a single constraint can enable the two switches to achieve ZVS, thereby more effectively reducing switching losses. Consequently, the benefit of adding this constraint is relatively high. Similarly, for S_6/S_7, adding ZVS constraints for S_4 only benefits this single switch, with the drawbacks of complicating optimization and potentially requiring more duty cycle adjustments that increase core loss, resulting in limited benefits. Moreover, S_4 achieves quasi-ZVS at light loads in the proposed scheme. Compared to complete hard switching, this also contributes to a notable reduction in switching losses, representing a satisfactory outcome.

The boundary values for ZVS current of switches S_5–S_8 converted to the primary side, denoted as I'_{ZVS2}, can be expressed as

$$I'_{\text{ZVS2}} = \frac{V_o}{N}\sqrt{2C_{\text{oss}}/L} \tag{11}$$

where C_{oss} is the junction capacitor of the switch. Therefore, the constraint conditions for S_5–S_8 to implement ZVS are

$$\begin{cases} i_L(t_2) \geq I'_{\text{ZVS2}} \\ i_L(t_5) \leq -I'_{\text{ZVS2}}. \end{cases} \tag{12}$$

For ease of analysis, (12) can be normalized using $i_{\text{base}} = \frac{NV_o}{f_s L}$. Combining this with (6) and (11), (12) can be rewritten as

$$\begin{cases} \frac{i_L(t_2)}{i_{\text{base}}} = -kD_1^2 + D_2^2 \geq \frac{I'_{\text{ZVS2}}}{i_{\text{base}}} = i'_{\text{ZVS2}} \\ \frac{i_L(t_5)}{i_{\text{base}}} = k(-D_1^2 + D_2 - D_3) + D_2^2 - D_2 \leq -\frac{I'_{\text{ZVS2}}}{i_{\text{base}}} = -i'_{\text{ZVS2}} \end{cases} \tag{13}$$

where i'_{ZVS2} represents the normalized critical ZVS current value, given by

$$i'_{\text{ZVS2}} = \frac{f_s}{N^2}\sqrt{2C_{\text{oss}}L}. \tag{14}$$

Hence, by incorporating (13), seven switches (S_1–S_3 and S_5–S_8) can achieve ZVS (S_1–S_3 naturally exhibit ZVS as they turn ON at the peak points of the current). Combining Table I, (13), and (14), the boundary condition $g_i(D_1,D_2,D_3)$ for achieving ZVS of seven switches in mode I is

$$\begin{cases} g_1 = 2D_1 - 2D_2 + D_3 \leq 0 \\ g_2 = -D_1 + D_2 - D_3 \leq 0 \\ g_3 = D_2 - 0.5 \leq 0 \\ g_4 = i'_{\text{ZVS2}} + kD_1^2 - D_2^2 \leq 0 \\ g_5 = k(-D_1^2 + D_2 - D_3) + D_2^2 - D_2 + i'_{\text{ZVS2}} \leq 0. \end{cases} \tag{15}$$

The Karush–Kuhn–Tucker (KKT) condition is a suitable method for solving optimization problems that include both equality and inequality constraints. To begin, the Lagrange equation with constraints needs to be formulated as

$$\begin{aligned} E(D_1, D_2, D_3, \lambda, \mu) &= i_{p-v}(D_1, D_2, D_3) \\ &+ \lambda[p(D_1, D_2, D_3) - p^*] + \sum_{i=1}^{l} \mu_i g_i(D_1, D_2, D_3) \end{aligned} \tag{16}$$

where E is the Lagrange equation, λ is the Lagrange multiplier for the equality constraint, and μ_i is the Lagrange multiplier for the inequality constraint. Then, the KKT conditions used to solve the optimization problem are

$$\begin{cases} \frac{\partial E}{\partial D_1} = 0,\ \frac{\partial E}{\partial D_2} = 0,\ \frac{\partial E}{\partial D_3} = 0 \\ \frac{\partial E}{\partial \lambda} = 0,\ \mu_i g_i = 0,\ \mu_i \geq 0,\ \lambda \neq 0. \end{cases} \tag{17}$$

By combining (15)–(17) and Table II, the optimal solution for mode I can be obtained

$$\begin{cases} D_1 = \frac{k+1}{4}\sqrt{\frac{2p}{k^2+2k-3}} & (0 \leq p \leq p_{b1}) \\ D_2 = \frac{k}{2}\sqrt{\frac{2p}{k^2+2k-3}} + 2i'_{\text{ZVS2}} & (0 \leq p \leq p_{b1}) \\ D_3 = \frac{k-1}{2}\sqrt{\frac{2p}{k^2+2k-3}} + 2i'_{\text{ZVS2}} & (0 \leq p \leq p_{b1}) \end{cases} \tag{18}$$

where

$$p_{b1} = \frac{(1 - 4i'_{\text{ZVS2}})^2(k-1)(k+3)}{2k^2}. \tag{19}$$

When $p \leq p_{b1}$, (18) fully satisfies the constraint. At $p = p_{b1}$, D_2 =0.5 is the critical condition, beyond which D_2 cannot increase further. However, when $p > p_{b1}$, all constraints (i.e., ZVS conditions) cannot be satisfied simultaneously. Therefore, for this power segment, setting D_2 =0.5 and discarding the ZVS

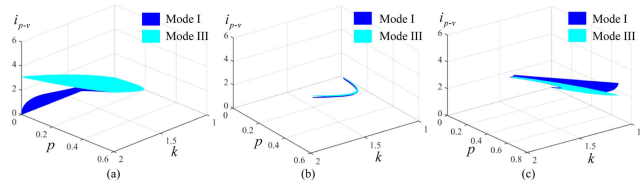

Fig. 4. Comparison of i_{p-v} between modes I and III in the three power intervals. (a) $p \in [0, p_{b1}]$. (b) $p \in [p_{b1}, p_{b2}]$. (c) $p \in [p_{b2}, p_{b3}]$.

constraints g_4 and g_5 allow for the optimization solution to be obtained

$$\begin{cases} D_1 = \begin{cases} \frac{k+1}{4}\sqrt{\frac{2p}{k^2+2k-3}} & (p_{b1} \le p \le p_{b2}) \\ \frac{1}{3}+\frac{1}{6}\sqrt{\frac{2-3p}{2}} & (p_{b2} \le p \le p_{b3}) \end{cases} \\ D_2 = \frac{1}{2} \qquad\qquad (p_{b1} \le p \le p_{b3}) \\ D_3 = \begin{cases} \frac{1}{2}-\frac{1}{2}\sqrt{\frac{2p}{k^2+2k-3}} & (p_{b1} \le p \le p_{b2}) \\ \frac{1}{3}-\frac{1}{3}\sqrt{\frac{2-3p}{2}} & (p_{b2} \le p \le p_{b3}) \end{cases} \end{cases} \tag{20}$$

where

$$p_{b2} = \frac{(k-1)(k+3)}{2k^2}, p_{b3} = \frac{2}{3}. \tag{21}$$

Similarly, the optimal solution for minimizing i_{p-v} in mode III is obtained as

$$\begin{cases} D_1 = \frac{1}{2} - \frac{k-1}{4}\sqrt{\frac{2(1-p)}{k^2-2k+3}} & (0 \le p \le 1) \\ D_2 = \frac{1}{2} & (0 \le p \le 1) \\ D_3 = \frac{1}{4} + \frac{k-2}{4}\sqrt{\frac{2(1-p)}{k^2-2k+3}} & (0 \le p \le 1). \end{cases} \tag{22}$$

The optimal solutions for mode III follow (22) for all $p \in [0, 1]$. However, the maximum transmission power for mode I is limited to p_{b3}. Therefore, for $p \in [p_{b3}, 1]$, the optimal solution of the DAB converter follows (22).

For $p \in [0, p_{b3}]$, a comparison between the optimal solutions of modes I and III is required to determine the global optimal solution. The magnitude of i_{p-v} for both modes at the same power level p is compared in Fig. 4. Dark blue represents mode I, while light blue corresponds to mode III. Fig. 4(a)–(c) illustrate the results for $p \in [0, p_{b1}]$, $p \in [p_{b1}, p_{b2}]$, and $p \in [p_{b2}, p_{b3}]$, respectively, necessitating a separate analysis for each interval.

1) For $p \in [0, p_{b1}]$, i_{p-v} for mode I is lower than that of mode III [see Fig. 4(a)]. Thus, the optimal solution for mode I in (18) is selected.
2) For $p \in [p_{b1}, p_{b2}]$, mode I still exhibits a lower i_{p-v} than mode III [see Fig. 4(b)], making (20) the optimal choice for this range.
3) For $p \in [p_{b2}, p_{b3}]$, mode III demonstrates a lower i_{p-v} compared to mode I [see Fig. 4(c)]. Consequently, (22) provides the optimal solution in this interval.

Therefore, the global optimal solution for the DAB converter, minimizing i_{p-v} while extending the ZVS range at light loads,

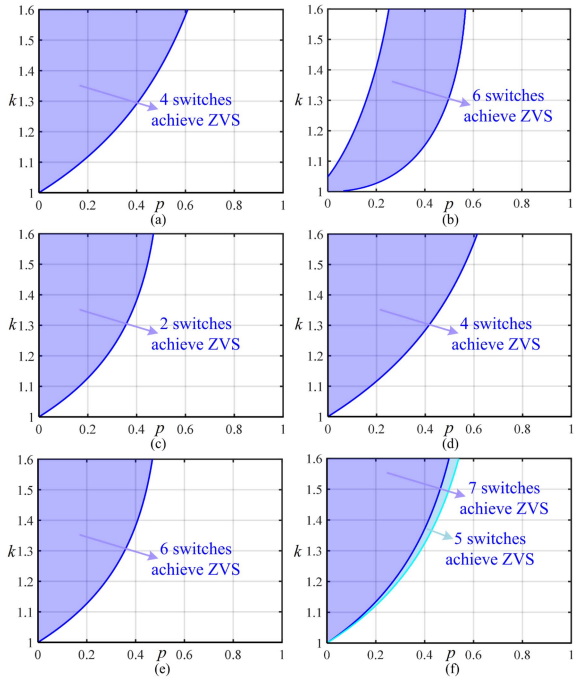

Fig. 5. ZVS range of different modulation strategies. (a) SPS. (b) FHA-TPS. (c) CSM-TPS. (d) UATPS. (e) 5-DoF. (f) MOATVM.

is given by

$$\begin{cases} D_1 = \begin{cases} \frac{k+1}{4}\sqrt{\frac{2p}{k^2+2k-3}} & (0 \le p \le p_{b2}) \\ \frac{1}{2} - \frac{k-1}{4}\sqrt{\frac{2(1-p)}{k^2-2k+3}} & (p_{b2} \le p \le 1) \end{cases} \\ D_2 = \begin{cases} \frac{k}{2}\sqrt{\frac{2p}{k^2+2k-3}} + 2i'_{\mathrm{ZVS2}} & (0 \le p \le p_{b1}) \\ \frac{1}{2} & (p_{b1} \le p \le 1) \end{cases} \\ D_3 = \begin{cases} \frac{k-1}{2}\sqrt{\frac{2p}{k^2+2k-3}} + 2i'_{\mathrm{ZVS2}} & (0 \le p \le p_{b1}) \\ \frac{1}{2} - \frac{1}{2}\sqrt{\frac{2p}{k^2+2k-3}} & (p_{b1} \le p \le p_{b2}) \\ \frac{1}{4} + \frac{k-2}{4}\sqrt{\frac{2(1-p)}{k^2-2k+3}} & (p_{b2} \le p \le 1). \end{cases} \end{cases} \tag{23}$$

C. ZVS Range

Fig. 5 illustrates the ZVS ranges of the proposed MOATVM in this article along with several other modulation strategies. Fig. 5(a) shows the ZVS range of SPS. Within the purple region, four switches achieve ZVS, while the remaining four lose ZVS. Fig. 5(b) depicts the ZVS range of FHA-TPS, where six switches maintain ZVS in the purple area, with two switches losing ZVS. The ZVS range of CSM-TPS is shown in Fig. 5(c), where only two switches achieve ZVS in the purple region. In contrast, UATPS achieves ZVS for four switches, as demonstrated in Fig. 5(d). The ZVS range of the 5-DoF scheme is presented in Fig. 5(e), with six switches achieving ZVS in the purple region. The proposed MOATVM method exhibits its ZVS range in Fig. 5(f), where seven switches achieve ZVS in the purple region, and five switches maintain ZVS in the blue region.

TABLE III
POWER RANGE DIVISION

Low power range		High power range
Power interval 1	Power interval 2	
$p \in [0,p_{b1}]$	$p \in [p_{b1},p_{b2}]$	$p \in [p_{b2},1]$

Nearly all switches achieve ZVS in the white region. Overall, comparing the ZVS ranges of these modulation methods, the proposed approach demonstrates excellent ZVS performance.

IV. SDD Scheme With Lower Computation

A. SDD Scheme Based on the MOATVM

Implementing the efficiency optimization of the DAB converter using (23) requires computing the duty cycles D_1, D_2, and D_3 from the power p, which involves multiple square root and division operations. If any of the variables D_1, D_2, or D_3 exhibits a globally monotonic relationship with p, then a one-to-one correspondence exists between them. This means that reaching a specific value of such a variable directly implies achieving the corresponding power level p, thereby eliminating the need to explicitly compute the variable from p. Fortunately, D_1 exhibits a global monotonic relationship with p, as analyzed below.

According to (23), the global optimization solution is divided into two power ranges (three power intervals), as shown in Table III. Power interval 1 and power interval 2 are defined as a low-power range, and the rest as a high-power range.

When p is in the low-power range ($p \in [0, p_{b2}]$), let

$$D_1 = \frac{k+1}{4}\sqrt{\frac{2p}{k^2+2k-3}} = f(p). \tag{24}$$

Because

$$\frac{\mathrm{d}f(p)}{\mathrm{d}p} > 0 \tag{25}$$

D_1 increases monotonically with p in the low-power range. When p belongs to the high-power range ($p \in [p_{b2},1]$), let

$$D_1 = \frac{1}{2} - \frac{k-1}{4}\sqrt{\frac{2(1-p)}{k^2-2k+3}} = g(p) \tag{26}$$

and

$$\frac{\mathrm{d}g(p)}{\mathrm{d}p} > 0. \tag{27}$$

Therefore, D_1 also increases monotonically with p in the high-power range. At the power boundary p_{b2}, it holds that

$$D_1 = f(p_{b2}) = \frac{k+1}{4k}. \tag{28}$$

and

$$g(p_{b2}) = \frac{k+1}{4k} = f(p_{b2}). \tag{29}$$

Therefore, D_1 is continuous for p in the whole power range.

To further illustrate the monotonic relationship between D_1 and p, the variations of D_1, D_2, and D_3 with respect to p are plotted in Fig. 6. As observed in Fig. 6, D_1 exhibits a globally monotonic relationship with p. For any given power level p, achieving the corresponding value of D_1 ensures reaching the desired p. Therefore, p can be replaced by D_1.

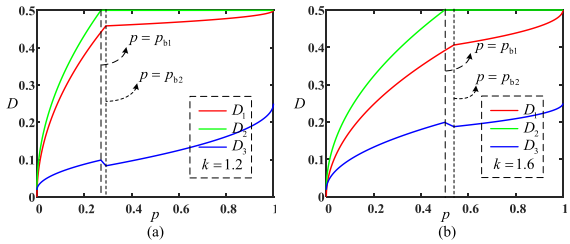

Fig. 6. Curve of the relation between free variables D_1, D_2, D_3, and p. (a) $k = 1.2$. (b) $k = 1.6$.

From (23), we obtain the following.

For $p \in [0, p_{b2}]$

$$p = \frac{8(k^2+2k-3)D_1^2}{(k+1)^2}. \tag{30}$$

For $p \in [p_{b2}, 1]$

$$p = 1 - \frac{8(k^2-2k+3)(0.5-D_1)^2}{(k-1)^2}. \tag{31}$$

Substituting (30) and (31) into the expressions for D_2 and D_3 in (23), (23) can be further simplified to

$$\begin{cases} D_2 = \begin{cases} \frac{2kD_1}{k+1} + 2i'_{\mathrm{ZVS2}} & (0 \le D_1 \le f(p_{b1})) \\ \frac{1}{2} & (f(p_{b1}) \le D_1 \le \frac{1}{2}) \end{cases} \\ D_3 = \begin{cases} \frac{2(k-1)D_1}{k+1} + 2i'_{\mathrm{ZVS2}} & (0 \le D_1 \le f(p_{b1})) \\ \frac{1}{2} - \frac{2D_1}{k+1} & (f(p_{b1}) \le D_1 \le g(p_{b2})) \\ \frac{3}{4} - \frac{2(k-2)D_1+1}{2(k-1)} & (g(p_{b2}) \le D_1 \le \frac{1}{2}) \end{cases} \end{cases} \tag{32}$$

where $f(p_{b1}) = \frac{(1-4i'_{\mathrm{ZVS}})(k+1)}{4k}$ and $g(p_{b2}) = \frac{k+1}{4k}$. Unlike (23), (32) eliminates the need for explicit power calculations to determine the duty cycles, thereby reducing computational complexity in the modulation process. This approach is referred to as the simplified duty cycle (SDD) scheme.

B. Comparison for Modulation Implementation of SDD (32) and Power-Based (23)

The modulation implementation system has three inputs: V_{in}, the target voltage V_{oref}, and the output voltage V_o of the DAB converter. Initially, V_{oref} and V_o are normalized and compared to compute the error $\Delta E = (V_{\mathrm{oref}} - V_o)/V_{\mathrm{oref}}$, which is then fed into a proportional–integral (PI) controller to determine O_p. The implementation of the SDD modulation scheme is illustrated in Fig. 7(a), where $D_1 = O_p$, and D_2 and D_3 are computed from (32) based on D_1. In contrast, the modulation scheme based on (23) computes D_1, D_2, and D_3 using power p, as depicted in Fig. 7(b).

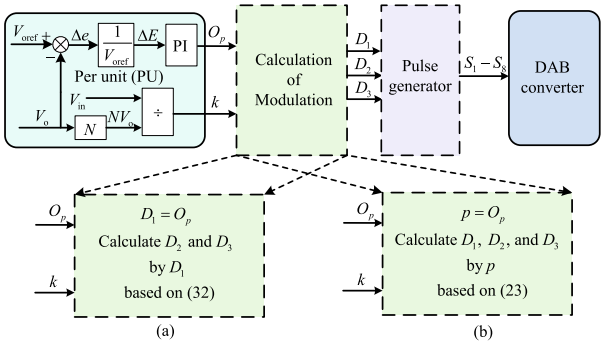

Fig. 7. Comparison of modulation implementation. (a) Calculation employing SDD scheme based on (32). (b) Calculation employing power-based method based on (23).

TABLE IV
COMPUTATIONAL TIME COMPARISON

Power Interval	Computational time of power-base method (23)	Computational time of SDD scheme (32)	Percentage reduction
$0 \le p \le p_{b1}$	8.35 μs	5.39 μs	35.45%
$p_{b1} \le p \le p_{b2}$	9.69 μs	7.1 μs	26.73%
$p_{b2} \le p \le 1$	9.79 μs	7.15 μs	29.97%

The SDD scheme can directly obtain D_1 from the PI controller. Compared to obtaining p through a PI controller to indirectly calculate D_1 as in (23), the SDD scheme reduces the need for division, square root, and other operations. Furthermore, the boundary points $f(p_{b1})$ and $g(p_{b2})$ in the SDD scheme are more concise than the boundary points p_{b1} and p_{b2} in (23). Therefore, the SDD scheme simplifies the complexity of modulation implementation.

C. Comparison of Computational Time

The computation time required to implement the modulation using both (23) (power-based method) and (32) (SDD scheme) on a CPU is given in Table IV. For $0 \le p \le p_{b1}$, the computation times for (23) and (32) are 8.35 and 5.39 μs, respectively. When $p_{b1} \le p \le p_{b2}$, the computation times are 9.69 and 7.1 μs, respectively, while for $p_{b2} \le p \le 1$, they are 9.79 and 7.15 μs, respectively. Compared to (23), the SDD scheme achieves reductions in computation time of 35.45%, 26.73%, and 29.97% across the three power intervals, demonstrating its efficiency in reducing the computational effort required for modulation implementation.

Remark 2: Compared to the 5-DoF scheme, the proposed MOATVM and SDD scheme significantly reduces the computation time for modulation implementation by over 40% at light-load conditions, primarily due to the elimination of numerous square root and division operations required in 5-DoF. This computational efficiency represents a key advantage of the proposed method over the 5-DoF.

TABLE V
SYSTEM PARAMETERS

Items	Descriptions	Values
V_{in}	Input Voltage	120 V
V_o	Output Voltage	120–75 V
N	Transformer Ratio	1:1
k	Mismatch Coefficient	1–1.6
L	Inductor	87 μH
f_s	Switching Frequency	50 kHz
C_1	Support Capacitor	1000 μF
C_2	Support Capacitor	1000 μF

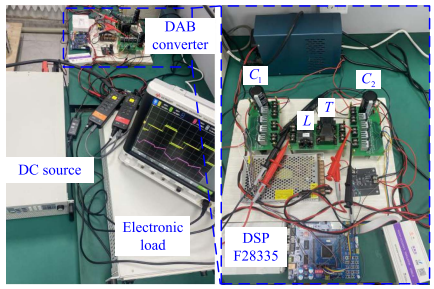

Fig. 8. Experimental system platform.

V. EXPERIMENTS AND ANALYSIS

The experimental platform is established based on the parameters listed in Table V, as illustrated in Fig. 8. The setup comprises a power source, an electronic load, a DSP28335 control board from Texas Instruments, a voltage sampler, and a DAB converter. The DAB converter consists of two full H-bridges incorporating SiC MOSFETs (SCT3060 from ROHM) and capacitors (C_1 and C_2), along with an inductor and an isolation transformer. Each of the two full H-bridges is equipped with dedicated drivers tailored for SiC MOSFETs. To verify the effectiveness of the proposed MOATVM and the SDD scheme, multiple experiments are conducted using six modulation strategies (SPS, FHA-TPS [12], CSM-TPS [16], UATPS [24], 5-DoF [20], and MOATVM + SDD) under different conditions with $k = 1.2$, $k = 1.4$, and $k = 1.6$.

A. Operating Waveforms of the MOATVM + SDD Scheme

Fig. 9 presents typical steady-state waveforms of v_{ab}, v_{cd}, and i_L under power variations employing the MOATVM + SDD with $k = 1.4$ as an example. Fig. 9(a)–(d) corresponds to power from 20 to 220 W with rms current from 0.509 to 2.952 A. The theoretical power boundary of low-power and high-power range can be calculated as $\frac{(k-1)(k+3)}{2k^2} \times \frac{NV_{in}V_o}{8f_sL} = 132.7$ W. Fig. 9(a) and (b) corresponding to 20 and 80 W belongs to the low-power range with characteristic of v_{cd} transiting from zero to high-level before v_{ab}. Fig. 9(c) and (d) corresponding to 160 and 220 W belongs to the high-power range with S_5 and S_8 turned ON simultaneously ($D_2 = 0.5$), lagging behind S_4. The results confirm the correctness of the MOATVM strategy and SDD method. Moreover, Fig. 10 demonstrates the dynamic waveforms of the MOATVM + SDD scheme. Specifically, Fig. 10(a) shows the dynamic response when the power changes from 30 to 170 W at

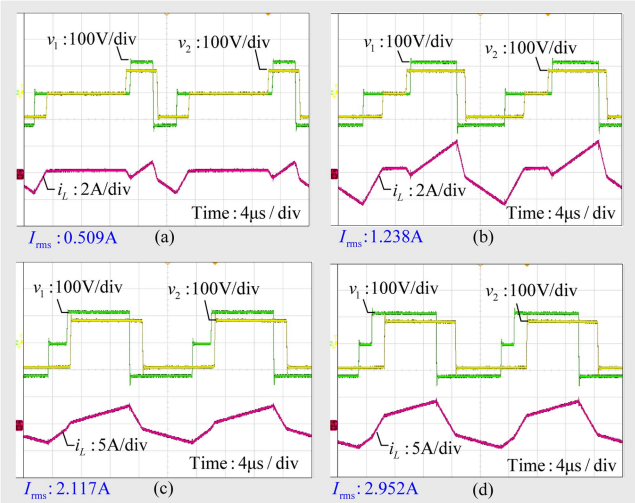

Fig. 9. Waveforms of v_{ab}, v_{cd}, and i_L under the MOATVM + SDD with $k = 1.4$. (a) 20 W. (b) 80 W. (c) 160 W. (d) 220 W.

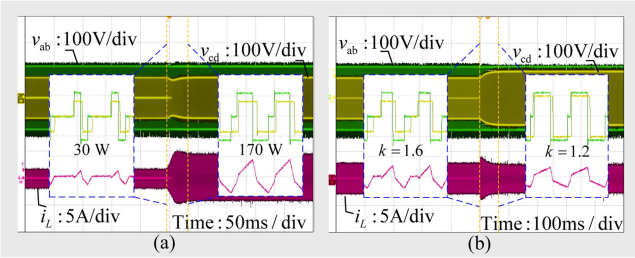

Fig. 10. Dynamic waveforms of the MOATVM + SDD scheme. (a) Power changes from 30 to 170 W at $k = 1.6$. (b) k changes from 1.6 to 1.2 at 70 Ω.

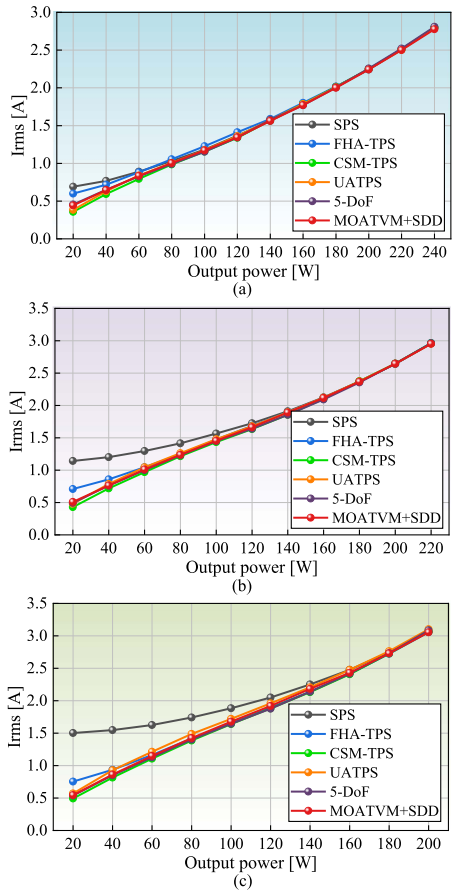

Fig. 11. Comparison of rms current experimental values for six modulation strategies. (a) $k = 1.2$. (b) $k = 1.4$. (c) $k = 1.6$.

$k = 1.6$, while Fig. 10(b) presents the dynamic behavior when k changes from 1.6 to 1.2 under a 70 Ω load. Fig. 10(a) and 10(b) operates in mode I before the transient and switches to mode III after the transition, indicating that the converter maintains stable operation under both power and voltage variations while continuing to implement the optimized modulation scheme.

B. Comparison of RMS Current

To comprehensively compare rms current performance, the experimental rms values for SPS, FHA-TPS [12], CSM-TPS [16], UATPS [24], 5-DoF [20], and MOATVM + SDD at $k = 1.2$, $k = 1.4$, and $k = 1.6$ are shown in Fig. 11. As can be observed in Fig. 11, the following general patterns can be obtained: under light load conditions, SPS exhibits the highest rms current and FHA-TPS has a moderate rms current, while CSM-TPS demonstrates the lowest rms current, with UATPS, 5-DoF, and MOATVM + SDD slightly higher than CSM-TPS. As the power increases, the difference in rms currents among the modulation strategies gradually diminishes until they eventually converge. The results of rms currents indicate that, compared to SPS, the other five modulation strategies can reduce the rms current, with CSM-TPS, UATPS, 5-DoF, and MOATVM + SDD showing particularly effective reduction in rms current.

C. Comparison of Operating Waveforms and ZVS Situation

To highlight the advantages of MOATVM + SDD, a comparison of operating waveforms for six modulation strategies is conducted, as shown in Fig. 12–14. Fig. 12 presents the waveforms of SPS, FHA-TPS [12], CSM-TPS [16], UATPS [24], 5-DoF [20], and MOATVM + SDD at $k = 1.2$ and 40 W, representing a low-power range case. Regarding ZVS performance, SPS, FHA-TPS, CSM-TPS, UATPS, 5-DoF, and MOATVM + SDD enable ZVS for 4, 6, 2, 4, 6, and 7 switches, respectively. Similarly, the numbers of switches achieving ZVS under six modulation strategies at $k = 1.6$ and 40 W are 4, 6, 2, 4, 6, 7, respectively, as shown in Fig. 13. From Figs. 12 and 13, it can be observed that under light-load conditions, FHA-TPS, 5-DoF, and MOATVM + SDD all perform well in terms of the number of ZVS achievements. However, similar to SPS, the secondary-side voltage v_2 of FHA-TPS operates at full duty cycle, which leads to higher transformer core loss. In contrast, CSM-TPS, UATPS, 5-DoF, and MOATVM + SDD can effectively reduce the rms current while maintaining a smaller voltage duty cycle, meaning they generate lower transformer core losses.

Building upon the achievement of both low rms current and low duty cycle operation, CSM-TPS, UATPS, 5-DoF, and MOATVM + SDD demonstrate progressively increasing numbers of ZVS realizations in the given order. Consequently,

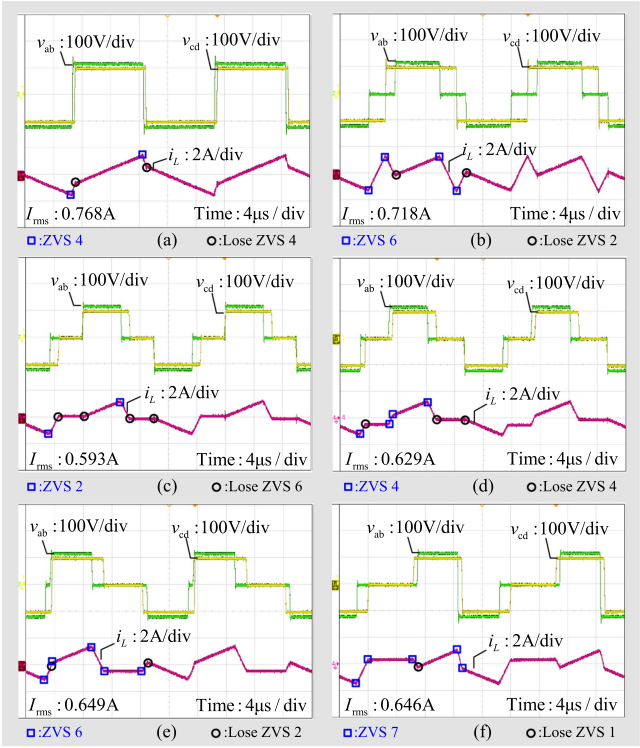

Fig. 12. Waveforms of v_{ab}, v_{cd}, and i_L under six modulation strategies at $k = 1.2$ and 40 W. (a) SPS. (b) FHA-TPS [12]. (c) CSM-TPS [16]. (d) UATPS [24]. (e) 5-DoF [20]. (f) MOATVM + SDD.

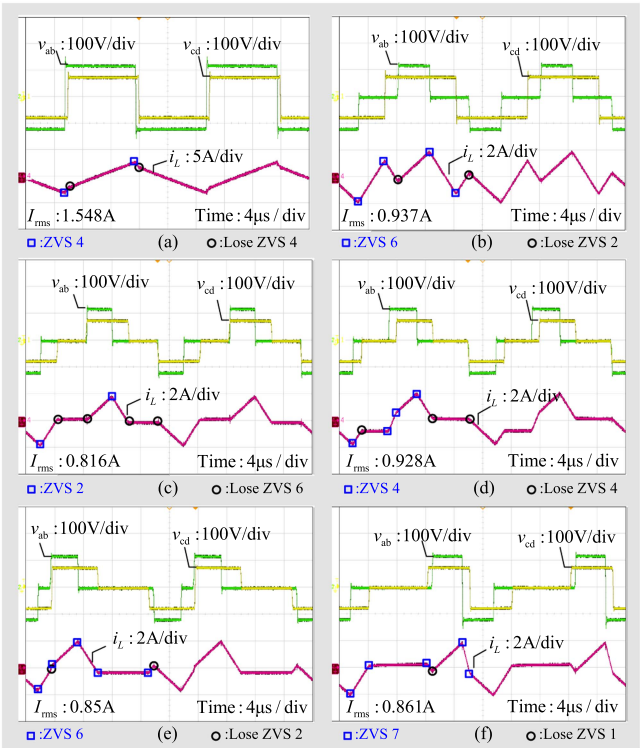

Fig. 13. Waveforms of v_{ab}, v_{cd}, and i_L under six modulation strategies at $k = 1.6$ and 40 W. (a) SPS. (b) FHA-TPS [12]. (c) CSM-TPS [16]. (d) UATPS [24]. (e) 5-DoF [20]. (f) MOATVM + SDD.

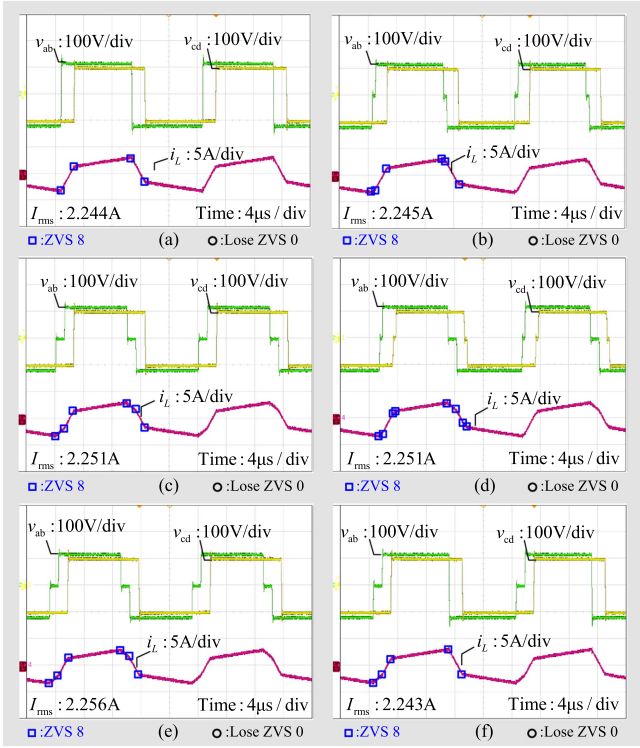

Fig. 14. Waveforms of v_{ab}, v_{cd}, and i_L under six modulation strategies at $k = 1.2$ and 200 W. (a) SPS. (b) FHA-TPS [12]. (c) CSM-TPS [16]. (d) UATPS [24]. (e) 5-DoF [20]. (f) MOATVM + SDD.

MOATVM + SDD exhibits superior overall performance under light-load conditions

Fig. 14 presents the waveforms of the six modulation strategies at 200 W, representing a case in the high-power range. All six modulation strategies exhibit similar RMS current, voltage duty cycle and achieve ZVS for all eight switches, indicating that their performance is comparable in the high-power range.

D. Experimental Validation of ZVS Waveforms

Furthermore, the waveforms of gate-source voltage (v_{gs}) and drain-source voltage (v_{ds}) employing MOATVM + SDD at the power point in Fig. 12(f) are shown in Fig. 15 to verify ZVS implementation. As depicted in Fig. 15, v_{gs} for S_1–S_3 and S_5–S_8 rises from zero after v_{ds} decreases to zero, confirming that these switches achieve ZVS, while only one switch (S_4) fails to achieve ZVS. This observation aligns well with the results in Fig. 12(f).

E. Efficiency and Power Loss Analysis

Fig. 16 presents the efficiency curves for SPS, FHA-TPS [12], CSM-TPS [16], UATPS [24], 5-DoF [20], and MOATVM + SDD under varying power levels for $k = 1.2$, $k = 1.4$, and $k = 1.6$. Across different k values, MOATVM + SDD consistently achieves the highest efficiency under light loads, while SPS has the lowest. FHA-TPS improves upon SPS but remains inefficient, whereas CSM-TPS performs better but still lags behind MOATVM + SDD due to limited ZVS performance. Since UATPS only achieves ZVS on four switches under light-load

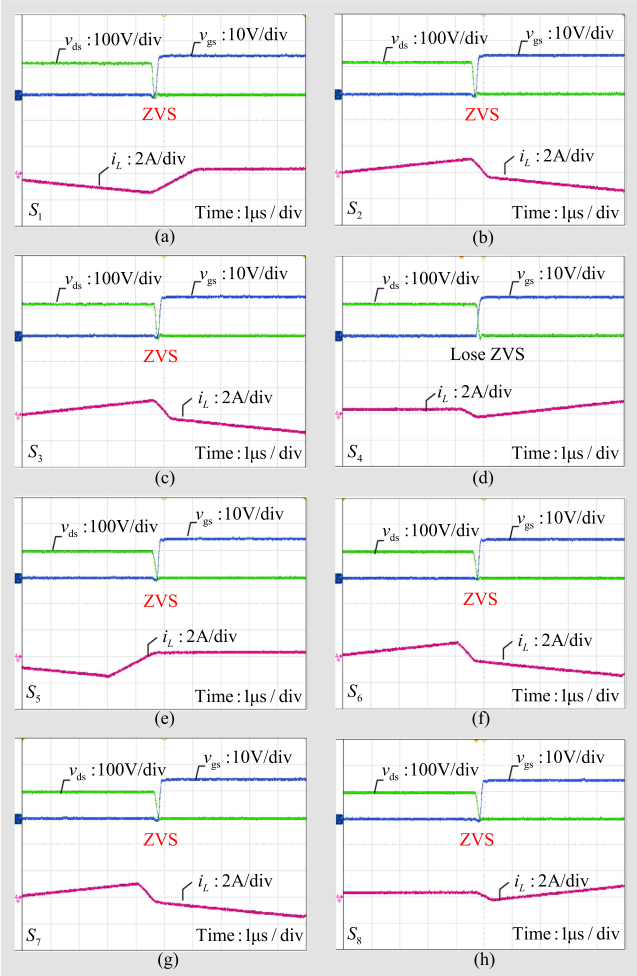

Fig. 15. Waveforms of v_{gs} and v_{ds} for S_1–S_8 corresponding to Fig. 12(f). (a) S_1. (b) S_2. (c) S_3. (d) S_4. (e) S_5. (f) S_6. (g) S_7. (h) S_8.

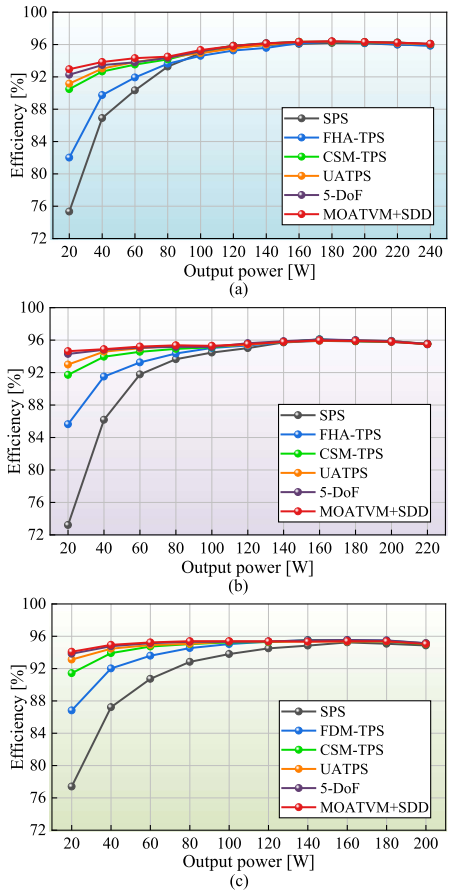

Fig. 16. Efficiency curves of four modulation strategies for different k. (a) $k = 1.2$. (b) $k = 1.4$. (c) $k = 1.6$.

conditions, its efficiency is also lower than that of MOATVM + SDD. In contrast, 5-DoF achieves ZVS on six switches, resulting in efficiency comparable to MOATVM + SDD. By building upon three modulation degrees of freedom, MOATVM + SDD achieves light-load efficiency on par with 5-DoF while surpassing that of other 3-DoF modulation strategies. The efficiency gains of MOATVM + SDD over SPS, FHA-TPS, CSM-TPS, and UATPS reach up to 17.603%, 10.938%, 2.469%, and 1.785% for $k = 1.2$, 21.414%, 9.014%, 2.923%, and 1.644% for $k = 1.4$, and 16.678%, 7.257%, 2.646%, and 0.971% for $k = 1.6$. As the load increases, the efficiencies of all six strategies converge, indicating comparable high-power performance. The results confirm the superior efficiency of MOATVM + SDD, demonstrating the effectiveness of the proposed MOATVM and SDD schemes.

Power loss analysis provides deeper insights into efficiency performance. The main power losses in a DAB converter include conduction loss, switching loss, and core loss [9].

1) Conduction losses are determined by the ON-state resistance of the switches, the winding resistance of the inductor and transformer, and the rms current, i.e.,

$$P_{\text{con}} = [(2 + 2N^2)R_{\text{on}} + R_{\text{L}} + R_{\text{Tp}} + N^2 R_{\text{Ts}}]I_{\text{rms}}^2 \tag{33}$$

where R_{on} represents the ON-state resistance of single switch, R_L is the winding resistance of the inductor, R_{Tp} denotes the primary-side winding resistance of the transformer, R_{Ts} is the secondary-side winding resistance of the transformer, and I_{rms} is the rms current.

2) Switching losses are determined by the turn-ON energy (E_{on}), turn-OFF energy (E_{off}), and the switching frequency (f_s) [25], i.e.,

$$P_{\text{sw}} = (E_{\text{on}} + E_{\text{off}})f_s \tag{34}$$

where E_{on} and E_{off} can be obtained through simulations using LTspice software.

3) Core losses can be calculated using the Steinmetz equation [26], i.e.,

$$P_{\text{core}} = V_{\text{core}} K f_{\text{s}}^{\alpha} B_{\text{m}}^{\beta} \tag{35}$$

where V_{core} is the core volume, K, α, and β are Steinmetz coefficients, and B_{m} is the peak magnetic flux density. The magnetic flux density for the inductor and transformer can be expressed as follows:

$$B_{\text{mL}} = \frac{LI_{\text{p}}}{n_{\text{L}} S_{\text{L}}} \tag{36}$$

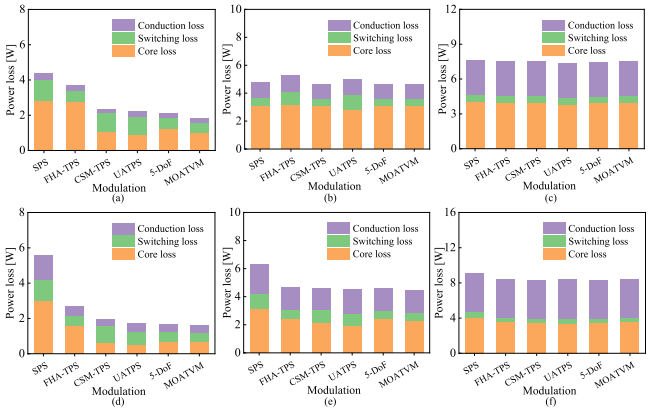

Fig. 17. Power loss analysis at $k = 1.2$ and 1.6. (a) $k = 1.2$ and 40 W. (b) $k = 1.2$ and 120 W. (c) $k = 1.2$ and 200 W. (d) $k = 1.6$ and 40 W. (e) $k = 1.6$ and 100 W. (f) $k = 1.6$ and 180 W.

where I_{p} is the peak current, n_{L} is the inductor turns, and S_{L} is the cross-sectional area of the inductor core.

$$B_{\mathrm{mT}} = \frac{V_{\mathrm{orms}}}{4.44 f_{\mathrm{s}} n_{\mathrm{T}} S_{\mathrm{T}}} \tag{37}$$

where V_{orms} is the root-mean-square value of the secondary-side voltage, n_{T} represents the transformer turns, and S_{T} is the cross-sectional area of the transformer core.

Taking $k = 1.2$ and 1.6 as examples, the power losses are calculated and represented in Fig. 17. Purple, green, and orange represent conduction loss, switching loss, and core loss, respectively. As shown in Fig. 17, the proposed MOATVM and SDD scheme consistently exhibit lower total power loss than other modulation methods at light load, primarily attributable to its significant reduction in switching losses through extended ZVS range and reduced conduction and core losses [see Fig. 17(a) and (d)]. With increasing output power, the loss difference among different strategies gradually narrows [see Fig. 17(b) and (e)], and at high power levels, the loss profiles converge to nearly identical values [see Fig. 17(c) and (f)]. These results confirm that the proposed method not only provides a distinct advantage under light-load conditions but also maintains comparable performance with existing approaches at high power, thereby demonstrating general applicability across the entire operating range. The power loss analysis aligns well with the efficiency test results.

F. Comprehensive Comparison

Based on a comprehensive comparison with existing optimization methods summarized in Table VI, the proposed MOATVM and SDD scheme demonstrates significant advantages in multiple dimensions. Compared to FHA-TPS and CSM-TPS, the proposed method achieves a wide ZVS range while maintaining low rms current. In addition, the FHA-TPS optimization solution involves trigonometric operations, resulting in a substantial computational burden. Compared to UATPS, the proposed method expands the ZVS range from four to seven switches under light-load conditions while maintaining comparable rms current characteristics. Although 5-DoF modulation exhibits comparable ZVS performance, it requires five optimization variables and complex boundary conditions, resulting in substantial computational overhead. In contrast, the proposed scheme utilizes only three variables and eliminates the need for duty cycle calculation through power mapping, significantly reducing computational complexity. These improvements collectively contribute to the superior efficiency performance of the proposed approach, achieving an optimal balance between computational complexity and optimization performance.

TABLE VI
COMPREHENSIVE COMPARISON WITH EXISTING OPTIMIZATION METHODS

Dimension of evaluation	[12]	[16]	[24]	[20]	This work
Model	FDM	TDM	TDM	TDM	TDM
Modulation	TPS	TPS	UATPS	5-DoF	MOATVM + SDD
Number of variables	3	3	3	5	3
Optimization objective	RMS current	Peak current	Peak current	Peak current +ZVS	Peak current +ZVS
RMS current	Middle	Low	Low	Low	Low
ZVS range	Wide	Narrow	Middle	Wide	Wide
Computation	Large	Middle	Middle	Large	Middle
Efficiency	Middle	Middle	Middle	High	High

VI. CONCLUSION

In this article, an MOATVM strategy is proposed with ZVS boundary conditions to optimize peak-to-valley current, aiming to improve the light-load efficiency of DAB converters. By minimizing peak-to-valley current as a proxy for rms current, conduction losses are indirectly reduced, while the introduced ZVS constraints can reduce switching losses. Subsequently, an SDD scheme eliminating the need for power-based duty cycle calculations is developed, which can simplify modulation implementation complexity and reduce the computation time by 35.45%, 26.73%, and 29.97% across three power intervals, compared to the power-based calculation method. Finally, extensive comparative experiments with SPS, FHA-TPS [12], CSM-TPS [16], UATPS [24], and 5-DoF [20] demonstrate that the proposed MOATVM strategy achieves both wide ZVS range and low rms current. Building upon a more easily implementable 3-DoF framework, the MOATVM and SDD scheme deliver efficiency performance comparable to the 5-DoF modulation, while providing better efficiency improvement compared to other modulation schemes. At $k = 1.2$, MOATVM and SDD achieve efficiency gains of up to 17.603%, 10.938%, 2.469%, and 1.785% over SPS, FHA-TPS, CSM-TPS, and UATPS, respectively. For $k = 1.4$ and $k = 1.6$, improvements reach 21.414%, 9.014%, 2.923%, and 1.644%, and 16.678%, 7.257%, 2.646%, and 0.971%, respectively.

In summary, the combination of the MOATVM strategy and the SDD scheme not only enhances system efficiency but also

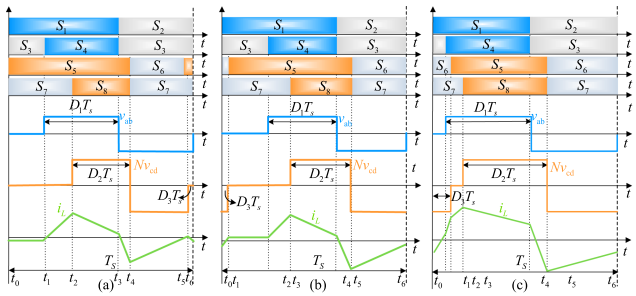

Fig. 18 Typical switching signals and outputs under the MOATVM when $k<1$. (a) Mode I. (b) Mode II. (c) Mode III.

reduces the modulation computational time, enhancing the overall performance of DAB converters compared to several existing modulation strategies.

Appendix

Fig. 18 shows the modulation diagram for the case of $k<1$. In this situation, adding ZVS constraints for the primary-side switches allows seven switches to achieve ZVS under light load. Using the same analytical method as presented in this article, mode I is adopted for light load and mode III for heavy load. For the condition of $k<1$, the optimal solution of MOATVM is given by (38). Since D_2 maintains a globally monotonic relationship with p, it can be used as a substitute for p. Ultimately, the optimization solution of the proposed MOATVM and SDD scheme for $k<1$ is given by (40).

$$\begin{cases} D_1 = \begin{cases} \frac{1}{2}\sqrt{\frac{2p}{1+2k-3k^2}} + \frac{2i'_{\mathrm{ZVS1}}}{k} & (0 \le p \le p_{b1}) \\ \frac{1}{2} & (p_{b1} \le p \le 1) \end{cases} \\ D_2 = \begin{cases} \frac{k+1}{4}\sqrt{\frac{2p}{1+2k-3k^2}} & (0 \le p \le p_{b2}) \\ \frac{1}{2} + \frac{k-1}{4}\sqrt{\frac{2(1-p)}{3k^2-2k+1}} & (p_{b2} \le p \le 1) \end{cases} \\ D_3 = \begin{cases} \frac{2i'_{\mathrm{ZVS1}}}{k} & (0 \le p \le p_{b1}) \\ \frac{1}{2} - \frac{1}{2}\sqrt{\frac{2p}{1+2k-3k^2}} & (p_{b1} \le p \le p_{b2}) \\ \frac{1}{4} - \frac{1}{4}\sqrt{\frac{2(1-p)}{3k^2-2k+1}} & (p_{b2} \le p \le 1) \end{cases} \end{cases} \tag{38}$$

where

$$p_{b2} = \frac{\left(k-4i'_{\mathrm{ZVS1}}\right)^2\left(1+2k-3k^2\right)}{2k^2},$$
$$p_{b3} = \frac{1+2k-3k^2}{k^2} \tag{39}$$

$$\begin{cases} D_1 = \begin{cases} \frac{2D_2}{k+1} + \frac{2}{k}i_{\mathrm{ZVS1}} & \left(0 \le D_2 \le \frac{(k+1)(k-4i_{\mathrm{ZVS1}})}{4}\right) \\ \frac{1}{2} & \left(\frac{(k+1)(k-4i_{\mathrm{ZVS1}})}{4} \le D_2 \le \frac{1}{2}\right) \end{cases} \\ D_3 = \begin{cases} \frac{2}{k}i_{\mathrm{ZVS1}} & \left(0 \le D_2 \le \frac{(k+1)(k-4i_{\mathrm{ZVS1}})}{4}\right) \\ \frac{1}{2} - \frac{2D_2}{k+1} & \left(\frac{(k+1)(k-4i_{\mathrm{ZVS1}})}{4} \le D_2 \le \frac{k+1}{4}\right) \\ \frac{1}{4} - \frac{0.5-D_2}{1-k} & \left(\frac{k+1}{4} \le D_2 \le \frac{1}{2}\right). \end{cases} \end{cases} \tag{40}$$

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Hao Li received the B.S. degree in electrical engineering and automation in 2021 from Northeastern University, Shenyang, China, where he is currently working toward the Ph.D. degree in electrical engineering with the College of Information Science and Engineering.

His research interests include the optimization of modulation and control strategies for dc–dc converters.

Chonghui Song (Member, IEEE) received the B.S. degree in energy and power engineering from Xi'an Jiaotong University, Xi'an, China, in 1996, and the M.S. and Ph.D. degrees in control theory and control engineering from Northeastern University, Shenyang, China, in 1999 and 2004, respectively.

From 2006 to 2008, he was a Visiting Scholar with the Department of Electrical and Computer Engineering, University of Illinois at Chicago. He is currently a Professor with the College of Information Science and Engineering, Northeastern University. His research interests include power electronics and optimal control.

Wenbing Hu received the B.S. degree in electric engineering in 2021 from the College of Information Science and Engineering, Northeastern University, Shenyang, China, where he is currently working toward the Ph.D. degree in electric engineering.

His research interests include power electronics, ac motor drives, and dc–dc converters.

Guangdi Li (Member, IEEE) received the B.E.E. degree in electrical engineering from the College of Information Science and Engineering, Northeastern University, Shenyang, China, in 2013, and the Ph.D. degree in power electronics and electric drive from the College of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2020.

He is currently an Associate Professor with the College of College of Information Science and Engineering, Northeastern University. His current research interests include resonant dc–dc converters, renewable energy generation, and its control technology. He has authored or coauthored more than 15 SCI or EI indexed papers.

Dr. Li is a Member of IEEE PES Intelligent Grid and Emerging Technologies Satellite Committee-China. He was the recipient of the first prize of science and technology progress award of Chinese Association of Automation and the second prize of science and technology progress award of China Machinery Industry Federation. He is also an Active Reviewer of some peer reviewed journals and international conferences.

Dongsheng Yang (Senior Member, IEEE) received the B.S. degree in testing technology and instrumentation, the M.S. degree in power electronics and electric drives, and the Ph.D. degree in control theory and control engineering from Northeastern University, Shenyang, China, in 1999, 2004, and 2007, respectively.

He is currently a Professor with Northeastern University. His work was supported by the Program for New Century Excellent Talents in University. He has authored or coauthored around 100 papers published in academic journals and conference proceedings, three monographs, and coinvented 80 patents. His current research interests include distributed generation and multienergy power system, and artificial intelligence-based fault diagnosis and protection.

Dr. Yang was the recipient of the Second Prize of National Science and Technology Progress.

Nie Hou (Member, IEEE) received the B.Sc. and M.Sc. degrees (Hons.) in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2014 and 2017, respectively, and the Ph.D. degree in electrical engineering from the University of Alberta, Edmonton, AB, Canada, in 2022.

From 2022 to 2024, he was a Postdoctoral Fellow with the University of Alberta. Since then, he has been a distinguished professor with Tianjin University, Tianjin, China. His current research interests include power systems driven power electronics, distributed generation, and microgrid. He has authored or coauthored more than 60 refereed papers and holds five Chinese patents.

Dr. Hou is currently the Topic Chair at the 14th IEEE Energy Conversion Congress and Exposition, and the Reviewing Chair and the Session Chair at the 10th International Power Electronics and Motion Control Conference. He was the recipient of the Outstanding Author Award from the Proceeding of the Chinese Society for Electrical Engineering in 2016, IAS Sustainable and Renewable Energy Conversion System Committee Conference Paper Awards in 2021, the Best Presenter at the 2nd International Power Electronics and Application Symposium in 2023, and the Best Special Session Chair Award at the 10th International Power Electronics and Motion Control Conference in 2024. He is recognized as 2022 World's Top 2% Scientists by Stanford University.

Wei Xu (Fellow, IEEE) received the double B.E. and M.E. degrees in electrical engineering from Tianjin University, Tianjin, China, in 2002 and 2005, respectively, and the Ph.D. degree in electrical engineering from the Institute of Electrical Engineering, Chinese Academy of Sciences (IEECAS), Beijing, China, in 2008.

From 2008 to 2012, he was a Postdoctoral Fellow with the University of Technology Sydney, Ultimo, NSW, Australia, the Vice-Chancellor Research Fellow with the Royal Melbourne Institute of Technology, Melbourne, VIC, Australia, and a Japan Science Promotion Society Invitation Fellow with Meiji University, Tokyo, Japan, respectively. From 2013 to 2023, he was a Professor with the Huazhong University of Science and Technology, Wuhan, China. Since 2024, he has been a Professor with IEECAS and Director for State Key Laboratory. His research interests include the design and control of linear machines and drives.

Dr. Xu is a Fellow of the Institute of Engineering and Technology. He was the General Chair of 2021 International Symposium on Linear Drives for Industry Applications and 2023 IEEE International Conference on Predictive Control of Electrical Drives and Power Electronics. He is an Associate Editor of more than ten peer-reviewed IEEE Journals, including IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE TRANSACTIONS ON POWER ELECTRONICS.