A Monolithic GaN Laser Diode Driver With Steep-Edge Driving Current for LiDAR Transmitters Using a 3× Self-Circulating Charge Pump

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***Abstract*—Direct time-of-flight light detection and ranging is widely used for real-time, long-range three-dimensional sensing. It requires narrow optical pulses with high peak power to achieve high detection resolution and long range, imposing high demands on the laser diode driver (LDD) in the LiDAR transmitter. Monolithic GaN integration is well-suited for LDD design, as it minimizes gate-drive loop parasitics and offers devices with superior figures of merit. However, conventional GaN-based gate drivers suffer from limited driving capability due to the lack of suitable p-type devices. This article presents an FET-controlled LDD based on a 0.25-μm GaN-on-Silicon process. A 3× self-circulating charge pump and zero-voltage-drop fast-charging switches strengthen the predriver, enabling high-speed switching of the GaN control switch. Experimental results show that the proposed LDD achieves a 10 A peak driving current with fast edge transitions of 434 ps (rise) and 252 ps (fall). Dead time insertion and an ON-chip filtering capacitor suppress shoot-through current in the final stage of the predriver. The LDD exhibits an average power loss of 420 mW at 10 MHz and achieves a peak efficiency of 92.44% .**

***Index Terms*—3× self-circulating charge pump (3× SCCP), direct time-of-flight (dTof), GaN, laser diode driver (LDD), light detection and ranging (LiDAR), monolithic integration, zero-voltage-drop fast-charging (ZVFC) switch.**

I. Introduction

TIME-OF-FLIGHT (ToF) light detection and ranging (LiDAR) is a real-time three-dimensional sensing technology, which can be classified into indirect ToF (iToF) and direct ToF (dToF). iToF estimates the distance by measuring the phase shift between emitted and reflected optical signals, while dToF determines distance based on the time interval between them [1], [2], [3]. Compared with iToF, dToF enables longer-range detection and is widely adopted in advanced driver assistance systems, robotic navigation, and unmanned aerial vehicle mapping [12], [13].

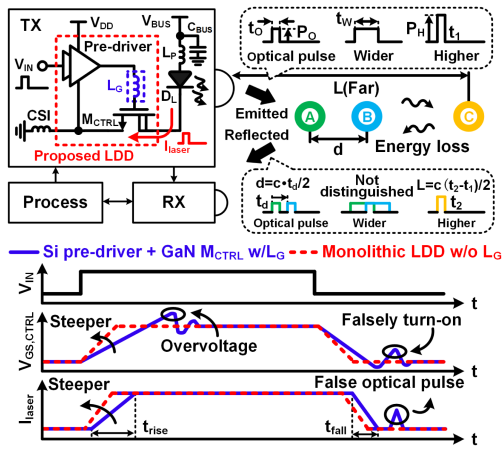

Fig. 1. Operating principles and design challenges of laser diode drivers in dToF LiDAR transmitter systems.

The operating principles of dToF LiDAR are shown at the top of Fig. 1. The transmitter (TX) emits optical pulses toward targets A, B, and C, while the receiver (RX) captures the reflections. The distance d between A and B is $d = c \times t_{\mathrm{d}} / 2$, where c is the speed of light (∼30 cm/ns), and t_{d} is the measured time interval. When the pulse width t_{w} exceeds t_{d}, reflections from A and B overlap, preventing the RX from distinguishing them. Therefore, narrower pulses are essential for higher detection resolution. To detect a distant target C, the emitted pulses must have sufficiently high peak power P_{H} to compensate for propagation loss. Additionally, to meet eye-safety regulations, the energy of the emitted pulse must stay below the eye-safe limit. This requires that the pulses achieve the desired peak power while maintaining the narrowest possible pulse width [14], [15]. In the TX, the shape of the optical pulse emitted by the laser diode $\mathrm{D_L}$ is mainly determined by the driving current I_{laser} generated by the laser diode driver (LDD), which consists of a predriver and a control switch $\mathrm{M_{CTRL}}$.

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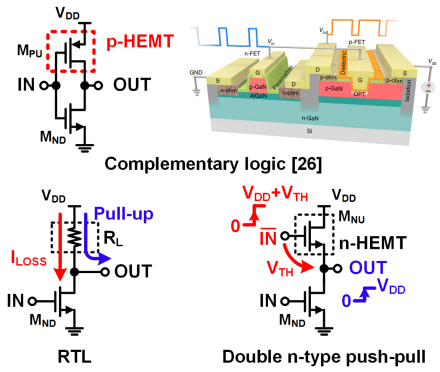


Fig. 2. Schematic of the GaN Complementary logic [26], resistor-transistor logic, and double n-type push–pull.

Based on Si process platforms, the LDDs reported in [4] and [5] employ controlled current source and double pulse overlapping techniques to achieve a high peak I_{laser} with a large slew rate $\text{d}I_{\text{laser}}/dt$. The mature Si process enables monolithic integration of functions such as real-time adaptive current control and switching regulation [4], [6]. However, the LDDs' driving capability is limited by the high figure of merit (FOM, defined as $Q_{\text{G}} \times R_{\text{ON}}$) of the LDMOS devices. The works in [7], [8], and [9] employ GaN devices with lower FOMs as M_{CTRL}. However, discrete Si-based predrivers introduce significant parasitic inductance L_{G} in the gate-drive loop. As shown at the bottom of Fig. 1, L_{G} degrades M_{CTRL} turn-ON speed and increases I_{laser} rise time. Ringing on the rising edge of V_{GS} may induce gate overvoltage, whereas ringing on the falling edge may unintentionally turn M_{CTRL} back on, resulting in false driving current pulses.

To mitigate these effects, Bettini et al. [10], [11] monolithically integrated the predriver and M_{CTRL} on the GaN process platform, taking advantage of the planar structure of GaN devices to minimize L_{G} [16], [17]. The GaN-on-SOI platform eliminates the back-gating effect, enabling monolithic integration of the GaN half-bridge with auxiliary circuits, thereby suppressing parasitic inductance and facilitating high-frequency operation [18], [19], [20]. The predriver can be implemented using a tapered inverter chain [21], [22], [23]. As shown in Fig. 2, complementary logic is widely adopted in Si process platforms due to its superior energy efficiency. However, in GaN process platforms, the hole mobility of p-type devices ($<$50 $\text{cm}^2(\text{V}\cdot\text{s})^{-1}$) is much lower than the mobility of two-dimension electron gas (2DEG) in n-type devices ($\sim$2000 $\text{cm}^2(\text{V}\cdot\text{s})^{-1}$). Consequently, GaN complementary logic is inadequate for supporting high-speed operation [24], [25], [26], [27]. In [25] and [28], the resistor-transistor logic inverter employs a resistor to pull up the output OUT. When OUT is low, a static current causes extra power dissipation. In a direct coupled FET logic inverter [29], [30], a gate-source shorted depletion-mode (d-mode) device serves as a current source to enhance pull-up capability, though a tradeoff with power consumption remains. The double n-type push–pull topology employs an enhancement-mode (e-mode) device to pull up OUT, but requires a higher voltage to fully turn it ON, which can be supplied by a charge pump [31], [32], [33] or an additional power rail [34].

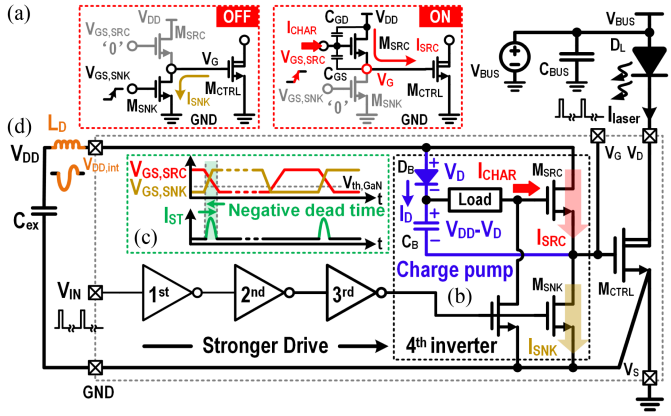


Fig. 3. Challenges of GaN-based monolithic LDDs. (a) Limited pull-up capability of the predriver. (b) Voltage loss and reduced replenish speed of the charge pump capacitor. (c) Negative dead time between the pull-up transistor M_{SRC} and the pull-down transistor M_{SNK} in the last inverter stage. (d) Drop of the internal power rail $V_{\text{DD,int}}$ due to parasitic inductance L_{D}.

This article proposes an FET-controlled LDD based on the GaN-on-Silicon platform to generate narrow optical pulses with high peak power. The discharge capacitor C_{BUS} is sufficiently large to store much more charge than consumed by I_{laser} in each period. The process platform used in this work provides four types of devices: 1) 2DEG resistors, 2) metal-insulator-metal (MIM) capacitors, 3) low-voltage (LV) e-mode n-type GaN HEMTs, and 4) high-voltage (HV) e-mode n-type GaN HEMTs.

The rest of this article is organized as follows. Section II discusses the design challenges and analyzes techniques to enhance driving capability. Section III presents the system architecture and circuit implementation of the proposed LDD. Section IV provides the experimental results. Finally, Section V concludes this article.

II. Design Challenges and Operation Strategies

As illustrated in Fig. 3, the proposed GaN-based monolithic LDD comprises a four-stage cascaded inverter chain. The driving capability progressively increases from the first to the fourth stage, effectively converting the input logic signal V_{IN} into the gate control signal V_{G} for M_{CTRL}. Even-numbered stages balance the propagation delays of the rising and falling edges between V_{IN} and V_{G}, thereby minimizing pulse-width distortion. All stages adopt a dual n-type push–pull topology to reduce static power consumption. Charge pumps supply the gate drive voltages for the pull-up transistors, enabling rail-to-rail output. The fourth-stage inverter is presented as an example to illustrate the detailed circuit structure.

Fig. 3 highlights four challenges in designing GaN-based monolithic LDDs. The first concerns the limited pull-up capability of the predriver, which is mainly determined by the fourth-stage inverter. As shown at the top of Fig. 3, during the turn-ON process of M_{CTRL}, the pull-up transistor M_{SRC} provides the pull-up current I_{SRC}. Turning on M_{SRC} requires a gate-to-source voltage $V_{\text{GS,SRC}}$ with respect to the floating voltage V_{G}. Additionally, the gate charging current I_{CHAR} of M_{SRC} should be sufficiently high to ensure rapid turn-ON of M_{SRC} and a steep rising edge at V_{G}. Therefore, the gate charging

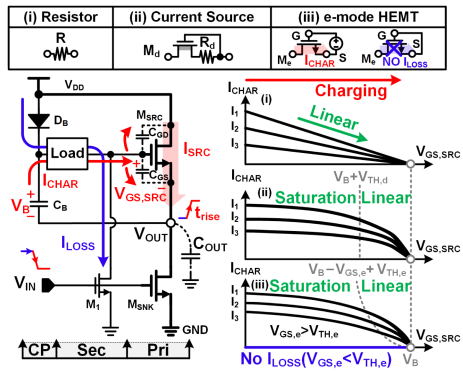


Fig. 4. Comparison of pull-up capabilities of inverter structures employing resistors, current sources, or e-mode HEMTs as loads.

circuit of M_{SRC} must be carefully designed to satisfy these requirements.

The second challenge lies in the voltage loss and limited replenish speed of the charge pump capacitor. During the replenishing process of C_B, the voltage across C_B is limited to $V_{DD} - V_D$, where V_D is the forward voltage drop across D_B. In FET-controlled dToF LiDAR, the high-level duty cycle of V_{IN} is typically very low, resulting in a limited time window for replenishing the pump capacitors in the first- and third-stage inverters. Therefore, a high charging current I_D is required to ensure sufficient voltage buildup.

While the first two challenges concern the driving capability of the predriver, the third focuses on power dissipation and long-term device reliability. As shown by the green dashed box in Fig. 3, a negative dead time exists between M_{SRC} and M_{SNK} in the fourth-stage inverter, causing a shoot-through current I_{ST}. To ensure strong pull-up and pull-down capability, both M_{SRC} and M_{SNK} in the fourth-stage inverter are designed with large aspect ratios, which exacerbates the magnitude of I_{ST}.

The fourth challenge arises from parasitic inductance L_D, introduced by PCB traces and packaging between the external filter capacitor C_{ex} and the V_{DD} pad. When M_{CTRL} is turned ON, the rapidly rising I_{SRC} generates a voltage drop across L_D, reducing the internal power rail $V_{DD,int}$. This drop may cause malfunction of the predriver and degrade its performance.

The following paragraphs present a detailed analysis of the pull-up capabilities of various inverter structures based on the GaN process platform, along with the influence of charge-pump voltage on inverter performance. The operating principles of the proposed techniques for addressing the challenges mentioned above are also systematically discussed.

A. Comparison of Inverter Structures Employing Resistors, Current Sources, and E-Mode HEMTs as Load Elements

Fig. 4 illustrates the charge-pump-assisted dual n-type push–pull inverter for LDD applications. The inverter comprises a primary path (consisting of M_{SRC} and M_{SNK}), a secondary path (consisting of load element and M_1) and a charge pump (CP, consisting of D_B and C_B). The primary path delivers the pull-up and pull-down currents to the output capacitance C_{OUT}, while the secondary path controls the switching behavior of M_{SRC}. The CP supplies the required gate-driving voltage to M_{SRC}, enabling the inverter output to reach V_{DD}.

When V_{IN} is high, M_1 is turned ON to turn OFF M_{SRC}, while M_{SNK} is turned ON to pull V_{OUT} low. Meanwhile, C_B is charged by V_{DD} through D_B. A static loss current I_{LOSS} flows through the load to ground, causing power dissipation. When V_{IN} is low, both M_1 and M_{SNK} are turned OFF, and C_B supplies I_{CHAR} to the gate of M_{SRC} through the load. A large I_{CHAR} is desirable to ensure the fast turn-ON of M_{SRC}, thereby enhancing the pull-up capability of the inverter. Since the load participates in both the I_{LOSS} and I_{CHAR} paths, there exists a trade-OFF between power consumption and pull-up capability. This tradeoff can be optimized by adjusting the load configuration. As illustrated at the top of Fig. 4, the load can be implemented using a resistor [32], a current source (consisting of a d-mode HEMT and a resistor) [31], or an e-mode HEMT [35]. Although d-mode HEMTs are not supported in the process platform adopted in this work, the resistor load can be readily replaced with a current-source load without modifying the inverter structure. Therefore, an analysis of the current-source load is presented to evaluate its potential advantages.

The output characteristics of the three load configurations are shown on the right side of Fig. 4. For the resistor load, I_{CHAR} decreases linearly with increasing $V_{GS,SRC}$, resulting in a gradual slowdown in the turn-ON process of M_{SRC}. For the current-source load, the d-mode HEMT M_d operates in the saturation region when $V_{GS,SRC} < V_B + V_{TH,d}$, where V_B is the voltage across C_B and $V_{TH,d}$ is the threshold voltage of M_d, thereby maintaining a nearly constant I_{CHAR} during most of the charging process. In both topologies, when V_{IN} is high, I_{LOSS} equals the initial I_{CHAR} at $V_{GS,SRC} = 0$, indicating a tradeoff between pull-up capability and power consumption.

For the e-mode HEMT load, similar to the current-source load, the e-mode HEMT M_e operates in the saturation region when $V_{GS,SRC} < V_B - V_{GS,e} + V_{TH,e}$, where $V_{TH,e}$ is the threshold voltage of M_e, keeping I_{CHAR} nearly constant during most of the charging process. The key difference is that I_{LOSS} can be eliminated by turning OFF M_e (i.e., when $V_{GS,e} < V_{TH,e}$) during the high level of V_{IN}.

The following paragraphs present a detailed analysis of the pull-up capabilities of inverters with three different load configurations.

1) Resistor Load: When V_{IN} is high, I_{LOSS} flows to ground through the resistor R, resulting in power dissipation. The value of I_{LOSS} can be calculated as follows:

$$I_{LOSS} = V_B/R. \tag{1}$$

The ON-resistance of M_1 is negligible compared to R. Critical waveforms during the pull-up process of the inverter are shown in Fig. 5(a), which can be divided into three phases. In the first phase, I_{CHAR} charges the gate input capacitance C_{ISS} (i.e., C_{GS} + C_{GD}) of M_{SRC}, raising the gate-to-source voltage $V_{GS,SRC}$ to $V_{TH,e}$, and turning ON M_{SRC}. In the second phase, the output voltage V_{OUT} begins to rise as M_{SRC} turns ON. The gate charging current of M_{SRC} during this phase is given as follows:

$$\begin{cases} I_{CHAR} = (V_B - V_{GS,SRC})/R \\ C_{GD} \times dV_{GD}/dt + C_{GS} \times dV_{GS,SRC}/dt = I_{CHAR} \end{cases}. \tag{2}$$

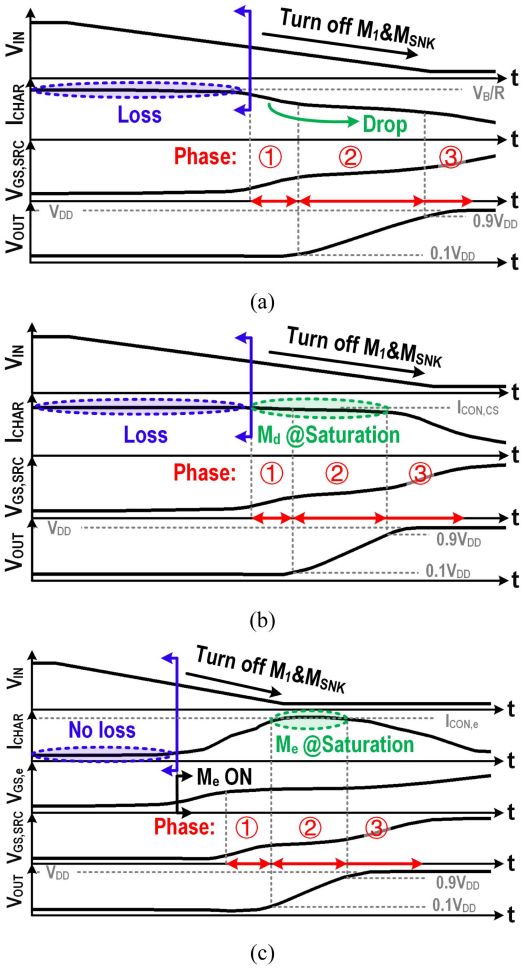


Fig. 5. Critical signals in the pull-up process of an inverter with (a) a resistor, (b) a current source, and (c) an e-HEMT as the secondary path load.

The relationship between the voltage slopes is given as follows:

$$dV_{\mathrm{OUT}}/dt + dV_{\mathrm{GS,SRC}}/dt = dV_{\mathrm{GD}}/dt. \tag{3}$$

During the rapid rise of V_{OUT}, C_{GD} is bootstrapped by C_{GS}, therefore, the current charging C_{GD} accounts for the majority of I_{CHAR}. As a result, $dV_{\mathrm{GS,SRC}}/dt$ can be neglected in comparison to dV_{GD}/dt and dV_{OUT}/dt. Consequently, (2) and (3) can be simplified as follows:

$$\begin{cases} I_{\mathrm{CHAR}} = \left(V_{\mathrm{B}} - V_{\mathrm{GS,SRC}}\right)/R \\ C_{\mathrm{GD}} \times dV_{\mathrm{GD}}/dt = I_{\mathrm{CHAR}} \end{cases} \tag{4}$$

$$dV_{\mathrm{OUT}}/dt = dV_{\mathrm{GD}}/dt. \tag{5}$$

By combining (4) and (5), the following equation can be derived:

$$dV_{\mathrm{OUT}}/dt = \left(V_{\mathrm{B}} - V_{\mathrm{GS,SRC}}\right)/\left(RC_{\mathrm{GD}}\right). \tag{6}$$

In the third phase, I_{CHAR} continues to charge the C_{ISS} of $\mathrm{M_{SRC}}$, allowing $V_{\mathrm{GS,SRC}}$ to rise fully to V_{DD}.

2) Current-Source Load: As shown in Fig. 5(b), when V_{IN} is high, $\mathrm{M_d}$ operates in the saturation region, and I_{LOSS} flows to ground through the current source. It is calculated as follows:

$$I_{\mathrm{LOSS}} = I_{\mathrm{CON,CS}}. \tag{7}$$

Here, $I_{\mathrm{CON,CS}}$ denotes the current provided by the current source. When V_{IN} transitions from high to low, the pull-up process is similar to that of the resistor-load case. During the second phase, as V_{OUT} rises, $\mathrm{M_d}$ operates in the saturation region, and I_{CHAR} primarily charges C_{GD}. Therefore, the following simplified equation can be similarly derived:

$$\begin{cases} I_{\mathrm{CHAR}} = I_{\mathrm{CON,CS}} \\ C_{\mathrm{GD}} \times dV_{\mathrm{GD}}/dt = I_{\mathrm{CHAR}} \end{cases}. \tag{8}$$

Combining (5) and (8), the following equation is obtained:

$$dV_{\mathrm{OUT}}/dt = I_{\mathrm{CON,CS}}/C_{\mathrm{GD}}. \tag{9}$$

3) E-Mode HEMT Load: As illustrated in Fig. 5(c), when V_{IN} is high, $\mathrm{M_e}$ is turned OFF, and I_{LOSS} is eliminated

$$I_{\mathrm{LOSS,e}} = 0. \tag{10}$$

When V_{IN} transitions from high to low, the pull-up process of the inverter is similar to that of an inverter with a current-source load. In the second phase, $\mathrm{M_e}$ operates in the saturation region and behaves as a current source, supplying a current $I_{\mathrm{CON,e}}$. Therefore, the turn-ON behavior of $\mathrm{M_{SRC}}$ in the inverter with an e-mode HEMT load closely resembles that of a current-source load case. The corresponding equation is

$$dV_{\mathrm{OUT}}/dt = I_{\mathrm{CON,e}}/C_{\mathrm{GD}}. \tag{11}$$

4) Compared to the Current-Source Load: The inverter with an e-mode HEMT load exhibits negligible I_{LOSS} when V_{IN} is high. Additionally, during the V_{IN} high-to-low transition, the turn-ON behavior of $\mathrm{M_{SRC}}$ is similar in both configurations. Therefore, the e-mode HEMT load provides higher inverter pull-up capability than the current-source load. The following discussion focuses on comparing the pull-up capabilities of inverters with resistor and current-source loads.

There is the following relationship between the pull-up current I_{SRC} and the output voltage rising slope dV_{OUT}/dt:

$$\begin{cases} I_{\mathrm{SRC}} = 0.5\mu_{\mathrm{n}}C_{\mathrm{ch}}(W/L)_{\mathrm{SRC}}\left(V_{\mathrm{GS,SRC}} - V_{\mathrm{TH}}\right)^2 \\ C_{\mathrm{OUT}} \times dV_{\mathrm{OUT}}/dt = I_{\mathrm{SRC}}. \end{cases} \tag{12}$$

where μ_{n} is the electron mobility, C_{ch} is the channel capacitance, W/L is the transistor aspect ratio, and V_{TH} is the threshold voltage. For simplicity, the first-order drain current equation for $\mathrm{M_{SRC}}$ is adopted [36], [37], [38]. After rearrangement, the following expression is obtained:

$$dV_{\mathrm{OUT}}/dt = 0.5\mu_{\mathrm{n}}C_{\mathrm{ch}}(W/L)_{\mathrm{SRC}}\left(V_{\mathrm{GS,SRC}} - V_{\mathrm{TH}}\right)^2/C_{\mathrm{OUT}}. \tag{13}$$

To provide a visual comparison, simulation results for devices corresponding to (6), (9), and (13) are plotted in Fig. 6. The black solid and dashed lines represent (6) and (9), respectively, under identical I_{LOSS} conditions. Their intersections with the red line (13) indicate $dV_{\mathrm{OUT,R}}/dt$ (resistor load) and $dV_{\mathrm{OUT,CS}}/dt$ (current-source load), respectively. As shown by the black solid line, the linear relationship between the current through the resistor and the voltage across it causes dV_{OUT}/dt in the resistor-load

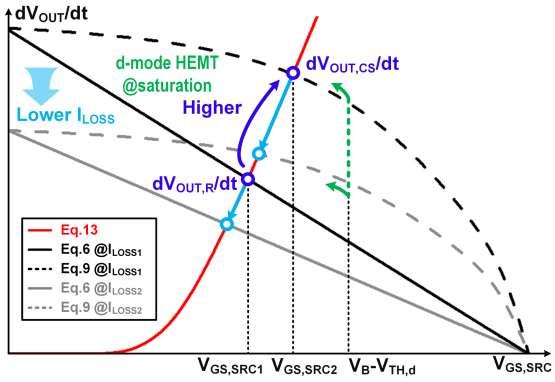


Fig. 6. Comparison of the pull-up capability of inverters with resistor and current-source loads in the secondary path.

inverter to decrease linearly as $V_{\mathrm{GS,SRC}}$ increases. However, for the current-source load, as shown by the black dashed line, the constant-current behavior ensures that dV_{OUT}/dt remains nearly constant with increasing $V_{\mathrm{GS,SRC}}$. Therefore, the following relationship holds:

$$dV_{\mathrm{OUT,R}}/dt < dV_{\mathrm{OUT,CS}}/dt. \tag{14}$$

This indicates that inverters with current-source loads have superior pull-up capability compared to those with resistor loads. The gray solid and dashed lines in Fig. 6 correspond to (6) and (9), respectively, under reduced I_{LOSS} conditions. For both configurations, a reduction in I_{LOSS} leads to a decrease in pull-up capability. For all three load types, if theoretical completeness is considered and the variation of $V_{\mathrm{GS,SRC}}$ in the second phase is not neglected, an error term associated with $dV_{\mathrm{GS,SRC}}/dt$ is introduced into (6), (9), and (11). This causes the intersection points of $dV_{\mathrm{OUT,R}}/dt$ and $dV_{\mathrm{OUT,CS}}/dt$ in Fig. 6 to shift slightly downward (as previous analyzed, the behavior of dV_{OUT}/dt with e-mode HEMTs loads is similar to $dV_{\mathrm{OUT,CS}}/dt$). However, this deviation does not affect the validity of the theoretical conclusions presented above.

In summary, for inverters requiring much higher pull-up capability, e-mode HEMTs are the preferred load option. However, implementing an e-mode HEMT load requires an additional switching circuit, which will be discussed in subsequent paragraphs. For inverters with moderate pull-up capability requirements, a current source can be used as the load, provided that the fabricated process supports d-mode HEMTs. In scenarios where d-mode HEMTs are unavailable, a resistor load remains a viable alternative for applications with relaxed performance requirements.

B. Concept of 3× Self-Circulating Charge Pump (3× SCCP)

As analyzed above, employing an e-mode HEMT as the load in the secondary path significantly enhances the pull-up capability of the inverter. To effectively control the e-mode HEMT and achieve enhanced pull-up capability, the 3×SCCP technique is proposed, as illustrated in Fig. 7(a). Considering the fan-out structure in the inverter chain design, the aspect ratio between $\mathrm{M_S}$ and $\mathrm{M_{SRC}}$ is maintained at a ratio of 1:f, where f denotes the effective fan-out [39]. Accordingly, the following relationship

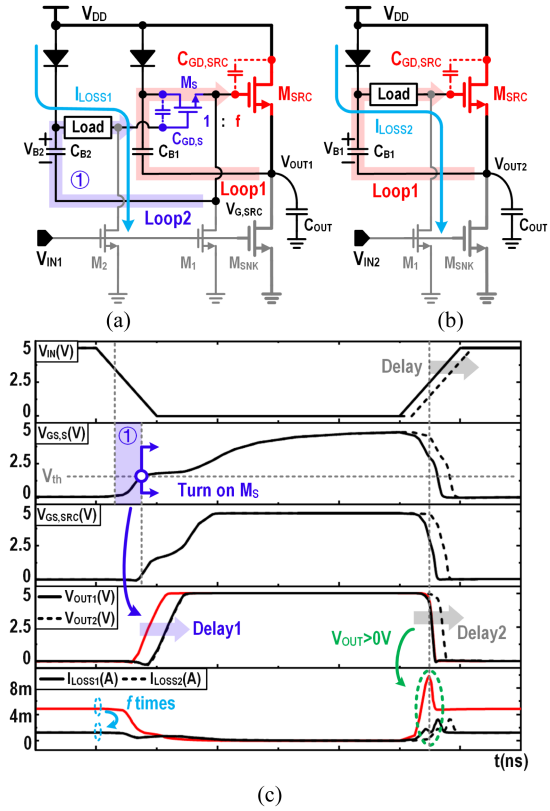


Fig. 7. Circuit structures of the (a) inverter with proposed 3× self-circulating charge pump (SCCP). (b) Conventional inverter. (c) Operating waveforms of inverters with and without 3× SCCP.

holds:

$$C_{\mathrm{GD,S}} = C_{\mathrm{GD,SRC}}/f. \tag{15}$$

Since the source of $\mathrm{M_S}$ is connected to the gate of $\mathrm{M_{SRC}}$, an additional bootstrap path, denoted as loop2, is required to turn ON $\mathrm{M_S}$. The load in loop2 can be implemented using either a resistor or a current source. As previously analyzed, loop2 introduces a new loss current I_{LOSS1}. To facilitate an analysis of I_{LOSS1}, a conventional inverter topology is shown in Fig. 7(b). The aspect ratio of $\mathrm{M_{SRC}}$ is kept identical and the same load element is employed in both inverters of Fig. 7(a) and (b), ensuring a fair comparison of performance. The loss current in Fig. 7(b) is denoted as I_{LOSS2}. As indicated by (15), the output capacitance in loop2 is $C_{\mathrm{GD,S}}$, which equals $1/f$ of $C_{\mathrm{GD,SRC}}$. Consequently, the conductance of the load in loop2 is scaled by a factor of $1/f$, (i.e., fR or I_{CON}/f), reducing the associated power dissipation to $1/f$ of its original value.

Fig. 7(c) presents the operating waveforms of the inverter with and without the proposed 3× SCCP. In this example, a resistor is employed as the load. When V_{IN} is high, I_{LOSS1} is reduced to $1/f$ of I_{LOSS2}, while the rise times of V_{OUT1} and V_{OUT2} remain identical. This indicates that, under the same power loss condition, a shorter V_{OUT} rise time can be achieved using the 3× SCCP technique, thereby enhancing the pull-up capability of the inverter.

When V_{IN} transitions from low to high, a current spike is observed in I_{LOSS2}. This spike arises because V_{OUT2} has not fully dropped to zero when M_1 turns ON, resulting in a momentary voltage across the load that rises to $V_{\mathrm{OUT1,2}} + V_{\mathrm{B}}$. This spike discharges the pump capacitor C_{B1}, causing a voltage drop across it. The reduced load conductance in Fig. 7(a) significantly suppresses the peak value of I_{LOSS1}, thereby mitigating the rapid discharge of C_{B2}.

When V_{IN} transitions to low, an additional turn-ON delay of $\mathrm{M_S}$ is introduced between the falling edge of V_{IN} and the rising edge of V_{OUT}. The rising edge of V_{IN} can be delayed by adjusting the pull-up of the first stage inverter in the predriver, thereby reducing the pulse width distortion introduced by the predriver. Employing the SCCP technique in the final inverter stage of the predriver increases the overall transmission delay by the delay of one inverter, however, it enhances the pull-up capability of the predriver by a factor of f without increasing power consumption.

C. Effect of Pump Capacitor Voltage V_B on the Pull-Up Capability of Inverters

The following paragraphs analyze the impact of V_{B} on the pull-up capability of inverters with different loads. Given the similar behavior of e-mode HEMT and current-source loads during the charging process of $\mathrm{M_{SRC}}$, the analysis focuses on a comparison between resistor and current-source load.

1) Resistor Load: As shown in (6), increasing V_{B} enhances dV_{OUT}/dt, thereby improving the pull-up capability of the inverter. However, as indicated in (1), a higher V_{B} also increases I_{LOSS}, resulting in higher power dissipation. To effectively quantify the impact of V_{B} on inverter performance, we draw inspiration from the energy-delay product commonly employed in inverter design [39] and propose a new quality metric: the energy-rise time product (ERP), defined as follows:

$$\begin{aligned}\mathrm{ERP} &= (P_{\mathrm{DB}} + P_{\mathrm{load}})\, t_{\mathrm{r}}^2 \\ &= DV_{\mathrm{DD}} I_{LOSS} [V_{\mathrm{DD}} / (dV_{\mathrm{OUT}}/dt)]^2 \\ &= (DV_{\mathrm{DD}} V_{\mathrm{B}}/R)\, [V_{\mathrm{DD}} / (dV_{\mathrm{OUT}}/dt)]^2. \end{aligned} \tag{16}$$

Here, D denotes the duty cycle when V_{IN} is high. P_{DB} and P_{load} represent the power losses on D_{B} and the load, respectively, during the high level of V_{IN}. Since the only difference between compared inverter structures lies in the load implementation, the loss considered here includes only that introduced by the I_{LOSS} path. For simplicity, it is assumed that V_{OUT} rises with a constant slope of dV_{OUT}/dt. After rearranging, the following expression is obtained:

$$\mathrm{ERP} = \left[V_{\mathrm{B}} / (dV_{\mathrm{OUT}}/dt)^2\right] \left(DV_{\mathrm{DD}}^3/R\right). \tag{17}$$

To visually illustrate the effect of V_{B}, the simulated results for the devices corresponding to (6) and (13) at different values of V_{B} are plotted in Fig. 8(a). The gray dashed line ($dV_{\mathrm{OUT}}/dt = kV_{\mathrm{GS,SRC}}$, where k is the slope) serves as an auxiliary reference, and its intersections with the green and black lines represent $dV_{\mathrm{OUT,B1}}/dt$ and $dV_{\mathrm{OUT,B2'}}/dt$, respectively. Since the green and black lines share the same slope, the following relationship

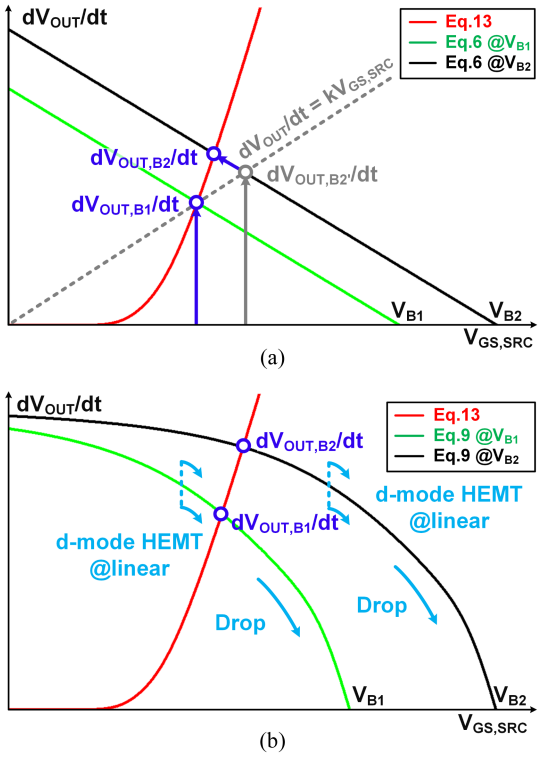


Fig. 8. Effect of bootstrap voltage V_{B} on the pull-up capability of inverters with (a) resistor loads and (b) current-source loads.

holds:

$$V_{\mathrm{B1}} / (dV_{\mathrm{OUT,\,B1}}/dt) = V_{\mathrm{B2}} / (dV_{\mathrm{OUT,\,B2'}})\, dt. \tag{18}$$

Meanwhile, the slope of the red line increases as $\mathrm{M_{SRC}}$ operates in the saturation region. Therefore, we derive

$$dV_{\mathrm{OUT,\,B2}}/dt > dV_{\mathrm{OUT,B2'}}/dt > dV_{\mathrm{OUT,B1}}/dt. \tag{19}$$

Combining (18) and (19) results in the following relationship:

$$V_{\mathrm{B2}}/(dV_{\mathrm{OUT,B2}}/dt)^2 < V_{\mathrm{B1}}/(dV_{\mathrm{OUT,B1}}/dt)^2. \tag{20}$$

Therefore, for inverters with resistor loads, increasing V_{B} results in a reduction in the ERP.

2) Current-Source Load: The simulated results for the devices corresponding to (9) and (13) at various values of V_{B} are plotted in Fig. 8(b). The ERP of the inverter with a current-source load can be expressed as

$$\begin{aligned}\mathrm{ERP} &= (P_{\mathrm{DB}} + P_{\mathrm{load}})\, t_{\mathrm{r}}^2 \\ &= DV_{\mathrm{DD}} I_{\mathrm{LOSS}} [V_{\mathrm{DD}} / (dV_{\mathrm{OUT}}/dt)]^2 \\ &= \left[I_{\mathrm{LOSS}} / (dV_{\mathrm{OUT}}/dt)^2\right] DV_{\mathrm{DD}}^3. \end{aligned} \tag{21}$$

Since the d-mode HEMT in the current source operates in the saturation region when V_{IN} is high, the following relationship holds:

$$I_{\mathrm{LOSS,B1}} = I_{\mathrm{LOSS,B2}} = I_{\mathrm{CON,CS}}. \tag{22}$$

However, when V_{IN} transitions to a low level and C_{B} begins charging the gate capacitor of $\mathrm{M_{SRC}}$, the d-mode HEMT must

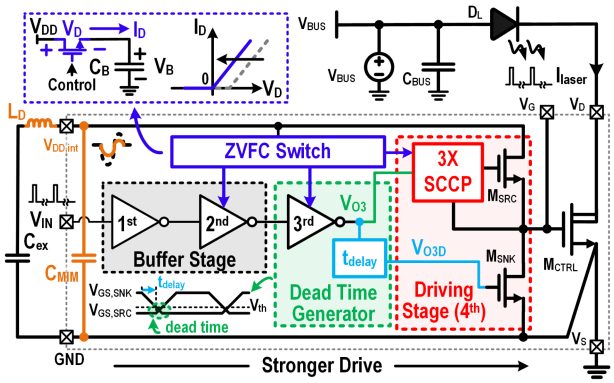


Fig. 9. Block diagram of the proposed GaN-based monolithic laser diode driver.

remain in the saturation region to maintain a constant current. This requires the following condition to be satisfied:

$$V_{\mathrm{GS,SRC}} < V_{\mathrm{B}} - |V_{\mathrm{TH,\,d}}|. \tag{23}$$

Therefore, for V_{B1}, the d-mode HEMT enters the linear region, resulting in a decrease in the current delivered by the current source. Consequently, the following relationship holds:

$$dV_{\mathrm{OUT,B1}}/dt < dV_{\mathrm{OUT,B2}}/dt. \tag{24}$$

Combining (22) and (24) results in the following relationship:

$$I_{\mathrm{LOSS,B2}}/(dV_{\mathrm{OUT,B2}}/dt)^2 < I_{\mathrm{LOSS,B1}}/(dV_{\mathrm{OUT,B1}}/dt)^2. \tag{25}$$

Therefore, for inverters with current-source loads, increasing V_{B} also leads to a reduction in ERP.

Based on the abovementioned analysis, increasing V_{B} reduces ERP in inverters employing either resistor or current-source loads, thereby enhancing their pull-up capability. Therefore, minimizing the voltage drop across the pump capacitor's charging device is essential.

III. System Architecture and Circuit Implementation

The system architecture and circuit implementation of the GaN-based monolithically integrated LDD are detailed in this section [40]. Based on the challenges and comparative analysis of various inverter topologies discussed in Section II, the block diagram of the proposed LDD is illustrated in Fig. 9. The fourth-stage inverter functions as the driving stage, supplying both pull-up and pull-down currents for the predriver. To ensure sufficient driving capability, the aspect ratios of M_{SRC} and M_{SNK} are significantly increased. Additionally, given the low duty cycle of the high-level portion of V_{IN}, the loss current I_{LOSS} of the fourth-stage inverter becomes the dominant contributor to the overall power consumption of the LDD. Therefore, the $3\times$ SCCP technique is adopted in the fourth-stage inverter to achieve a high pull-up capability.

Zero-voltage-drop fast-charging (ZVFS) switches are introduced to replace the conventional charging diodes in the second-, third- and fourth-stage inverters. As shown in the blue dashed box in Fig. 9, the ZVFS switch eliminates the ON-state voltage drop, allowing the pump voltage V_{B} to be charged up to V_{DD}. Furthermore, the linear-region conduction characteristics of the ZVFS switch enhance the charging current I_{D}, thereby accelerating the charging process of C_{B}.

To suppress the shoot-through current caused by the negative dead time between $\mathrm{M_{SRC}}$ and $\mathrm{M_{SNK}}$, a delay time t_{delay} is introduced between the rising edges of V_{O3D} and V_{O3}, ensuring that $\mathrm{M_{SRC}}$ is completely turned OFF before $\mathrm{M_{SNK}}$ is turned ON. In addition, a monolithically integrated filter capacitor C_{MIM} is incorporated within the LDD to mitigate the voltage drop of $V_{\mathrm{DD,int}}$ during the turn-ON process of $\mathrm{M_{CTRL}}$.

Fig. 10 illustrates the schematic of the proposed LDD. The first- and second-stage inverters function as buffer stages to preliminarily enhance the driving capability of the logic input signal V_{IN}. Therefore, the pull-up transistors $\mathrm{M_{H1}}$ and $\mathrm{M_{H2}}$ in these two stages are designed with small aspect ratios, and resistor-load topologies are adopted. Given the very low duty cycle of the high-level portion of V_{IN}, the input signal V_{O2} of the dead time generator (i.e., the third-stage inverter) remains low most of the time. Therefore, the loss current I_{LOSS} in the dead time generator is sustained only briefly and contributes minimally to power dissipation. As a result, a resistor-load topology is adopted in the dead time generator, and its pull-up capability can be enhanced by reducing the load resistance. If the process platform supports d-mode HEMTs, the first three inverters can be replaced with current-source load topologies to further enhance the pull-up capability. The driving stage (i.e., the fourth-stage inverter) adopts the $3\times$ SCCP technique, comprising C_{B4A}, R_{4A}, and $\mathrm{M_S}$, to achieve strong pull-up capability. If d-mode HEMTs are available, R_{4A} can also be replaced with a current source to further enhance pull-up capability.

Transistors $\mathrm{M_{B2}}$ to $\mathrm{M_{B4}}$ and $\mathrm{M_{B4A}}$ function as zero-voltage-drop fast-charging (ZVFC) switches, with their gates connected to the upper plates V_{C1} to V_{C3} of the pump capacitors C_{B1} to C_{B3} in the preceding inverter stages. This configuration enables the switches to operate in linear region while charging pump capacitors C_{B2}, C_{B3}, C_{B4}, and C_{B4A}. The first-stage inverter in buffer employs a diode-connected transistor ($\mathrm{M_{B1}}$, with its gate and source shorted) to charge C_{B1}. Due to the low duty cycle of the high-level portion of V_{IN}, $\mathrm{M_1}$ remains OFF for most of the time, making the I_{LOSS} of the first-stage inverter negligible. Consequently, the voltage drop at V_{B1} can be compensated by reducing R_1. Given the small size of the pull-up transistor $\mathrm{M_{H1}}$ in the first-stage inverter, only a small amount of charge is required from C_{B1} to turn it ON. Therefore, the diode-connected $\mathrm{M_{B1}}$ is sufficient to replenish the lost charge in C_{B1} within a very short period.

In the dead time generator, the low duty cycle of the high-level portion of V_{IN} results in a very short duration for $\mathrm{M_{B3}}$ to recharge C_{B3}. To mitigate this limitation, in addition to leveraging ZVFC technology to enhance the conductivity of $\mathrm{M_{B3}}$, its aspect ratio can also be appropriately increased to further improve the charging speed. A delay unit composed of $\mathrm{M_{3D}}$, $\mathrm{M_{L3D}}$, R_{3D}, and $\mathrm{M_{H3D}}$ is integrated to generate the required dead time. When V_{O2} transitions from high to low, $\mathrm{M_{H3D}}$ is turned ON later than $\mathrm{M_{H3}}$ due to the delay introduced by R_{3D}. As a result, the rising edge of V_{O3D} lags behind that of V_{O3} by t_{delay}. Since both $\mathrm{M_{L3}}$ and $\mathrm{M_{L3D}}$ are controlled by V_{O2}, the falling edges of V_{O3} and

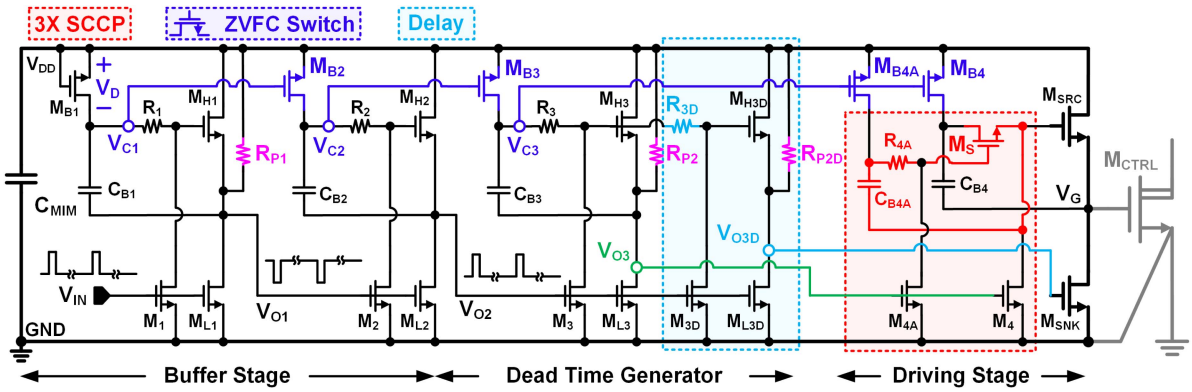


Fig. 10. Circuit schematic of the proposed GaN-based monolithic laser diode driver.

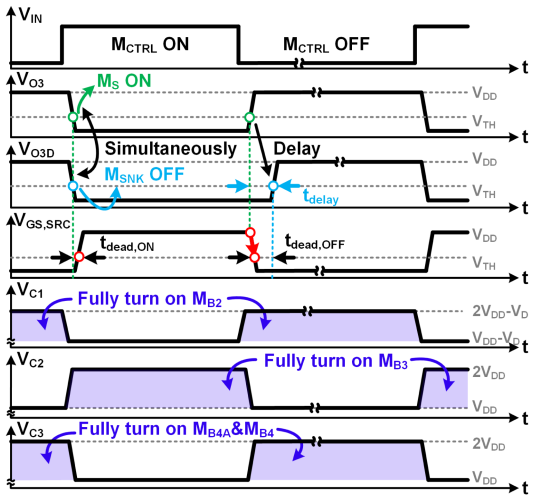


Fig. 11. Timing diagram for the operation of the zero-voltage-drop switch and the dead time generator.

V_{O3D} occur simultaneously when V_{O2} transitions from low to high.

Resistors R_{P1}, R_{P2}, and R_{P2D} initialize the voltages at V_{O1}, V_{O3}, and V_{O3D}, respectively. This ensures that V_G remains low and M_{CTRL} stays off in the absence of a valid V_{IN}. Since the pull-up transistors in the first- and third-stage inverters remain on for extended periods, and considering the gate leakage of p-GaN HEMTs, C_{B1} and C_{B3} can be appropriately increased to maintain sufficient pump voltage.

Fig. 11 presents the voltage timing diagrams of several critical nodes, while Fig. 12 illustrates the operating principle of the proposed LDD during the transitions of M_{CTRL}. The simplified model of the M_{CTRL} turn-ON and turn-OFF processes is shown in Fig. 13. During the turn-ON transition, as V_{IN} transitions from low to high, V_{O1} is pulled low, and C_{B2} serves as the voltage source to charge the gate of M_{H2} through I_{CHAR2}. Once M_{H2} is turned ON, V_{O2} is pulled high by I_{SRC2}, thereby turning ON M_{L3} and M_{L3D}. Consequently, V_{O3} and V_{O3D} are pulled low, simultaneously turning OFF M_{4A}, M_4, and M_{SNK} in the driving stage. Subsequently, loop1 of the 3× SCCP is activated, and C_{B4A} charges the gate of M_S through I_{CHAR4A}. After M_S is turned ON, C_{B4} serves as the voltage source, charging the gate of M_{SRC} through I_{CHAR4} and to turn it ON. A natural dead time $t_{dead,on}$ occurs between the turn-OFF of M_{SNK} and the turn-ON of M_{SRC}. When V_{IN} is high, V_{C2} of the second-stage inverter in the buffer rises to $2V_{DD}$, fully turning ON M_{B3} in the dead time generator and allowing C_{B3} to be charged to V_{DD}. And C_{B1} is charged by diode-connected M_{B1}. Meanwhile, the loss currents I_{LOSS1} and I_{LOSS2} in the first-stage inverter of the buffer and dead time generator flow from V_{DD} to GND, resulting in power dissipation.

During the turn-OFF transition, as V_{IN} transitions from high to low, C_{B1} serves as the voltage source to charge the gate of M_{H1} through I_{CHAR1}. Once M_{H1} is turned ON, V_{O1} is pulled high by I_{SRC1}, turning ON M_{L2}. Consequently, V_{O2} is pulled low, turning OFF M_3, M_{L3}, M_{3D}, and M_{L3D} in the dead time generator. Subsequently, C_{B3} begins charging M_{H3} and M_{H3D} through I_{CHAR3}. Due to the delay t_{delay} introduced by resistor R_{3D}, M_{H3D} is turned ON slightly later than M_{H3}, causing the rising edge of V_{O3D} to lag behind that of V_{O3} by t_{delay}. As a result, M_{4A} and M_4 in the driving stage are first turned on by V_{O3}, which subsequently turns OFF M_{SRC}. After t_{delay}, M_{SNK} is turned ON by V_{O3D}, introducing a dead time $t_{dead,off}$ between the turn-OFF of M_{SRC} and the turn-ON of M_{SNK}. The duration of $t_{dead,OFF}$ can be adjusted by modifying the value of R_{3D}. When V_{IN} is low, V_{C1} in the first-stage inverter of the buffer rises to $2V_{DD} - V_D$ and V_{C3} in the dead time generator rises to $2V_{DD}$, fully turning on M_{B2}, M_{B4A}, and M_{B4}, which allows C_{B2}, C_{B4A}, and C_{B4} to be charged up to V_{DD}. Meanwhile, loss currents I_{LOSS2} and I_{LOSS4} in the second-stage inverter of the buffer and driving stage flow from V_{DD} to GND, resulting in power dissipation.

The GaN platform process design kit used in this work adopts the asmHEMT model to characterize the electrical performance of both LV and HV HEMTs. Fig. 14 presents the simulated waveforms demonstrating the enhanced driving capability and integrated dead time insertion of the proposed LDD under a bus voltage V_{BUS} of 15 V and a driving current I_{laser} of 10 A. With the integration of the 3× SCCP technique and ZVFC switches, the predriver achieves a peak I_{SRC} of 1.75 A and a peak I_{SNK} of 1.99 A. Benefiting from the enhanced driving capability of the predriver, the gate voltage V_G of M_{CTRL} achieves a rising edge of 463 ps and a falling edge of 348 ps. When V_{IN} transitions from low to high, both V_{O3D} and V_{O3} decrease synchronously.

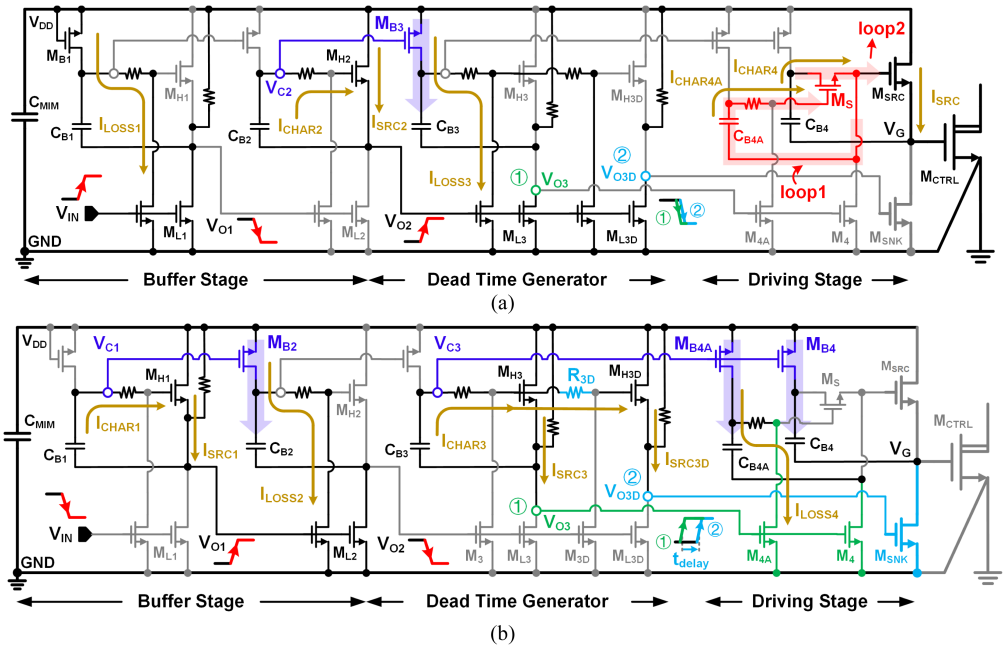


Fig. 12. Operating principles of the proposed laser diode driver during (a) the turn-ON process of M_{CTRL} and (b) the turn-OFF process of M_{CTRL}.

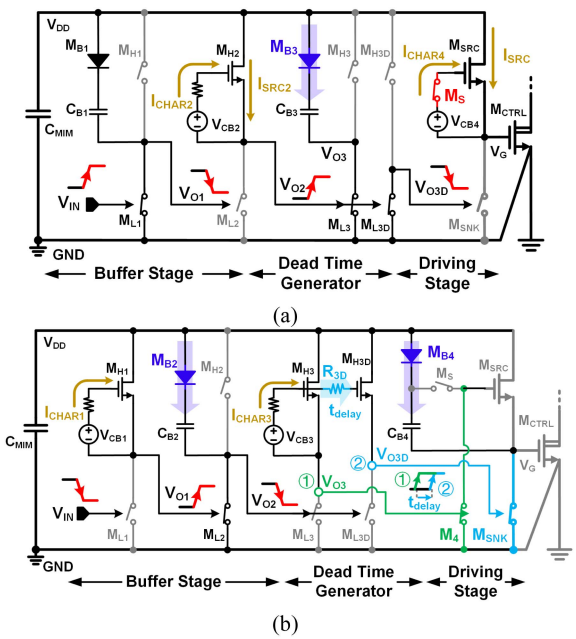


Fig. 13. Simplified operating principles of the proposed laser diode driver during (a) the turn-ON process of M_{CTRL} and (b) the turn-OFF process of M_{CTRL}.

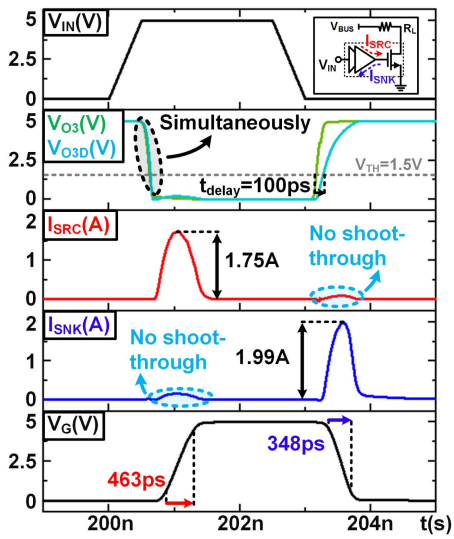


Fig. 14. Simulated working waveforms demonstrating enhanced driving capability and integrated dead time insertion.

When V_{IN} transitions from high to low, the rising edge of V_{O3D} is delayed by 100 ps relative to V_{O3}, due to the integrated dead time generator. This delay effectively eliminates the shoot-through current between M_{SRC} and M_{SNK} in the driving stage.

The simulated power loss analysis of the proposed LDD is shown in Fig. 15. Different output powers are obtained by adjusting the load resistor R_L. As shown in Fig. 15(a), at an operating frequency of 10 MHz, I_{laser} flowing through M_{CTRL} decreases with the output power, thereby the conduction loss of M_{CTRL} decreases simultaneously. However, the power loss of the predriver remains nearly independent of the output power. Within the predriver, due to the low duty cycle of the high-level portion of V_{IN}, the loss of the first-stage inverter is only 0.77 mW. The second-stage inverter incurs higher losses of 18.87 mW, mainly due to I_{LOSS2}. To enable fast turn-ON of M_{SNK}, the dead time generator employs GaN HEMTs with large aspect ratio to increase I_{SRC3D}, leading to loss of 9.02 mW. In the driving stage, the low duty cycle of V_{IN} causes I_{LOSS4} to persist for most of the cycle. Furthermore, the driving stage must supply a large I_{SRC} to drive the gate of M_{CTRL}. Therefore, it contributes the largest power loss in the predriver, which is 92.55 mW. Fig. 15(b) shows the simulated power loss analysis at 20 MHz. Compared

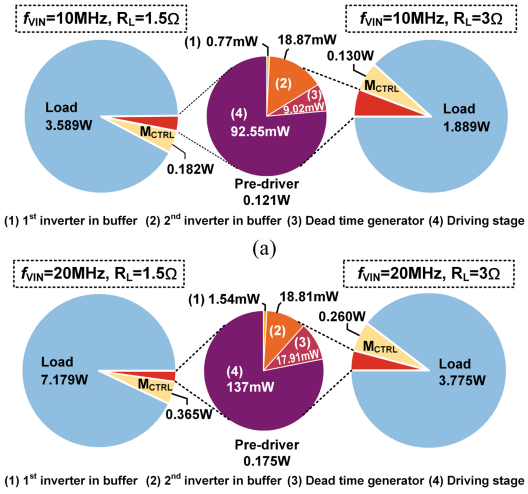


Fig. 15. Simulated losses of the proposed laser diode driver at operating frequencies of (a) 10 MHz and (b) 20 MHz.

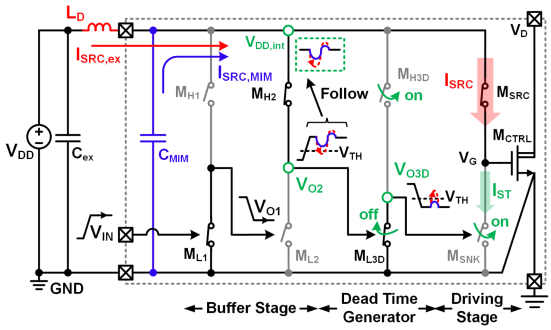


Fig. 16. Monolithically integrated C_{MIM} filter for internal power rail.

with 10 MHz, the higher operating frequency increases both the output power and the total power loss of the LDD. Nevertheless, the efficiency improves from 92.21% to 93.00% when R_L = 1.5 Ω, and from 88.27% to 89.66% when R_L = 3 Ω.

Fig. 16 shows the filtering effect of the monolithically integrated C_{MIM} on the internal power rail $V_{DD,int}$. During the turn-ON process of M_{CTRL}, the rapidly rising I_{SRC} flowing through L_D induces a significant drop in $V_{DD,int}$. Since M_{H2} in the second-stage inverter is conducting, V_{O2} decreases synchronously with $V_{DD,int}$. If the minimum value of $V_{DD,int}$ falls below V_{TH}, M_{L3D} in the dead time generator is turned OFF, thereby turning ON M_{H3D} and pulling up V_{O3D}. Once V_{O3D} exceeds V_{TH}, M_{SNK} in the driving stage is unintentionally turned ON, causing a shoot-through current I_{ST} to flow between M_{SRC} and M_{SNK}. With C_{MIM} integration, a portion of the charge required by I_{SRC} is supplied by the C_{MIM}, thereby alleviating the $V_{DD,int}$ drop. Fig. 17 shows the simulated C_{MIM} filtering for $V_{DD,int}$, with a low-parasitic WLCSP package and low-ESL filter capacitors C_{ex}, L_D is set to 600 pH. By integrating 50 pF C_{MIM}, the minimum $V_{DD,int}$ increases from 2 V to 2.5 V, while the maximum V_{O3D} rise decreases from 1.8 V to 1 V. This value is lower than the 1.5 V threshold voltage of M_{SNK}, thus preventing the occurrence of I_{ST}.

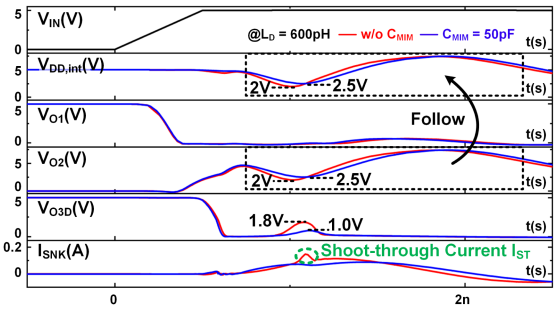


Fig. 17. Simulation of C_{MIM} filtering for internal power rail.

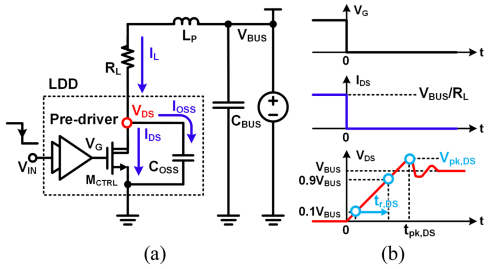


Fig. 18. (a) Simplified model of parasitic effects in the power loop. (b) Key signal waveforms during the turn-OFF process of M_{CTRL}.

During the turn-OFF process of M_{CTRL}, there is a tradeoff between the rise time and the voltage overshoot of V_{DS}. Fig. 18(a) illustrates a simplified model of the parasitic elements in the power loop, including the loop parasitic inductance L_P and the output capacitance C_{OSS} of M_{CTRL}. Fig. 18(b) shows the key waveforms during the turn-OFF process of M_{CTRL}. Based on the model in Fig. 18(a), the corresponding equations are derived as follows:

$$\begin{cases} I_L = I_{DS} + I_{OSS} \\ V_{DS} = V_{BUS} - L_P \times dI_L/dt - I_L \times R_L \\ I_{OSS} = C_{OSS} \times dV_{DS}/dt \\ V_{DS}\left(0^+\right) = 0, dV_{DS}/dt\left(0^+\right) = V_{BUS}/\left(R_L C_{OSS}\right). \end{cases} \tag{26}$$

The peak value $V_{pk,DS}$ of the V_{DS} overshoot can be expressed as

$$V_{pk,DS} = V_{BUS}\left[1 + \frac{1}{2\xi^2\sqrt{1-\xi^2}} e^{-\frac{\zeta}{\sqrt{1-\xi^2}}(\pi-\theta)}\right]$$
$$\begin{cases} 0 < \xi = \frac{1}{2} R_L \cdot \sqrt{\frac{C_{OSS}}{L_P}} < 1 \\ \theta = \tan^{-1}\left(\frac{1-2\xi^2}{2\xi\sqrt{1-\xi^2}}\right). \end{cases} \tag{27}$$

Assuming that V_{DS} increases linearly from 0 V to $V_{pk,DS}$, the rise time $t_{r,DS}$ can be approximated as

$$\begin{cases} t_{r,DS} = 0.8 t_{pk,DS} \times V_{BUS}/V_{pk,DS} \\ t_{pk,DS} = \frac{\pi-\theta}{\omega_n\sqrt{1-\xi^2}} \\ \omega_n = 1/\sqrt{L_P C_{OSS}}. \end{cases} \tag{28}$$

As shown in Fig. 19(a), with increasing load current I_L, $V_{pk,DS}$ increases, while $t_{r,DS}$ decreases. Fig. 19(b) shows that with increasing L_P, $V_{pk,DS}$ increases, whereas $t_{r,DS}$ decreases.

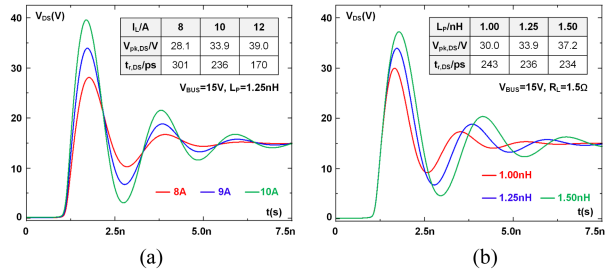


Fig. 19. Simulated V_{DS} ringing versus (a) load current I_{DS} and (b) parasitic inductance L_P.

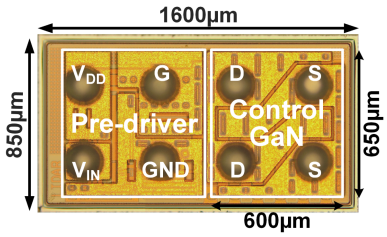


Fig. 20. Chip micrograph of the proposed GaN-based laser diode driver.

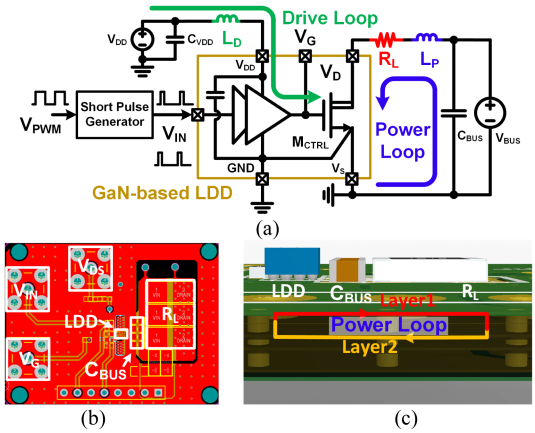


Fig. 21. (a) Circuit schematic of the evaluation module (EVM) used to assess the performance of the proposed LDD. (b) Top and (c) side views of the low parasitic power loop in the EVM.

IV. Experimental Results

The proposed GaN-based monolithically integrated LDD is designed and fabricated using a 0.25-μm GaN-on-Silicon process, with an active area of 1600 μm × 850 μm, as illustrated in Fig. 20. The integrated 40 V GaN control switch occupies an area of 600 μm×650 μm. The chip is packaged in a chip-scale package to achieve a compact form factor and minimize parasitic inductance.

Fig. 21(a) shows the schematic of the evaluation module (EVM) used to assess the performance of the proposed LDD. A resistor R_L is adopted to emulate the laser diode as the load for the proposed LDD, facilitating the measurement of driving current pulses [8], [41]. A short-pulse generator provides a square-wave signal with a narrow pulse width, which is applied to the input V_{IN} of the LDD. Although monolithic integration eliminates the gate parasitic inductance L_G, parasitic inductance L_D still exists in the drive loop, originating from the equivalent

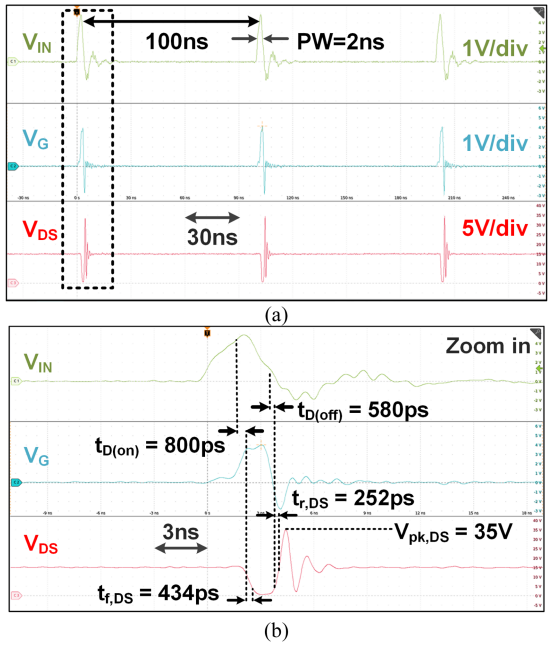


Fig. 22. (a) Measured operating waveform of the proposed laser diode driver at V_{BUS} = 15 V, I_{laser} = 10 A and an operating frequency of 10 MHz, and (b) a zoomed-in of one pulse.

series inductance (ESL) of the filter capacitor C_{VDD}, PCB trace parasitic inductance, and package inductance. To minimize L_D, a low-ESL C_{VDD} should be selected and placed as close as possible to the V_{DD} pin of the LDD in the PCB layout. For further reduction of L_D, directly bonding chip-scale silicon capacitors to the GaN IC offers a more effective solution [34].

L_P represents the parasitic inductance associated with the power loop. A large L_P induces a voltage spike at the drain of M_{CTRL}, which imposes stricter requirements on its drain-to-source voltage rating. Fig. 21(b) and (c), respectively, depicts the top and side views of the low-parasitic power loop design implemented in the EVM. The design adopts a four-layer PCB structure (layers 1 through 4), where the power loop forms a return current path between layers 1 and 2. This configuration shortens the return path length and enhances magnetic field cancellation between opposing currents in layers 1 and 2, effectively reducing L_P [42], [43].

Figs. 22 and 23 show the measured waveforms of the proposed LDD operating at frequencies of 10 MHz and 20 MHz, respectively, under test conditions of V_{BUS} = 15 V and I_{laser} = 10 A (R_L = 1.5 Ω). Due to the limitations of the short-pulse generator, the pulse width of the input signal V_{IN} applied to the LDD is set to 2 ns. V_G denotes the gate voltage of M_{CTRL}, and the drain-to-source voltage V_{DS} of M_{CTRL} is measured to characterize the driving current I_{laser}.

The zoomed-in waveform of a single switching cycle at 10 MHz is shown in Fig. 22(b). With the implementation of the proposed 3× SCCP and ZVFC switches, the rising and falling edges of V_G are measured to be 393 ps and 374 ps, respectively. During the falling edge of V_G, no unintended turn-ON of M_{CTRL} is observed. The corresponding falling and rising edges of V_{DS} are 434 ps and 252 ps. The peak drain-source voltage $V_{pk,DS}$

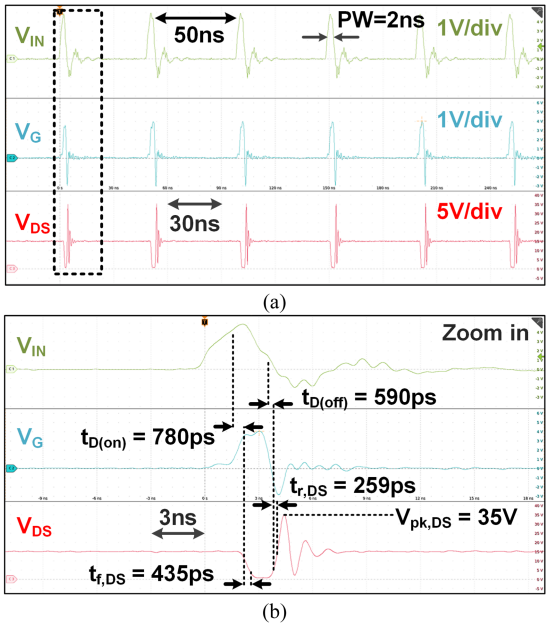
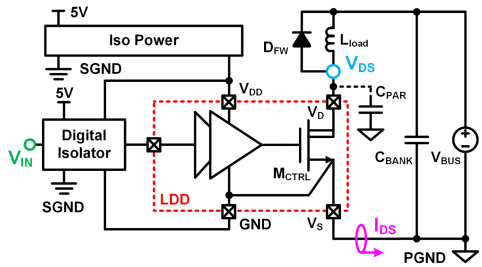
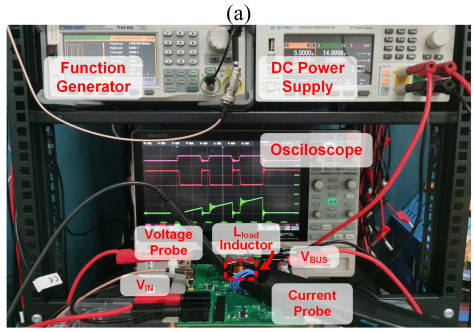


Fig. 23. (a) Measured operating waveform of the proposed laser diode driver at $V_{\mathrm{BUS}} = 15$ V, $I_{\mathrm{laser}} = 10$ A, and an operating frequency of 20 MHz, and (b) a zoomed-in of one pulse.



Symbol	Description	Quantity
L_{load}	3.3μH, Coilcraft SER2918H-332	1 pieces
D_{FW}	100V Schottky, SMA, Slkor SS510	3 pieces

(a)



(b)

Fig. 24. (a) Schematic circuit of the double pulse test. (b) Photograph of experimental setup.

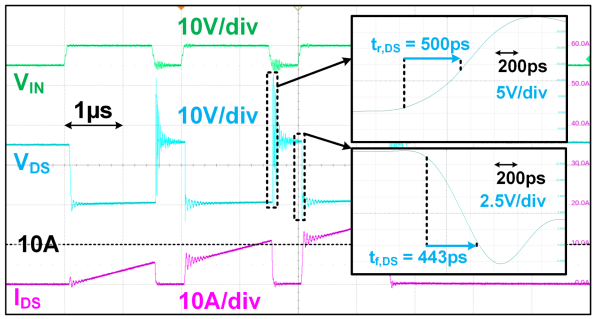


Fig. 25. Measured waveforms of the double pulse testing for the proposed laser diode driver.

during the rising edge of V_{DS} is 35 V, which remains below the breakdown voltage of $\mathrm{M_{CTRL}}$. This peak voltage can be further mitigated by reducing the parasitic inductance L_{P} in the power loop through direct mounting of the load on top of the LDD [5], [44], at the expense of a slight increase in the rise time of V_{DS}. The turn-ON and turn-OFF delays are 800 ps and 580 ps, respectively.

The zoomed-in waveform at 20 MHz is shown in Fig. 23(b) The falling and rising edges of V_{DS} are measured to be 435 ps and 259 ps, respectively. The turn-ON and turn-OFF delays are 780 ps and 590 ps, respectively. Although the charging times of the pump capacitors in the second- and fourth-stage inverters decrease within each cycle as the frequency increases, the changes in the dynamic characteristics of the proposed LDD are minimal.

The double pulse testing (DPT) was conducted under the condition of 10 A/15 V, the test schematic and test board of the DPT are shown in Fig. 24, and the measured waveform is shown in Fig. 25. The load current I_{DS} reaches 10 A during the second pulse. The rise time of V_{DS} is limited by the parasitic capacitor of the freewheeling diode $\mathrm{D_{FW}}$ and the load L_{load}. The ringing of V_{DS} during turn-OFF and turn-ON process is mainly caused by parasitic inductances from the PCB traces and package, which can be further optimized by shortening the power loop and using a low parasitic package. No false turn-ON of $\mathrm{M_{CTRL}}$ was observed on the rising edge of V_{DS}, therefore, a negative gate voltage is not required to prevent false turn-ON events in the proposed LDD.

The performance of the proposed GaN-based monolithically integrated LDD is summarized in Table II and compared with other state-of-the-art designs. The proposed LDD achieves the steepest rising and falling edges of the driving current among the designs compared. Considering both efficiency and maximum driving current slope, it achieves the lowest FOM, which is 74.21 ps/A.

Fig. 26 illustrates the measured operating efficiency η and operating current I_{VDD} drawn from the V_{DD} as functions of operating frequency. The quiescent current I_{VDD}, measured with V_{IN} held low, is 12 mA. During normal operation with a 2 ns

TABLE I
COMPARISON OF LASER DIODE DRIVER SOLUTIONS

Process	BCD [4], [5], [6]	Si + GaN [7], [8], [9]	GaN [10], [11]
Pre-driver	Si-based	Si-based	GaN-based
$\mathrm{M_{CTRL}}$	LDMOS	GaN HEMT	GaN HEMT
Adv.	Mature Process, Low L_{G}	Low FoM $\mathrm{M_{CTRL}}$	Low FoM $\mathrm{M_{CTRL}}$, Low L_{G}
Lim.	High FoM $\mathrm{M_{CTRL}}$	Large L_{G}	Lack of p-type device

TABLE II
COMPARISON WITH STATE-OF-THE-ART WORKS

	This Work	JESTPE'20 [4]	ESSCIRC'23 [6]	JSSC'24 [5]	TPE'25 [8]	EPC21601 [45]
Process	250 nm GaN-on-Silicon	180 nm*	180 nm BCD	180 nm BCD	LMG1020	GaN
Switch Type	Integrated GaN	Integrated LDMOS	Integrated LDMOS	Integrated LDMOS	GS61004B	Integrated GaN
Laser Diode Driver Type	FET Controlled	Controlled Current Source	FET Controlled	Double-pulse Overlapping	Capacitive Discharge	FET Controlled
Bus Voltage V_{BUS}	15V	5 V	5.0–8.5 V	20 V	15 V	20 V
Peak Output Current $I_{laser,pk}$	10 A	5 A	6.5 A	15 A	15 A	15 A
Peak Output power $P_{laser,pk}$	150 W	100 W**	55.25 W	300 W	40 W**	300 W
Min. Rise Time t_r @I_{laser}	434 ps @10 A	900 ps @5 A	860 ps @4.8 A**	1 ns @15 A**	1.36 ns @15 A**	750 ps @10 A
Min. Fall Time t_f @I_{laser}	252 ps @10 A	2.5 ns @5 A	860 ps @4.8 A**	1 ns @15 A**	4.72 ns @15 A**	320 ps @10 A
Average Power Consumption $P_{diss,av}$	420 mW @10 MHz	N/A	N/A	N/A	860 mW @10 MHz**	410 mW @10 MHz
Peak Efficiency η	92.44% @20 MHz	N/A	N/A	N/A	75% @10 MHz	91.32% @20 MHz
FOM=(1−η)(t_r+t_f)/(η·Q_G)	124ps/nC	N/A	N/A	N/A	614ps/nC	137ps/nC
Active Area	1.36 mm^2	2.56 mm^2	0.98 mm^2***	2.30 mm^2	NA	1.50 mm^2

*5-V-gated power management process w/ custom designed LDMOS. **Estimated from the graph.
***Estimated value, including only current control, pre-driver and driver output stage.

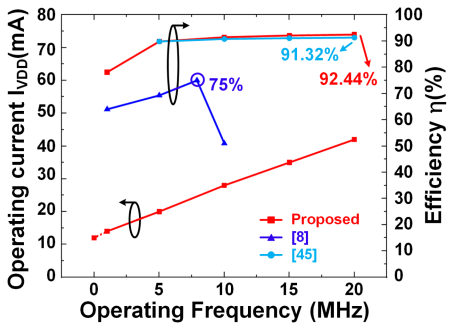
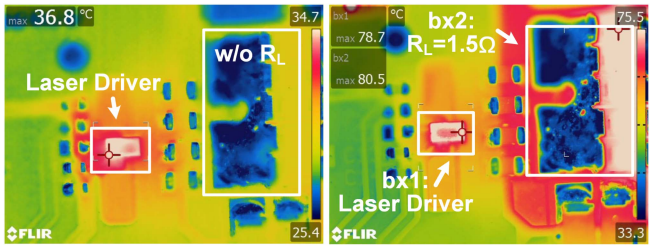


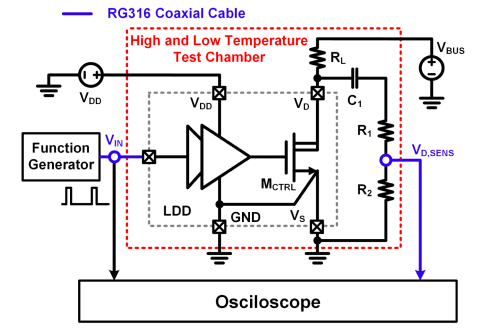
Fig. 26. Measured operating efficiency and operating current drawn from the V_{DD} supply of the proposed laser driver as a function of operating frequency (with a pulse width of V_{IN} of 2 ns).



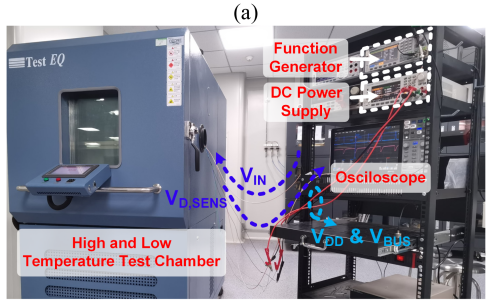
(a) (b)

Fig. 27. Measured thermal imaging of the laser driver at f_{VIN} = 10 MHz, pulse width = 2 ns. (a) Without load current. (b) With V_{BUS} = 15 V, I_{laser} = 10 A.

pulse width for V_{IN}, I_{VDD} increases linearly with operating frequency, primarily due to the charging and discharging of parasitic capacitances in the transistors. As the frequency increases to 20 MHz, I_{VDD} rises to 42 mA, while the efficiency reaches its peak value of 92.44% . Fig. 27 shows the measured thermal images of the LDD operating at 10 MHz with a pulse width of 2 ns. As shown in Fig. 27(a), the maximum temperature of the LDD without load current is 36.8 °C. Fig. 27(b) shows that with



(a)



(b)

Fig. 28. (a) Circuit schematic and (b) experimental setup of high- and low-temperature tests.

V_{BUS} = 15 V and I_{laser} = 10 A, the maximum temperature of the LDD reaches 78.7 °C.

Fig. 28 presents the circuit schematic and experimental setup for high- and low-temperature tests, while the measured waveforms are shown in Fig. 29. The proposed LDD maintains stable operation across the temperature range from −40 °C to 125 °C. With increasing temperature, the ON-resistance of M_{CTRL} rises, leading to a higher on-state voltage. Within the tested temperature range, the charge pump voltage is established within a single cycle, the bootstrap switches enable zero-voltage-drop fast-charging, and normal LDD operation is ensured.

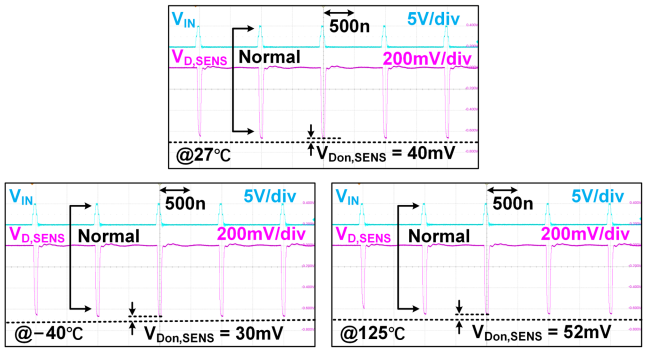


Fig. 29. Measured operating waveforms of the proposed laser diode driver at temperature of 27 °C, −40 °C, and 125 °C.

V. Conclusion

In this work, a GaN-based LDD fabricated in a 0.25-μm GaN-on-Silicon process is developed for dToF LiDAR transmitters, capable of generating high-peak, narrow-pulse laser-driving currents. To overcome the limited driving capability of conventional GaN-based gate drivers due to the lack of suitable p-type devices, a 3× SCCP technique and ZVFC switches are employed, enabling fast switching of the control switch. The proposed LDD achieves a 10 A peak driving current with rise and fall times of 434 ps and 252 ps, respectively. Furthermore, dead time control and an ON-chip filtering capacitor effectively suppress shoot-through current in the final stage of the predriver. The LDD exhibits an average power loss of 420 mW and a peak efficiency of 92.44% , demonstrating the potential of GaN integration for high-performance LiDAR transmitters.

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