A Modularized Partial Power Converter Based Uninterruptible Power Supply Scheme for DC Power Feeding Servers in Data Centers

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***Abstract*—This article proposes a novel partial power converter based uninterruptible power supply (PPC-UPS) scheme for dc power feeding servers in data centers, in which a server load and its local backup battery are connected in series and compactly integrated to a common dc bus through one PPC. The proposed PPC-UPS scheme is modularized and distributed in multiple dc loads of a data center, with high scalability and reliability. The PPC-UPS scheme can reduce the number of power electronic converters by diverting the battery energy directly to the dc load via the PPC, while power conversion losses can also be significantly reduced as the PPC only undertakes a fraction of the dc load power. A PPC-UPS multimode control strategy is designed to autonomously and flexibly secure its continuous operations under various contingencies. Small-signal analysis is carried out to assess the system stability and obtain optimal control parameters. The performances of the PPC-UPS scheme are evaluated through hardware experiments, which illustrate that the PPC-UPS can reliably supply the dc loads under the contingencies of converter or battery outage and facilitate load reconnections.**

***Index Terms*—Backup battery, data centers, multimode operations, partial power converter (PPC), uninterruptible power supply (UPS).**

I. INTRODUCTION

EXPONENTIAL growth of Big Data and cloud computing technologies will inevitably accompany significant increases in the power consumptions of data centers [1]. Global data center electricity consumption in 2021 was approximately 220–320 TWh, accounting for 0.9%–1.3% of the global total electricity demand [2], and a dramatic rise is anticipated to reach 8% by 2030 [3]. Reducing data center power consumption has become a primary task for data center operators all over the world.

Uninterruptible power supply (UPS), as an essential device to ensure the continuous operation of critical server loads, can take approximately 12% (third-largest) of data center total electricity consumption [4]. Under this context, strong demand to provide more efficient power supply for server loads in data centers drives the gradual replacement of UPS scheme from ac to dc with less energy conversions [4], [5]. Generally, the dc UPS scheme lumps all the batteries at a common dc bus as presented in [6], [7], where the battery is charged by the grid through a rectifier and discharges to servers if a grid outage occurs. However, due to the lack of discharge control, the server voltage may unfavorably fluctuate in a wide range. To improve the server power quality, a central dc–dc full power converter (FPC) is added in a dc UPS for battery discharge control as presented in [8] and [9], as shown in Fig. 1(a). Nevertheless, major power disruption may occur if the centralized battery is out of operation, leading to compromised reliability. Such a centralized UPS failure has been regarded as the main cause of the historical data center contingencies as reported in [10] and [11]. A representative contingency was the entire shutdown of a data center in South Korea caused by a fire of UPS batteries in 2022 [12]. Hence, the dc UPS has to be uneconomically over-planned to fulfill the requirement for $N-1$ contingency.

To address aforementioned reliability issue, "distributed" modularized dc UPS units installed in or adjacent to server racks exhibit their advantages of high compactability and reliability [13], [14], [15], as shown in Fig. 1(b). Due to the short distance between a battery and a server load in the distributed UPS scheme, the possibility of faults developing along a power chain is substantially reduced. Lighter weight and higher portability facilitate plug-and-play installation and expansion of the distributed UPS [14]. Moreover, compared to the overall power disruption during troubleshooting in traditional centralized UPS schemes, failed modules in distributed modular UPS scheme could be directly replaced and independently troubleshoot

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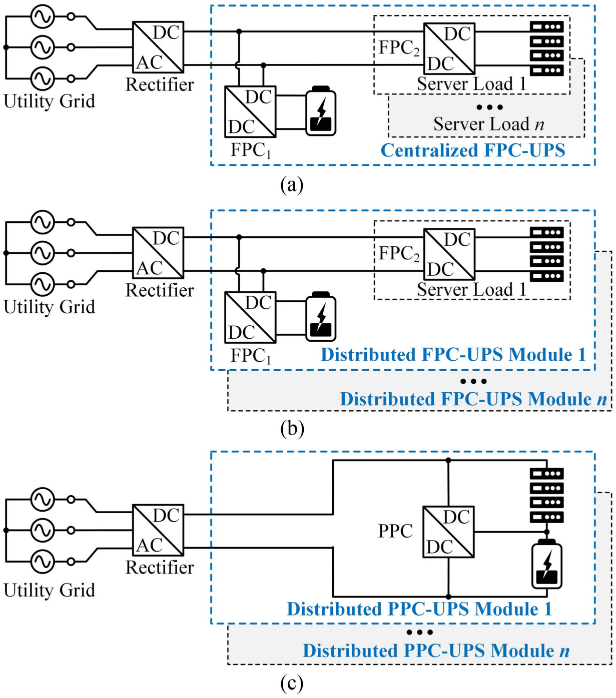


Fig. 1. Different topologies of DC UPS schemes. (a) Centralized FPC-UPS scheme. (b) Distributed FPC-UPS scheme. (c) Proposed distributed PPC-UPS scheme in this paper.

without interrupting normal operations of the rest modules with better power supply reliability due to its inherent "plug-and-play" and "hot-swap" capabilities [16]. However, for existing distributed modularized FPC-UPS schemes, whole server power is still processed via the FPCs, leading to high power losses which may not be economically justified.

A partial power converter (PPC), which is connected in parallel as a current regulator or in series as a voltage regulator [17], [18], [19], is technically appealing to establish a novel modularized dc UPS scheme. As the PPC only processes a fraction of the input power and allows the rest of the power directly delivered to the output side, smaller power rating of the converter, reduced cost and increased efficiency in overall system-level can be readily realized as stated in [17], [18], [19]. Due to these benefits, the PPC has been widely utilized in many dc systems, such as photovoltaic collection systems [20], [21], balancers for series battery strings [22], [23], chargers for electric vehicles [24], [25], et al. For its application in data centers, a series-stacked power delivery architecture with the PPC for series dc server loads is proposed in [26], [27], [28], which equally regulates the voltage of each server. Multiple hard disk drives in a data storage server are connected in series through a multiport PPC as proposed in [29] and [30], realizing inherent voltage step-down capability. The PPC is also applied to balance the voltages and handle the mismatch of currents amongst core stacks in a microprocessor as presented in [31], [32], and [33]. However, all these schemes in [26], [27], [28], [29], [30], [31], [32], [33] mainly focus on the power distribution via PPC from main grid to dc server loads, without considering PPC application in UPS to tackle grid outages.

Therefore, it is desirable to design a novel UPS scheme in both the topology and the corresponding control strategy to address aforementioned issues. To this end, this article elaborates a novel modularized PPC-UPS scheme as shown in Fig. 1(c) for dc power feeding servers aiming at improving efficiency in data centers, with the key features as follows:

1) *Modularized and Distributed Architecture with Enhanced Scalability:* Compared to the traditional centralized FPC-UPS scheme as shown in Fig. 1(a), the proposed PPC-UPS scheme as shown in Fig. 1(c) adopts a fully modularized and distributed architecture across multiple dc loads in data centers, providing superior scalability and reliability. Furthermore, unlike the conventional distributed FPC-UPS scheme with two converters as shown in Fig. 1(b), a server load and a backup battery in a proposed PPC-UPS module are connected in series and integrated to a common dc bus through only one PPC in a compact manner, offering better modularity for UPS to facilitate the data center expansion.
2) *Improved Overall System Efficiency with Partial Power Processing Capability:* Compared to the conventional distributed FPC-UPS scheme as shown in Fig. 1(b), the proposed PPC-UPS scheme as shown in Fig. 1(c) employs only one PPC to divert the battery energy to the dc server load, substantially reducing the number of power-electronic converters and consequently UPS size, weight as well as power losses. Crucially, the PPC's unique capability to process only a fraction of the overall load power could further reduce the power conversion losses and improve the system efficiency as well as the power density.
3) *Autonomous and Flexible Multi-Mode Operations:* With an elaborated control strategy, multimode operations [i.e., grid-connected (GC) mode, islanded (IL) mode, battery outage (BO) mode, and server outage (SO) mode] of the proposed PPC-UPS can be switched autonomously and flexibly, satisfying various requirements under different conditions.

The rest of this article is arranged as follows. Section II presents the proposed PPC-UPS configuration and efficiency evaluation. Section III elaborates the multimode control strategy of the PPC-UPS. Then the stability analysis and parameter optimization of PPC-UPS are carried out in Section IV with a small-signal model (SSM). Hardware experiments are carried out to evaluate the performances of the proposed scheme in Section V. Finally, Section VI concludes this article.

II. PPC-UPS CONFIGURATION AND POWER EFFICIENCY EVALUATION

A. PPC-UPS Configuration

The proposed modularized PPC-UPS scheme is illustrated in Fig. 2 as highlighted with the blue dotted line, which could interconnect to an ac utility grid through a rectifier [14] as an example in this article or directly to a dc grid with the stable dc bus voltage [13]. A server load and its local backup battery are connected in series and then integrated to a common dc bus

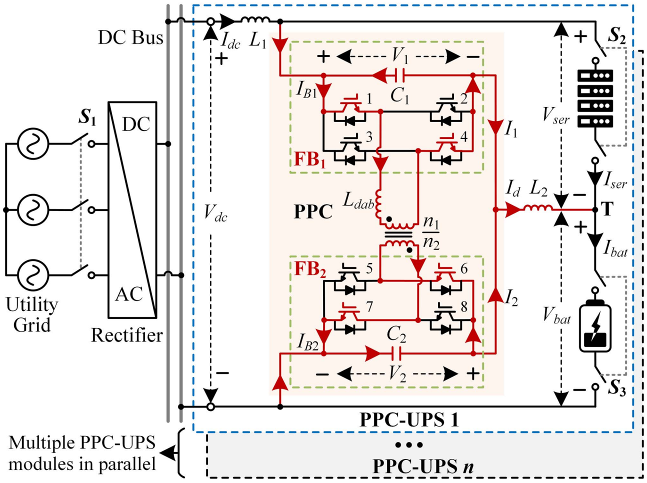


Fig. 2. Topology of the proposed PPC-UPS scheme.

through only one PPC. The PPC is a modified version of a dual active bridge (DAB) converter, with its two dc poles directly interconnected to produce a third dc connection point, as shown in Fig. 2. To be specific, one full bridge (denoted as FB_1) of the DAB is connected in parallel with the server load, whereas the other full bridge (denoted as FB_2) is connected in parallel with the battery. The PPC implemented through the DAB could not only prevent from accidentally shorting out with the DAB internal galvanic isolation, but also facilitate the bidirectional power transferring capability for the battery charging/discharging. To secure the battery power quality, filtering inductor L_2 is placed in the T node connected wire of the PPC. Selection of inductors L_1 and L_2 is presented in Appendix A. It is noted that the galvanic isolation for the server power supply is typically provided by the step-down dc–dc converter inside the server or the server rack as stated in [34], which is out of this article's scope.

As illustrated in Fig. 2, the FB_1 voltage V_1, as established by the capacitor C_1, is regulated by the PPC to control the server voltage V_{ser}, whereas the FB_2 voltage V_2, as established by the capacitor C_2, is clamped to be equal to the battery voltage V_{bat}. In view of energy conversion low, with the voltage turn ratio of high-frequency transformer (HFT) set as $n_1 : n_2 = V_1 : V_2 \approx 1 : 1$ as an example, $I_1 \approx I_2$ is realized through the HFT power regulation. It is noted that V_1 and V_2 of PPC could be set flexibly, where the HFT must be redesigned to match different levels of V_1 and V_2. The currents of I_1 and I_2, regulated by FB_1 and FB_2, respectively, are combined to compensate the current difference I_{d} between the server load current I_{ser} and the battery current I_{bat} at the T node, as highlighted in red as an example when switches 1, 4, 6, and 7 turn ON. Under specific load current I_{ser} variation, the PPC regulates I_{d} to balance the current difference $I_{\mathrm{bat}} - I_{\mathrm{ser}}$ between the server load and the battery connected in series.

Compared to the conventional FPC-UPS scheme in Fig. 1(b), the proposed PPC-UPS scheme provides the following advantages: 1) Reduces the rated voltage of the converter under same levels of V_{dc}, V_{bat}, and V_{ser}, due to the parallel connection of the PPC-UPS FB_1 with the server load at 380 V is much lower than that of FPC-UPS which is directly connected to the dc bus at 750 V. The reduced rated voltage of the converter directly yields the benefit of the lower voltage ratings of the switching devices, and thereby achieving the significant cost reduction in power electronic components. 2) Promotes the modularity and scalability as a UPS battery is integrated into a server load through only one PPC in the proposed PPC-UPS scheme with less components and cost, rather than two FPCs for both the battery and the server load. From this basis on, the converter current rating is mainly planned against the power demand of the server load when the battery discharges, whereas current rating of FPC_1 and FPC_2 as shown in conventional schemes of Fig. 1(b) should be planned against the power demands of the battery and the server load, respectively. 3) Decreases the processed power of the converter and increases the system-level efficiency due to the inherent partial power processing capability of PPC. Such advantage enables the use of switching devices with lower power ratings and less cost. The processed power and the system-level efficiency of PPC-UPS is to be analyzed in the following content.

B. *Power Processing Factor of PPC-UPS*

Power processing factor (PPF) is one of important indexes to evaluate the performance of a PPC [17]. It is defined as the ratio of the power processed by the PPC (denoted as P_{PPC}) to the total power (denoted as P_{total}), given as

$$\mathrm{PPF} = \frac{|P_{\mathrm{PPC}}|}{|P_{\mathrm{total}}|}. \tag{1}$$

According to (1), the less power the PPC processes, the smaller the PPF is resulted.

As shown in Fig. 2, the power processed by the PPC in the PPC-UPS is equal to the DAB transferred active power as

$$P_{\mathrm{PPC}} = \eta_{\mathrm{c}} V_1 I_1 = V_2 I_2 \tag{2}$$

where η_{c} is the efficiency of the DAB itself.

As the total power P_{total} in the PPC-UPS module is dictated by the power sum of the server load and the battery, PPF of the PPC as shown in Fig. 2 is given as

$$\mathrm{PPF_{PPC}} = \frac{|\mathrm{V_2 I_2}|}{|\mathrm{V_{ser} I_{ser}}| + |\mathrm{V_{bat} I_{bat}}|}. \tag{3}$$

When neglecting the voltage drop of the filtering inductors, the voltages V_1 and V_2 are expressed as

$$\begin{cases} V_1 = V_{\mathrm{ser}} = V_{\mathrm{dc}} - V_{\mathrm{bat}} \\ V_2 = V_{\mathrm{bat}}. \end{cases} \tag{4}$$

With the direction notations as shown in Fig. 2, the current relationships of the PPC-UPS are given as

$$\begin{cases} I_{\mathrm{dc}} = I_{\mathrm{ser}} + I_1 \\ I_{\mathrm{d}} = I_1 + I_2 \\ I_{\mathrm{d}} = I_{\mathrm{bat}} - I_{\mathrm{ser}} \end{cases} \tag{5}$$

where I_{dc} is the current conducting from the common dc bus.

By solving (2), (4), and (5), the currents I_1 and I_2 can be obtained as

$$\begin{cases} I_1 = \frac{V_{\mathrm{bat}}(I_{\mathrm{bat}}-I_{\mathrm{ser}})}{\eta_c V_{\mathrm{dc}}+(1-\eta_c)V_{\mathrm{bat}}} \\ I_2 = \frac{\eta_c(I_{\mathrm{bat}}-I_{\mathrm{ser}})(V_{\mathrm{dc}}-V_{\mathrm{bat}})}{\eta_c V_{\mathrm{dc}}+(1-\eta_c)V_{\mathrm{bat}}}. \end{cases} \tag{6}$$

By substituting (6) into (3), $\mathrm{PPF_{PPC}}$ can be obtained under different battery and server currents, as

$$\mathrm{PPF_{PPC}} = \begin{cases} \frac{\eta_c(1-M)}{\eta_c+(1-\eta_c)M} \times \frac{M|1-M_t|}{M+(1-M)|M_t|}, & I_{\mathrm{ser}} \neq 0 \& I_{\mathrm{bat}} \neq 0 \\ \frac{\eta_c(1-M)}{\eta_c+(1-\eta_c)M}, & I_{\mathrm{ser}} = 0 \& I_{\mathrm{bat}} \neq 0 \\ \frac{\eta_c M}{\eta_c+(1-\eta_c)M}, & I_{\mathrm{ser}} \neq 0 \& I_{\mathrm{bat}} = 0 \end{cases} \tag{7}$$

where $M = V_{\mathrm{bat}}/V_{\mathrm{dc}}$ is the system voltage gain, indicating the voltage regulation degree of the PPC (this article designs the battery to share half of the dc bus voltage with $M = 0.5$, but other voltage designs are allowed according to the HFT voltage turn ratio), and $M_t = I_{\mathrm{ser}}/I_{\mathrm{bat}}$ represents the current regulation degree of the PPC at the T node.

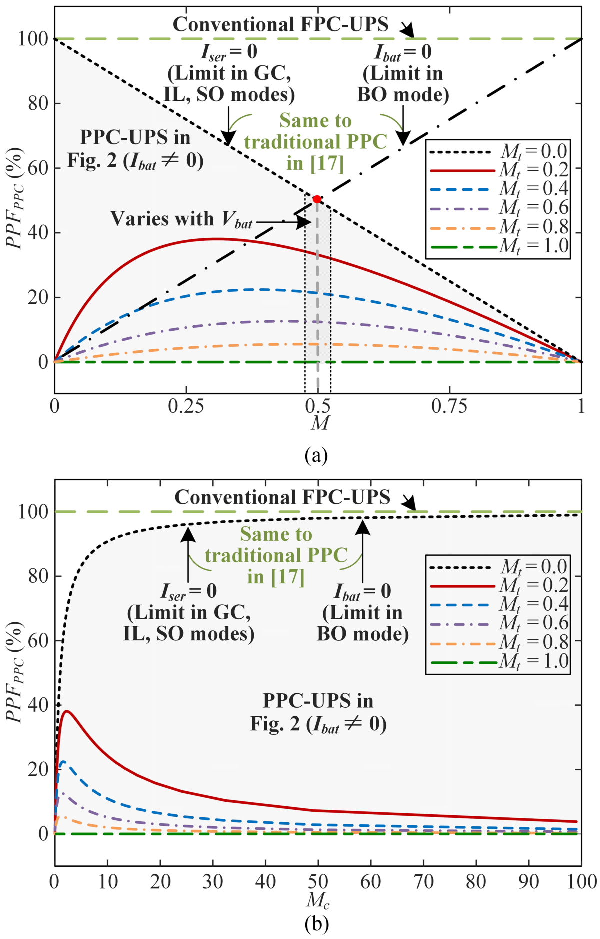
Further, $\mathrm{PPF_{PPC}}$ in (7) can be expressed as (8) against the converter voltage gain M_c and current regulation degree M_t.

$$\mathrm{PPF_{PPC}} = \begin{cases} \frac{\eta_c M_c}{\eta_c M_c+1} \times \frac{|1-M_t|}{1+M_c|M_t|}, & I_{\mathrm{ser}} \neq 0 \& I_{\mathrm{bat}} \neq 0 \\ \frac{\eta_c M_c}{\eta_c M_c+1}, & I_{\mathrm{ser}} = 0 \& I_{\mathrm{bat}} \neq 0 \\ \frac{\eta_c}{\eta_c M_c+1}, & I_{\mathrm{ser}} \neq 0 \& I_{\mathrm{bat}} = 0 \end{cases} \tag{8}$$

where $M_c = V_1/V_2$ is the converter voltage gain, and $M = 1/(1 + M_c)$.

For better illustration of the $\mathrm{PPF_{PPC}}$ variations against M and M_t, Fig. 3(a) exhibits $\mathrm{PPF_{PPC}}$ variations as produced by (7). When either $I_{\mathrm{bat}} = 0$ or $I_{\mathrm{ser}} = 0$ (which leads to $M_t = 0$), $\mathrm{PPF_{PPC}}$ variation is only affected by M, which has the same amount of processed power with the traditional PPC in [17]. When $M_t \neq 0$, $\mathrm{PPF_{PPC}}$ of the proposed PPC favorably further decreases compared to the traditional PPC in [17] as shown in the gray area of Fig. 3(a). In other words, the proposed PPC processes equal or less power compared to a single conventional PPC in [17]. In essence, this is caused by I_d which flows via the T circuit of the proposed PPC as shown in Fig. 2. In general, the amount of the PPC processed power, as indicated by $\mathrm{PPF_{PPC}}$, decreases when M is close to value at 1, or when M_t increases as shown in Fig. 3(a). Further, Fig. 3(b) displays the $\mathrm{PPF_{PPC}}$ variations against M_c and M_t. Similar to Fig. 3(a), $\mathrm{PPF_{PPC}}$ of the proposed PPC decreases when M_t increases in Fig. 3(b), indicating the less processed power of the proposed PPC compared to the traditional PPC in [17].

The proposed PPC for UPS can be regarded as an improved version of Type II PPC in [17]. Type II PPC in [17] only processes the partial power between the input and output two terminals. Nevertheless, the proposed PPC can not only process the partial power between the input terminal (dc bus) and output terminal (battery), but also compensate the current difference I_d between I_{ser} and I_{bat} at T node through regulating currents I_1 and I_2. This characteristic represents the most distinctive advantage in less processed power and smaller $\mathrm{PPF_{PPC}}$ of the proposed PPC compared to Type II PPC in [17].



(a)

(b)

Fig. 3. $\mathrm{PPF_{PPC}}$ variations under different voltage and current regulation degrees. (a) $\mathrm{PPF_{PPC}}$ variation against M and M_t. (b) $\mathrm{PPF_{PPC}}$ variation against M_c and M_t.

C. System Efficiency Evaluation of PPC-UPS

Further, the PPC-UPS can promote system-level power efficiency, which is deduced as follows.

The power losses of the PPC-UPS module can be expressed as

$$P_{\mathrm{PPC-loss}} = |V_1 I_1 - V_2 I_2|. \tag{9}$$

Combing (3) and (9), the PPC-UPS system efficiency $\eta_{\mathrm{s-PPC}}$ is given as

$$\eta_{\mathrm{s-PPC}} = \frac{P_{\mathrm{ser}} + P_{\mathrm{bat}}}{P_{\mathrm{ser}} + P_{\mathrm{bat}} + P_{\mathrm{PPC-loss}}} = \frac{\eta_c}{\eta_c + (1-\eta_c)\mathrm{PPF_{PPC}}}. \tag{10}$$

Equation (10) indicates that the system efficiency $\eta_{\mathrm{s-PPC}}$ depends on both the efficiency η_c of the converter itself and $\mathrm{PPF_{PPC}}$ of the PPC, different from the conventional FPC-UPS

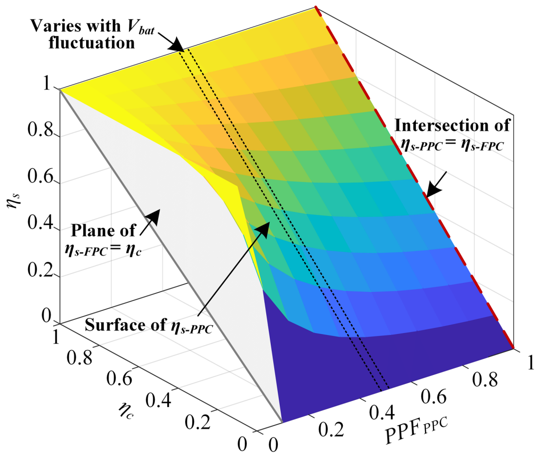


Fig. 4. 3-dimensional relationship of the system efficiency $\eta_{\text{s-PPC}}$ against η_{c} and PPF_{PPC} of the PPC-UPS, compared to $\eta_{\text{s-FPC}}$ of the conventional FPC-UPS.

system efficiency $\eta_{\text{s-FPC}} = \eta_{\text{c}}$ as stated in [17]. Fig. 4 exhibits $\eta_{\text{s-PPC}}$ variations of the PPC-UPS against η_{c} and PPF_{PPC} as expressed in (10), compared to $\eta_{\text{s-FPC}}$ of the conventional FPC-UPS. $\eta_{\text{s-PPC}}$ of the PPC-UPS as shown in the colored surface is always higher than the gray plane of $\eta_{\text{s-FPC}} = \eta_{\text{c}}$ of the conventional FPC-UPS as long as $\text{PPF}_{\text{PPC}} < 1$. The lower the PPF_{PPC} is, more obvious the system efficiency improvement of the PPC-UPS is, when compared to the conventional FPC-UPS. In a practical PPC-UPS, due to the specified narrow voltage variation of V_{bat}, PPF_{PPC} would fluctuate at the narrow variation as denoted in the mesh region of Fig. 3, so that $\eta_{\text{s-PPC}}$ would also fluctuate at the narrow band as shown in Fig. 4.

III. PPC-UPS MULTIMODE CONTROL STRATEGY

In this section, the control strategy for the proposed PPC-UPS module is elaborated to achieve the multimode operations of GC mode, IL mode, BO mode, and SO mode.

A. Fundamental Current and Voltage Controllers for PPC-UPS

A current controller for battery constant-current (CC) charging and a voltage controller to maintain server load voltage are designed, respectively, as shown in Fig. 5.

1) Current Controller for Battery Charging: The battery is typically charged with a constant current. In PPC-UPS, as $I_{\text{d}} = I_{\text{bat}} - I_{\text{ser}}$ as illustrated in (5), the battery current I_{bat} can be regulated indirectly by controlling I_{d} under a specific I_{ser}. Therefore, the CC reference $I_{\text{d-ref}}$ of the current controller for the PPC-UPS is designed as

$$I_{\text{d-ref}} = I_{\text{bat-ref}} - I_{\text{ser}}. \tag{11}$$

With $I_{\text{d-ref}}$ obtained by (11), a simple current proportional–integral (PI) controller (denoted as PI_{c} in Fig. 5) is design as

$$D_{c\text{-ref}} = \left(k_{c-p} + \frac{k_{c-i}}{s}\right)(I_{\text{d-ref}} - I_{\text{d}}) \tag{12}$$

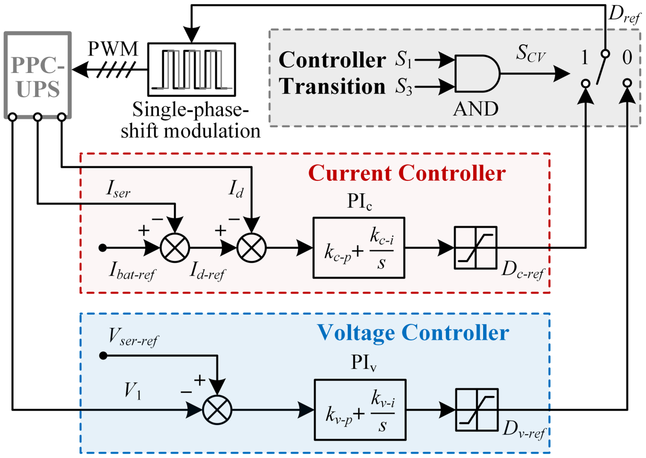


Fig. 5. Control strategy for PPC-UPS multimode operations.

where $D_{c\text{-ref}}$ is a phase-shift duty ratio reference generated by the PI_{c} controller for DAB single-phase-shift modulation, and k_{c-p} and k_{c-i} are the proportional and integral coefficients of PI_{c}, respectively.

With such current controller, I_{bat} could be regulated equal to $I_{\text{bat-ref}}$ through (11), even when I_{ser} varies with the practical server load power.

CC charging controller in (11) and (12) is widely utilized for rapid battery charging. As the battery approaches to full charged, the battery switches to the constant voltage (CV) charging to ensure the safety. Due to $V_2 = V_{\text{bat}}$, CV charging could be achieved by precisely regulating the FB_2 voltage V_2 at a constant reference value of $V_{\text{bat-ref}}$ with a PI controller, which is similar to the constant load voltage controller in (13) and will not be discussed in detail considering page limit.

2) Voltage Controller for Server Load: When the battery discharges, the server load voltage should be regulated stably. As explained in (4) that $V_1 = V_{\text{ser}}$, the FB_1 voltage V_1 shall be regulated at a constant value through a simple designed voltage PI_{v} controller, as

$$D_{v\text{-ref}} = \left(k_{v-p} + \frac{k_{v-i}}{s}\right)(V_{\text{ser-ref}} - V_1) \tag{13}$$

where $D_{v\text{-ref}}$ is a phase-shift duty ratio reference generated by the PI_{v} controller as shown in Fig. 5, and k_{v-p} and k_{v-i} are the proportional and integral coefficients of PI_{v} controller, respectively.

On top of these fundamental current controller and voltage controller, advanced operation modes shall be appropriately designed to tackle possible device contingencies. This will be detailed in the following subsection.

B. Designs of Four PPC-UPS Operation Modes

The following four possible PPC-UPS operation modes of GC mode, IL mode, BO mode and SO mode can be achieved using the current and voltage controllers in Section A manipulated by predefined decision logics. Table I summarizes the four designed PPC-UPS operation modes, judging from their relevant device statuses (ON = 1 / OFF = 0) to activate appropriate

TABLE I
DECISION LOGICS FOR MULTIMODE OPERATIONS

Operation Mode	Device Statuses S_1 (Rectifier)	 S_2 (Server)	 S_3 (Battery)	 S_{CV}	Activated Controller
GC mode	1	1	1	1	Current Controller
IL mode	0	1	1	0	Voltage Controller
BO mode	1	1	0	0	Voltage Controller
SO mode	1	0	1	1	Current Controller

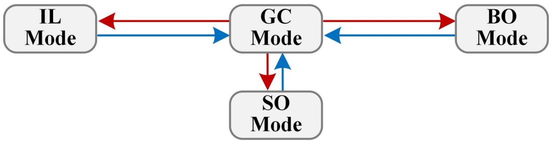


Fig. 6. Switching sequence among four PPC-UPS operation modes.

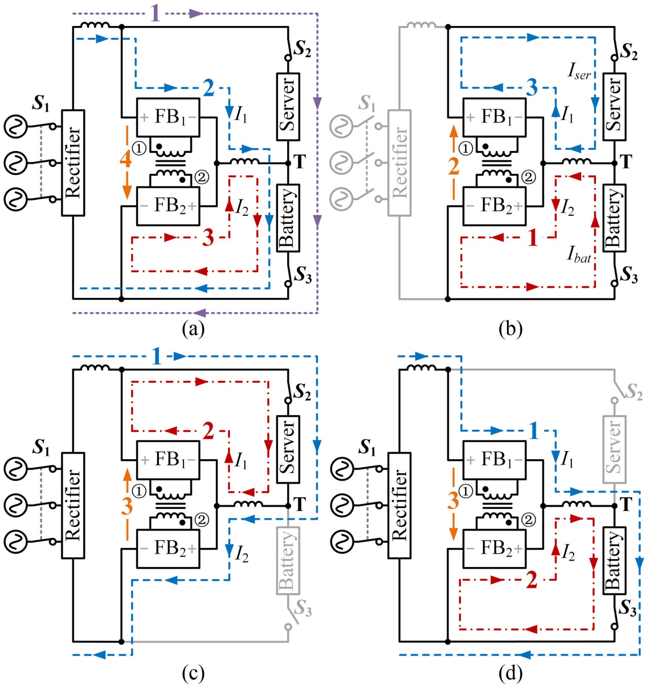


Fig. 7. Current flows of four PPC-UPS operation modes. (a) GC mode. (b) IL mode. (c) BO mode. (d) SO mode.

controllers. Fast electrical relays of S_1, S_2, and S_3 similarly to those adopted in [35] are the switches for ON or OFF transitions of the rectifier, the server load, and the battery, respectively, as shown in Fig. 2. Fig. 6 displays the switching sequence among four PPC-UPS operation modes. It is noted that there is no precheck when PPC-UPS shifts from GC mode to the other three modes as denoted in red arrows due to the device outage occurs suddenly, whereas precheck is needed when PPC-UPS shifts from one of the other three modes to GC mode as denoted in blue arrows to judge whether the device outage or failure has been solved.

From Table I, the current controller adopted in GC or SO mode is activated only when $S_1 = 1$ and $S_3 = 1$ but irrelevant to the value of S_2. The voltage controller is activated when $S_1 = 0$ & $S_3 = 1$ in IL mode, or when $S_1 = 1$ & $S_3 = 0$ in BO mode. From this basis on, a simple decision logic command S_{CV} implemented with a Logic AND for the transition between the current controller and the voltage controller is designed as

$$S_{\text{CV}} = S_1 \text{ AND } S_3. \tag{14}$$

The current controller is activated so that $D_{\text{ref}} = D_{c-\text{ref}}$ when $S_{\text{CV}} = 1$, whereas the voltage controller is activated with $D_{\text{ref}} = D_{v-\text{ref}}$ when $\bar{S}_{\text{CV}} = 1$ (i.e., $S_{\text{CV}} = 0$). When the current controller is activated, PI$_{\text{v}}$ in the voltage controller may be saturated. Once the saturated voltage controller is activated when $\bar{S}_{\text{CV}} = 1$, the windup caused by accumulated error in the integrator may occur. Thus, the antiwindup technique as presented in [36] is adopted to prevent windup of the controller during switching.

1) GC Mode: In GC mode, the power for the server load and the battery charging are simultaneously supplied by the utility via the dc bus, with all the relays S_1, S_2, and S_3 closed as shown in Fig. 7(a). The dc bus voltage is regulated by the front-end rectifier supported by the utility in GC mode, while the battery as an essentially voltage source needs to be controlled by the current controller. While V_{dc} is regulated at the nominal value, variation of the server voltage $V_{\text{ser}} = V_{\text{dc}} - V_{\text{bat}}$ can be effectively limited within a small deviation when V_{bat} fluctuates at the specified narrow voltage variation (i.e., 95%–105%). In this mode, the current controller as proposed in (11) and (12) is activated to realize the battery constant charging by the decision logic $S_{\text{CV}} = 1$ as presented in Table I.

In GC mode, there are four circuit branches carrying with currents as illustrated in Fig. 7(a). The dc-bus branch connecting the server and the battery in series delivers the common current I_{ser} to both the server load and the battery, as denoted with the purple dotted line. The other two circuit branches, through FB$_1$ and FB$_2$ respectively, compensate the current difference $I_{\text{d}} = I_{\text{bat}} - I_{\text{ser}} = I_1 + I_2$ at the T node as denoted in the blue dotted line and red chain-dotted line, respectively, which are regulated by the branch of HFT as denoted in the orange solid line.

As seen in Fig. 7(a), the PPC only processes the current difference I_{d} in GC mode, rather than large I_{ser} or I_{bat}. In GC mode, specific PPF_{PPC} can be evaluated through the case of $I_{\text{ser}} \neq 0$ and $I_{\text{bat}} \neq 0$ in (7), whose limit is 50% resulting from the intersection between the line of $M = 0.5$ and the gray area boundary as shown in Fig. 3.

2) IL Mode: IL mode is also known as an emergency supply mode, which is generally caused by grid blackout or the rectifier outage. Under such an event, the relay S_1 as shown in Fig. 7(b) is opened, shifting the PPC-UPS operation from GC mode to IL mode, enabling the server load to be continuously powered by the battery. Due to the absence of the dc bus voltage control by the rectifier in IL mode, the rectifier is outage and the server load voltage is maintained through the PPC by activating the voltage controller with the decision logic $S_{\text{CV}} = 0$ as presented in Table I.

As seen from the current flows in IL mode of Fig. 7(b), the battery current conducts through FB$_2$ to the HFT, while HFT transmits this power to the server load through FB$_1$. In IL mode, power supply to the load is achieved uninterruptibly under power islanding events.

Similar to GC mode, PPF_{PPC} in IL mode can also be evaluated through the case of $I_{\text{ser}} \neq 0$ and $I_{\text{bat}} \neq 0$ in (7), with a limit of 50%.

3) BO Mode: When conducting a periodical battery maintenance or battery being subject to an unexpected contingency, the battery is out of operation with the relay S_3 switched OFF as shown in Fig. 7(c), shifting the PPC-UPS from GC mode to BO mode. In BO mode, the server load is controlled through the PPC with the voltage controller as designed in (13) by the decision logic $S_{\text{CV}} = 0$ as presented in Table I, while the dc bus voltage is still regulated by the rectifier.

The PPC-UPS currents in BO mode are displayed in Fig. 7(c). The current from the dc bus is distributed to the server load simultaneously through both FB_1 and FB_2 as denoted in blue dotted line and red chain-dotted line, respectively. Meanwhile, FB_2 conducts power to FB_1 through the HFT as denoted in orange solid line.

In BO mode, PPF_{PPC} can be evaluated through the case of $I_{\text{ser}} \neq 0$ but $I_{\text{bat}} = 0$ in (7) denoted as the black chain-dotted line in Fig. 3, which is equal to 50% when $M = 0.5$.

4) SO Mode: The relay S_2 is switched OFF under the server outage due to planned or unplanned server disruptions, shifting the PPC-UPS from GC mode to SO mode. In SO mode, the voltages of the dc bus and the battery must be regulated standby for the potential reconnection of the server load. In SO mode, the PPC-UPS current controller as proposed in (11) and (12) is activated by the decision logic $S_{\text{CV}} = 1$ as presented in Table I to facilitate the battery charging, while the dc bus voltage is also regulated by the rectifier.

PPC-UPS currents in SO mode are displayed in Fig. 7(d). The current from the dc bus conducts to the battery simultaneously through both the PPC FB_1 and FB_2 as denoted in blue dotted line and red chain-dotted line, respectively. Meanwhile, FB_1 conducts power to FB_2 through the HFT as denoted in orange solid line.

In SO mode, PPF_{PPC} can be evaluated through the case of $I_{\text{ser}} = 0$ but $I_{\text{bat}} \neq 0$ in (7) denoted as the black dotted line in Fig. 3, which is also equal to 50% when $M = 0.5$.

IV. STABILITY ANALYSIS AND CONTROLLER OPTIMIZATION OF PPC-UPS THROUGH SSM

To optimize the parameters of the proposed PPC-UPS current and voltage controllers as presented in Fig. 5, the SSM for the PPC-UPS as shown in Fig. 2 is established in this section, with its system parameters as listed in Table II. The server load is modeled as a current source as in [27], and the battery is modeled as a voltage source as in [37].

The complete SSM of the PPC-UPS is established based on the state-space modular sub-systems of the circuits and controllers, which are connected as shown in Fig. 8. The SSM after linearization is expressed as

$$\begin{cases} \Delta\dot{\mathbf{X}} = \mathbf{A}\Delta\mathbf{X} + \mathbf{B}\Delta\mathbf{U} \\ \Delta\mathbf{Y} = \mathbf{C}\Delta\mathbf{X} + \mathbf{D}\Delta\mathbf{U} \end{cases} \tag{15}$$

TABLE II
SYSTEM PARAMETERS OF THE PPC-UPS

Elements	Items	Values
PPC-UPS circuit	Nominal DC bus voltage, $V_{dc\text{-}N}$	750 V
	HFT power rating	7500 W
	Server power (Inspur NF5280M5), P_{ser}	5 × (0 ∼ 1412 W)
	Server current, I_{ser}	0 A ∼ 18.6 A
	Battery configuration	30 × 12 V
	Battery voltage, V_{bat}	370 V
	Switching frequency, f_s	10 kHz
	HFT voltage turn ratio, n_1:n_2	1:1
	HFT leakage inductance, L_{dab}	0.23 mH
	Filtering inductance, L_1	1 mH
	Filtering inductance, L_2	0.5 mH
	Filtering capacitance, C_1	660 µF
	Filtering capacitance, C_2	660 µF
Controller	Charging current reference, $I_{bat\text{-}ref}$	20 A
	Server load voltage reference, $V_{ser\text{-}ref}$	380 V
	Current controller PI_c, ($k_{c\text{-}p}$, $k_{c\text{-}i}$)	(0.016, 0.211)
	Voltage controller PI_v, ($k_{v\text{-}p}$, $k_{v\text{-}i}$)	(0.006, 0.851)

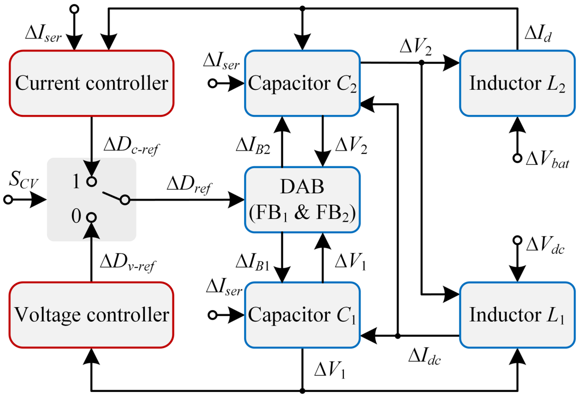


Fig. 8. Closed-loop SSM of the PPC-UPS.

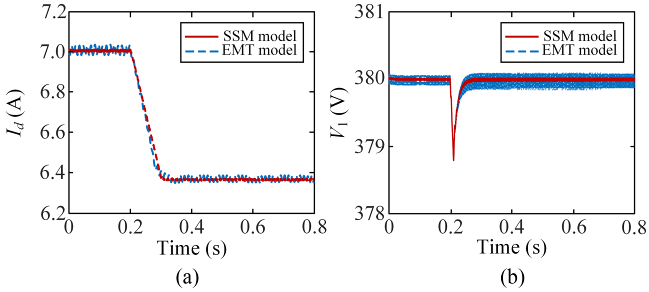
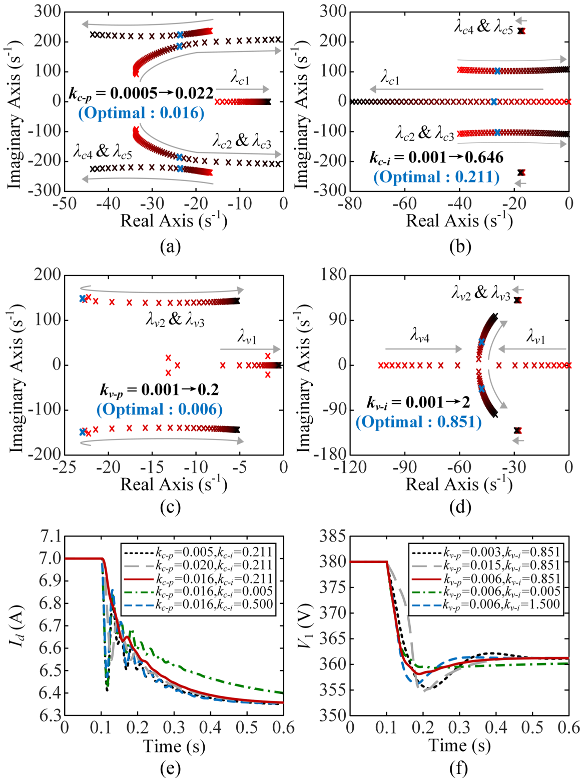


Fig. 9. Step response comparisons of the SSM model and EMT model. (a) I_d response. (b) V_1 response.

where Δ represents the small perturbation change; $\mathbf{X}$ is the state vector; $\mathbf{U}$ is the input vector; $\mathbf{Y}$ is the output vector; $\mathbf{A}$ is the state matrix after linearization; $\mathbf{B}$ is the input matrix; $\mathbf{C}$ is the output matrix; and $\mathbf{D}$ is the feedforward matrix. All of them are detailed presented in Appendix B.

The SSM response to a step increasing of the load from 13 to 13.65 A is compared to that of the same EMT simulation model, as seen in Fig. 9. The dynamic responses of the SSM in terms of I_d under the current controller in GC mode and V_1 under the voltage controller in IL mode as examples are accurately



(a) (b) (c) (d) (e) (f)

Fig. 10. Eigenvalue loci and dynamic responses with various control parameters. (a) $k_{c-p} = 0.0005 \longrightarrow 0.022$. (b) $k_{c-i} = 0.001 \longrightarrow 0.646$. (c) $k_{v-p} = 0.001 \longrightarrow 0.2$. (d) $k_{v-i} = 0.001 \longrightarrow 2$. (e) I_d dynamic response. (f) V_1 dynamic response.

aligned with those of the EMT simulation model, confirming the correctness and accuracy of the SSM.

To optimize the parameters of current controller PI$_\mathrm{c}$ and voltage controller PI$_\mathrm{v}$, the eigenvalue loci are obtained as shown in Fig. 10. Fig. 10(a) and (b) present the PI$_\mathrm{c}$ optimization, in which the increase of k_{c-p} moves the conjugated eigen pairs λ_{c2} & λ_{c3} toward the imaginary axis with its stability compromised, and meanwhile moves λ_{c4} & λ_{c5} away from the imaginary axis with its stability enhanced. λ_{c2} & λ_{c3} are shifted to the right-half plane of the instability area when k_{c-p} is greater than 0.022. The optimal $k_{c-p} = 0.016$ is identified, when the real-axis values of λ_{c2} & λ_{c3} and λ_{c4} & λ_{c5} match, with overall the furthest distance to the imaginary axis, as highlighted in bold blue in Fig. 10(a). Fig. 10(b) shows that the influence of k_{c-i} change on λ_{c2} & λ_{c3} is much larger than that on λ_{c4} & λ_{c5}. Similarly, the optimal $k_{c-i} = 0.211$ is identified with overall the furthest distance to imaginary axis.

Fig. 10(c) and (d) present the PI$_\mathrm{v}$ optimization. Fig. 10(c) shows that increasing k_{v-p} firstly moves λ_{v2} & λ_{v3} away from the imaginary axis and then toward the imaginary axis with damping ratio reduced, identifying the optimal $k_{v-p} = 0.006$ at the furthest distance to the imaginary axis. Fig. 10(d) shows that increasing k_{v-i} moves λ_{v1} & λ_{v4} toward each other in the real axis, until λ_{v1} & λ_{v4} become conjugated and move away from the real axis but towards the imaginary axis, identifying the optimal $k_{v-i} = 0.851$ at their damping ratio of 0.707.

Fig. 10(e) compares the system dynamic performances with different sets of k_{c-p} and k_{c-i}, under the step change of $I_{\mathrm{d}-ref}$ from 7 to 6.35 A. It can be observed that the identified optimal parameters result in an improved system dynamic performance over the other four nonoptimal parameter sets. Fig. 10(f) also confirms the improved dynamic performance with the identified optimal parameters of k_{v-p} and k_{v-i} under the step change of V_1 from 380 to 361 V.

The optimal controller parameters identified by the aid of SSM analysis above are applied to the hardware experiments in the next Section V.

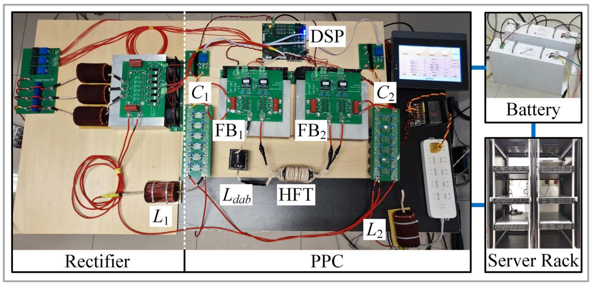
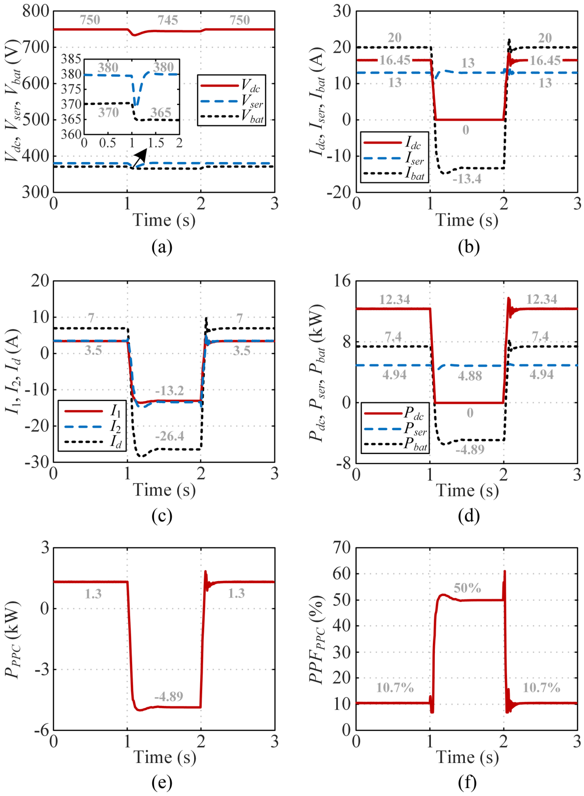


Fig. 11. Hardware experimental platform.



(a) (b) (c) (d) (e) (f)

Fig. 12. Experimental results under the temporary rectifier outage (GC Mode to IL Mode). (a) Voltages V_dc, V_ser, V_bat. (b) Currents I_dc, I_ser, I_bat. (c) Currents I_1, I_2, I_d. (d) Power P_dc, P_ser, P_bat. (e) Power P_PPC. (f) $\mathrm{PPF}_\mathrm{PPC}$.

V. HARDWARE VERIFICATIONS

In this section, hardware experiments are carried out to evaluate the performances of the proposed PPC-UPS scheme with the same system parameters as presented in Table II. The hardwares of the proposed PPC-UPS illustrated in Fig. 2 is established as shown in Fig. 11, in which the control system as shown in

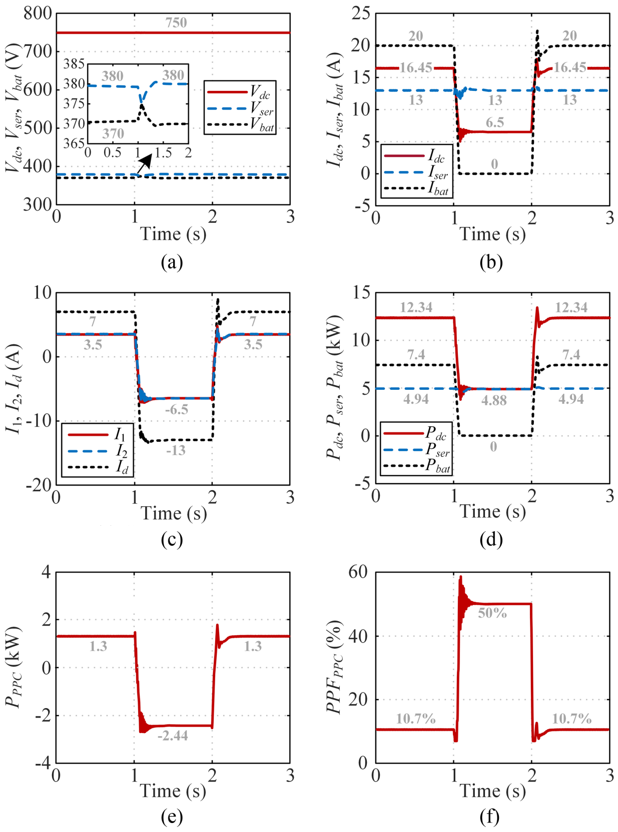


Fig. 13. Experimental results under the temporary battery outage (GC mode to BO mode). (a) Voltages V_{dc}, V_{ser}, V_{bat}. (b) Currents I_{dc}, I_{ser}, I_{bat}. (c) Currents I_1, I_2, I_{d}. (d) Power P_{dc}, P_{ser}, P_{bat}. (e) Power P_{PPC}. (f) $\mathrm{PPF}_{\mathrm{PPC}}$.

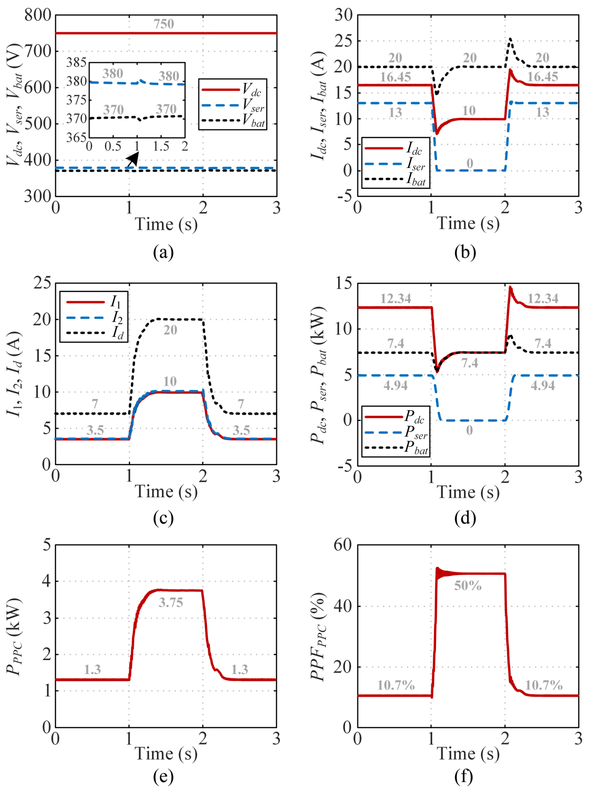


Fig. 14. Experimental results under the temporary server outage (GC mode to SO mode). (a) Voltages V_{dc}, V_{ser}, V_{bat}. (b) Currents I_{dc}, I_{ser}, I_{bat}. (c) Currents I_1, I_2, I_{d}. (d) Power P_{dc}, P_{ser}, P_{bat}. (e) Power P_{PPC}. (f) $\mathrm{PPF}_{\mathrm{PPC}}$.

Fig. 5, with optimal control parameters identified in Section IV, is programmed in the DSP controller of TMS320F28335.

Initially, the PPC-UPS operates in GC mode, with dc bus voltage and battery voltage at $V_{\mathrm{dc}} = 750$ V and $V_{\mathrm{bat}} = 370$ V, respectively, clamping the server load voltage at $V_{\mathrm{ser}} = V_{\mathrm{dc}} - V_{\mathrm{bat}} = 380$ V. The server load current and battery current are at $I_{\mathrm{ser}} = 13$A and $I_{\mathrm{bat}} = 20$A, respectively, with $I_{\mathrm{d}} = I_{\mathrm{bat}} - I_{\mathrm{ser}} = 7$ A at T node (the current of the PPC FB$_1$ and FB$_2$ $I_1 \approx I_2 \approx 3.5$ A). The $\mathrm{PPF}_{\mathrm{PPC}}$ of the PPC-UPS, as defined in (7), is approximately 10.7%.

Four case studies are conducted to evaluate the PPC-UPS performances as follows.

A. Case 1: Rectifier Outage (GC Mode to IL Mode)

The rectifier is temporarily out of operation during period $t = 1$ s ~ 2 s as shown in Fig. 12, with the relay S_1 opened, triggering a mode transition from GC mode to IL mode according to the decision logics as presented in Table I.

As shown in Fig. 12(a), the voltage controller is activated by IL mode at $t = 1$ s, uninterruptedly maintaining a constant V_{ser} at 380 V in the absence of the grid power support. It is clear in Fig. 12(b) that in IL mode the battery shifts to the discharging state with $I_{\mathrm{bat}} = -13.4$ A during $t = 1$ s $\sim$ 2 s. The current difference $I_{\mathrm{d}} = I_{\mathrm{bat}} - I_{\mathrm{ser}}$ at T node is regulated by the PPC FB$_1$ and FB$_2$ with $I_1 \approx I_2$ as show in Fig. 12(c), as explained in (5). $\mathrm{PPF}_{\mathrm{PPC}}$ is approximately 50% as shown in Fig. 12(f), indicating that the PPC processes only around 50% of the total power in IL mode.

At $t = 2$ s, when the rectifier is restored into operation, all the system states are rapidly recovered to the initial states with minimal overshoots as in GC mode as seen in Fig. 12.

B. Case 2: Battery Outage (GC Mode to BO Mode)

Fig. 13 evaluates the PPC-UPS performance under the temporary battery outage during $t = 1$ s $\sim$ 2 s, with S_3 opened against Table I, triggering a mode transition from GC mode to BO mode.

The voltage controller is activated in BO mode, continuously maintaining V_{ser} constant at 380 V as observed in Fig. 13(a). As shown in Fig. 13(b), $I_{\mathrm{d}} = -I_{\mathrm{ser}} = -13$ A is regulated through the PPC FB$_1$ and FB$_2$, with $I_1 \approx I_2 \approx -6.5$ A in Fig. 13(c). Fig. 13(d) and (e) shows that the power processed by PPC is -2.44 kW, much smaller than the server power $P_{\mathrm{ser}} = 4.88$ kW, which is again a key advantage of the PPC in terms of power efficiency enhancement.

C. Case 3: Server Outage (GC Mode to SO Mode)

Fig. 14 presents the PPC-UPS performance under the temporary server outage during $t = 1$ s $\sim$ 2 s, with S_2 opened, triggering a mode transition from GC mode to SO mode.

During the server outage, FB$_1$ in parallel with the server load manages to maintain the voltage of the server connection node at 380 V, as shown in Fig. 14(a), facilitating the server load

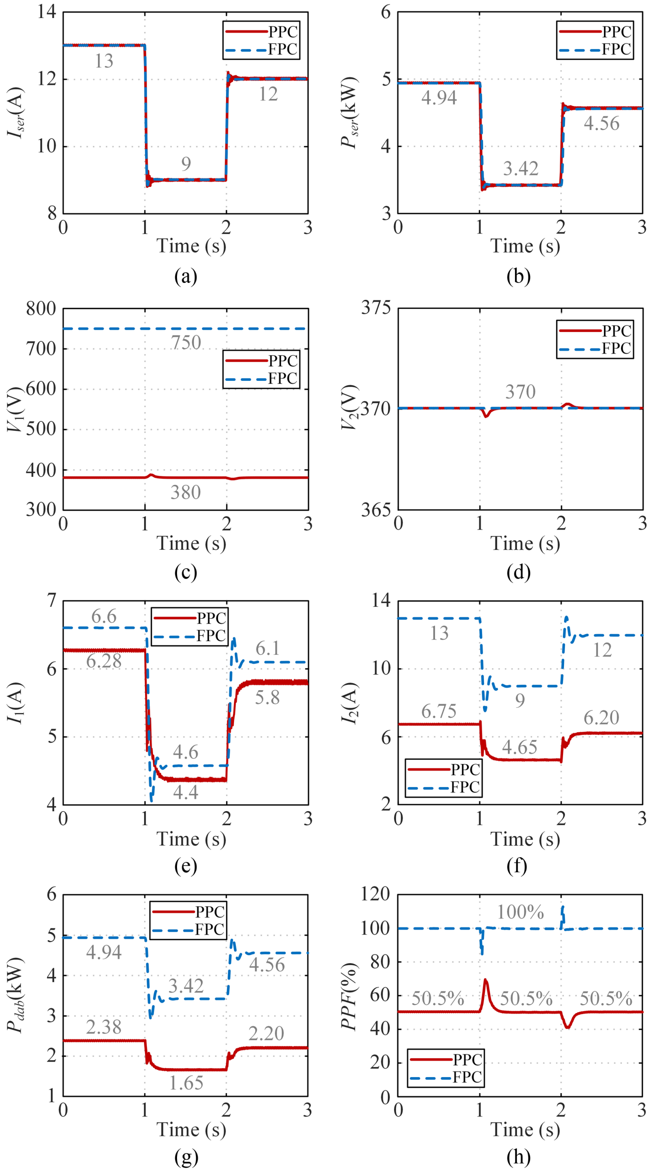


Fig. 15. Experimental results of comparisons between the proposed PPC-UPS and conventional FPC-UPS.(a) Server load current I_{ser}. (b) Server load power P_{ser}. (c) DAB FB$_1$ voltage V_1. (d) DAB FB$_2$ voltage V_2. (e) DAB FB$_1$ current I_1. (f) DAB FB$_2$ urrent I_2. (g) DAB power P_{dab}. (h) PPF.

reconnection. As shown in Fig. 14(b), the battery is charged with $I_{\text{d}} = I_{\text{bat}} = 20$A, being supplied through FB$_1$ and FB$_2$ equally as shown in Fig. 14(c). Figs. 14(d) and (e) indicate that $P_{\text{PPC}} = 3.75$ kW is smaller than $P_{\text{bat}} = 7.4$ kW, and the PPC only processes approximately 50% of P_{bat} when $P_{\text{ser}} = 0$ kW as shown in Fig. 14(f).

D. Case 4: Comparisons Between PPC-UPS and FPC-UPS

The performance of the PPC-UPS is compared to that of the conventional isolated DAB-based FPC-UPS scheme as shown in Fig. 1(b) under server load variations in GC mode, so that both converter efficiencies of which are consistent and only system efficiencies are compared. As shown in Fig. 15, the operation states of $V_{\text{bat}} = 370$ V, $V_{\text{ser}} = 380$ V and $I_{\text{bat}} = 0$ A, as well as other variables V_{dc}, I_{dc}, I_{ser} are identical to both schemes. As can be observed in Fig. 15(c), V_1 of the PPC-UPS, due to the parallel connection of the PPC-UPS FB$_1$ with the server load at 380 V, is much lower than that of FPC-UPS which is directly connected to the dc bus at 750 V. Thus, the rated voltage of FB$_1$ in PPC-UPS is favorably less than that of the FPC-UPS. Furthermore, as shown in Fig. 15(e) and (f), both I_1 and I_2 of FB$_1$ and FB$_2$ currents in the proposed PPC-UPS are obviously smaller than those of the FPC-UPS under different I_{ser}, effectively reducing the DAB

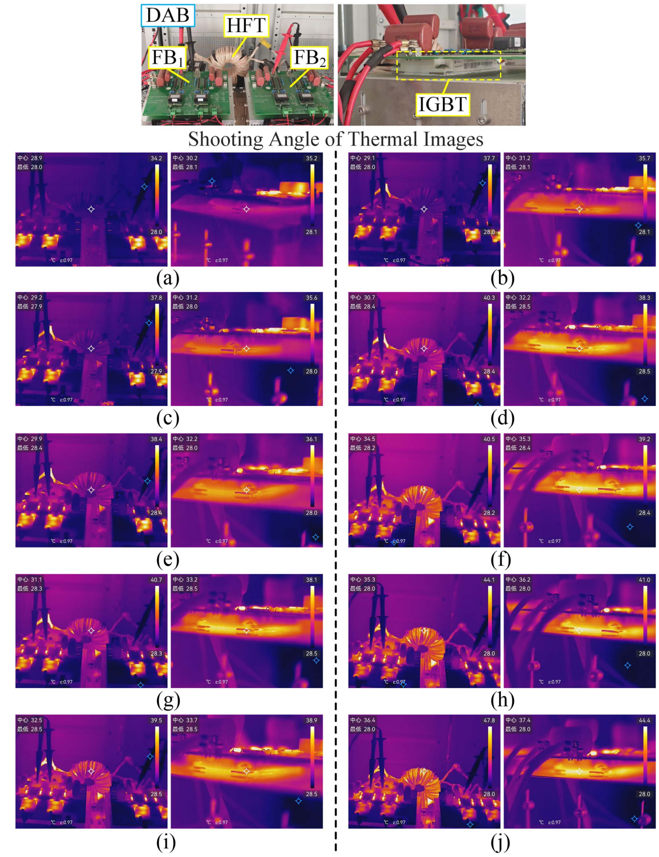


Fig. 16. Thermal images under varying load conditions of PPC and FPC. (a) 20% load of PPC. (b) 20% load of FPC. (c) 40% load of PPC. (d) 40% load of FPC. (e) 60% load of PPC. (f) 60% load of FPC. (g) 80% load of PPC. (h) 80% load of FPC. (i) 100% load of PPC. (j) 100% load of FPC.

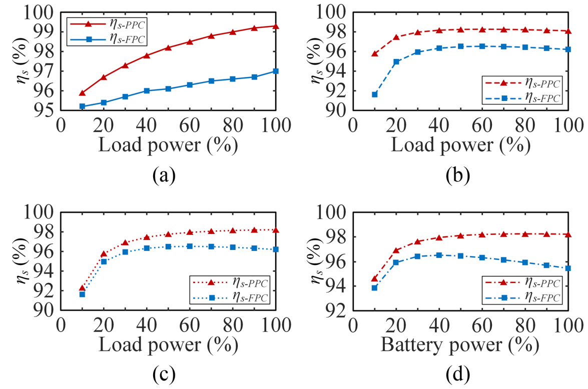


Fig. 17. System efficiency curves of PPC-UPS and FPC-UPS. (a) GC mode. (b) IL mode. (c) BO mode. (d) SO mode.

power losses. Both smaller values of PPC-UPS V_1 and I_1 result in less DAB power losses than that of FPC-UPS as shown in Fig. 15(g). As a result, smaller PPF for the PPC-UPS compared to that of the conventional FPC-UPS, as shown in Fig. 15(h).

Fig. 16 compares the thermal images of DAB and its one IGBT switch under varying load conditions in the proposed PPC-UPS and the conventional FPC-UPS. The results demonstrate lower operating temperatures of DAB and IGBT across all load conditions in the proposed PPC-UPS scheme, compared to the conventional FPC-UPS scheme. Such thermal advantage stems from the partial power processing capability of PPC, which effectively reduces the conduction and switching losses of the converter.

Furthermore, Fig. 17 compares the system efficiency curves of PPC-UPS and FPC-UPS under four operation modes. As clearly demonstrated in Fig. 17, the proposed PPC-UPS obtains higher system efficiency than the conventional FPC-UPS, throughout the entire power range from light to heavy load conditions. This superiority can be attributed to the partial power processing capability with less converter losses in the proposed PPC-UPS. Due to the power processed by the proposed PPC is equal to the DAB transferred power, the power loss composition, and the loss breakdown of PPC are identical to those of the DAB, which has been extensively and deeply studied in [38], [39], [40], [41] and will not be discussed in detail. Besides the system-level efficiency improvement through the PPC in this article, various device-level efficiency enhancement approaches as presented in [38], [39], [40], [41] can be applied simultaneously for comprehensive efficiency improvement of PPC-UPS further.

In addition, the proposed PPC-UPS scheme also exhibits the better performance compared to the scheme implemented with two Type II PPCs (as presented in [17]) as shown in Fig. 1(b). On the one hand, unlike two Type II PPCs to interconnect the dc bus, the server load, and the backup battery three terminals, the proposed PPC-UPS scheme coordinates these three terminals through only one PPC. This significantly reduces the required number of converters along with their associated semiconductor switches, inductors, and capacitors, thereby decreasing both the system complexity and the component count while enhancing the UPS modularity and scalability. On the other hand, as analyzed in Section II, the proposed PPC processes equal or less power compared to a single conventional PPC in [17]. Consequently, the proposed PPC-UPS scheme would achieve the reduced power losses and the improved overall system efficiency, when compared to the scheme implemented with two Type II PPCs.

VI. CONCLUSION

A novel PPC-UPS scheme for dc power feeding servers in data centers is proposed in this article. The proposed scheme employs only one PPC to modularly integrate a server load and a distributed backup battery to a common dc bus, effectively reducing the converter number when compared to the traditional FPC-based schemes. The PPC-UPS diverts the battery energy directly to the dc load but only processing a fraction of the load power, reducing converter power losses. On top of the proposed circuit topology, a multimode control scheme for PPC-UPS, with designed controllers and their decision logics for mode switching, is designed to autonomously and flexibly secure its uninterruptible operations under possible contingencies. In future, the proposed PPC-UPS scheme will significantly promote the scalability for data center UPS on a server-level basis.

APPENDIX

A. Inductor Selection

Inductors L_1 and L_2 can be selected with (A.1)

$$\begin{cases} L_1 \geq \frac{V_{\text{dc}}-[V_1+(n_2/n_1)V_1]}{2f_{\text{s}}\Delta I_{\text{dc,max}}} \\ L_2 \geq \frac{(n_2/n_1)V_1-V_{\text{bat}}}{2f_{\text{s}}\Delta I_{\text{bat,max}}} \end{cases} \tag{A.1}$$

where $\Delta I_{\text{dc,max}} = 5\% I_{\text{dc},N}$, and $\Delta I_{\text{bat,max}} = 5\% I_{\text{bat},N}$.

B. SSM of PPC-UPS

For the PPC-UPS with the multimode control strategy, the state vector $\Delta\mathbf{X} = [\Delta I_{\text{dc}}, \Delta I_{\text{d}}, \Delta V_1, \Delta V_2, \Delta z]^{\text{T}}$, the input vector $\Delta\mathbf{U} = [\Delta V_{\text{dc}}, \Delta V_{\text{bat}}, \Delta I_{\text{ser}}, \Delta D_{\text{ref}}, \Delta I_{\text{d}-\text{ref}}, \Delta V_{\text{ser}-ref}]^{\text{T}}$ and the output vector $\Delta\mathbf{Y} = [\Delta D_{\text{ref}}]$. The state matrix $\mathbf{A}$, the input matrix $\mathbf{B}$, the output matrix $\mathbf{C}$ and the feedforward matrix $\mathbf{D}$ are given as

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 \\ \frac{1}{C_1} & 0 & 0 & -\frac{G_2}{C_1} & 0 \\ \frac{1}{C_2} & -\frac{1}{C_2} & \frac{G_2}{C_2} & 0 & 0 \\ 0 & -S_{\text{CV}}k_{c-i} & -\bar{S}_{\text{CV}}k_{v-i} & 0 & 0 \end{bmatrix} \tag{A.2}$$

$$\mathbf{B} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{L_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_1} & -\frac{G_1}{C_1} & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} & \frac{G_3}{C_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{\text{CV}}k_{c-i} & \bar{S}_{\text{CV}}k_{v-i} \end{bmatrix} \tag{A.3}$$

$$\mathbf{C} = \begin{bmatrix} 0, & -S_{\text{CV}}k_{c-p}, & -\bar{S}_{\text{CV}}k_{v-p}, & 0, & 1 \end{bmatrix} \tag{A.4}$$

$$\mathbf{D} = \begin{bmatrix} 0, & 0, & 0, & 0, & S_{\text{CV}}k_{c-p}, & \bar{S}_{\text{CV}}k_{v-p} \end{bmatrix} \tag{A.5}$$

where $G_1 = n_1 V_2(1 - 2D_{\text{ref}})/(2n_2 f_{\text{s}} L_{\text{dab}})$, $G_2 = n_1 D_{\text{ref}}(1 - D_{\text{ref}})/(2n_2 f_{\text{s}} L_{\text{dab}})$, $G_3 = n_1 V_1(1 - 2D_{\text{ref}})/(2n_2 f_{\text{s}} L_{\text{dab}})$.

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