Letters

A Low-Frequency *LC*-Resonant Inverter Architecture and its Demonstration in BLDC Drive Application

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***Abstract*—This letter presents a low-frequency *LC*-resonant inverter architecture for brushless dc (BLDC) motor drives that eliminates the conventional 3-phase half-bridge structure and its inherent high-side switching challenges. The proposed topology employs only low-side power devices and utilizes an *LC* resonance mechanism to directly synthesize sinusoidal winding currents from square-wave inputs of the same frequency. This approach enables low-frequency sinusoidal current generation without high-frequency PWM chopping, significantly reducing electromagnetic interference and switching stress on power devices. A restructured 3-phase 6-terminal BLDC winding enables independent current injection into each phase, facilitating the realization of stable and low-distortion sinusoidal excitation. Hardware experiments validate the feasibility of the architecture, achieving stable motor operation at 2286 rpm with smooth current waveforms at the *LC* resonance frequency of 266 Hz. Beyond BLDC applications, the demonstrated ability to generate intrinsic low-frequency resonance without high-frequency excitation may provide a novel foundation for applications such as wearable or implantable biomedical power transfer, underwater wireless communication, brain–computer interface systems, etc.**

***Index Terms*—Brushless DC (BLDC) motor, high reliability, low-frequency *LC* resonance, sinusoidal driver.**

I. Introduction

THE brushless dc motor (BLDC) is widely adopted in applications such as electric vehicles, drones, robotics, and industrial automation. Conventional BLDC drives are typically based on a 3-phase half-bridge inverter architecture with both high-side and low-side power switches to generate SPWM or SVPWM voltages and produce sinusoidal currents in the motor windings, as shown in Fig. 1(a). This classical topology has served as the foundation for BLDC drive systems, based on which, a range of technologies have emerged, including control algorithms [1], power device advancements [2], [3], [4], [5], gate driving, and protection circuits.

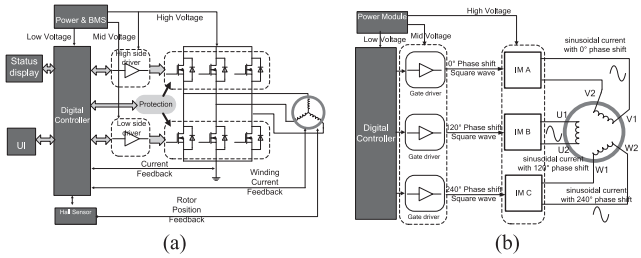

Fig. 1. (a) Conventional BLDC driving architecture with 3-phase half-bridge. (b) Novel architecture proposed.

The third-generation power semiconductor devices such as GaN and SiC have opened new possibilities for improving BLDC drive performance for their superior properties, including high breakdown voltages, faster switching speeds, and lower conduction losses compared to conventional silicon-based devices, making them promising for next-generation high-efficiency, high-power-density motor drive systems, particularly in high-speed and space-constrained applications.

However, integrating GaN or SiC devices into conventional half-bridge architectures introduces new challenges. The high dV/dt and dI/dt of these devices lead to significant reliability concerns, including low-side switches false turn-ON events, increased electromagnetic interference (EMI), and premature failure of motor insulation and bearings [6], [7], [8], [9], [10], [11]. Although several studies have proposed mitigation techniques [12], [13], [14], [15], [16], [17], [18], these solutions can only alleviate rather than eliminate the underlying issues. As operating voltages and switching frequencies continue to rise, the fundamental limitations of the half-bridge topology become increasingly pronounced.

In the specific context of BLDC drives, we argue that the half-bridge structure is not an inherent necessity, especially considering that the desired current is sinusoidal. According to the [19], the inverse class-E ZVS inverter is a possible solution as it could output the sinusoidal current for the wireless power transfer (WPT) applications, unfortunately, the startup of the BLDC requires the low-frequency sinusoidal magnetic field, whereas the realization of a low frequency class-E is difficult, furthermore, the inverse class-E inverter delivers power during

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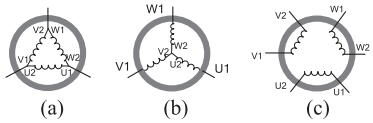

Fig. 2. The conventional BLDC (a) △ and (b) Y winding style; (c) the isolated winding style for the 3P6T BLDC.

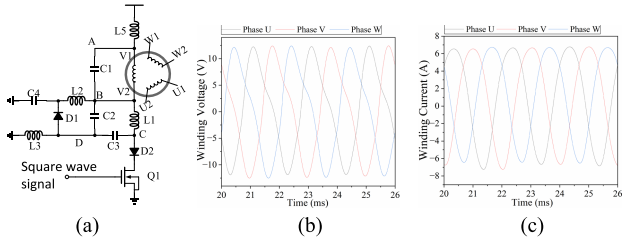

Fig. 3. (a) Intrinsic circuit of the IM, (b) voltage, and (c) current on the windings by the SIMPLIS simulation.

only one half of the switching cycle and relies on the load-side capacitor to maintain voltage continuity, whose power transfer capability is limited and not suitable for the BLDC driving.

In the letter, we propose a novel drive architecture that eliminates the bridge structure with no high-side power devices that capable of directly synthesizing 3-phase sinusoidal current in the motor windings using *LC* resonance. With the induction of a parasitic dc-dc boost converter, the topology achieves full-cycle excitation to the BLDC without relying on any conventional half-bridge structures, which offers several advantages: it eliminates reliability issues associated with high dV/dt and dI/dt, simplifies gate driver design, reduces overall system complexity, and significantly reduces the EMI. Experimental results show that the prototype achieves stable *LC* resonance at 266 Hz while driving a BLDC motor at 2286 rpm, validating both the feasibility and the power transfer capability of the proposed low-frequency resonant architecture. These results suggest a promising pathway not only for reliable and high-performance BLDC drives, but also for potential extensions to low-frequency resonant applications, such as implantable biomedical power transfer, underwater magnetic communication, and brain-computer interface systems.

II. Mechanism and Simulation Studies

Unlike the conventional 3-phase half-bridge driver, the proposed architecture [see Fig. 1(b)] employs three low-frequency square-wave signals with each phase-shifted by 120°generated by a digital controller and fed into three inverter modules (IM). Notably, the square-wave signals are not high-frequency SPWM or SVPWM signals; their frequency equals that of the desired sinusoidal current in the motor windings. Each IM itself converts its square wave directly into a 3-phase sinusoidal current for BLDC excitation via *LC* resonance, obviating any bridge topology or high-side switches.

Before digesting into the IMs, the motor winding must be reconfigured, a 3-phase, 6-terminal (3P6T) winding is required. As shown in Fig. 2, the 3P6T winding comprises 3electrically isolated coils, each brought out to two terminals (U_1/U_2, V_1/V_2, W_1/W_2). This isolation allows each phase to be independently driven by its own sinusoidal current. Moreover, because the 3 windings are in parallel magnetically rather than interconnected, the 3P6T configuration delivers higher torque and power under identical flux conditions, avoiding the mutual flux cancellation inherent in the Y or Δ connections.

The intrinsic circuit of the IM for the terminal V_1/V_2 and the 3-phase sinusoidal voltage and current on the winding by simulation are shown in the Fig. 3(a), (b), and (c), respectively. The winding is embedded inside of the IM, no bridge structures exist and the low-side power FET (Q1) is the only active device with absolutely no high-side active device; thus, the dV/dt issue is eliminated. Furthermore, the circuit is free of high-frequency source or switch, which significantly reduces the EMI.

The operation of the IM is complicated but interesting, as shown in the Fig. 4(a), there are seven states from (1) to (7) in a full cycle, and the waveforms for critical device are shown in Fig. 4(b). Two mechanisms exist in the IM, one is the *LC* resonator for the sinusoidal current generation, the other is the parasitic dc-dc boost converter to compensate the dc offset at the output. The *L4* and *R1* are introduced to represent the winding inductance and electromotive force (EMF) of the BLDC for the successive circuit simulation.

As shown in Fig. 4(a), the *LC* resonator is composed of *L4* (the winding inductance), *L5, L1, C3*, and *L3*. Ideally, a sinusoidal current is generated in L4 due to the *LC* resonance. However, it is not feasible to drive the 3P6T BLDC with such *LC* resonator, because the sinusoidal signal decays due to parasitic resistance especially at low frequency; moreover, dc offset exists in *L4*. To address the issue of the current decay, Q1 and D2 are introduced at node C. In the state (1), when Q1 initially turns OFF, the freewheeling current flowing through *L5, L4, L1*, and *L3* charges capacitor *C3* using energy from the voltage source. During this process, the voltage across *C3* increases while the current through the inductors decreases. Once the inductor current reaches zero, the voltage on *C3* peaks and begins to recharge the voltage source through the loop formed by *L3, L1, L4*, and *L5* while Q1 remains OFF. At this point, the current through the inductors begins to rise in the reverse direction, which is the state (2) in the Fig. 4.

As the inductors are negatively energized and before *C3* is fully discharged, Q1 turns ON. At this moment, the voltage at node C is sharply pulled down to ground by Q1. Due to the fact that the voltage across C3 cannot change instantaneously, node D also experiences a rapid voltage drop, as the state (3) shown in Fig. 4. This abrupt voltage change causes the current in L3 to rise sharply, charging C3 through the path: node D→C3→D2→Q1→ ground. As a result, the voltage at node D rises immediately due to the sudden peak charging current, preventing *L3* from continuing to deliver high current to *C3*, the remaining freewheeling current in *L3* is redirected through D1 to capacitor *C4*, forming a parasitic dc-dc conversion path. This transition causes a negative current peak in *L3*, as shown in the Fig. 4(a)(3) and (b), indicating a rapid energy transfer from *L3* to *C3*, which breaks the *LC* resonance equilibrium and helps suppress the natural decay of the sinusoidal current. Next, the freewheeling current in *L3, L1, L4*, and *L5* resumes charging *C3* and the voltage source. Since *C3* is now charged in reverse, the

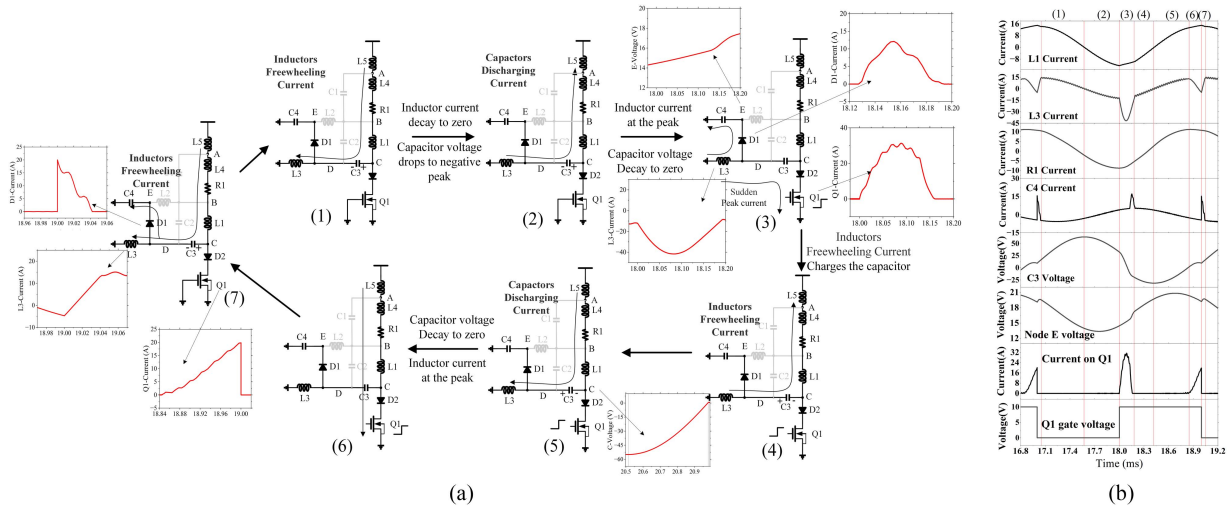

Fig. 4. Operation of the IM in a full cycle with 7 states, the *R1* and *L4* represent the BLDC EMF and winding in the circuit simulation by the SIMPLIS, where the power device switches are not used for DC chopping but rather to regulate and sustain the *LC* oscillation at the low frequency, preventing its decay and is free of the current and voltage ripple, no high frequency source exists.

voltage at node C becomes negative, which effectively turns OFF Q1 at its drain terminal even though the gate remains ON, due to the presence of diode D2 as illustrated in the state (4) in Fig. 4.

As *C3* continues to be reverse-charged by the freewheeling current from the inductors while Q1 remains ON, the voltage on the *C3* increases to the negative peak and the inductors current decrease to zero in a sinusoidal manner. The current then reverses direction: Now flowing from the voltage source through *L5, L4, L1, C3*, and *L3* to ground as the energy stored in *C3* begins to discharge. This causes the voltage at node C to rise (state 5). Since the GATE voltage of Q1 remains high, once the voltage at node C exceeds the threshold voltage of diode D2, the energizing current from the voltage source flows through *L5, L4, L1, D2*, and Q1 directly to ground bypassing *C3* and *L3*, which causes a sudden drop in current through *C3* and *L3* as illustrated in the state (6). Meanwhile, the residual freewheeling current in *L3* continues to charge *C3*.

Then, the next cycle begins and Q1 is turned OFF by the GATE signal, the freewheeling current from *L5, L4*, and *L1* continues to flow through *C3* and *L3*. As the *L3* current experienced a drop whereas and *L1* current increase in the state (6), the current through *L3* is momentarily smaller than that through *L1*. As a result, the excess current from *L1* flows through D1 to charge *C4*, thereby activating the parasitic dc-dc converter that compensates for the dc offset at the output, as shown in state (7) in the Fig. 4(a).

This process then repeats, generating sinusoidal current in the winding via *LC* resonance, following which, Q1 is again turned OFF by the gate signal, and the freewheeling current from *L5, L4, L1*, and *L3* charges *C3* once again, as shown in Fig. 4(a), initiating a new cycle from state (1) again.

Because the voltage source is positive, a dc component inevitably exists in the sinusoidal current through *L4*. To address this, *C4* and D1 are introduced to form a parasitic boost dc-dc converter. In the state (3) and (7), the current flowing through *L3* and *C3* is unbalanced, the excess current charges *C4* via D1, thereby boosting the voltage at node E. Although the voltage on *C4* (node E) fluctuates sinusoidally due to the resonance

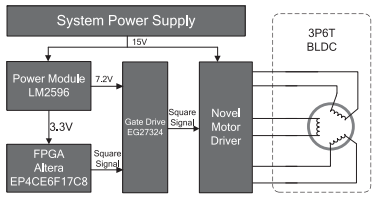

Fig. 5. Experimental setup of the BLDC driver.

and is unable to be modeled at the current stage, a positive dc offset higher than the voltage source is established as Fig. 4(b) shows. This offset compensates the output voltage and effectively eliminates the dc component across *C1*, providing the full-cycle excitation to the *L4* and enabling a pure sinusoidal output.

In addition, *C2* and *L2* are introduced to decouple mutual energy exchange between elements and to sustain the freewheeling paths for the capacitors and inductors.

III. Experimental Results

As a novel architecture, no existing literatures reports relevant algorithm and control method, therefore, we adopt an open-loop control scheme to demonstrate the feasibility of the mechanism. The experimental setup is as shown in Fig. 5. SENQI-VE500 is used as the voltage source to provide the 15 V voltage for the whole system, which is then converted to 7.2 V and 3.3 V voltage by the LM2596 development board to provide power for the gate drive (EG27324) and the FPGA (EP4CE6F17), respectively. The FPGA generates three 3.3 V square-wave at the frequency of 266 Hz as the gate signals, each phase-shifted by 120°. As the most vulnerable member in the power-device family, GaN transistors (RC65D110A) are used in each IM as the switching device (Q1) to demonstrate the reliability of the novel BLDC driver. As noted previously, square waves applied on the Q1 are converted by the IMs into 3-phase sinusoidal winding currents with the same frequency to drive the BLDC.

Fig. 6. (a) 3P6T BLDC, (b) winding style, and (c) test bench.

TABLE I
DEVICE PARAMETER FOR THE EXPERIMENTAL SETUP OF ONE IM

Inductors	Inductance(H)	Capacitors	Capacitance(F)
L1	1m	**C1**	85μ
L2	50μ	**C2**	200n
L3	50μ	**C3**	200μ
L5	50μ	**C4**	470μ

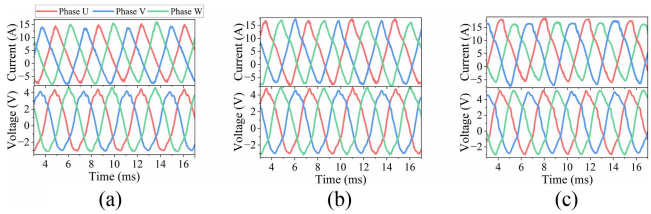

Fig. 7. Measured voltage and current on each winding with duty cycle of (a) 40%, (b) 50%, and (c) 60%, the voltage and current THD are 8.91%, 13.33%, 7.74%, and 9.33%, 16.56%, 9.37%, respectively.

A DJI M2212 compatible BLDC with seven pole-pairs served as the load. The 3 windings were rewired as electrically isolated coils (3P6T configuration), yielding six external terminals [see Fig. 6(a)]. Each winding measured 50 μH are shown in Fig. 6(b). The parameters of the passive devices are listed in the Table I, under open-loop excitation at a square-wave period of 3.75 ms and 50% duty cycle, the motor reached 2286 rpm as shown in the Fig. 6(c), confirming the feasibility of the topology and the correctness of the mechanism.

The measured voltage and current on each winding with driving square wave duty cycle of 40%, 50%, and 60% under the period of 3.75 ms (266 Hz) are shown in the Fig. 7. All voltage and current waveforms experience some distortions in Fig. 7 instead of the perfect sinusoidal in the simulation, this is because the simulation of the BLDC behaviors is almost impossible with the circuit simulator. As an electro-mechanical device, the position of the rotor is unable to be modeled by a circuit simulator, an inductor and a resistor are used in our SIMPLIS simulation to represent the winding inductance and EMF generated by the BLDC as shown in the Fig. 4, which is undoubtedly inaccurate, as a result, deviations exist between the simulation and experimental results. However, although the winding voltage is not the perfect sinusoidal, it successfully drives the BLDC with GaN device. Furthermore, experimental results with 40%, 50%, and 60% duty cycles confirm that the inverter sustains stable resonance and sinusoidal current generation across this range, which demonstrates the inherent robustness and practical applicability to BLDC drive systems.

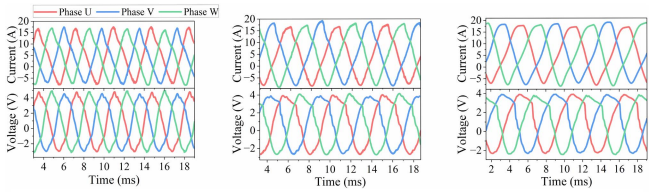

Fig. 8. Winding voltage and current with the input square-wave period of (a) 3.75 ms, (b) 4.75 ms, and (c) 5.75 ms.

TABLE II
MEASURE VALUE OF THE WINDING CURRENT AND VOLTAGE

Speed	2285 rpm	1804 rpm	1490 rpm
Peak-to-Peak Volt. (V)	7.8339	6.697	6.232
Maxim Volt. (V)	4.7857	4.008	3.923
Minimum Volt. (V)	-3.0482	-2.689	-2.309
Volt. offset (V)	0.6595	0.807	0.86875
Peak-to-Peak Cur. (A)	25.683	25.705	26.111
Maxim Cur. (A)	17.476	17.663	17.943
Minimum Cur. (A)	-8.207	-8.448	-7.762
DC offset (A)	4.6075	4.6345	5.0905
Voltage THD (%)	13.33	15.36	6.71
Current THD (%)	16.56	9.47	10.20

Another issue is the high winding-current and dc offset in the Fig. 7. As a high-speed BLDC with low winding inductance, high winding-current is needed for the initial start to compensate its low torque otherwise the rotor will remain stationary. Unfortunately, as a novel structure, no existing literatures reported the close-loop control method, furthermore, if a high-frequency square-wave excitation were used, the torque is too small to overcome the inertia of the rotor because the rotor acceleration required for startup is high under the high-frequency. Consequently, we have to drive the BLDC at the open-loop configuration with fixed low frequency. Because the EMF is small at low speed, the winding, therefore, experiences high current and the voltage and current phase-lag is small in the Fig. 7. The voltage drops on the parasitic resistance is high with the large winding-current, which causes the dc offset.

As Fig. 8 shows, the frequency of output voltage changes with the input square-wave period of 3.75 ms, 4.75 ms, and 5.75 ms, respectively, with the fixed duty cycle. The waveform data is listed in the Table II, with higher frequency, the BLDC rotor always generates larger EMF on the winding, as a result, the voltage on the winding is higher and the current is much smaller, so too is the dc offset, higher frequency introduces the smaller dc offset, which agrees on with the analysis above. As an electro-mechanical device, the operation of the BLDC, including back-EMF, rotor position, and speed change the effective load seen by the resonator, which impacts the THD together with the *LC* operation frequency itself, therefore, the THD under different frequency or duty cycle indicates no monotonic behaviors, as shown in Fig. 7 and Table II.

The dc offset produces an unwanted magnetic flux in the core, which causes partial saturation, torque ripple, and increased losses, thereby reducing overall efficiency and smoothness of operation. Precise modeling and closed-loop current regulation can reduce the offset. However, a solution that allows complete dc cancellation at the flux level is available in practice, bifilar

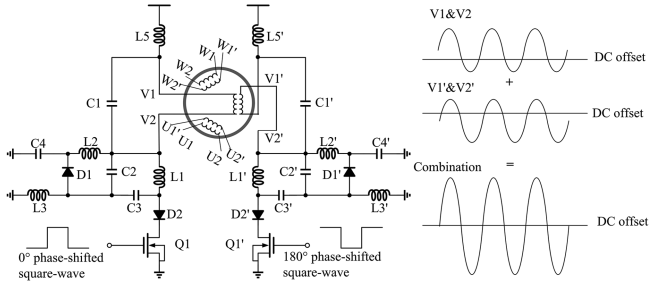

Fig. 9. Bifilar configuration for DC offset cancellation. Each phase employs two electrically isolated windings with opposite polarities, driven by 180° phase-shifted square-wave voltages. The current in the winding pair are sinusoidal + DC and sinusoidal–DC, respectively. Due to the opposite winding orientations, the sinusoidal flux components reinforce each other, while the DC components cancel out.

winding that applied in the single-phase BLDC [20] is suitable for the 3P6T motor as all the windings are isolated. As illustrated in Fig. 9, two isolated windings are connected in opposite directions for each phase and driven by 180° phase-shifted square-wave gate voltages. The sinusoidal components reinforce each other, while their dc components cancel perfectly due to opposite polarity, eliminating dc offset and ensuring balanced torque production.

IV. Conclusion

Motivated by overcoming the reliability limitations of GaN-based half-bridge drives, this work proposes and experimentally validates a novel BLDC drive architecture using only low-side GaN switches in an *LC*-resonant topology. By eliminating high-side power devices, the design inherently avoids key reliability issues such as high dV/dt, parasitic turn-ON, and EMI. Experimental results confirm sinusoidal current generation and open-loop motor operation with low frequency. The novel structure is ideal for high-reliability BLDC drive applications with 3rd generation power devices. Moreover, the capability of producing low-frequency sinusoidal currents without relying on high-frequency switching makes the proposed topology particularly attractive for the applications such as biomedical implants WPT, brain–computer interfaces, and stealth communication technologies.

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