A High-Power Modular Radio Frequency Converter With Wide-Range Power Regulation Under ZVS Operation

Jingtao Wang, Xin Liu, *Senior Member, IEEE*, Dehong Zhou, *Senior Member, IEEE*, Zewei Shen, *Member, IEEE*, and Jianxiao Zou, *Member, IEEE*

***Abstract*—Radio frequency converter (RFC) is widely used in semiconductor manufacturing, demanding high power levels, high efficiencies, and wide power regulation ranges. However, existing solutions face issues like discrete regulation ranges, low efficiencies at low power levels due to high reactive power and hard switching, or complex auxiliary circuits for balancing the power regulation range and efficiency. This article proposes an efficient modular power amplifier architecture with multiple RFC modules using full-bridge class-D power amplifiers. Its individual modules' constant-current characteristics and system-level power transmission are analyzed. A hybrid modulation strategy combining module number adjustment and dc voltage control enables wide-range power regulation without auxiliary circuits. A 3-kW four-module RFC prototype tested at 400 kHz shows output power levels from 100 W to 2.8 kW with a peak efficiency of 93.7% and low current harmonics, validating its superior performance in practice.**

***Index Terms*—Modular design, multiple power amplifiers, radio frequency converters, wide-range power regulation.**

I. Introduction

RADIO frequency converters (RFCs) are power electronic systems designed to generate high-frequency sinusoidal voltages, typically operating within the frequency spectrum of hundreds of kHz to tens of MHz. These systems find critical applications in industrial scenarios including semiconductor manufacturing [1], radio frequency thermal processing [2], wireless power transmission [3], and electrosurgical instrumentation [4].

Fig. 1 depicts the conventional architecture of a high-power RFC utilizing multiple parallel power amplifiers (PAs) [5]. The dc power supply, typically implemented by a grid-connected power factor corrector (PFC), provides a regulated dc voltage to the PAs. The PFC achieves ac–dc rectification with an enforced unity power factor and exhibits inherent voltage regulation capability. The driver system delivers fixed-frequency switching signals to activate the PAs, thereby determining the RFC's fundamental operating frequency. The control system can realize output power regulation through two primary mechanisms: 1) Selective activation/deactivation of PA units to achieve discrete power steps, and 2) Continuous adjustment of PA duty cycles for fine-grained power tuning. Each PA efficiently converts dc voltage/current into RF The power combiner sums outputs from individual PA channels through impedance matching networks.

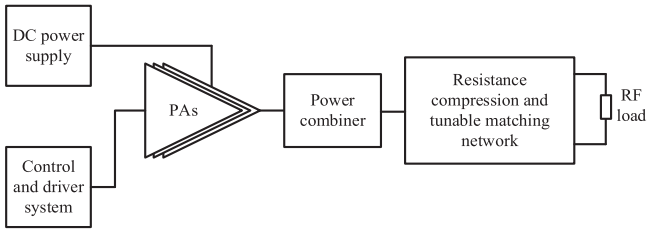

Fig. 1. General architecture block diagram of a multi-PA RFC.

RF loads typically exhibit nominal 50-Ω impedance, yet practical RF power supplies often operate under rapidly varying load conditions, such as dynamic plasma impedance variations during plasma generation [6], [7]. Such load deviations severely degrade the performance of RF amplifiers. For linear-mode PAs (Class A/B/AB/C) where transistors function as controlled current sources, load impedance mismatches induce elevated voltage/current stress across switching devices, leading to increased conduction losses and potential device breakdown [8], [9].

In contrast, switch-mode PAs (Class D/E/Φ) theoretically achieve superior efficiency by operating under soft-switching conditions (e.g., Zero Voltage Switching, ZVS). However, their practical efficiency is constrained by parasitic capacitance-induced losses during switching transitions. Specifically, load impedance deviations under dynamic RF operating conditions may destabilize resonant tank characteristics, forcing partial operation in hard-switching regions. This results in abrupt COSS charging/discharging currents and consequent efficiency degradation [10], [11], [12]. Therefore, active maintenance of ZVS conditions across load variations becomes imperative to preserve the efficiency advantages of these topologies.

Received 22 April 2025; revised 14 August 2025; accepted 30 September 2025. Date of publication 8 October 2025; date of current version 19 January 2026. This work was supported in part by the National Natural Science Foundation of China under Grant 52307012 and in part by the Shenzhen Science and Technology Program under Grant JCYJ20240813114213019 and Grant JCYJ20250604180514018. Recommended for publication by Associate Editor K. Basu. *(Corresponding author: Xin Liu.)*

The authors are with the Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen 518110, China, and also with the School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China (e-mail: 202322280531@std.uestc.edu.cn; liu_xin@uestc.edu.cn; dhzhou@uestc.edu.cn; shenzw@uestc.edu.cn; jxzou@uestc.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3619219.

Digital Object Identifier 10.1109/TPEL.2025.3619219

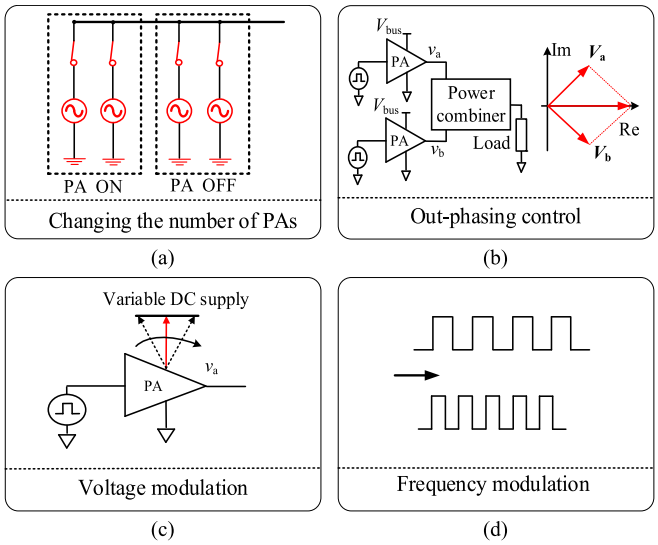

Fig. 2. Several methods of regulating power. (a) Multiple PAs in parallel in [16]. (b) Out-phasing control in [19] and [20]. (c) Drain voltage adjustment in [24]. (d) Frequency modulation in [25].

To address load impedance variations, researchers have proposed two approaches of impedance compression networks (ICNs) and tunable matching networks (TMNs), as illustrated in Fig. 1. The ICNs compress impedance variation ranges, and the TMNs dynamically match load impedance. These two approaches collectively enhance system stability under impedance-varying conditions [13], [14], [15]. As this constitutes established prior art beyond the scope of our investigation, detailed analysis is intentionally omitted.

RF power systems require wide-range power regulation with high efficiency, achieved through topologies and control methods. Several ways to regulate the power are illustrated in Fig. 2. In terms of topology, increasing the number of PAs can be an option. As shown in Fig. 2(a), several Φ_2 PAs modules are connected in parallel in [16], and the output power range is discretely adjusted by controlling the number of active PAs [17]. In [18], full-bridge and half-bridge topology switching in class-D PAs is used to halve the power, though this approach requires precautions to prevent the occurrence of dc bias voltage. In terms of modulation, Fig. 2(b) demonstrates that out-phasing control between PAs is proposed in [19] and [20] to regulate the output power by adjusting the output phase between different PAs. However, when the required output power is small, a large phase difference is needed, which will lead to higher reactive power, further decreasing the efficiency of the inverter and increasing the risk of deregulation [21]. Therefore, this method is more suitable for small-range power adjustments and should be used together with other modulation strategies. Nuyts et al. [22] and Lu et al. [23] proposed another hybrid modulation method: when the output power is above the critical value, the phase-shifting method is adopted; when the power is below the critical value, the phase angle remains unchanged, and the amplitude of the input signal is controlled to avoid the deep out-phasing. Fig. 2(c) demonstrates that the PA employs discretely adjustable drain voltages in [24], which can be set to 100 V, 200 V, or 400 V, and then out-phasing and power synthesis are performed using the Chireix power combiner. This method enables large-range discrete and small-range continuous power regulation; however, it comes with higher control complexity. As shown in Fig. 2(d), the output power can also be adjusted by changing the frequency of the driver system to alter the gain of the resonant network [25]. However, the feasibility of this approach is challenged by load impedance variations in RFCs and may conflict with the characteristics of the subsequent TMN network.

In summary, the challenge of RFCs lies in achieving high output power, wide-range power regulation, and fast adjustment capability under large load variations while maintaining high efficiency. This article presents a high-performance RFC implementation that employs a modular architecture with multiple full-bridge Class-D PAs to improve both power capacity and scalable efficiency. Compared with other PA topologies, the Class-D configuration demonstrates superior voltage stress characteristics [26], [27]. Furthermore, an *LCL* resonant network architecture is proposed. Specifically, this architecture leverages the resonant tank characteristics to facilitate both power summation across parallel modules and autonomous intermodule current sharing, as validated in [28]. The principal contributions are summarized as follows:

1) A modular high-power architecture with parallel-connected PA modules via an *LCL* resonant network is developed, featuring load-independent constant-current output, intermodule current sharing, and scalable power superposition.
2) A hybrid modulation strategy that integrates module number adjustment with dc voltage control is proposed, enabling continuous wide-range regulation of output power.
3) A 3-kW laboratory prototype is designed and experimentally validated, offering practical design guidelines for implementing multimodule high-power RFC systems.

The rest of this article is organized as follows. Section II introduces the modular parallel topology with multi-PAs, and analyzes the system's frequency characteristics and power transmission characteristics. Section III presents the wide-range power regulation modulation method employed by the system, along with output analysis. Section IV provides experimental verification. Finally, Section V concludes this article.

II. Structure of the Proposed RFC

This section demonstrates the proposed topology, presents its constant current characteristics and soft-switching conditions, and evaluates the power transfer characteristics.

A. Proposed Topology

The proposed topology is illustrated in Fig. 3. The dc-link voltage $V_{\rm bus}$ serves as the input source, while the parallel module number m is configured based on the rated power. Each module employs four MOSFETS ($S_{i\,1}$–S_{i4}) as power switches, generating a differential output voltage $v_{{\rm in}\,i}$. An *LCL*-type resonant tank is adopted, comprising a series compensation inductor $L_{{\rm sr}\,i}$, a parallel compensation capacitor $C_{{\rm pr}\,i}$, and a parallel compensation inductor $L_{{\rm pr}\,i}$. The primary and secondary currents of the

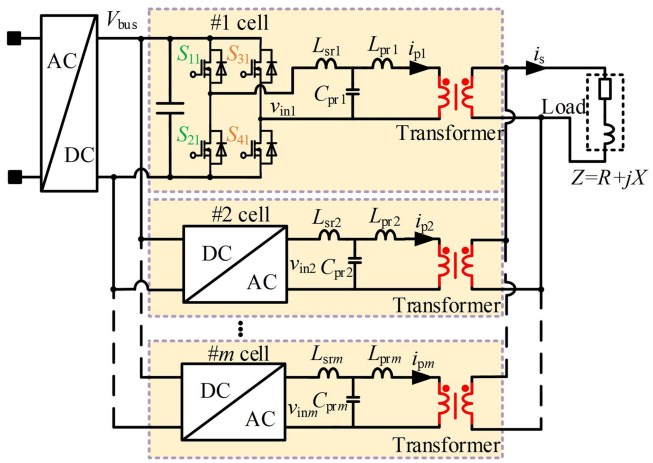

Fig. 3. Proposed high-power modular RFC.

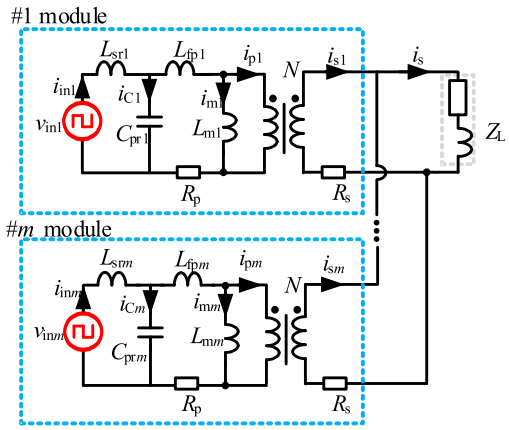

Fig. 4. Equivalent circuit for the proposed topology.

#i module are denoted as $i_{\mathrm{p}i}$ and $i_{\mathrm{s}i}$, respectively. N is the turns ratio of the transformer, defined as

$$N = \frac{n_{i1}}{n_{i2}}. \tag{1}$$

The equivalent circuit is shown in Fig. 4. R_{p} and R_{s} are the primary and secondary parasitic resistances of the *#i* transformer, respectively. $L_{\mathrm{m}i}$ is the magnetizing inductance of the *#i* transformer. Since the transformer is designed without an air gap, it has a large $L_{\mathrm{m}i}$ with several millihenries. Under high-frequency conditions, the magnetizing current $i_{\mathrm{m}i}$ can be neglected. Thus, the relationship between $i_{\mathrm{p}i}$ and the inverter current $i_{\mathrm{in}i}$ can be defined as

$$i_{\mathrm{p}i} = i_{\mathrm{in}i} - i_{\mathrm{C}i}. \tag{2}$$

The resonant angular frequency of the system is defined as ω_{s}. To ensure constant output current and zero phase angle (ZPA), one can obtain the following equations:

$$\omega_{\mathrm{s}} L_{\mathrm{sr}i} = \frac{1}{\omega_{\mathrm{s}} C_{\mathrm{pr}i}} \tag{3}$$

$$L_{\mathrm{sr}i} = L_{\mathrm{pr}i}. \tag{4}$$

The proposed topology utilizes identical device parameters across all modules, enabling a modular architecture that achieves both scalable output power and wide-range power regulation via module number adjustment. Furthermore, the *LCL* resonant tank exhibits superior harmonic attenuation characteristics, enabling the neglect of higher order harmonic effects in circuit analysis while significantly improving the sinusoidality of the output current.

Crucially, current sharing can be achieved without active balancing control, which stems from the constant-current characteristic of the *LCL* resonant network and the consistency of module parameters: the *LCL* network is equivalent to a constant current source at the resonant frequency, making the primary current of each module unaffected by load changes; when the resonant parameters and transformer characteristics of each module are consistent, balanced currents are naturally formed under the same input voltage. It should be noted that large loop inductance mismatches (such as differences in parasitic inductance of PCB traces) may disrupt this mechanism—currents may concentrate in modules with lower inductance, leading to a narrowed ZVS range and increased switching losses in overloaded modules, and this issue is more prominent in high-frequency scenarios. However, the impact of mismatches is effectively suppressed by controlling the consistency of transformer leakage inductance (approximately 1 μH) and magnetizing inductance in this article.

Although the modular parallel architecture can increase power capacity by adding modules, the actual number is limited by two factors. First is the constraint of synchronous driving. Multiple modules require strictly synchronized PWM signals, but the number of controller interfaces is limited. In this experiment, TMS320F280049 supports a maximum of 4 full-bridge units. Additional controllers may introduce timing deviations and affect output stability, which can be resolved by multicontroller synchronization methods. Second is the balance between power and efficiency. Redundant modules will increase losses and costs, so the number of modules should match the target power range to avoid overdesign.

B. Constant Current Characteristics of Primary Winding

The *LCL* resonant circuit employed in the system exhibits strong constant-current source characteristics at its resonant frequency, effectively transforming the input circuit into an equivalent constant current source. This section will demonstrate how these characteristics are achieved and their impact on modular current sharing.

Based on Norton's theorem, the primary-side circuit adopts a constant-current topology design, which facilitates power scaling through modular expansion. As illustrated in Fig. 5, the primary input voltage $v_{\mathrm{in}i}$ is determined by the dc-link voltage V_{bus}. Through Norton equivalence, the voltage-source inverter topology integrated with the *LCL* resonant tank can be modeled as a current-source network, which is analyzed as follows.

By applying Norton's theorem, the voltage-source inverter topology is equivalently transformed into a current-source network, wherein $L_{\mathrm{sr}i}$ and $C_{\mathrm{pr}i}$ are configured in parallel. As derived in (3), the equivalent conductance G of the network

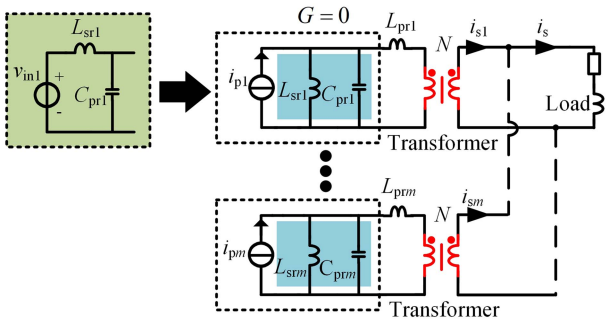

Fig. 5. Constant current characteristic of primary side.

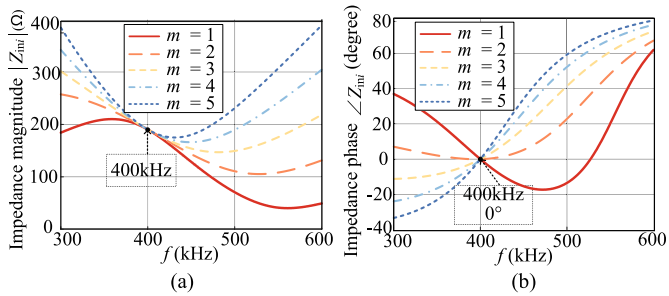

Fig. 6. Amplitude and phase frequency characteristics of $Z_{\mathrm{in}i}$ where $V_{\mathrm{bus}} = 210$ V, $R_{\mathrm{L}} = 50\ \Omega$, $N = 1$. (a) Relationship among $|Z_{\mathrm{in}i}|$, f, and m. (b) Relationship among $|Z_{\mathrm{in}i}|$, f, and m.

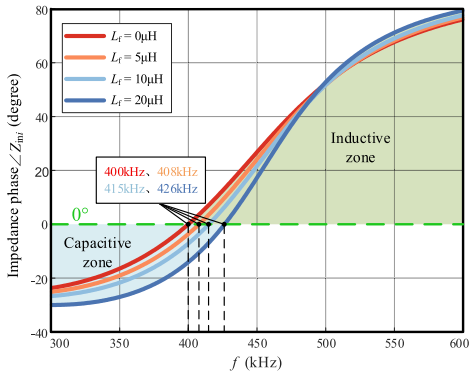

Fig. 7. Phase-frequency characteristics of input impedance $Z_{\mathrm{in}i}$ under different leakage inductances L_{f}, where $V_{\mathrm{bus}} = 210$ V, $R_{\mathrm{L}} = 50\ \Omega$, $N = 1$.

becomes zero when $L_{\mathrm{sr}i}$ and $C_{\mathrm{pr}i}$ achieve full resonance at the fundamental harmonic. Under this condition, the Norton-equivalent current source directly corresponds to the primary-side coil current $i_{\mathrm{p}i}$, expressed as

$$i_{\mathrm{p}i} = \frac{v_{\mathrm{in}i}}{j\omega L_{\mathrm{sr}i}}. \tag{5}$$

Then, the input voltage source can be equated to a current source $i_{\mathrm{p}i}$. Therefore, in the resonant state, the current $i_{\mathrm{p}i}$ of each module is determined solely by the input voltage and resonant parameters, resulting in a constant-current characteristic for each module that is unaffected by changes in the load R_{L}. However, it should be noted that when the supply voltage V_{bus} changes, the output current adjusts accordingly to achieve power regulation, and thus, $i_{\mathrm{p}i}$ does not remain constant with variations in the power supply.

The constant-current characteristics of the proposed topology remain invariant regardless of series-connected inductive or capacitive components within or across modules. This characteristic ensures uniform current distribution among all modules through an inherent current-sharing mechanism, thereby preventing localized overloading conditions.

C. Soft-Switching Conditions of the System

In high-frequency converters, the application of soft-switching techniques can effectively improve system efficiency. The following analysis focuses on the conditions required to achieve soft-switching in the proposed system.

The ZVS necessitates that the current of the switching devices in the PA slightly lags behind their voltage, ensuring the devices turn ON when the voltage crosses zero and thereby avoiding instantaneous losses caused by voltage-current overlap during turn-ON transitions. This requirement is intrinsically related to the input impedance $Z_{\mathrm{in}i}$ of the #i module. $Z_{\mathrm{in}i}$ can be expressed as

$$Z_{\mathrm{in}i} = j\omega L_{\mathrm{sr}i} + \left(\frac{1}{j\omega C_{\mathrm{pr}i}} // \left(j\omega L_{\mathrm{pr}i} + N^2 m Z_{\mathrm{L}}\right)\right). \tag{6}$$

Fig. 6 illustrates the magnitude $|Z_{\mathrm{in}i}|$ and phase angle $\angle Z_{\mathrm{in}i}$ of the input impedance for different module numbers m, derived from (6). As shown in Fig. 6(a), when the system operates at the resonant frequency 400 kHz, $|Z_{\mathrm{in}i}|$ remains consistent across all m. This observation confirms the system's constant-current characteristic: the input current $i_{\mathrm{in}i}$ of each module remains unaffected by variations in m at the resonant frequency.

From Fig. 6(b), the impedance exhibits purely resistive behavior at the resonant frequency. When operating above the resonant frequency, the phase angle $\angle Z_{\mathrm{in}i}$ becomes inductive for most cases, except when $m = 1$. Specifically, when $m = 1$, within the frequency range where ZVS can be achieved for multimodule configurations ($m \geq 2$), the input impedance curve of the single module exhibits a capacitive characteristic over a broad range (i.e., $\angle Z_{\mathrm{in}i} < 0$). This capacitive behavior prevents the single module from achieving ZVS operation within this frequency range.

Furthermore, the influence of transformer leakage inductance on the soft-switching range is non-negligible. The leakage inductance L_{f} is in series with the parallel resonant inductor L_{sr}, which equivalently changes the total inductance of the network, causing the resistive point of the input impedance $Z_{\mathrm{in}i}$ to shift toward higher frequencies. When L_{f} increases, the inductive impedance region at a fixed frequency shrink, and the ZVS range is compressed. This is because, as a series inductance, increasing L_{f} strengthens the inductive characteristics of the circuit across all frequencies. However, the inductive reactance increases more rapidly at higher frequencies, necessitating a shift of the ZPA point toward higher frequencies to reestablish equilibrium. Fig. 7 shows the variation of $\angle Z_{\mathrm{in}i}$ under different L_{f} values.

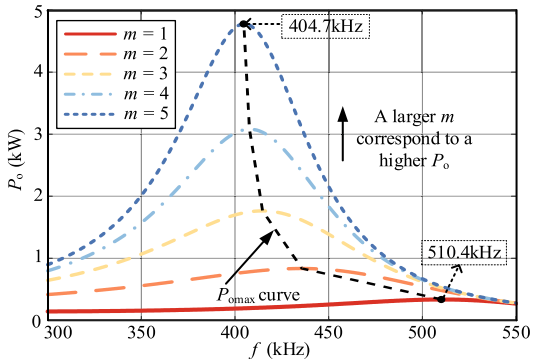

Fig. 8. P_o curves for different values of m at various frequencies where V_{bus} = 210 V, R_L = 50 Ω, and N = 1.

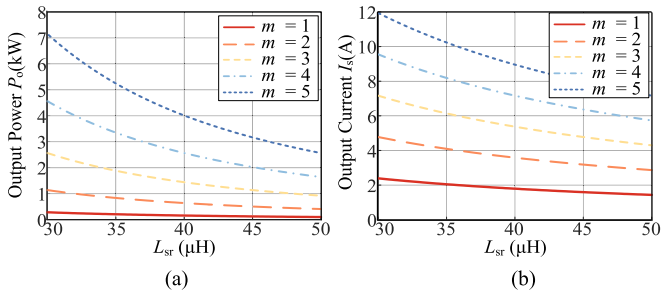

Fig. 9. Relationship between output power P_o and output current I_s with respect to L_{sr} and m, where V_{bus} = 210 V, R_L = 50 Ω, and N = 1. (a) The relationship between Po and different Lsr. (b) The relationship between Is and different Lsr.

D. Power Transfer Characteristics

Evaluating its power transfer capability is of critical importance for the RFC design, which will be thoroughly analyzed here.

When the system operates at a nonresonant frequency, the input current i_{ini} cannot be equated to a constant current source, which is

$$i_{ini} = \frac{v_{ini}}{Z_{ini}}. \tag{7}$$

The transformer's primary current i_{pi} can be expressed as

$$i_{pi} = i_{ini}\frac{1/j\omega C_{pri}}{j\omega L_{pri} + N^2 m Z_L}. \tag{8}$$

All the parameters are the same between the modules, the output current i_s on the load is

$$i_s = \sum_{i-1}^{m} i_{si} = \sum_{i=1}^{m} N i_{pi} = mN i_{pi}. \tag{9}$$

Then, the resulting output power P_o can be calculated as

$$P_o = \left|\mathbf{I}_s^2 R_L\right|. \tag{10}$$

Fig. 8 illustrates the system's output power under varying frequencies and module numbers. Due to the parallel configuration of the modules, each module is effectively connected to an equivalent load of mR_L. This results in significant variations in the frequency and bandwidth of P_{omax} as m changes. Furthermore, when m is small, the frequency corresponding to P_{omax} substantially exceeds the resonant frequency.

When the system operates at the resonant frequency, the circuit current is solely determined by V_{bus} and L_{sr}. Furthermore, the resonant current i_s can be calculated using (5) and (9)

$$i_s = mN i_{pi} = \frac{mN v_{ini}}{j\omega L_{sri}}. \tag{11}$$

Then, the output power P_o is related to L_{sr} and m as follows:

$$P_o = \frac{m^2 N^2 v_{ini}^2}{\omega^2 L_{sri}^2} R_L. \tag{12}$$

Using the fundamental component equivalence method, the root-mean-square (rms) value of the fundamental component of v_{ini} can be used for calculation. The rms value V_{ini_rms} of the fundamental component of v_{ini} can be expressed as

$$V_{ini\_rms} \le \frac{2\sqrt{2}V_{bus}}{\pi}. \tag{13}$$

The output power P_o can then be expressed as

$$P_o = \frac{m^2 N^2 V_{ini}^2}{\omega^2 L_{sri}^2} R_L \le \frac{8m^2 N^2 V_{bus}^2}{\pi^2 \omega^2 L_{sri}^2} R_L. \tag{14}$$

Fig. 9 presents the relationship between the secondary-side current i_s, output power P_o, resonant inductor L_{sr}, and module number m under resonant operation. With L_{sr} varying from 30 μH to 50 μH, the other resonant components can be derived from (3) and (4). This analysis provides critical insights for circuit design, as the appropriate value of L_{sr} can be systematically designed based on the target output power of the system.

III. Proposed Control Method

In practical applications of RFCs, they are typically required to achieve rapid output power regulation and deliver specified power across a wide range of load impedances. Meanwhile, maintaining high efficiency throughout the power range and ensuring ZVS operation are also critical. This section presents a power regulation method and analyzes the circuit's harmonic characteristics and efficiency performance.

A. Proposed Hybrid Modulation Method

When the circuit operates at the resonant frequency, the output power can be straightforwardly derived from (14) due to the system's constant-current characteristic. With fixed circuit parameters, adjusting the dc-link voltage V_{bus} and module number m over a defined range enables effective power regulation, as detailed in the following analysis.

V_{bus} modulation can be achieved without introducing additional front-end dc–dc converters. In high-power applications in China, the PFC utilizing the three-phase Vienna topology provides a stable V_{bus} within [640 V, 840 V]. The normalized input voltage is denoted as λ, defined as the ratio of V_{bus} to the base voltage, expressed as

$$\lambda = \frac{V_{bus}}{V_0} \tag{15}$$

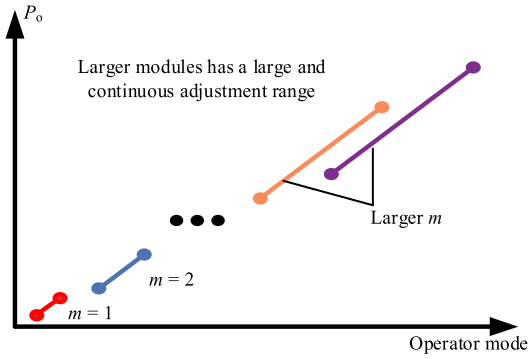

Fig. 10. Output power P_o adjustment range is achieved by varying the λ and m.

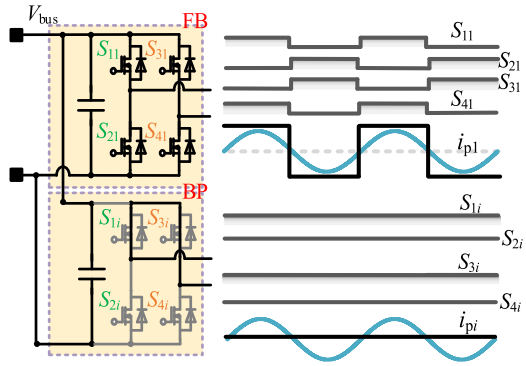

Fig. 11. Two different modes and their typical waveforms.

where V_0 represents the minimum voltage provided by the PFC. Consequently, the normalized input voltage λ ranges approximately from 1 to 1.3. Therefore, a wide range of power regulation can be achieved by adjusting the combination of λ and m.

Fig. 10 illustrates the power regulation mechanism through dc voltage adjustment. When m is small, the achievable power range becomes narrower. If the voltage adjustment range is constrained, discontinuous power transitions between different m values may occur. However, as m increases, the power adjustment range expands significantly, and continuous power regulation can be achieved even when dynamically enabling or disabling modules.

Module number adjustment can be achieved by controlling the operating states of PA units: the full-bridge (FB) mode and the bypass (BP) mode. In FB mode, switches S_{1i} and S_{4i} are simultaneously turned ON/OFF, while S_{2i} and S_{3i} operate inversely, enabling each pair of MOSFETS to conduct for half a cycle.

This configuration allows the PA to function as a standard full-bridge inverter, generating a 50% duty cycle inverted voltage output. Conversely, in BP mode, either S_{1i} and S_{3i} remain continuously on (with S_{2i} and S_{4i} OFF) or vice versa, resulting in a collapsed inverted voltage and a short-circuit current flow similar to the FB-mode inverter current. Notably, the half-bridge configuration of class-D PA is intentionally excluded to prevent the generation of dc bias voltage. Fig. 11 illustrates the switching states and typical waveforms for both modes.

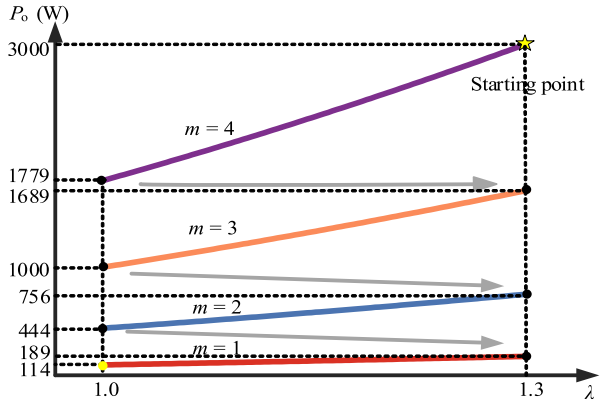

Fig. 12. Diagram of the control scheme for rated power 3 kW.

Fig. 12 illustrates the specific steps of the modulation strategy. Taking $m = 4$ with a rated power of 3 kW as an example, the process begins at the maximum power point. Initially, power reduction is achieved by adjusting the input dc voltage. A larger m enables a wider power adjustment range through voltage regulation. Once the minimum input voltage is reached, the power is further reduced by decreasing the number of active modules, i.e., switching one PA unit to BP mode. This iterative process continues until the system reaches the theoretical minimum power of 114 W at $\lambda = 1$ and $m = 1$.

This hybrid modulation strategy demonstrates the capability for continuous and wide-range power regulation without requiring additional hardware circuits. A critical aspect of this regulation performance lies in the system's linearity, which characterizes how output power responds to changes in control parameters. In the RFC system, linearity mainly refers to the proportional relationship between control parameters and output power, which is an important indicator for evaluating the performance of the RFC system. The two key control variables in this design are the dc-link voltage V_{bus} and the number of active PA modules m. As shown in (14), when the system parameters are fixed, the output power P_o can be simplified to be proportional to m [2] and $V2$ bus. As illustrated in Fig. 12, P_o increases synchronously with the rise of V_{bus} and m, demonstrating a smooth power regulation characteristic.

B. Output Harmonic Analysis

A high sinusoidality of the output waveform across the load is required for the design of RFCs. Thus, an analysis of the harmonic components in the output current is conducted in this section.

The dc-link voltage V_{bus} is converted by a full-bridge PAs operating at frequency f, generating a square-wave signal with an amplitude of V_{bus}, where the relationship between the period T and f is defined as

$$T = \frac{1}{2\pi f}. \tag{16}$$

By performing Fourier decomposition on the square wave, the frequency-domain representation of each harmonic component

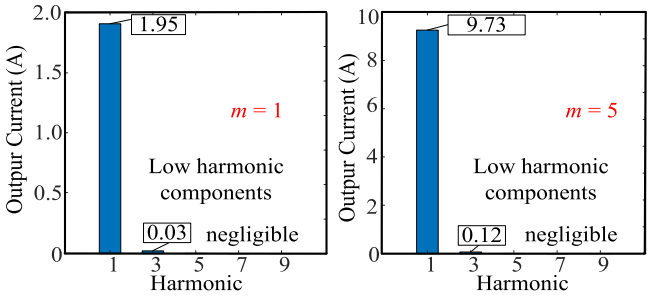

Fig. 13. First, third, fifth, seventh, and ninth harmonic components of the output current of the system at $m = 1$, 2, 3, 4, and 5 where $f = 400$ kHz, $V_{\text{bus}} = 210$ V, $R_{\text{L}} = 50\ \Omega$, and $N = 1$.

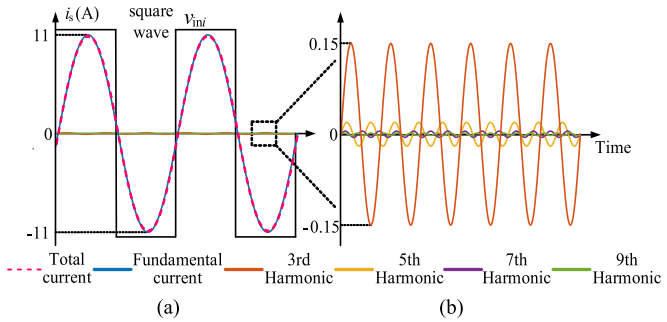

Fig. 14. Waveforms of fundamental and harmonic currents of i_{s}, where $f = 400$ kHz, $V_{\text{bus}} = 210$ V, $R_{\text{L}} = 50\ \Omega$, and $N = 1$. (a) Waveforms of fundamental current and third, fifth, seventh, and ninth harmonic currents of i_{s}. (b) Harmonic current waveforms with the fundamental current removed.

in the input square-wave voltage v_{in} can be derived as follows:

$$v_{\text{in}}(f) = \frac{4V_{\text{bus}}}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \delta\left(f - \frac{n}{T}\right) \tag{17}$$

where n is the number of harmonics and $\delta(f - n/T)$ is an impulse function indicating the signal has a harmonic component at frequency $f = n/T$.

Consistent with the method for analyzing power transfer characteristics, the rms values of the fundamental component and high-order harmonic components are treated as input voltages, respectively. The corresponding output current I_{s} for each component can be calculated using (5) and (11). By comparing the rms values of each component, the composition of the output current I_{s} can be determined. Under the fundamental resonance condition, the harmonic components and distortion rate of I_{s} are illustrated in Fig. 13.

Fig. 14 indicates that the fundamental component dominates the waveform, while the third and higher harmonics are negligible. Fig. 14(a) and (b) depicts the waveforms of the fundamental current and harmonic current of I_{s} at $m = 3$, respectively, demonstrating that the fundamental component remains the predominant constituent in the output current.

Total harmonic distortion (THD) is a metric commonly used to quantify the distortion degree of a current waveform related to a pure sinusoidal waveform. The THD calculation formula is

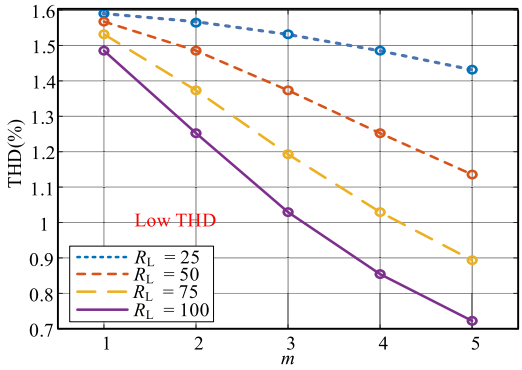

Fig. 15. Line plots of THD for different m and R_{L}, where $f = 400$ kHz, $V_{\text{bus}} = 210$ V, $N = 1$, $L_{\text{sr}} = 38\ \mu$H, $C_{\text{pr}} = 4$ nF, and $L_{\text{pr}} = 38\ \mu$H.

expressed as

$$\text{THD}(\%) = \frac{\sqrt{i_2^2 + i_3^2 + i_4^2 + \cdots}}{i_1} \times 100\% \tag{18}$$

where i_1 is the fundamental current, and i_2 and i_3 represent higher order harmonic currents. A higher THD value indicates more severe waveform distortion and a larger proportion of harmonic components in the current. Conversely, a lower THD implies reduced harmonic contents. The THD values under different m conditions are illustrated in Fig. 15. It can be seen that the THD is smaller than 1.6% under different conditions, which is satisfying.

C. Power Loss and Efficiency Analysis

Once the system's operational status has been determined, the overall efficiency of the system can be assessed. In this section, the power loss and efficiency of the system will be analyzed.

The conduction loss of MOSFETS denoted as $P_{\text{loss}\cdot i}$ is caused by their ON-resistance R_{dsON} , and can be calculated by

$$P_{\text{on}i} = 2I_{\text{in}i}^2 R_{\text{dson}}. \tag{19}$$

The ferrite loss of #i transformer is related to the frequency f, the magnetic field strength B_i, and the magnetic core volume V_{e}. It can be calculated as (20) where x, y, and z are determined by material characteristics

$$P_{\text{fe}i} = x f^y B_i^z V_{\text{e}}. \tag{20}$$

There is also copper loss of $P_{\text{loss}\,i}$ due to the parasitic resistors R_{p} and R_{s}, which can be expressed as

$$P_{\text{loss}i} = I_{\text{in}i}^2 R_{\text{p}} + I_{si}^2 R_{\text{s}} \approx I_{\text{in}i}^2 R_{\text{p}} + (N I_{\text{in}i})^2 R_{\text{s}}. \tag{21}$$

The parasitic resistance losses in the resonant components of the circuit can be expressed as

$$P_{\text{lossR}i} = I_{\text{in}i}^2 R_{\text{Lr}} + I_{\text{C}i}^2 R_{\text{Cr}} + I_{\text{p}i}^2 R_{\text{Lr}} \tag{22}$$

where R_{Lr} is the parasitic resistance of the resonant inductor, and R_{Cr} is the parasitic resistance of the resonant capacitor.

When m modules are in operation, the total loss $P_{\text{tot}\cdot\text{loss}}$ is

$$P_{\text{tot\_loss}} = m\left(P_{\text{fe}i} + P_{\text{on}i} + P_{\text{loss}i} + P_{\text{lossR}i}\right). \tag{23}$$

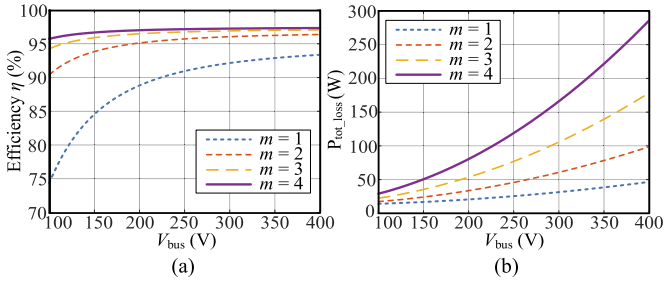

Fig. 16. Power loss and overall efficiency with respect to $V_{\rm bus}$ and m, where $f = 400$ kHz, $R_{\rm dson} = 0.03\ \Omega$, $R_{\rm p} = 0.1\ \Omega$, $R_{\rm s} = 0.05\ \Omega$, $R_{\rm Lr} = 0.5\ \Omega$, $R_{\rm Cr} = 0.1\ \Omega$, $P_{{\rm fe}i} = 4$ W, $N = 1$. (a) η with m. (b) $P_{\rm tot\_loss}$ with m.

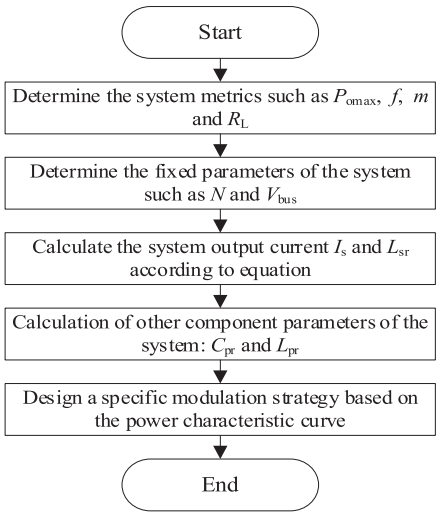

Fig. 17. Design procedure of the proposed system.

Finally, the total efficiency can be derived as

$$\eta = \frac{P_o}{P_o + P_{\rm tot\_loss}}. \tag{24}$$

Fig. 16(a) and (b) illustrates the relationships of the power loss and efficiency with respect to $V_{\rm bus}$ and m. Under the same $R_{\rm L}$, the power loss increases with higher $V_{\rm bus}$. Additionally, a larger m corresponds to an increased output power. Overall, the system maintains relatively high efficiency even at elevated power levels.

D. Design Procedure

The design of a comprehensive system requires consideration of all component parameters and adherence to established design procedures. Thus, this section details the system design. As shown in Fig. 17, the design procedure of the proposed system can be categorized into the following stages:

1) At first, define the key operational metrics, including maximum power $P_{\rm omax}$, resonant frequency f, maximum module number m, and load $R_{\rm L}$, while identifying fixed parameters such as the transformer turns ratio N and the input dc voltage range $V_{\rm bus}$.

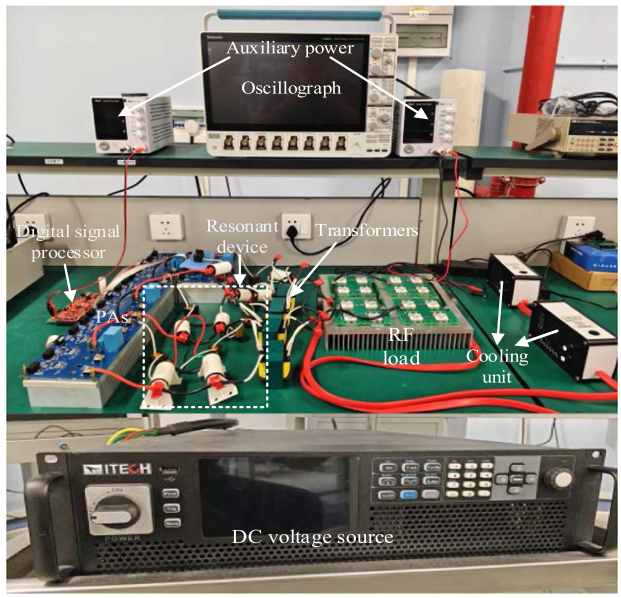

Fig. 18. 3-kW multi-PA RFC prototype.

TABLE I
KEY PARAMETERS OF PROPOSED PROTOTYPE

Symbol	Parameter	Value
$P_{\rm o}$	Output power	100 W–2831 W
$V_{\rm bus}$	Dc-link voltage	160 V–210 V
f	Operating frequency	410 kHz
$L_{{\rm sr}i}$	Series resonant inductor of #i module	38 μH
$C_{{\rm pr}i}$	Parallel resonant capacitor of #i module	4 nF
$L_{{\rm pr}i}$	Parallel resonant inductor of #i module	38 μH
m	Number of inverters	4
N	Turn ratio of transformers	9:9

2) The next step is to calculate the secondary-side current $I_{\rm s}$ based on the constant-current characteristics, and determine the resonant inductance $L_{\rm sr}$ using the appropriate equations.
3) After that, derive the remaining resonant component parameters using the obtained values of $I_{\rm s}$ and $L_{\rm sr}$.
4) Finally, establish specific modulation schemes based on the analysis of the power characteristic curves.

IV. EXPERIMENTAL VERIFICATION

A 3-kW multi-PA prototype has been constructed to validate the proposed topology. The experimental setup is shown in Fig. 18, and the key parameters are listed in Table I. Four parallel modules with identical parameters are controlled by a digital signal processor (TMS320F28049), where each unit generates synchronized square-wave signals with phase coherence. The dc voltage input is supplied by an ITECH IT7802-350 power source. Due to laboratory constraints, the input voltage is scaled to [160 V, 210 V]. All experimental waveforms are captured using an eight-channel oscilloscope platform (Tektronix MSO58B). Four SiC MOSFETS (SCT3030AL) are used in each module. Four identical transformers are used with a turns ratio of 9:9 and a magnetization inductance of 2 mH. The device parameters of the four modules are the same, with a $C_{\rm pr}$ of 4 nF

TABLE II
PARASITIC PARAMETERS OF THE COMPONENTS

Component	Number	Parasitic resistances	Parasitic capacitances	Parasitic inductances
MOSFETS	16	30 mΩ	89 nF	/
Resonant inductor	8	500 mΩ	/	/
Resonant capacitor	4	50 mΩ	/	/
Transformer	4	R_p:100 mΩ R_s:100 mΩ	/	L_m:2–3 mH L_f:0.9–1.3 μH
Load	1	/	/	0.2 μH

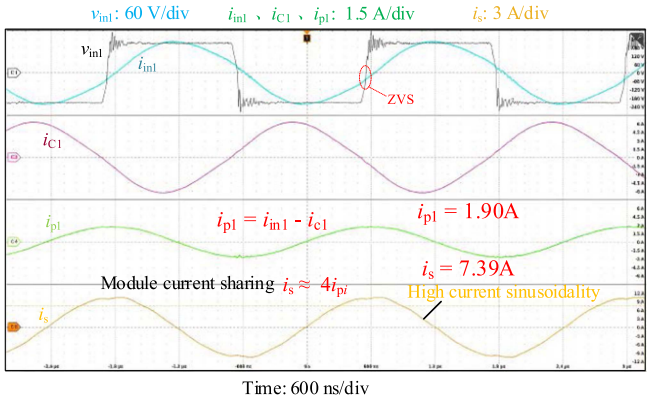

Fig. 19. Experimental waveforms of the inverter voltage and currents v_{in1} and i_{in1} of the first module, the current i_{C1} of the shunt capacitor, the primary current i_{p1}, and the total secondary current i_s.

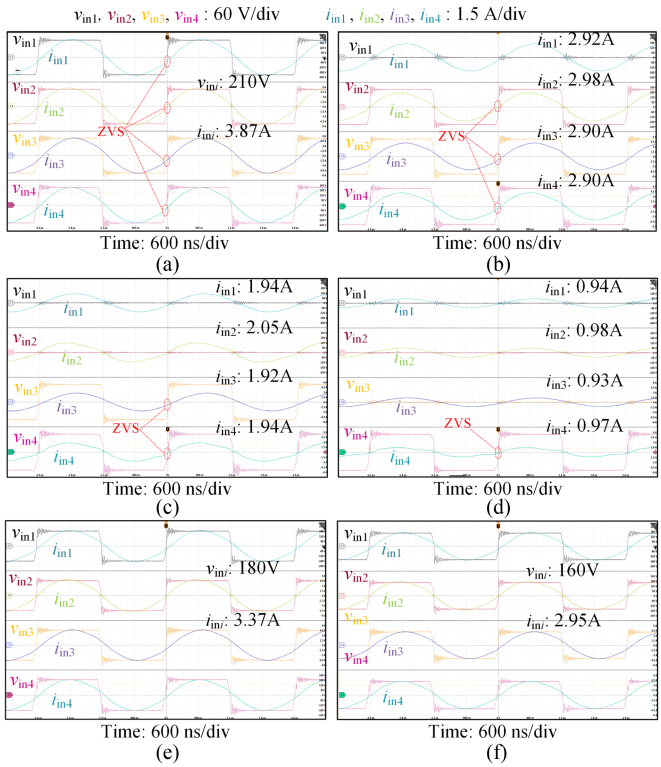

Fig. 20. Inverter voltage v_{ini} and current i_{ini} for experiments with different numbers of m. (a) $m = 4$ and $V_{bus} = 210$ V. (b) $m = 3$ and $V_{bus} = 210$ V. (c) $m = 2$ and $V_{bus} = 210$ V. (d) $m = 1$ and $V_{bus} = 210$ V. (e) $m = 4$ and $V_{bus} = 180$ V. (f) $m = 4$ and $V_{bus} = 160$ V.

obtained by paralleling two 2 nF capacitors, and L_{sr} and L_{pr} both of 38 μH. An RF resistor with an equivalent inductance of about 0.1 μH is used as a load. The operating frequency is set at 410 kHz with a dead time of 50 ns, which is slightly higher than the resonant frequency to ensure the ZVS operation.

Table II lists the measured parasitic parameters of the components in the prototype. The main parasitic resistances are the MOSFET ON-resistance R_{dsON} , transformer winding resistances R_p and R_s, and the equivalent series resistances of the resonant inductor and capacitor, contributing about 10–25% of the total power losses at a peak output power. The dominant parasitic capacitance is the MOSFET output capacitance C_{oss}, which can cause switching loss under non-ZVS operation; this can be avoided by operating slightly above resonance to maintain ZVS operation in all modules. Transformer leakage and magnetizing inductance mismatches are minimized by identical design and an air-gap-free magnetic core, ensuring uniform current sharing. The RF load's parasitic inductance is only 0.2 μH and has a negligible impact on system performance.

A. Experimental Typical Waveforms

To verify the feasibility and performance of the proposed system, experiments were conducted under various conditions, including variable dc voltages, variable numbers of modules, and different loading resistors.

As illustrated in Fig. 19, the system's typical waveforms under $m = 4$ and $V_{bus} = 210$ V are given, including the inverter voltage v_{ini} and current i_{ini}, the parallel capacitor current i_c on C_{pr} in the *LCL* resonant circuit, the primary-side winding current i_{pi}, and the secondary-side winding current i_s. The theoretical relationship among i_{ini}, i_c, and i_{pi} described in (10) is explicitly reflected in the measured waveforms. With $m = 4$, the amplitude of i_{pi} is observed to be one-quarter of i_s, consistent with the modular scaling principle. The secondary-side current i_s exhibits high sinusoidality with low THD.

The inverter waveforms of the system under $m = 1, 2, 3, 4$ are shown in Fig. 20(a)–(d), with all labeled values being rms values. When $m = 4$, the waveforms in Fig. 20(a) demonstrate that the inverting current and voltage of all units have similar magnitudes. The voltage slightly leads the current, enabling ZVS operation to reduce losses. For $m = 1, 2, 3$, the corresponding BP modules exhibit only short-circuit currents, while the FB modules retain inverter voltage but show significantly reduced inverter currents, indicating a lower system power rating. The consistent inverting currents across all modules reflect the system's current-sharing capability. Fig. 20(e) and (f) illustrates the inverting waveforms under $m = 4$ with $V_{bus} = 180$ V and 160 V, demonstrating that the output power can be adjusted by varying the input dc voltage.

B. System Performance Analysis

Experiments are conducted to measure output power and efficiency across different module numbers m and load resistances R_L, with the dc voltage varied from 160 V to 210 V. As derived from (10) and the circuit's constant-current characteristics, the

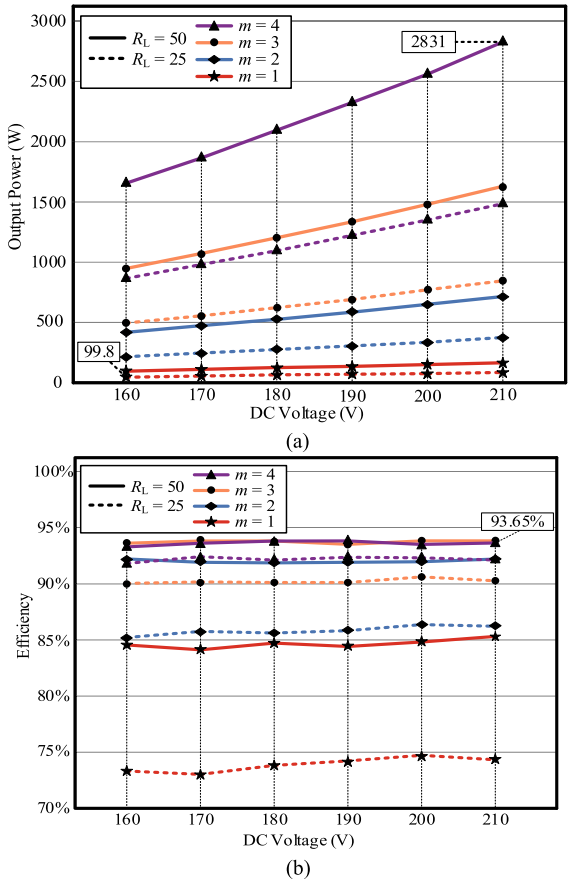

Fig. 21. Output power P_o and efficiency η of the system measured in the experiment. (a) Output power variation under different voltages and numbers of modules. (b) Efficiency under different voltages and numbers of modules.

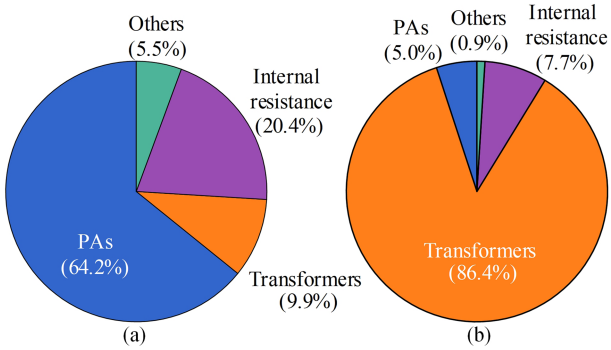

Fig. 22. Power loss breakdowns under two power levels at $R_L = 50\ \Omega$. (a) $P_o = 2831$ W. (b) $P_o = 99.8$ W.

output power at $R_L = 25\ \Omega$ is approximately half of that at $R_L = 50\ \Omega$, as shown in Fig. 21(a). The measured output power aligns with the calculated results in Fig. 12, indicating that higher values of m correspond to wider power regulation ranges. When m is changing from 3 to 4, the output power is nearly continuous, demonstrating that the proposed topology can achieve a continuous power adjustment range.

Figs. 21(b) and 22 jointly reveal the correlation between system efficiency and power levels. Fig. 22 shows the proportion of various power losses at the maximum power of 2831 W and the minimum power of 99.8 W. Based on the power loss distributions in Fig. 22, it can be seen that MOSFET switching losses and parasitic resistance losses account for the highest proportion at high power, while transformer ferrite losses dominate at low power. Therefore, further efficiency improvement can be achieved through four approaches as follows:

1) Optimizing dead time to balance ZVS and body diode forward voltage losses.
2) Dynamically adjusting the frequency at low power to maintain inductive impedance.
3) Using devices such as GaN MOSFETs to reduce switching losses.
4) Selecting high-frequency magnetic core materials and optimizing winding designs to reduce ferrite losses and copper losses.

These measures can specifically address the power loss bottlenecks in different power segments and further improve the system efficiency.

The efficiency results presented in this study do not include the power losses of the front-end PFC stage. As the three-phase Vienna topology PFC itself features relatively high efficiency [29], it may have a limited impact on the overall efficiency of the system. It should be noted that PFC is an essential component in all RFC architectures to ensure the stability of input power and unit power factor. By eliminating the additional dc–dc circuits, this system avoids the extra power conversion losses incurred in such stages, enabling the peak efficiency of the RFC system to remain above 93%.

Unlike traditional RFC architectures that require an additional dc–dc converter for power regulation [30], our system eliminates this stage. Conventional "PFC + dc–dc + RFC" cascaded structures rely on dc–dc converters with typical efficiency around 95% for kilowatt-level units [31], introducing extra conversion losses. By avoiding such redundant stages, our design enables the RFC subsystem to maintain a peak efficiency above 93%, resulting in higher overall efficiency compared to traditional setups.

C. Comparison and Discussion

Several methods have been proposed to improve the overall efficiency and power transfer capacity of the RFCs as mentioned in Section I. To show the advantages and disadvantages intuitively, a detailed comparison and discussion are given in this section.

Table III compares the converter design proposed in this article with other wide-range power regulation approaches, including multi-PA out-phasing regulation [16], multi-inverter discrete source regulation [24], and multi-inverter frequency modulation [25]. The proposed design has a wide power regulation range, broader operational load range, lower control complexity, and higher efficiency compared to these methods. Furthermore, the power regulation range and output power level can be expanded by increasing the number of modules owing to the modular architecture.

Meanwhile, Fig. 23 presents a comparison of efficiencies across different methods within the 0–3 kW power range, including the multi-inverter discrete back-OFF in [24], out-phasing control in [16], multimodule phase-shifting method in [17], and

TABLE III
COMPARISON OF DIFFERENT SYSTEMS

	[16]	[24]	[25]	This article
Wide power regulation range	Yes	Yes	Yes	Yes
Power rating level	Low	Low	High	High
Current sharing among modules	Yes	No	Yes	Yes
Wide load range	No	No	Yes	Yes
Modular design	Yes	Yes	Yes	Yes
Fixed frequency	Yes	Yes	No	Yes
Cascaded circuits	No	Yes	No	No
Power devices number	4	8	8	16
LCT number	30	33	10	16
Overall efficiency	93.5%	Above 90%	93.2%	93.65%

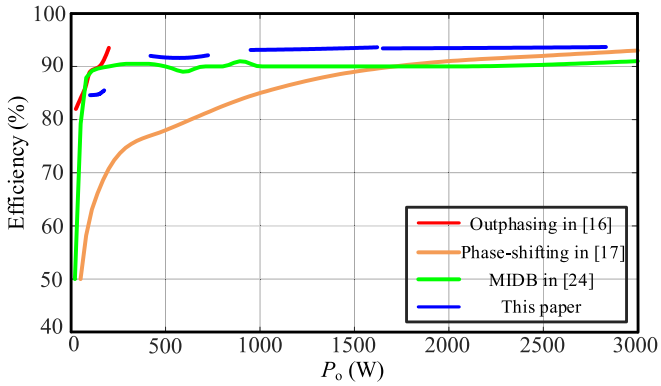

Fig. 23. Comparison of power efficiency among multiple papers related to RFC.

the method proposed in this article. Since the output power range of [25] is higher than 3 kW, its power-efficiency curve is not included in the figure. The comparison indicates that the proposed method exhibits superior efficiency performance over a wider power regulation range.

V. CONCLUSION

This work presents a high-efficiency, high-power multi-PA RFC architecture designed for wide-range power regulation under soft-switching conditions. By integrating a scalable multimodule class-D PA configuration with an *LCL* resonant network, the proposed system achieves constant-current output and autonomous current sharing without additional control overhead. A hybrid modulation strategy, combining input dc voltage control and module-number adjustment, enables continuous and flexible power regulation across a wide dynamic range. Experimental validation of a 3-kW prototype confirms the system's ability to deliver output power from 100 W to 2.8 kW while maintaining low harmonic distortion and a peak efficiency of 93.7%, demonstrating the feasibility and effectiveness of the proposed approach for advanced RF power delivery applications.

REFERENCES

[1] A. Gupta, Y. Arondekar, S. V. G. Ravindranath, H. Krishnaswamy, and B. N. Jagatap, "A 13.56 MHz high power and high efficiency RF source," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2013, pp. 1–4.
[2] F. H. Raab et al., "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 814–826, Mar. 2002.
[3] H. Tebianian, Y. Salami, B. Jeyasurya, and J. E. Quaicoe, "A 13.56-MHz full-bridge class-D ZVS inverter with dynamic dead-time control for wireless power transfer systems," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1487–1497, Feb. 2020.
[4] A. Abuelhaija, K. Solbach, and A. Buck, "Power amplifier for magnetic resonance imaging using unconventional cartesian feedback loop," in *Proc. German Microw. Conf.*, Mar. 2015, pp. 119–122.
[5] A. Al Bastami, H. Zhang, A. Jurkov, A. Radomski, and D. Perreault, "Comparison of radio-frequency power architectures for plasma generation," in *Proc. IEEE 21st Workshop Control Model. Power Electron.*, Nov. 2020, pp. 1–8.
[6] D. J. Economou, "Pulsed plasma etching for semiconductor manufacturing," *J. Phys. D, Appl. Phys.*, vol. 47, no. 30, Jul. 2014, Art. no. 303001.
[7] S. Banna, A. Ankargul, G. Cunge, M. Darnon, E. Pargon, and O. Joubert, "Pulsed high-density plasmas for advanced dry etching processes," *J. Vac. Sci. Technol. A*, vol. 30, no. 4, 2012, Art. no. 040801.
[8] M. K. Kazimierczuk, *RF Power Amplifiers*, Hoboken, NJ, USA: Wiley, 2014.
[9] J. M. Saso, A. J. Lopez-Martin, M. P. Garde, and J. Ramirez-Angulo, "Power-efficient class AB fully differential amplifier," *Electron. Lett.*, vol. 53, no. 19, pp. 1298–1300, 2017.
[10] N. O. Sokal, "Class-E switching-mode high-efficiency tuned RF amplifier: Improvements," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Boston, MA, USA, Jun. 2000, vol. 2, pp. 779–782.
[11] L. Gu, G. Zulauf, Z. Zhang, S. Chakraborty, and J. Rivas-Davila, "Push–pull class Φ_2 RF power amplifier," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10515–10531, Oct. 2020.
[12] Y. Wang, Z. Sun, Y. Guan, and D. Xu, "Overview of megahertz wireless power transfer," *Proc. IEEE*, vol. 111, no. 5, pp. 528–554, May 2023.
[13] A. Al Bastami et al., "Dynamic matching system for radio-frequency plasma generation," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 1940–1951, Mar. 2018.
[14] Y. Li et al., "Extension of ZVS region of series–series WPT systems by an auxiliary variable inductor for improving efficiency," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7513–7525, Jul. 2021.
[15] A. Al Bastami, A. Jurkov, D. Otten, D. T. Nguyen, A. Radomski, and D. J. Perreault, "A 1.5 kW radio-frequency tunable matching network based on phase-switched impedance modulation," *IEEE Open J. Power Electron.*, vol. 1, pp. 124–138, 2020.
[16] C. Liu, Y. Guan, J. Liu, Y. Wang, and D. Xu, "Seamless control strategy and hybrid module architecture of wide power range inverter," *IEEE Trans. Ind. Inform.*, vol. 19, no. 8, pp. 8575–8587, Aug. 2023.
[17] K. Surakitbovorn and J. M. Rivas-Davila, "Modular ON/OFF and phase-shifting for high-speed radio frequency power modulation," *IEEE Open J. Power Electron.*, vol. 1, pp. 393–406, 2020.
[18] X. Liu et al., "A multi-inverter high-power wireless power transfer system with wide ZVS operation range," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14082–14095, Dec. 2022.
[19] A. Bastami and A. Ibrahim, "Efficient radio frequency power generation and impedance matching," Ph.D. dissertation, Massachusetts Institute of Technology, Cambridge, MA, USA, 2020. [Online]. Available: https://dspace.mit.edu/handle/1721.1/129241
[20] S. Moloudi and A. A. Abidi, "The outphasing RF power amplifier: A comprehensive analysis and a class-B CMOS realization," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1357–1369, Jun. 2013.
[21] T. Barton, "Not just a phase: Outphasing power amplifiers," *IEEE Microw. Mag.*, vol. 17, no. 2, pp. 18–31, Feb. 2016.
[22] P. A. J. Nuyts, B. Francois, W. Dehaene, and P. Reynaert, "A CMOS burst-mode transmitter with watt-level RF PA and flexible fully digital front-end," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 10, pp. 613–617, Oct. 2012.
[23] J. Lu, A. Kumar, and K. K. Afridi, "Step-down impedance control network resonant DC–DC converter utilizing an enhanced phase-shift control for wide-input-range operation," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 4523–4536, Sep./Oct. 2018.
[24] H. Zhang et al., "High-efficiency wide-range RF power generation systems with discrete power back-off from multiple inverters," *IEEE Trans. Power Electron.*, vol. 40, no. 1, pp. 290–302, Jan. 2025.

[25] X. Li, D. Zhou, S. Jia, X. Liu, and J. Zou, "A WPT system with wide-range voltage gains and soft switching via primary-side hybrid modulation," *IEEE Trans. Power Electron.*, vol. 39, no. 7, pp. 8985–8997, Jul. 2024.
[26] D. J. Perreault, C. R. Sullivan, and J. M. Rivas, "GaN in switched-mode power amplifiers," in *Gallium Nitride-enabled High Frequency and High Efficiency Power Conversion*, G. Meneghesso, M. Meneghini, and E. Zanoni, Eds., Integrated Circuits and Systems. Berlin, Germany: Springer, 2018, pp. 181–223.
[27] H. Li, Y. Yang, J. Chen, J. Xu, M. Liu, and Y. Wang, "A hybrid class-E topology with constant current and constant voltage output for light EVs wireless charging application," *IEEE Trans. Transp. Electrific.*, vol. 7, no. 4, pp. 2168–2180, Dec. 2021.
[28] H. Hu, J. Su, F. Chen, and Y. Sun, "Modularized inductive power transfer systems with inherent impedance decoupling for high-power applications," *IEEE Trans. Ind. Electron.*, vol. 71, no. 2, pp. 1492–1502, Feb. 2024.
[29] X. Liu et al., "A multi-inverter multi-rectifier wireless power transfer system for charging stations with power loss optimized control," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9261–9277, Aug. 2023.
[30] V. Yousefzadeh, Narisi Wang, Z. Popovic, and D. Maksimovic, "A digitally controlled DC/DC converter for an RF power amplifier," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 164–172, Jan. 2006.
[31] N. Swaminathan and Y. Cao, "An overview of high-conversion high-voltage DC–DC converters for electrified aviation power distribution system," *IEEE Trans. Transp. Electrific.*, vol. 6, no. 4, pp. 1740–1754, Dec. 2020.

Jingtao Wang was born in Ningxia, China. He received the B.Eng. degree in measurement and control technology and instruments from Nanjing University of Posts and Telecommunications, Nanjing, China, in 2023. He is currently working toward the master's degree in control engineering with the University of Electronic Science and Technology of China, Chengdu, China.

His current research interests include RF power amplifiers and power converters.

Xin Liu (Senior Member, IEEE) received the B.S. degree from Wuhan University, Wuhan, China, in 2015, and the Ph.D. degree from Shanghai Jiao Tong University, Shanghai, China, in 2019, both in electrical engineering.

From 2019 to 2021, he was with Huawei Technologies Company, Ltd. From 2021 to 2023, he was with the Department of Electrical Engineering, Shanghai Jiao Tong University, Shanghai, China, as a Postdoctoral Researcher. Since 2023, he has been with Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China as an Associate Researcher. His current research interests include wireless power transfer and radio frequency converter.

Dehong Zhou (Senior Member, IEEE) received the B.S. and Ph.D. degrees in control science and engineering from Huazhong University of Science and Technology, Wuhan, China, in 2012 and 2016, respectively.

From 2016 to 2018, he was a Postdoctoral Research Fellow with Nanyang Technological University, Singapore. From 2018 to 2020, he was a Postdoctoral Fellow with the University of Alberta, Canada. Since 2020, he has been a Full Professor with the School of Automation Engineering, University of Electronic Science and Technology of China (UESTC), Chengdu, China, and Shenzhen Institute for Advanced Study, UESTC, Shenzhen, China. His research interests include power electronics and motor drives.

Zewei Shen (Member, IEEE) was born in Hubei, China. He received the B.S. degree in control science and engineering and the Ph.D. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2012 and 2020, respectively.

From 2020 to 2022, he was a Postdoctoral Research Fellow with the School of Automation Engineering, University of Electronic Science and Technology of China (UESTC), Chengdu, China, and Shenzhen Institute for Advanced Study, UESTC. From 2022 to 2024, he has been with the University of Electronic Science and Technology of China, Chengdu, China, as a Lecturer. Since Jun. 2024, he has been with the University of Electronic Science and Technology of China, Chengdu, China, as an Associate Professor. His current research interests include renewable energy, electromagnetic interference, high power density power supply, and electric motor drives.

Jianxiao Zou (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in control science and engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2000, 2003, and 2009, respectively.

He is currently a Professor with UESTC, and has been serving as the Vice Dean of Shenzhen Institute for Advanced Study, UESTC since 2020. He was a Visiting Scholar with the University of California, Berkeley, CA, USA, in 2010, and a Senior Visiting Professor with Rutgers, the State University of New Jersey, New Brunswick, NJ, USA, in 2014. His current research interests include control theory and control engineering, renewable energy control technologies, and intelligent information processing and control.