A High-Efficiency Fast-Transient Double Hysteretic Control Point-of-Load Converter

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***Abstract*—As portable devices become increasingly sophisticated, the demands for their power management in terms of high power-efficiency and fast-transients are congruously higher. We present herein a point-of-load (PoL) converter with two interesting features. One, compared to state-of-the-art PoLs with comparable transient performance, it features higher power-efficiency across most of the load range. Two, compared to state-of-the-art PoLs with similar power-efficiency, it features faster transients. These attractive features are achieved by our novel proposed double hysteretic control that integrates a voltage-mode hysteretic controller (VMHC) and a current-mode hysteretic controller (CMHC). The modus operandi of the VMHC operates its discontinuous-conduction-mode and continuous-conduction-mode without a mode-selection circuit to derive high power-efficiency. The CMHC combines two conventional current-mode controls to prolong on-time and off-time extensions, enabling fast transients. On the basis of measurements on a monolithic prototype, the power-efficiency is >90% across the 2 mA–3 A load range with a peak-efficiency of 96.1%. The voltage undershoot and overshoot are 70 and 40 mV with recovery times of 3 and 2 μs in response to 2.7 A step-up and step-down load current transients (1 A/μs slew-rate), respectively. Compared to state-of-the-art designs, our PoL optimizes both power-efficiency and transient response, features the best figures of merit, and is highly competitive.**

***Index Terms*—Fast transients, high efficiency, hysteretic control, point-of-load (PoL) converter.**

I. Introduction

ELECTRONIC portable devices are evolving with increasingly sophisticated central processing units, graphics processing units, mobile AI processors, envelop tracking amplifiers [1], [2], etc. Their ensuing demands for power-efficient, stable, and adaptable power management systems with small form factors are congruously increasing. Central to enabling the seamless operation of advanced integrated circuits (ICs) in next-generation portable devices are efficient and reliable power management solutions, including linear and switching regulators [3], [4], [5]. Amongst these solutions, point-of-load (PoL) converters—a subset of switch-mode buck converters—are pivotal components that are placed in close proximity to the load devices. Placing the converter close to the load yields two worthy advantages. One, power losses in the power distribution wires are minimized. Two, the response time to load changes is reduced.

However, with the increasing complexity and power demands of next-generation portable devices, traditional PoLs typically struggle to balance two imperative performance metrics: power-efficiency and transient response. Power-efficiency is typically the priority due to the limited power storage in portable devices and the usual need for prolonged operation time between charging. As portable devices operate in either standby or high-performance mode, the power-efficiency in the standby mode is often as important as that in the high-performance mode [6], [7]. This is the case when the duration of high-performance mode is short and the ensuing overall power dissipation is largely dominated by the long-duration low-power standby mode [8]. Put simply, attaining high power-efficiency across a wide load range is imperative.

Transient response, on the other hand, is likewise imperative, particularly for ensuring smooth and rapid operations during transitions between the standby mode and the high-performance mode. As ICs (constituting the load to the PoL) are fabricated with increasingly finer technological nodes and operate at higher frequencies, the magnitude of load current transients [9] is expected to increase. At the same time, the rise and fall times of load current transients conversely decrease. The ensuing voltage overshoots and undershoots may increase with a prolonged recovery time. This could undesirably lead to timing errors, malfunctions, and may cause permanent damage if the output voltage of the PoL exceeds the safe operating range of load ICs [10].

Based on classic pulsewidth modulation (PWM) Control, pulsed-frequency-modulation control and hysteretic control, several other control schemes [6], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [22], [26], [27] have been reported to improve the power-efficiency and transient response of PoLs. However, these reported schemes are not optimized for both power-efficiency and transient response and are somewhat inadequate for next-generation devices.

Consider the limitations of the reported controls that aim to optimize both power-efficiency and transient response.

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First, for the constant on-time (COT) control [8], [18], [19] where the on-time is fixed, the maximum increment of the inductor current per cycle is limited. Specifically, when a large step-up load current transient with a short rise time is imposed, it takes several switching cycles for the inductor current to track the load current. This leads to larger voltage undershoots and longer recovery time compared to controls [20], [21] capable of prolonging their on-time extensions during critical load transients. Although recent efforts [10], [22] include realizing prolonged on-time extensions in the COT control, they do not support discontinuous-conduction-mode (DCM) operation. Hence, they suffer from low power-efficiency at light loads, where switching losses dominate.

Second, reported multimode control schemes [6], [14], [15], [16], [17], [26], [27] employ multiple always-active control circuits and a mode selection circuit. However, these circuits require a large silicon area and the quiescent current consumption is high, except [27]. Consequently, the power-efficiency at light loads is compromised, with the maximum power-efficiency typically falling below 80% at a 1 mA load. On the other hand, Wang et al. [27] achieves power-efficiency >90% at a load smaller than 1 mA by reducing the quiescent current to 100 nA. However, the transient response of [27] is significantly compromised.

Third, a reported current-mode hysteretic control [12] utilizes an *RC* pair to emulate the inductor current. However, the load regulation of this control degrades as the load current increases due to the parasitic resistance (R_{DCR}) of the inductor. To mitigate the R_{DCR} effects and to support higher load currents, two R_{DCR} offset cancellation techniques were reported [9], [13]. However, both techniques require two highly-matched *RC* pairs, which occupy additional silicon area. Furthermore, additional challenges may arise during mass production to achieve the required matching of the *RC* pairs (e.g., trimming, testing, etc.)

Put simply, the design of a PoL featuring high power-efficiency across a wide load range with fast transient response remains a challenge.

In this article, we address the said challenge by our proposed novel double hysteretic control (DHC), which integrates a voltage-mode hysteretic controller (VMHC) and a current-mode hysteretic controller (CMHC). The modus operandi of the DHC is as follows. The VMHC operates the PoL in DCM and CCM without a mode-selection circuit to achieve high power-efficiency across a wide load range. The CMHC combines conventional current-mode controls to prolong on-time and off-time extensions with on-chip compensation. This renders fast transient response while retaining a small overall form-factor. Note that the fast transient response of our design is the primary parameter for its application as a PoL.

Our monolithic PoL prototype achieves an efficiency >90% across the 2 mA–3 A load range with a peak efficiency of 96.1%. For 2.7 A step-up and step-down load current transients with 1 A/μs slew rate, the voltage undershoot and overshoot are 70 and 40 mV while the transient recovery times are 3 and 2 μs, respectively. Compared to state-of-the-art PoLs with comparable transient response, it features higher power-efficiency across most of the load range. Compared to state-of-the-art PoLs with similar power-efficiency, it features faster transient response.

The rest of this article is organized as follows. Section II delineates the architecture of our proposed DHC scheme. Section III elaborates on design considerations and circuit implementations of the DHC in a PoL. Section IV provides a stability analysis and a design of the compensation network. Section V presents measurement results of our PoL prototype, which are benchmarked against reported designs. Finally, Section VI concludes this article.

II. Proposed DHC

The block diagram of the PoL with the proposed DHC is depicted in Fig. 1. The shaded area encompasses all on-chip functional blocks. The VMHC and the CMHC blocks therein are the major constituent blocks of the proposed DHC, leading to the desired high power-efficiency (over a wide load range) and to fast transients. We will now delineate the operating principles of our proposed control depicted in Fig. 1.

Initially, if V_{FB} is higher than the upper bound of the voltage hysteresis defined by the VMHC, $V_{\mathrm{HYS\_OUT}}$ and *EN* are both low. Both M_{HS} and M_{LS} are OFF. Conversely, when V_{FB} is pulled low by the load and drops below the lower bound of the voltage hysteresis, $V_{\mathrm{HYS\_OUT}}$ and *EN* are pulled high. The CMHC and the Dead-Time Controller are subsequently enabled. The CMHC generates two voltage signals ($V_{\mathrm{PK\_REF}}$ and $V_{\mathrm{VC\_REF}}$) to regulate the inductor current. At the same time, the Dead-Time Controller initiates the nonoverlapping signals to switch M_{HS} and M_{LS}.

The increase and decrease in the inductor current are sensed by the high-side (HS) and low-side (LS) current sensors, respectively. The outputs of the current sensors ($V_{\mathrm{PK\_SEN}}$ and $V_{\mathrm{VC\_SEN}}$) are compared against the outputs of the error amplifier (EA) ($V_{\mathrm{PK\_REF}}$ and $V_{\mathrm{VC\_REF}}$) to ascertain the turn-OFF of M_{HS} and M_{LS}, respectively.

When the load drops and V_{FB} exceeds the upper bound of the VMHC, $V_{\mathrm{HYS\_OUT}}$ and EN are pulled low. Subsequently, M_{HS} and M_{LS} are both turned OFF.

With the proposed control, we will now delineate how high power-efficiency, yet with few, if any, compromises to transient response, is derived. Thereafter, we will delineate how fast transients, yet with few, if any, compromises to power-efficiency, are derived in our design.

To derive the high power-efficiency attribute across a wide load range, the most pertinent consideration is the power-efficiency at light loads. This is because high power-efficiency at medium and heavy loads is easily derived using conventional methods.

In our design, the high power-efficiency at light loads is achieved primarily by a novel means of reducing the quiescent current, yet with minimum compromise on transient response. Specifically, the VMHC in our design combines the functions of two circuits (a control circuit and a mode selection circuit) while consuming a quiescent current equivalent to that of only one circuit—the control circuit.

Compared to reported multimode (e.g., 2-mode) controls [6], [14], [15], [16], [17], our proposed DHC is an improved 2-mode control with fewer always-active circuits and consumes less quiescent current. Compared to the said reported works with

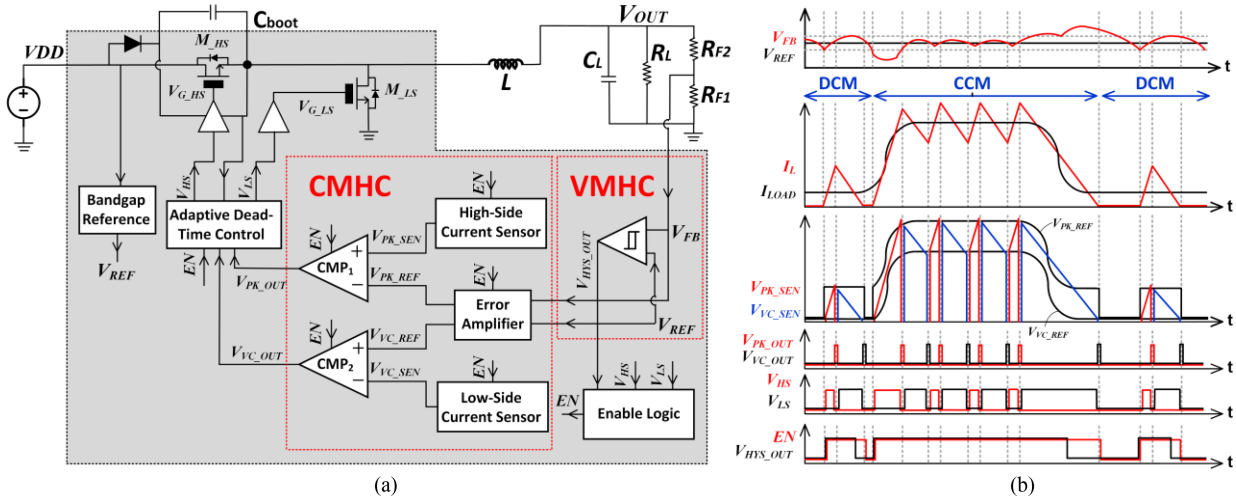

Fig. 1. (a) Main functional blocks of the PoL converter with the proposed DHC and (b) key operating waveforms.

the same fast transients [15], [17], our proposed PoL achieves a worthy 10% –15% power-efficiency improvement at 1 mA load and particularly when the powered device is mostly operating in the standby mode.

For completeness, it is interesting to note that while designs featuring lower quiescent current [8], [13] have been reported, their transient response is significantly compromised, particularly the transient recovery time. Specifically, their transient recovery time is 5–20 times longer than our proposed design.

The reason for their compromised transient response is in part due to the lack of a wide-bandwidth controller, which would otherwise consume a significantly higher quiescent current. In our design, we address this challenge by employing a power-gated wide-bandwidth CMHC that is enabled and disabled by an enable signal. Since the CMHC is power-gated and when disabled, it does not consume quiescent current, thereby not compromising the power-efficiency.

Put simply, high power-efficiency can be derived with minimum compromise to transient response.

To derive the fast-transient attribute, the most pertinent consideration is the transient response during load current transients which traverse >90% of the load range within a short rise/fall time. Conventionally, a wide-bandwidth control [12], [13] is designed to improve the transient response. However, for load current transients with a large magnitude and a short rise/fall time, a wide-bandwidth control alone is insufficient [21]—prolonged on-time and off-time is required. The reported means [21] of obtaining prolonged on-time and off-time incurs relatively complex hardware, which in turn dissipates relatively high quiescent current. This leads to undesirable low power-efficiency.

Our proposed CMHC conversely achieves prolonged on-time and off-time extensions primarily by a novel means of realizing a current-mode hysteretic control, yet with minimum compromise to power-efficiency. Specifically, the proposed CMHC is designed by combining the conventional peak current-mode control (PCMC) and conventional valley current-mode control (VCMC), as depicted in Fig. 1. We will now delineate three

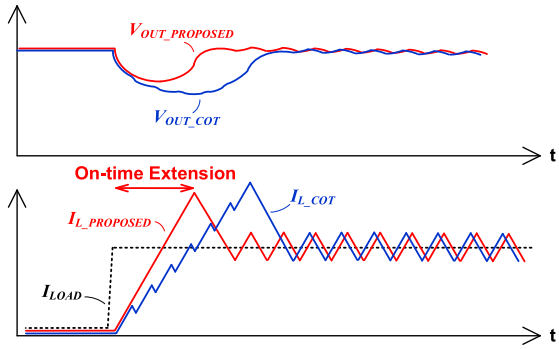

Fig. 2. Comparison between the COT control scheme and the proposed DHC scheme under a large step-up load current transient.

features offered by our proposed CMHC. This delineation serves in part as a preamble to the detailed designs in the next section.

First, a wide-bandwidth CMHC is derived with simplified compensation. Conventionally, Type II compensation is employed in current-mode control to achieve stability [23] and slope compensation [23] to avoid subharmonic oscillations when the duty cycle is >50% in PCMC and <50% in VCMC. In our proposed CMHC, we adopt the Type II compensation but without the need for slope compensation, yet without subharmonic oscillations in all duty cycles. It is desirable that slope compensation is not needed because the ensuing complexity of the control circuit, the quiescent current and the form factor are all reduced. In this perspective, our design is somewhat similar to a reported current-mode hysteretic control design [12] but with significantly faster transients.

Second, our proposed CMHC features the proposed prolonged on-time and off-time extensions. Unlike PWM control or COT control [6], [18], our proposed CMHC is clockless, where the on-time and off-time extensions are not constrained by a fixed period or on-time.

Fig. 2 compares the transient response of our proposed control to that of a COT control. $V_{\rm OUT}$ is the output voltage, I_L is the inductor current, and $I_{\rm LOAD}$ is the load current. It can be

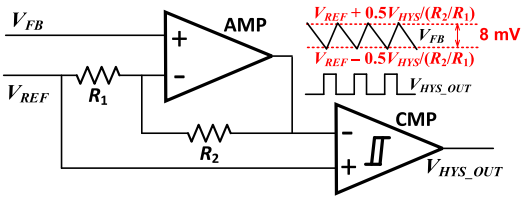

Fig. 3. Design of the VMHC.

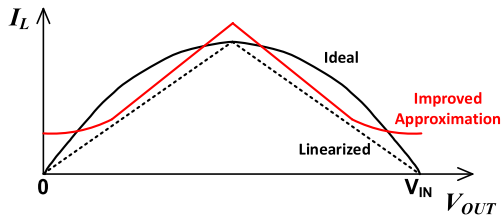

Fig. 4. Relationship between V_{OUT} and I_L – ideal, linearized and improved approximation.

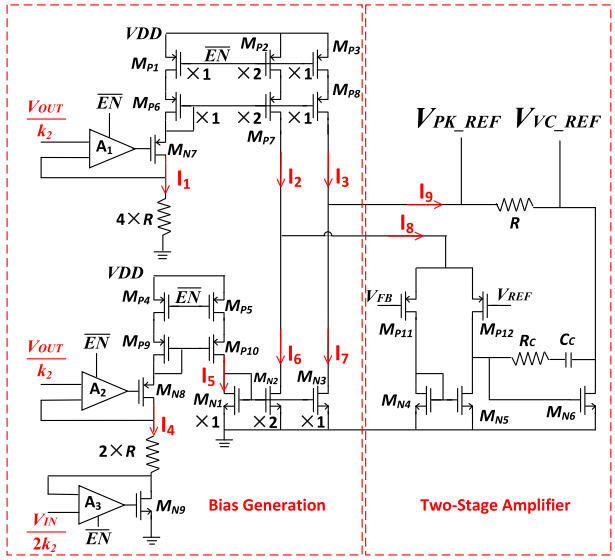

Fig. 5. Schematic of the EA embodying a novel adaptive current hysteresis control.

observed that when a step-up load current transient occurs, our proposed control extends the on-time significantly longer within a single cycle to derive faster transients.

Third, our proposed CMHC imposes minimum compromise on power-efficiency over a wide load range for two main reasons. One, at light loads, since the CMHC is power-gated, it does not consume quiescent current when disabled. In this fashion, the CMHC imposes minimum compromise to light load power-efficiency. Two, at heavy loads, since the power loss caused by the CMHC is significantly lower compared to conduction and switching losses, the CMHC largely does not compromise the heavy load power-efficiency.

In summary, from the three aforesaid features, fast transients can be derived with minimum compromise to power-efficiency over a wide load range.

III. Design Considerations and Circuit Implementations

In this section, we will delineate the design considerations and the ensuing circuit implementations for critical functional blocks of the VMHC and the CMHC.

A. Design of the VMHC

The simplified schematic of the VMHC in our design is depicted in Fig. 3. It embodies a voltage-mode hysteretic control and produces an output which in part power-gates the CMHC. The VMHC embodies two stages. The first stage and second stage embody a signal amplifier (AMP) and a comparator with hysteresis (CMP), respectively. The voltage hysteresis of the VMHC is defined by the reference voltage (V_{REF}, 800 mV), hysteresis of the CMP (V_{HYS}) and the ratio between R_1 and R_2 (i.e., $V_{\mathrm{REF}}\pm 0.5V_{\mathrm{HYS}}/(R_2/R_1)$). The output of the VMHC ($V_{\mathrm{HYS\_OUT}}$) is pulled high or low when the feedback voltage (V_{FB}) exceeds the upper bound or drops below the lower bound, respectively.

There are two key considerations. First, the VMHC needs to dissipate very low quiescent current ($\sim$10 μA), yet with little compromise to its speed. This is to derive high power-efficiency (i.e., $>$ 85%) at light loads and without compromising the fast transients. The latter is because the CMHC is in part enabled by the VMHC where any delay in VMHC would delay CMHC regulation.

Second, the VMHC needs to feature a small voltage hysteresis to derive small output voltage ripple, yet with sufficient margin to prevent misoperations. To illustrate the misoperation, consider the following scenario. In a heavy load condition, the PoL is supposed to operate in CCM. However, due to nonidealities, V_{FB} may inadvertently exceed the upper bound of the voltage hysteresis and consequently the PoL may erroneously enter DCM. This could undesirably lead to large voltage ripples on V_{OUT} and significantly deteriorate the power-efficiency of the PoL.

Misoperations are caused by nonidealities arising from the variations in IC fabrication, nonidealities of passives and PCB parasitics. The major nonideality arises from the equivalent series resistance (ESR) of the output capacitor, which increases voltage ripple on V_{OUT} as well as V_{FB}.

In our design, the maximum voltage ripple on V_{FB} in the CCM is estimated to be 4 mV at the nominal condition (i.e., 1 μH inductor, 22 μF ceramic capacitor with 4 mΩ ESR, 2 MHz switching frequency). An additional 4 mV margin is added to account for other minor nonidealities, including input voltage offsets, noise, etc. We judiciously and conservatively design the voltage hysteresis on V_{FB} regulation to be 8 mV, and the ensuing V_{HYS} is designed to be 80 mV and a resistor ratio (i.e., R_2 /R_1 in Fig. 3) designed to be 10.

B. Design of the CMHC EA

The CMHC in our design embodies current-mode hysteretic control and consists of an EA, two current sensors and two comparators (depicted in Fig. 1). The design of the EA depicted

in Fig. 5 embodying a novel adaptive current hysteresis control is now delineated.

The EA amplifies the difference between $V_{\rm FB}$ and $V_{\rm REF}$, and outputs two signals ($V_{\rm PK\_REF}$ and $V_{\rm VC\_REF}$), which control the peak and valley current of the inductor current hysteresis (I_L), respectively. The EA embodies two stages: the bias generation and the two-stage amplifier.

The key consideration for the EA design is to reduce the range of the switching frequency (f), which can otherwise be very large (e.g., 1.5–3 MHz). This is because of the clockless design in our proposed PoL with a fixed current hysteresis, vis-à-vis the conventional PoL, which does not suffer from this due to the clock. To this end, we propose an EA to realize an adaptive current hysteresis (I_L) which approximates the ideal I_L in conventional clocked PoL. The ideal I_L is expressed in (1), where L is the inductance, $V_{\rm IN}$ is the input voltage, and $V_{\rm OUT}$ is the output voltage

$$I_L = \frac{1}{Lf} \cdot \frac{(V_{\rm IN} - V_{\rm OUT}) \cdot V_{\rm OUT}}{V_{\rm IN}}. \tag{1}$$

To realize the quadratic function of (1), a complex circuit is needed, which would occupy a large chip area and incur power loss. To mitigate these overheads, we linearize (1) to realize an approximation with our proposed EA.

The ideal quadratic relationship is represented by the black solid parabola in Fig. 4, where L, f, and $V_{\rm IN}$ are considered to be constant. We linearize the quadratic function in (1) to (2) with $k_1 = 1$, which is represented by the black dotted 2-segment polyline. As the linearized I_L value is always less than or equal to that of the ideal I_L value, the ensuing f is always higher or equal to the ideal f. We improve the approximation by designing k_1 to be slightly larger. The improved approximation is represented by the red solid curve. Comparing the improved approximation to the ideal, if I_L is larger, the ensuing f is lower, and vice versa

$$I_L = \begin{cases} \frac{k_1}{2Lf} \cdot V_{\rm OUT} & \text{if } 0 < V_{\rm OUT} < \frac{V_{\rm IN}}{2} \\ \frac{k_1}{2Lf} \cdot (V_{\rm IN} - V_{\rm OUT}) & \text{if } \frac{V_{\rm IN}}{2} \le V_{\rm OUT} < V_{\rm IN} \end{cases}. \tag{2}$$

In Fig. 4, note that at both the left-most ($V_{\rm OUT}$ approaching 0) and the right-most ($V_{\rm OUT}$ approaching to $V_{\rm IN}$) ends of the improved approximation, the designed I_L tracks the ideal I_L more closely as the gradient flattens out. This is because we implement minimum on-time and minimum off-time ($\sim$20 ns). I_L is hence clamped and the designed f deviates less from the ideal f at extreme $V_{\rm OUT}/V_{\rm IN}$ (i.e., $<$0.2 or $>$0.8). To reduce the range of the switching frequency to a minimum, we judiciously design $k_1 = 1.07$.

Consider now our circuit design of the EA depicted in Fig. 5 to realize the adaptive current hysteresis control [expressed in (2)]. As delineated in Section I, our design employs a power-gated CMHC to reduce quiescent current and improve power-efficiency. Specifically, M_{P1}–M_{P5} are switches controlled by an enable signal ($\overline{EN}$). When disabled, M_{P1}–M_{P5} are turned OFF and the EA dissipates no quiescent current.

When enabled, fractions (realized by voltage dividers) of $V_{\rm IN}$ and $V_{\rm OUT}$ (i.e., $V_{\rm OUT}/k_2$ and $V_{\rm IN}/2k_2$) are input into three amplifiers (A_1–A_3). Bias currents I_1 and I_4 are generated and their values are ascertained as in (3) and (4), respectively. M_{P6}–M_{P8} and M_{N1}–M_{N3} are current mirrors to generate I_8 and I_9, which thereafter bias the two-stage amplifier. Values of I_8 and I_9 are ascertained as in (5)

$$I_1 = V_{\rm OUT} \,/\, (4k_2 R) \tag{3}$$

$$I_4 = \begin{cases} 0 & \text{if } 0 < V_{\rm OUT} < \frac{V_{\rm IN}}{2} \\ (2V_{\rm OUT} - V_{\rm IN}) \,/\, (4k_2 R) & \text{if } \frac{V_{\rm IN}}{2} \le V_{\rm OUT} < V_{\rm IN} \end{cases} \tag{4}$$

$$I_8 = 2I_9 = 2\,(I_3 - I_7) = \; 2\,(I_1 - I_4)\,. \tag{5}$$

In our proposed CMHC, I_L is the difference between the peak current and the valley current, as expressed in (6). The peak and valley current are derived by multiplying current sensor gains (i.e., $A_{\rm CS\_HS}$ and $A_{\rm CS\_LS}$) and EA outputs (i.e., $V_{\rm PK\_REF}$ and $V_{\rm VC\_REF}$), respectively. The derivation of $A_{\rm CS\_HS}$ and $A_{\rm CS\_LS}$ is provided in Section III-C in conjunction with the designs of the current sensors

$$I_L = A_{\rm CS\_HS} \cdot V_{\rm PK\_REF} - A_{\rm CS\_LS} \cdot V_{\rm VC\_REF}. \tag{6}$$

If $A_{\rm CS\_HS} = A_{\rm CS\_LS} = A_{\rm CS}$

$$I_L = A_{\rm CS} \cdot (V_{\rm PK\_REF} - V_{\rm VC\_REF}) = A_{\rm CS} \cdot I_9 \cdot R$$

$$I_L = A_{\rm CS} \cdot (I_1 - I_4) \cdot R. \tag{7}$$

Substituting (3) and (4) into (7), we derive I_L as expressed in (8). As desired, I_L depends on $V_{\rm IN}$ and $V_{\rm OUT}$

$$I_L = \begin{cases} A_{\rm CS} \cdot \frac{V_{\rm OUT}}{4k_2} & \text{if } 0.2V_{\rm IN} < V_{\rm OUT} < 0.5V_{\rm IN} \\ A_{\rm CS} \cdot (V_{\rm IN} - V_{\rm OUT}) \,/\, (4k_2) & \text{if } 0.5V_{\rm IN} \le V_{\rm OUT} < 0.8V_{\rm IN} \end{cases}. \tag{8}$$

We realize the aforesaid improved approximation by equating (8)–(2), yielding the value of k_2 derived in the following equation:

$$k_2 = \; 1.07 \cdot A_{\rm CS} \cdot L \cdot f/2. \tag{9}$$

For completeness, R in Fig. 5 is designed to be 20 kΩ to bias all transistors in their respective operating regions when enabled.

The design of the compensation network (i.e., R_C and C_C) in Fig. 5 is discussed in Section IV in conjunction with the stability analysis.

C. Design of the Current Sensors

To realize a current-mode hysteretic control that embodies both PCMC and VCMC, two current sensors are employed. We design a HS current sensor and a LS current sensor, which convert the inductor current to voltage signals when HS and LS power transistors (i.e., $M_{\rm HS}$ and $M_{\rm LS}$) are ON, respectively. When disabled (i.e., EN $= 0$ and $\overline{\rm EN} = 1$), both current sensors are turned OFF, hence consuming no quiescent current. The circuit implementations and operations of the HS and LS current sensors are depicted in Figs. 6 and 7, respectively. The half-bridge of the PoL is enclosed by the dotted boxes. The operation principles of the current sensors are briefly described as follows.

In Fig. 6(a), the HS current sensor is turned OFF. $V_{\rm PK\_SEN}$ is small, as only I_B flows into the sense resistor. Conversely, in

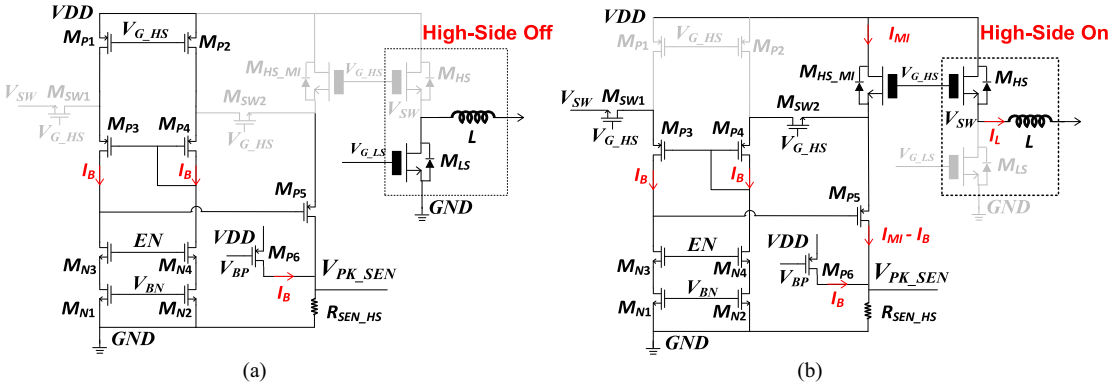

Fig. 6. Schematic and operation of the HS current sensor. (a) OFF. (b) ON.

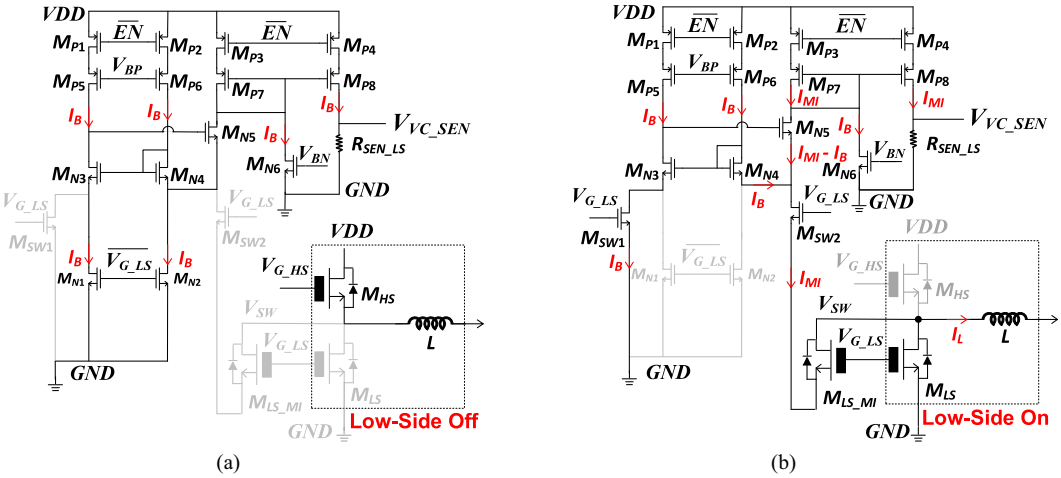

Fig. 7. Schematic and operation of the LS current sensor. (a) OFF. (b) ON.

Fig. 6(b), the HS current sensor is turned ON. The common gate amplifier ($M_{P3\text{-}5}$) regulates the voltage at the source of M_{P3} to be equal to the voltage at the source of M_{P4}. Since M_{SW1} and M_{SW2} are large, the voltage drops across M_{SW1} and M_{SW2} are negligible. Hence, the voltage at the source of $M_{\mathrm{HS\_MI}}$ is regulated to V_{SW}, rendering $M_{\mathrm{HS\_MI}}$ a near-perfect mirror for M_{HS}. To compensate for the bias current loss, M_{P6} is employed. In this fashion, the output of the current sensor (i.e., $V_{\mathrm{PK\_SEN}}$) is proportional to I_L when M_{HS} is ON.

The LS current sensor, depicted in Fig. 7, operates with the same principles. The ensuing $V_{\mathrm{VC\_SEN}}$ is proportional to I_L when M_{LS} is ON.

Consider three critical design considerations. The first design consideration is the matching of the respective current sensor gains (i.e., $A_{\mathrm{CS\_HS}}$ and $A_{\mathrm{CS\_LS}}$) of the two current sensors. This is critical to derive a consistent I_L [as expressed in (6)], which in turn derives a stable switching frequency regardless of load variations. To achieve A_{CS} matching, both current sensors are designed to be as symmetrical as possible. Critical devices are matched in layout to achieve A_{CS} matching. In terms of sizing, the following device pairs are designed to be equal-sized: M_{HS} and M_{LS}; $M_{\mathrm{HS\_MI}}$ and $M_{\mathrm{LS\_MI}}$; and $R_{\mathrm{SEN\_HS}}$ and $R_{\mathrm{SEN\_LS}}$. In terms of placement, M_{HS} and M_{LS} are horizontally symmetrical; $M_{\mathrm{HS\_MI}}$ and $M_{\mathrm{LS\_MI}}$ are placed next to M_{HS} and M_{LS}, respectively; and $R_{\mathrm{SEN\_HS}}$ and $R_{\mathrm{SEN\_LS}}$ are placed in the middle of the chip and are matched using the common centroid method.

Fig. 8(a) and (b) depicts the Monte Carlo simulations to derive the variations of $A_{\mathrm{CS\_HS}}$, $A_{\mathrm{CS\_LS}}$, and $A_{\mathrm{CS\_HS}}/A_{\mathrm{CS\_LS}}$ due to process variations; the variations due to voltage and temperature are marginal and are hence not depicted. From Fig. 8(a), $A_{\mathrm{CS\_HS}}$ and $A_{\mathrm{CS\_LS}}$ have a mean value of 3.011 with a standard deviation of 0.184. High current sensing accuracy is hence derived since $>90\%$ $A_{\mathrm{CS\_HS}}$ and $A_{\mathrm{CS\_LS}}$ fall in the $\pm 10\%$ range. From Fig. 8(b), $A_{\mathrm{CS\_HS}}/A_{\mathrm{CS\_LS}}$ has a mean value of 1 and a standard deviation of 0.074. Relatively good current sensing matching is derived since $>80\%$ $A_{\mathrm{CS\_HS}}/A_{\mathrm{CS\_LS}}$ fall in the $\pm 10\%$ range. For completeness, note that the variations of $R_{\mathrm{SEN\_HS}}$ and $R_{\mathrm{SEN\_LS}}$ are included in the derivation of Fig. 8(a) but excluded in the derivation of Fig. 8(b) because they are well matched in their layout.

The second design consideration is to achieve high bandwidth with low power loss. A high bandwidth design can be achieved if I_B and I_{MI} are large. However, a large I_B and I_{MI} would reduce the power-efficiency. To achieve a somewhat optimal design, under nominal operating conditions (i.e., $V_{\mathrm{IN}} = 5$ V, $V_{\mathrm{OUT}} = 1.8$ V, and $I_L = 1$ A), we judiciously design $I_B = 50$ μA and $I_{\mathrm{MI}} = 185$ μA. The ensuing bandwidth of the HS current sensor depicted in Fig. 6 is 70 MHz. To achieve the 70 MHz bandwidth

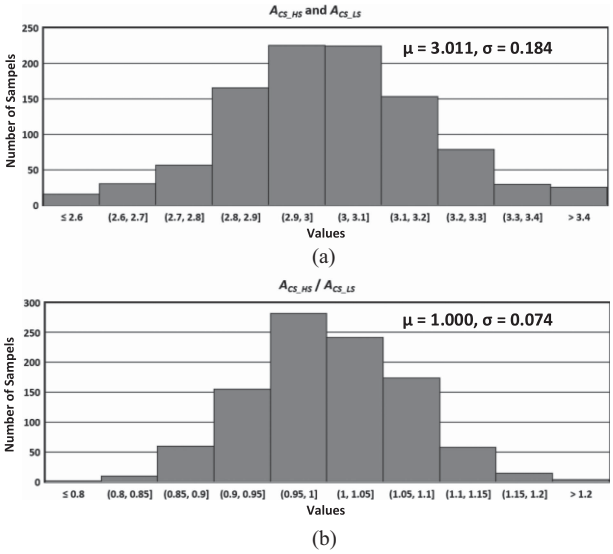

Fig. 8. Monte carlo simulation on (a) 1000 samples of $A_{\mathrm{CS\_HS}}$ and $A_{\mathrm{CS\_LS}}$, and (b) 1000 samples of $A_{\mathrm{CS\_HS}}/A_{\mathrm{CS\_LS}}$.

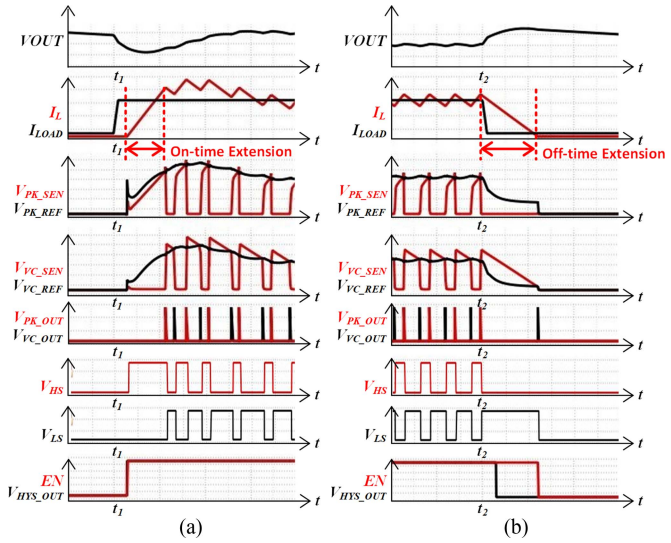

Fig. 9. Waveforms of the CMHC. (a) Step-up load current transient. (b) Step-down load current transient.

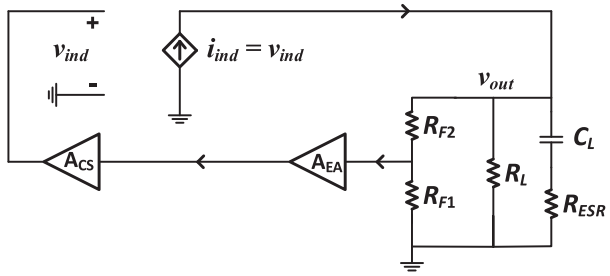

Fig. 10. Linearized model for the loop-gain analysis.

with 185 μA I_{MI}, the mirror ratio (width of M_{HS} divided by the width of $M_{\mathrm{HS\_MI}}$) is designed to be 5400 (i.e., 1 A / 185 μA). The LS current sensor is similarly designed (see Fig. 7) to derive the same bandwidth. Note that I_B of the LS current sensor is 20 μA (vis-à-vis 50 μA in the HS current sensor). This is because M_{N4} in Fig. 7(b) achieves the same transconductance with less bias current compared to M_{P4} in Fig. 6(b).

The third design consideration pertains to the design of an appropriate $A_{\mathrm{CS\_HS}}$, which produces $V_{\mathrm{PK\_SEN}}$ with a reasonable output range for the input of the subsequent comparator. As the minimum value of $V_{\mathrm{PK\_SEN}}$ is 0 V when $I_L = 0$ A, a PMOS input comparator (i.e., CMP_1 in Fig. 1) is employed to compare $V_{\mathrm{PK\_SEN}}$ and $V_{\mathrm{PK\_REF}}$. Since V_{IN} has a minimum value of 2.5 V and a headroom of 1 V is typically reserved, the maximum $V_{\mathrm{PK\_SEN}}$ should not exceed 1.5 V. We conservatively design the maximum $V_{\mathrm{PK\_SEN}}$ to be ~1 V at the maximum load of 3 A. Hence, $A_{\mathrm{CS\_HS}} = 3$ (i.e., 3 A / 1 V). To derive this $A_{\mathrm{CS\_HS}}$, we design $R_{\mathrm{SEN\_HS}} = 1800\ \Omega$ (i.e., $R_{\mathrm{SEN\_HS}}$ = mirror ratio / $A_{\mathrm{CS\_HS}} = 1800$). The LS current sensor is similarly designed (see Fig. 7) to derive the same A_{CS} (i.e., $A_{\mathrm{CS\_LS}} = A_{\mathrm{CS\_HS}} = A_{\mathrm{CS}} = 3$).

With the designed CMHC amplifier (see Fig. 5) and current sensors (see Figs. 6 and 7), we simulate our design to verify the effectiveness our design in improving transient response. Fig. 9 depicts the waveforms of the CMHC—all responses delineated below are as expected. At t_1, when a step-up current transient occurs, $V_{\mathrm{PK\_REF}}$ increases. As M_{HS} is turned ON, I_L rises and $V_{\mathrm{PK\_SEN}}$ increases since $V_{\mathrm{PK\_SEN}}$ is proportional to I_L. When $V_{\mathrm{PK\_SEN}}$ exceeds $V_{\mathrm{PK\_REF}}$, the output ($V_{\mathrm{PK\_OUT}}$) of the peak current comparator (CMP_1 in Fig. 1) is pulled high. M_{HS} is subsequently turned OFF. In this fashion, prolonged on-time extension is achieved in the step-up transient response. Similarly, at t_2, when a step-down load current transient happens, prolonged off-time extension is achieved.

IV. Stability Analysis

Consider now the stability analysis and the design of the compensation network (i.e., R_C and C_C in Fig. 5) in our proposed PoL. The key consideration is to derive a stable wide-bandwidth control, yet with a small form factor. We will derive only the stability analysis for CCM operations because DCM operations are innately stable under the control of the VMHC.

Fig. 10 depicts an average model to approximate the current-loop regulation, where the inductor is depicted as an ideal voltage-controlled current source. The contributing factors of the loop-gain (A_L) are the output impedance (r_{out}), feedback factor (β), EA gain (A_{EA}), and the current sensor gain (A_{CS}). Amongst these factors, r_{out} and β are easily derived as expressed in (10) and (11), respectively. A_{EA} is derived based on the proposed EA in Section III-B (see Fig. 5) and expressed in (12). A_{CS} is derived similarly to a reported work [25] and is expressed in (13), where p_{cs1} and p_{cs2} arise from high impedance nodes in the designed current sensors. A_L is hence derived as expressed in (14)

$$r_{\mathrm{out}}(s) = \frac{1 + sR_{\mathrm{ESR}}C_L}{1 + s\left(R_{\mathrm{ESR}} + R_L\right)C_L} \tag{10}$$

$$\beta = \frac{R_{F1}}{R_{F1} + R_{F2}} \tag{11}$$

$$A_{\mathrm{EA}}(s) = -\frac{|A_{\mathrm{EA}}| \cdot \left(1 + s\left(R_C - \frac{1}{g_m}\right) C_C\right)}{1 + s g_m {R_{\mathrm{out}}}^2 C_C} \tag{12}$$

$$A_{\mathrm{cs}}(s) = \frac{|A_{\mathrm{cs}}|}{\left(1 + \frac{s}{p_{\mathrm{cs1}}}\right)\left(1 + \frac{s}{p_{\mathrm{cs2}}}\right)} \tag{13}$$

$$\begin{aligned} A_L(s) = {} & \frac{1 + sR_{\mathrm{ESR}}C_L}{1 + s\left(R_{\mathrm{ESR}} + R_L\right)C_L} \times \frac{R_{F1}}{R_{F1} + R_{F2}} \\ & \times \frac{-|A_{\mathrm{EA}}| \cdot \left(1 + s\left(R_C - \frac{1}{g_m}\right) C_C\right)}{1 + s g_m {R_{\mathrm{out}}}^2 C_C} \\ & \times \frac{|A_{\mathrm{cs}}|}{\left(1 + \frac{s}{p_{\mathrm{cs1}}}\right)\left(1 + \frac{s}{p_{\mathrm{cs2}}}\right)}. \end{aligned} \tag{14}$$

From (14), A_L has 4 poles and 2 zeros. Of these, only the EA pole (p_e), output pole (p_o), and the EA zero (z_e) are important and are expressed in (15)–(17), respectively. The other poles and zero do not significantly impact the stability of the system because they reside at frequencies higher than the unity-gain frequency. Specifically, our proposed PoL operates at 2.1 MHz and the maximum unity-gain frequency is designed to be about 400 kHz. The ESR zero is neglected because it resides at a frequency >2 MHz, which is considerably larger than the unity-gain frequency. The two current sensor poles (p_{cs1} and p_{cs2}) are neglected because they reside at frequencies >20 MHz

$$f_{p_e} = -\frac{1}{2\pi \times g_m {R_{\mathrm{out}}}^2 C_C} \tag{15}$$

$$f_{p_o} = -\frac{1}{2\pi \times \left(R_{\mathrm{ESR}} + R_L\right) C_L} \tag{16}$$

$$f_{z_e} = -\frac{1}{2\pi \times \left(R_C - \frac{1}{g_m}\right) C_C}. \tag{17}$$

We design R_C and C_C to be 150 kΩ and 10 pF, respectively. Both R_C and C_C are designed using on-chip resistors and on-chip capacitors to derive a small form factor. Fig. 11 depicts the bode plots of loop-gain A_L at 0.3 A and 3 A load currents. These two load conditions are considered because 0.3 A is approximately the minimum load for the PoL to operate in CCM and 3 A is the maximum load the PoL is designed to deliver. The solid lines represent the loop-gains when A_{CS} is accurate and matched. The dotted lines, on the other hand, represent the loop-gains at worst-case A_{CS} variations. From our simulations, at 0.3 A load, the phase margin is 61°–70° and the bandwidth is 180–220 kHz. At 3 A load, on the other hand, the phase margin is 91°–105° and the bandwidth is 350–450 kHz.

A phase margin ≥60° is always assured for sake of stability. Of particular note, a salient feature of our EA design is that when the load current decreases to 0.3 A, the frequency of p_e increases and the frequency of z_e decreases. This leads to the phase margin remaining slightly >60° and the response is overdamped. This is because, as the load current decreases to 0.3 A, $V_{\mathrm{VC\_REF}}$ (depicted in Fig. 5) decreases, and M_{N6} in the EA enters the linear region. The transconductance of M_{N6} (g_m) decreases, which in turn increases the frequency of p_e and decreases the frequency of z_e according to (15) and (17), respectively. This overdamped response is critical since it prevents misoperations (i.e., the upper bound of the voltage hysteresis delineated in Section III-A is not tripped) when the proposed PoL transits from DCM to CCM.

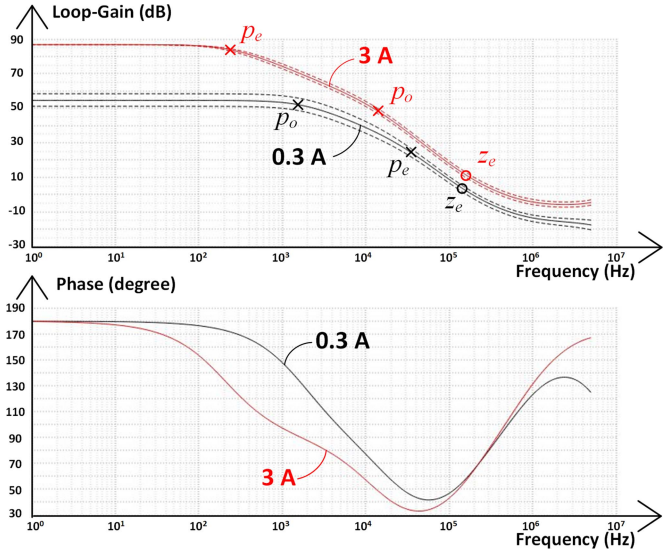

Fig. 11. Bode plots of the loop gain at 0.3 A load and 3 A load ($V_{\mathrm{IN}} = 5$ V, $V_{\mathrm{OUT}} = 1.8$ V and $C_L = 22$ μF).

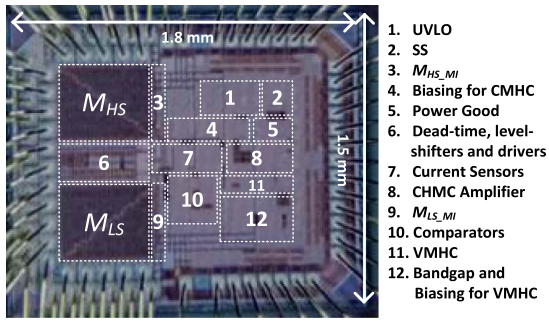

Fig. 12. Chip micrograph of the proposed PoL.

V. Measurement Results

Fig. 12 depicts the chip micrograph of our proposed PoL fabricated in 130-nm BCD process. The die area is 2.7 mm^2 and the IC is packaged in a 5 mm × 5 mm QFN package. The external passives—the inductor and the output capacitor—are 1 μH and 22 μF, respectively. Our proposed PoL is designed to operate under V_{IN} that ranges from 2.5–5 V and generate V_{OUT} that ranges from 0.8–3.3 V with a maximum load current of 3 A. Figs. 13 –16 depict measurement results of our PoL prototype where V_{IN} is the input voltage, V_{OUT} is the output voltage, I_{LOAD} is the load current, and I_L is the inductor current.

Fig. 13 depicts the measured V_{OUT} and I_L when the proposed PoL transits seamlessly from DCM to CCM. These results are congruous to our designs delineated in Section III-A. In Fig. 13(a) and (b), under light loads (i.e., 50 mA and 100 mA), the PoL operates in DCM as expected. The voltage ripple on V_{OUT} is desirably small (i.e., 22 mV), which is less than 1%

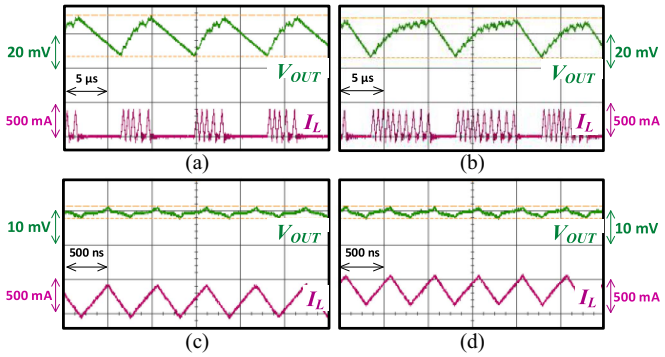

Fig. 13. Measured V_{OUT} and I_L ripple under $V_{\rm IN} = 4$ V and $V_{\rm OUT} = 2.5$ V at different load currents. (a) 50 mA. (b) 100 mA. (c) 200 mA. (d) 300 mA.

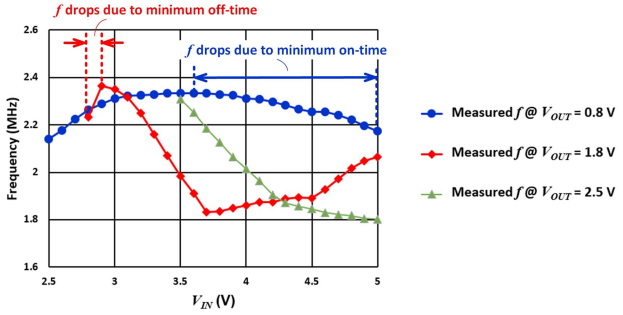

Fig. 14. Measured switching frequencies at different $V_{\rm IN}$ and $V_{\rm OUT}$.

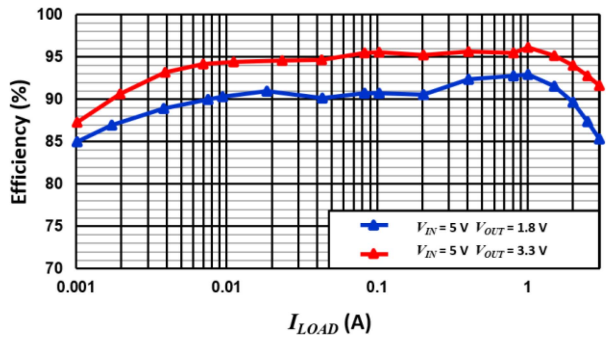

Fig. 15. Measured power-efficiency at different $V_{\rm IN}$, $V_{\rm OUT}$, and $I_{\rm LOAD}$.

of $V_{\rm OUT}$ (i.e., 2.5 V). As the load current increases to 200 mA, the PoL enters CCM smoothly without any misoperations as depicted in Fig. 13(c) and (d).

Fig. 14 depicts the measured switching frequency (f) of our PoL operating in CCM at different $V_{\rm IN}$ and $V_{\rm OUT}$. The measured f range is 1.8–2.4 MHz with an average value of 2.1 MHz. The measured f, as delineated in current hysteresis control, approximates the constant f of a clocked design. Variations in f are expected since our proposed PoL is clockless. Delays in pertinent circuits (e.g., current sensors, level-shifters, etc.), to some extent, also contribute to f variations.

Fig. 15 depicts the measured power-efficiency under two typical $V_{\rm IN}$ and $V_{\rm OUT}$ conditions. For $V_{\rm IN} = 5$ V and $V_{\rm OUT} = 3.3$ V, a peak power-efficiency of 96.1% is achieved at $I_{\rm LOAD} = 1$ A. The power-efficiency remains >90% across the 2 mA–3 A load range. For $V_{\rm IN} = 5$ V and $V_{\rm OUT} = 1.8$ V, a peak power-efficiency of 92.9% is achieved at $I_{\rm LOAD} = 1$ A. The power-efficiency remains >85% across the 1 mA–3 A load range. In short, high power-efficiency across a wide load range is achieved and is in part attributed to the proposed VMHC. The comparisons with reported work are tabulated in Tables I and II later.

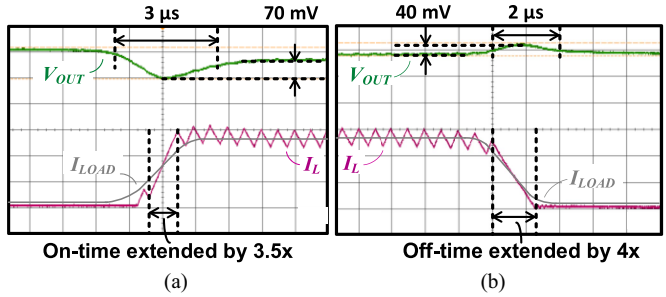

Fig. 16. Measured transient response of the proposed PoL when tested with (a) a 2.7-A step-up load current transient, and (b) a 2.7-A step-down load current transient ($V_{\rm IN} = 5$ V and $V_{\rm OUT} = 1.8$ V).

Fig. 16(a) and (b) depicts the measured transient response of our proposed PoL when tested with 2.7 A step-up and step-down load current transients (with 1 A/μs slew rate), respectively. In Fig. 16(a), when our PoL is tested with a 0.1–2.8 A step-up load current transient, the voltage undershoot is 70 mV while the undershoot recovery time is short—3 μs. In Fig. 16(b), when our PoL is tested with a 2.8–0.1 A step-down load current transient, the voltage overshoot is 40 mV and the overshoot recovery time is likewise short—2 μs. These fast transients are largely attributed to the proposed CMHC.

It is interesting to note that our proposed PoL achieves faster transient response compared to a reported design with similar bandwidth but without prolonged on-time and off-time extensions [12]; the comparisons with other pertinent state-of-the-art are tabulated in Tables I and II later. Specifically, compared to [12], the step-up and step-down transient recovery times of our design are reduced by 36% and 61%, respectively. These results highlight the importance of prolonged on-time and off-time extensions (3.5× and 4× respectively, as depicted in Fig. 15) in addition to attaining a wide bandwidth for deriving fast transients.

For ease of benchmarking key parameters of our proposed PoL against pertinent state-of-the-art buck converters [9], [13], [16], [17], [18], [22], we tabulate two tables. Table I benchmarks our design to state-of-the-art buck converters with comparable power-efficiencies [13], [16], [18], [28]. Table II, on the other hand, benchmarks our design to state-of-the-art buck converters with comparable transient response [17], [18], [22], [30].

On the basis of Table I, we make the following comments. First, our design features the fastest transient response amongst design with comparable power-efficiency [13], [16], [18], [28]. Specifically, our step-up and step-down transient recovery times are the shortest—3 μs and 2 μs, respectively. The step-up and step-down transient recovery times are equivalent and 26% shorter, respectively, compared to the best amongst the reported converters [18].

TABLE I
PERFORMANCE COMPARISON TO STATE-OF-THE-ART BUCK CONVERTERS WITH COMPARABLE POWER-EFFICIENCY

	This work	TPEL' 2019 [13]	TPEL' 2021 [18]	ISSCC' 2022 [28]	TPEL' 2024 [16]
Maximum Load Current (A)	**3**	0.3	2	2	2
Switching Frequency (MHz)	**1.8–2.4**	1	2	2	2
Inductor (µH), Capacitor (µF)	**1, 22**	2.2, 2.2	2.2, 10	0.4, 20	4.7, 22
Load Step (A), Slew Rate (A/µs)	**0.1–2.8, 1**	0–0.3, N.A.	0–2, 0.5*	0–2, 0.2*	0.02–2, 0.2*
Undershoot, Overshoot (mV)	**70, 40**	37, 34	72, 85	23, 23.8	60, 160
Step-up and Step-down Transient Recovery Times (µs)	**3.0, 2.0**	40, 15	3.0, 2.7	25, 30	15, 120
Light Load Power-Efficiency (%) @ V_{IN}, V_{OUT}, I_{LOAD}	**90.6 @ 5 V, 3.3 V, 2 mA**	90 @ 1.8 V, 1.5 V, 0.1 mA	82.6 @ 12 V, 5 V, 10 mA	92.5 @ 5 V, 1 V, 50 mA	80 @ 5.5 V, 3 V, 15 mA
Peak Power-Efficiency (%) @ V_{IN}, V_{OUT}, I_{LOAD}	**96.1 @ 5 V, 3.3 V, 1 A**	94.9 @ 1.8 V, 1.5 V, 40 mA	95.6 @ 12 V, 5 V, 0.5 A	96 @ 5 V, 1 V, 150 mA	94 @ 5.5 V, 3 V, 150 mA
Heavy Load Power-Efficiency (%) @ V_{IN}, V_{OUT}, I_{LOAD}	**91.7 @ 5 V, 3.3 V, 3 A**	90 @ 1.8 V, 1.5 V, 0.3 A	89 @ 12 V, 5 V, 2 A	77 @ 5 V, 1 V, 2 A	78 @ 5.5 V, 3 V, 2 A
FoM – the higher the better (Step-up, Step-down)	**0.62, 1.62**	0.02, 0.06	0.44, 0.42	0.17, 0.134	0.10, 0.005

*The slew rate is estimated from measurement results provided in the article.

$$FoM = \frac{Peak\ Efficiency\ (\%) \times Load\ Step\ (A)}{Transient\ Response\ (\mu s) \times Switching\ Frequency\ (MHz) \times Overshoot\ or\ Undershoot\ (mV)}$$ [29]

TABLE II
PERFORMANCE COMPARISON TO STATE-OF-THE-ART BUCK CONVERTERS WITH COMPARABLE TRANSIENT RESPONSE

	This work	TPEL' 2020 [22]	TPEL' 2021 [18]	TPEL' 2023 [17]	JSSC' 2025 [30]
Maximum Load Current (A)	**3**	0.6	2	0.5	5
Switching Frequency (MHz)	**1.8–2.4**	1	2	1	2.5
Inductor (µH), Capacitor (µF)	**1, 22**	4.7, 10	2.2, 10	4.7, 4.7	0.88, 8
Load Step (A), Slew Rate (A/µs)	**0.1–2.8, 1**	0.1–0.5, 0.25*	0–2, 0.5*	0.05–0.5, 0.85*	2, 2000
Undershoot, Overshoot (mV)	**70, 40**	30, 60	72, 85	70, 80	70,128
Step-up and Step-down Transient Recovery Times (µs)	**3.0, 2.0**	2.6, 2.2	3.0, 2.7	1.6, 2.0	1.14, 2.0
Light Load Power-Efficiency (%) @ V_{IN}, V_{OUT}, I_{LOAD}	**90.6 @ 5 V, 3.3 V, 2 mA**	79 @ 3.3 V, 2.5 V, 0.1 A	82.6 @ 12 V, 5 V, 10 mA	75 @ 3.3 V, 2.5 V, 20 mA	N.A.**
Peak Power-Efficiency (%) @ V_{IN}, V_{OUT}, I_{LOAD}	**96.1 @ 5 V, 3.3 V, 1 A**	90 @ 3.3 V, 2.5 V, 0.3 A	95.6 @ 12 V, 5 V, 0.5 A	95 @ 3.3 V, 2.5 V, 0.4 A	95.8 @ 5 V, 2.5 V, 1 A
Heavy Load Power-Efficiency (%) @ V_{IN}, V_{OUT}, I_{LOAD}	**91.7 @ 5 V, 3.3 V, 3 A**	87.6 @ 3.3 V, 2.5 V, 0.5 A	89 @ 12 V, 5 V, 2 A	92 @ 3.3 V, 2.5 V, 0.5 A	89.8 @ 5 V, 2.5 V, 5 A
FoM – the higher the better (Step-up, Step-down)	**0.62, 1.62**	0.46, 0.27	0.44, 0.42	0.38, 0.27	0.95, 0.30

**The minimum load of the reported work is 200 mA which is not considered light load.

Of particular note, our design features the fastest transients despite the larger load step (i.e., 2.7 A) and a faster slew rate (i.e., 1 A/μs) than those of designs benchmarked in Table I, where in the latter, the load step is 26% lower, at 2 A. If our design were subjected to the same load step of 2 A, even faster transients are achieved—2.7 μs and 1.9 μs, respectively. This is equivalent to 10% and 30% faster than the best amongst the reported converters [18].

Second, our design features the highest power-efficiency in peak and heavy load power-efficiency—96.1% and 91.7%, respectively. This is equivalent to 0.1% and 1.9% higher than the best amongst the reported design [13], [16], [18], [28], respectively. The average power-efficiency (i.e., the mean value of light load, peak and heavy load power-efficiency) of our design is the also the highest—92.8%. This is equivalent to 1.3% higher than the best (91.6%) amongst the reported converters [13].

Of particular note, our proposed PoL stands out as it maintains a power-efficiency above 90% across the broadest load range (i.e., 2 mA–3 A), which is significantly wider than the state-of-the-art benchmarked designs [13], [16], [18], [28].

Third, our design features the highest figures-of-merit (FoM) compared to reported designs [13], [16], [18], [28]. These FoMs indicate that our design best balances high power-efficiency with fast transient response amongst these reported designs.

On the basis of Table II, we make the following comments. First, in part similar to the second comment on Table I, our design features the highest light load and peak power-efficiency compared to reported designs with comparable transient response [17], [18], [22], [30]. The heavy load power-efficiency of our design is high, albeit 0.3% lower than that of [17]. The average power-efficiency of our design is the highest—92.8%, equivalent to 4.3% higher than the best (89%) amongst the reported converters [18]. Further, similar to the second comment on Table I, our proposed PoL features high power-efficiency (>90%) across the broadest load range. Note that the >90% load range of our work is ×1500 (2 mA–3 A) vis-à-vis ×25 (200 mA–5 A) of [30].

Second, although [17], [22], [30] achieve either a shorter step-up or a shorter step-down transient recovery time, their light load power-efficiency is significantly compromised. Specifically, the light load power-efficiency of [17] and [22] is 17.2% and 12.8% lower, respectively, compared to our design. Although the power-efficiency of [30] is 91% at 200 mA, the power-efficiency is expected to drop significantly as the load current decreases.

This is because the quiescent current of [30] (i.e., 1.98 mA) is much larger compared to that of our work (i.e., 20 μA).

Third, our design features the highest average FoM. This indicates that our design best balances high power-efficiency with fast transient response amongst the reported designs [17], [18], [22], [30].

In summary, our design demonstrates significant advantages and is highly competitive, particularly in terms of achieving the best optimization in both power-efficiency and transient response.

VI. Conclusion

We have designed a PoL with our proposed DHC embodying the VMHC and the CMHC. The VMHC operated the PoL in DCM and CCM without a mode selection circuit to derive high power-efficiency. The CMHC combined conventional PCMC and VCMC to derive prolonged on-time and off-time extensions, enabling fast transients. On the basis of measurements on a monolithic prototype, the power-efficiency was >90% across the 2 mA–3 A load range with a peak-efficiency of 96.1% at $V_{\rm IN}$ = 5 V and $V_{\rm OUT}$ = 3.3 V. The voltage undershoot and overshoot were 70 mV and 40 mV with recovery times of 3 μs and 2 μs in response to 2.7 A step-up and step-down load current transients (1 A/μs slew-rate), respectively. Compared to state-of-the-art buck converters with similar power-efficiency, it featured faster transient response. Compared to state-of-the-art buck converters with comparable transient performance, it featured higher power-efficiency across most of the load range. In short, our proposed PoL optimizes both power-efficiency and transient response, features the best average FoM and is hence highly competitive.

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