A Grid-Connected AC–DC Converter With an Autonomous Internal Power Buffer

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***Abstract*—The active power buffer is a promising solution for mitigating power pulsations, owing to its advanced merits in implementing power buffering with high reliability and power density. However, conventional active power buffers typically require external buffering components and dedicated power buffering control loops, which limit system compactness and increase the complexity of controller design. To address these limitations, this article proposes a grid-connected ac–dc converter with an autonomous internal power buffer (AIPB), eliminating the need for both external buffering components and dedicated power buffering control loops. The concept, typical circuit configuration, power buffering mechanism, and control scheme of the proposed converter are provided. In the proposed converter, the AIPB shares the existing filter inductor and active switches of the grid-connected ac–dc converter, resulting in a compact circuit configuration. Besides, the power buffering function is autonomously achieved by fully utilizing the three-port essence of the proposed converter, resulting in a simplified controller design. Experimental validation under unbalanced grid conditions is presented to demonstrate the effectiveness of the proposed converter.**

***Index Terms*—Active power buffer, grid-connected ac–dc converter, power pulsations, unbalanced grid conditions.**

I. Introduction

MOTIVATED by the substantial potential of renewable energy sources to mitigate environmental pollution and reduce carbon emissions, an increasing number of renewable energy generation units and modern loads are being integrated into the ac grid through power electronic converters [1]. As the critical interface, grid-connected ac–dc converters play a vital role in transmitting high-quality power for power systems [2] and maintaining grid reliability [3], [4].

Grid-connected ac–dc converters are installed to maintain steady active power delivery to the dc side [5]. However, their operation is frequently disturbed by power pulsations arising from increasing penetration of renewable energy sources [6], grid faults [7], and unbalanced or nonlinear loads [8]. When these power pulsations propagate to the dc link, they can degrade dc voltage regulation performance [9] and, in severe cases, potentially damage power equipment [10]. In photovoltaic applications, such power pulsations deteriorate maximum power point tracking performance [11], while in onboard battery charging systems, they shorten the lifetime of the battery [12]. Therefore, suppressing dc-side power pulsations is essential for ensuring the reliable operation of grid-connected ac–dc converters.

The active power buffer is an attractive solution for suppressing dc-side power pulsations due to its advanced merits in implementing power buffering with high reliability [13] and power density [14]. Its basic principle is to divert power pulsations into long-lifetime energy storage components [15], such as film and ceramic capacitors, by adding external power buffering circuits or fully using the original switches and passive components of converters [16]. Generally, active power buffers are classified as either external or internal types, depending on whether component multiplexing is present.

External power buffers have been utilized in various applications to suppress dc-side power pulsations. In [17], an external power buffer is introduced to implement power pulsation suppression in three-phase systems operating under unbalanced grid conditions, where an ac-side controller is employed to mitigate grid current imbalance, and a dc-side controller is used to suppress power pulsations. Similar external power buffers presented in [18] and [19] can support dc-side power pulsation suppression while maintaining balanced voltage control. Furthermore, external power buffers have been extended to low-frequency pulsed load applications [20], [21], enabling efficient power buffering with reduced power conversion stages. Since these buffers are independent of the ac–dc conversion stage, their control design can be independently designed. Nevertheless, their reliance on external buffering components increases system volume and limits system compactness.

To reduce external component requirements and improve system compactness, internal power buffers that reuse existing

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switches and passive components are preferred. For example, the buffers proposed in [22] and [23] utilize existing switches or filter inductors to divert power pulsations into the film capacitors, with power regulation achieved through proportional–resonant (PR) controllers. Likewise, [24] demonstrates an internal power buffer that fully leverages existing switches, filter inductors, and flying capacitors. By designing a dedicated power control loop, flying capacitors can effectively absorb power pulsations without requiring external buffering components. Although these solutions reduce external component requirements by reusing existing components, the power buffer is coupled with the ac–dc power conversion stage, which increases the complexity of both control design and power flow analysis.

Given this, this article proposes a grid-connected ac–dc converter with an autonomous internal power buffer (AIPB), which achieves power buffering without the need for external buffering components or dedicated control loops. The typical topology, power buffering mechanism, and control scheme of the proposed converter are explained. In the proposed converter, the AIPB shares the existing filter inductor and active switches of the grid-connected ac–dc converter, resulting in a compact circuit configuration. Furthermore, the power buffering function is autonomously achieved by fully leveraging the three-port nature of the proposed converter, thereby simplifying the controller design.

II. Grid-Connected AC–DC Converter With an AIPB

In this Section, the typical circuit configuration of the grid-connected ac–dc converter with an AIPB is introduced first. Then, the autonomous power buffering mechanism of the proposed converter is explained.

A. Typical Circuit Configuration of Grid-Connected ac–dc Converter With an AIPB

Active power buffers typically rely on external buffering components and dedicated power buffering control loops, which reduce system compactness and increase controller design complexity. To overcome these challenges, this article proposes a multilevel converter–based circuit configuration that enables internal active power buffering by fully utilizing existing components, thereby improving system compactness. By leveraging the rich set of output voltage vectors inherent in multilevel converters, different components of active power can be actively regulated without requiring dedicated power buffering control loops, thereby simplifying controller design complexity.

The typical circuit structure of the grid-connected ac–dc converter with an AIPB is shown in Fig. 1(a). It can be seen that the proposed converter retains a similar circuit structure to the multilevel converter, but its internal power flow pathways are functionally reconfigured to enable internal power buffering. The dc link capacitors of the multilevel converter are split, where the upper capacitor is used to support the regulated dc load voltage, whereas the lower capacitor serves as a buffering capacitor that absorbs or releases power pulsations. Together with the shared inductors and switches, the multilevel converter is configured as a compact three-port network that connects

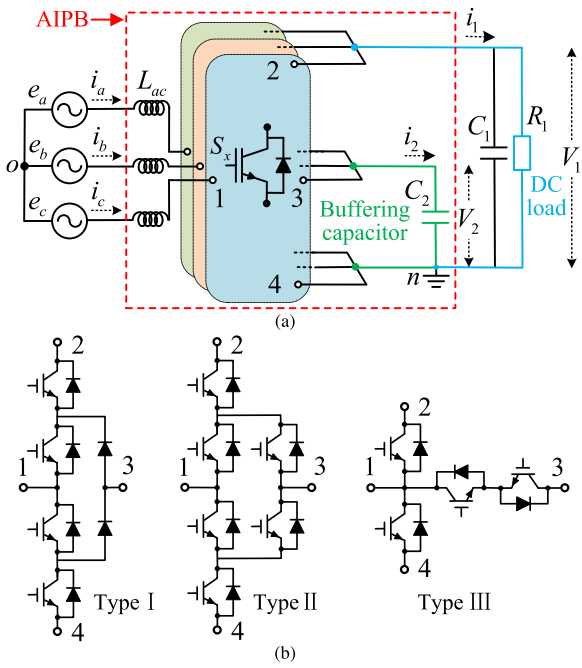

Fig. 1. Typical circuit configuration of grid-connected AC–DC converter with an AIPB. (a) Circuit structure. (b) Alternative circuit topologies.

the ac grid, the dc load, and the buffering capacitor through a single-stage power stage.

The key feature of the proposed converter is that the AIPB fully utilizes existing filter inductors L_{ac} and active switches S_x, where L_{ac} stores and releases active power, while S_x regulates the active power flow through the AIPB. By controlling the operating states of the active switches, the AIPB can buffer power pulsations, thereby stabilizing the dc load voltage. Since the power buffering function is seamlessly integrated into the proposed converter without requiring external buffering components, the compactness of the overall system is enhanced.

As shown in Fig. 1(a), the proposed converter includes two dc links, where one, with voltage V_1, is connected to the dc load R_1, and the other, with voltage V_2, is connected to the buffering capacitor C_2. Various types of circuit topologies can be selected for this converter, with several examples shown in Fig. 1(b). Among them, the neutral-point-clamped (NPC) type (i.e., Type I) is employed for further research because it has been widely investigated by researchers [25] and utilized in industrial applications [26].

B. Autonomous Power Buffering Mechanism

From the equivalent circuit shown in Fig. 2, the dynamic equation of the grid current can be derived and is expressed as

$$L_{\text{ac}}\frac{d\boldsymbol{i}_{\alpha\beta}}{dt} = \boldsymbol{e}_{\alpha\beta} - \boldsymbol{v}_{\text{ref}} \tag{1}$$

where $\boldsymbol{i}_{\alpha\beta} = i_\alpha + ji_\beta$ represents the grid current vector, $\boldsymbol{e}_{\alpha\beta} = e_\alpha + je_\beta$ represents the grid voltage vector, and $\boldsymbol{v}_{\text{ref}} = v_\alpha + jv_\beta$ denotes the reference voltage vector generated by the grid-connected ac–dc converter.

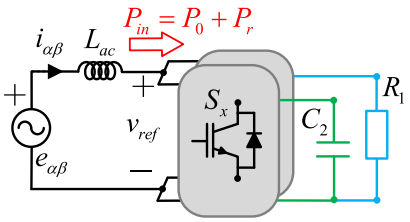

Fig. 2. Equivalent circuit of the proposed AC–DC converter.

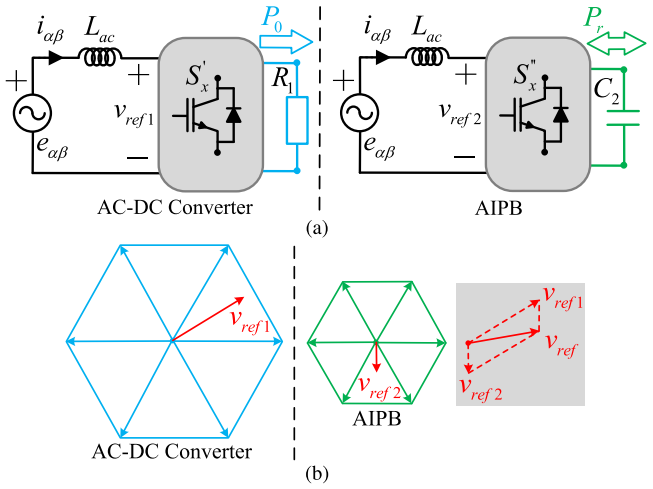

Fig. 3. Equivalent model of the proposed AC–DC converter. (a) Decomposition of the equivalent circuit. (b) Decomposition of the space vector diagram.

According to (1), grid current control is achieved once $\boldsymbol{v}_{\text{ref}}$ is determined. To facilitate the tracking of $\boldsymbol{v}_{\text{ref}}$ and decouple the power buffering stage from the ac–dc conversion stage, an equivalent two-level model [27] is adopted in this article. As illustrated in Fig. 3(a), this model decomposes the proposed converter into two independent converters, where one is responsible for power conversion between the ac grid and the dc load, referred to as the ac–dc converter, and the other performs power buffering, referred to as the AIPB. This equivalent model allows for the design of a modulation strategy within the two-level converter frame, where the reference voltage vector is decomposed into two parts generated by different converters, as illustrated in Fig. 3(b).

In the proposed converter, grid current control can be achieved by ensuring that $\boldsymbol{v}_{\text{ref}}$ equals the sum of the reference voltage vectors generated from the two decomposed converters. Thus, $\boldsymbol{v}_{\text{ref}}$ can be decomposed as

$$\boldsymbol{v}_{\text{ref}} = \boldsymbol{v}_{\text{ref1}} + \boldsymbol{v}_{\text{ref2}} \tag{2}$$

where $\boldsymbol{v}_{\text{ref1}}$ and $\boldsymbol{v}_{\text{ref2}}$ are reference voltage vectors generated from the decomposed ac–dc converter and AIPB, respectively.

Considering the power balance between the input and the output, the active power that AIPB should buffer can be expressed as

$$P_2 = P_{\text{out}} - P_1 = P_{\text{in}} - P_1 \tag{3}$$

$$\begin{cases} P_{\text{out}} = \frac{3}{2}\text{Re}(\overline{\boldsymbol{i}_{\alpha\beta}}\boldsymbol{v}_{\text{ref}}) \\ P_1 = \frac{3}{2}\text{Re}(\overline{\boldsymbol{i}_{\alpha\beta}}\boldsymbol{v}_{\text{ref1}}) \\ P_2 = \frac{3}{2}\text{Re}(\overline{\boldsymbol{i}_{\alpha\beta}}\boldsymbol{v}_{\text{ref2}}) \end{cases} \tag{4}$$

where P_{in} is instantaneous input active power, and P_{out} is instantaneous output active power. P_1 and P_2 are active power flowing through the decomposed ac–dc converter and AIPB, respectively. $\overline{\boldsymbol{i}_{\alpha\beta}}$ is the conjugate of $\boldsymbol{i}_{\alpha\beta}$.

From the perspective of output voltage vectors, the active power delivered to the proposed ac–dc converter and its decomposed converters can be controlled by regulating their respective reference voltage vectors. Once two out of the three reference voltage vectors are determined, the remaining vector can be calculated based on the vector operation principle. According to (3) and (4), when $\boldsymbol{v}_{\text{ref}}$ and $\boldsymbol{v}_{\text{ref1}}$ are tracked, P_2 will be autonomously controlled. From the circuit network perspective, the proposed converter is essentially a three-port circuit network, where the active power of two ports should be controlled, and the rest is controlled autonomously by following the power balance restriction. According to (3), active power buffering can be implemented by regulating P_{in} on the ac side and P_1 on the dc side. When the required active power component is injected into the decomposed ac–dc converter, power pulsations will be autonomously transferred to the AIPB. This solution requires no additional power buffering controllers and is, therefore, referred to as autonomous power buffering.

III. Control Scheme of the Proposed AC–DC Converter

The effectiveness of the proposed converter is verified under the unbalanced grid voltage application. First, the power buffering analysis for the AIPB is discussed under unbalanced grid conditions. Then, the control scheme, which consists of balanced current control on the ac side and active power regulation on the dc side, is presented. Its overall control scheme is depicted in Fig. 4. Finally, the active power regulation range of the proposed converter is discussed.

A. Power Buffering Analysis of the AIPB Under Unbalanced Grid Conditions

Under unbalanced grid conditions, the instantaneous input active power P_{in} can be calculated as [28], [29]

$$P_{\text{in}} = P_0 + P_r \tag{5}$$

$$\begin{cases} P_0 = \frac{3}{2}(e_\alpha^+ i_\alpha^+ + e_\beta^+ i_\beta^+ + e_\alpha^- i_\alpha^- + e_\beta^- i_\beta^-) \\ P_r = \frac{3}{2}(e_\alpha^- i_\alpha^+ + e_\beta^- i_\beta^+ + e_\alpha^+ i_\alpha^- + e_\beta^+ i_\beta^-) \end{cases} \tag{6}$$

where P_0 and P_r denote, respectively, the dc component and power pulsations of P_{in}. e_α^+, e_β^+, e_α^-, and e_β^- are the positive- and negative-sequence components of grid voltage vector $\boldsymbol{e}_{\alpha\beta}$, respectively. i_α^+, i_β^+, i_α^-, and i_β^- are the positive- and negative-sequence components of grid current vector $\boldsymbol{i}_{\alpha\beta}$, respectively.

According to (6), the cross-coupling between positive- and negative-sequence components of $\boldsymbol{e}_{\alpha\beta}$ and $\boldsymbol{i}_{\alpha\beta}$ generates power pulsations P_r.

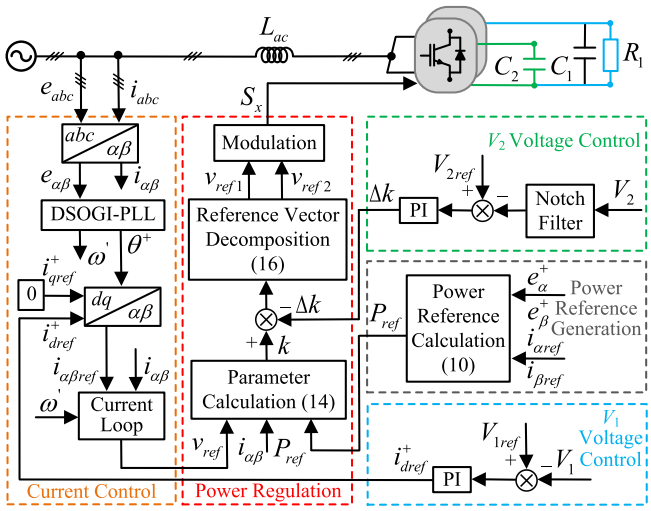

Fig. 4. Overall control scheme for the proposed AC–DC converter.

When P_r propagates to the dc side of the proposed converter, the control performance of the dc output voltage will be degraded. To mitigate this issue, P_r should be buffered by the AIPB. Assuming that P_r is purely sinusoidal and free of harmonics, P_r can be rewritten as

$$P_r = P_m \sin 2\omega_g t \tag{7}$$

where P_m is the magnitude of P_r, and ω_g is the angular frequency of the ac grid.

When P_2 equals P_r, active power buffering can be successfully implemented. Consequently, the differential equation describing the dynamics of the buffering capacitor voltage V_2 is given by

$$P_2 = \frac{C_2}{2}\frac{dV_2{}^2}{dt} = P_r = P_m \sin 2\omega_g t. \tag{8}$$

By solving the differential equation (8), the capacitor voltage V_2 can be derived as [30]

$$V_2 = \sqrt{V_{2\max}^2 - \frac{P_m}{C_2\omega_g}(1+\cos 2\omega_g t)} \tag{9}$$

where $V_{2\max}$ is the maximum of V_2.

To achieve power buffering, an open-loop method, proposed in [17], regulates the buffering capacitor voltage to match the right-hand side of (9). Alternatively, a closed-loop method [22], [23], [24], which regulates dc-side voltage ripples to zero, can also serve as a feasible solution. However, both methods require dedicated power buffering control loops, which complicate controller design. To avoid the complicated buffering controller design, the autonomous power buffering explained in Section II-B is utilized for the proposed converter under unbalanced grid conditions. The mechanism of the autonomous power buffering is illustrated in Fig. 5, where P_{in} is determined by balanced current control, and P_1 is determined by active power regulation. With autonomous power buffering, the power difference between the ac grid and the dc load can be autonomously transferred to the AIPB.

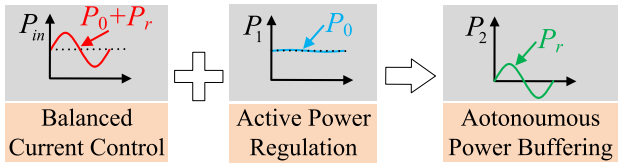

Fig. 5. Autonomous power buffering mechanism of the proposed AC–DC converter.

B. Balanced Current Control on the ac Side

To improve ac-side power quality and alleviate overcurrent issues under unbalanced grid conditions [17], [24], the current control loop is designed to eliminate the negative-sequence current component and ensure balanced grid current injection. This control objective is accomplished by regulating the grid current to track a reference that follows the positive sequence of the grid voltage.

In the current control loop, the positive-sequence phase angle θ^+ and the grid angular frequency ω', both estimated by the dual second-order generalized integrator frequency-locked loop (DSOGI-FLL) [31], serve as adaptive parameters to achieve robust synchronization with the grid voltage. The direct-axis current reference i^+_{dref} is generated by V_1 voltage control loop, while the quadrature-axis current reference i^+_{qref} is set to zero to ensure a high power factor. Subsequently, these current references in the dq frame are transformed to the stationary $\alpha\beta$ frame via an inverse Park transformation. Since the resulting current reference $\boldsymbol{i}_{\alpha\beta\text{ref}}$ contains only the positive-sequence component, regulating the grid current $\boldsymbol{i}_{\alpha\beta}$ to track $\boldsymbol{i}_{\alpha\beta\text{ref}}$ will effectively eliminate negative-sequence current components [32]. With balanced current control implemented, the active power reference required for power buffering can be calculated based on (6), as given by

$$P_{\text{ref}} = P_0 = \frac{3}{2}(e^+_\alpha i_{\alpha\text{ref}} + e^+_\beta i_{\beta\text{ref}}) \tag{10}$$

where e^+_α and e^+_β are extracted via the DSOGI-FLL. The terms $i_{\alpha\text{ref}}$ and $i_{\beta\text{ref}}$ denote the α and β components of the reference current vector $\boldsymbol{i}_{\alpha\beta\text{ref}}$, respectively.

When balanced current control is achieved on the ac side, the power pulsations can be rewritten from (6), which yields

$$P_r = \frac{3}{2}(e^-_\alpha i^+_\alpha + e^-_\beta i^+_\beta) = \frac{3}{2}(e^-_\alpha i_{\alpha\text{ref}} + e^-_\beta i_{\beta\text{ref}}). \tag{11}$$

As indicated in (11), the power pulsations under balanced current control originate from the interaction between the positive-sequence current and the negative-sequence voltage. To ensure the reliable operation of grid-connected ac–dc converters, these pulsations should be buffered by the AIPB.

C. Active Power Regulation on the DC Side

The control objective of the power control loop is to inject the dc component P_0 into the decomposed ac–dc converter. This objective is achieved by regulating active power P_1 to track the power reference P_{ref}.

By combining (1) and (4), it can be seen that grid current control and power control are closely related to $\boldsymbol{v}_{\text{ref}}$. To decouple

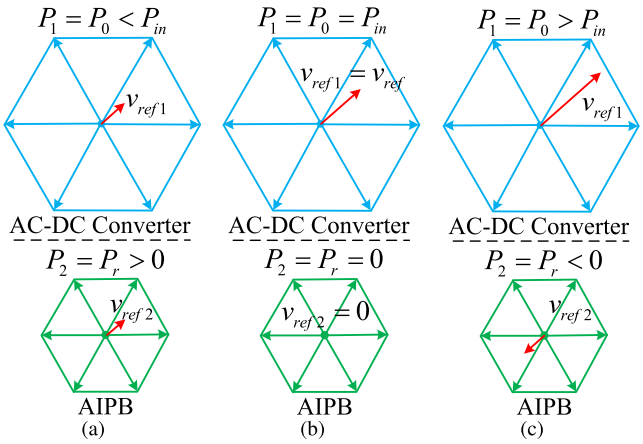

Fig. 6. Different operation modes for the proposed AC–DC converter. (a) Case I: $k < 1$. (b) Case II: $k = 1$. (c) Case III: $k > 1$.

the control design, a proportion parameter k is introduced, which is used to proportionally decompose $\boldsymbol{v}_{\text{ref}}$. Then, $\boldsymbol{v}_{\text{ref1}}$ is calculated by

$$\boldsymbol{v}_{\text{ref1}} = k\boldsymbol{v}_{\text{ref}}. \tag{12}$$

Since the decomposed ac–dc converter shares the same current vector $\boldsymbol{i}_{\alpha\beta}$ as the proposed ac–dc converter, the active power P_1 delivered to the decomposed ac–dc converter can be expressed as

$$P_1 = \frac{3}{2}k\text{Re}(\overline{\boldsymbol{i}_{\alpha\beta}}\boldsymbol{v}_{\text{ref}}) = kP_{\text{out}}. \tag{13}$$

From (13), the active power P_1 can be regulated by adjusting the proportion parameter k. Once P_1 tracks the dc component P_0, the autonomous power buffering can be implemented. Thus, k can be calculated as follows:

$$k = \frac{P_0}{P_{\text{out}}} = \frac{P_{\text{ref}}}{P_{\text{out}}} = \frac{2P_{\text{ref}}}{3\text{Re}(\overline{\boldsymbol{i}_{\alpha\beta}}\boldsymbol{v}_{\text{ref}})}. \tag{14}$$

Considering the power balance between the input and the output, k can be rewritten as

$$k = \frac{P_0}{P_{\text{in}}} = \frac{P_0}{P_0 + P_r}. \tag{15}$$

According to (15), different operation cases for the developed ac–dc converter can be obtained, which are described in Fig. 6. When $k < 1$, active power injected into the decomposed ac–dc converter will be lower than input active power P_{in}, and $\boldsymbol{v}_{\text{ref1}}$ is in phase with $\boldsymbol{v}_{\text{ref2}}$. When $k = 1$, all active power is injected into the decomposed ac–dc converter, and $\boldsymbol{v}_{\text{ref1}}$ is equal to $\boldsymbol{v}_{\text{ref}}$. When $k > 1$, active power injected into the decomposed ac–dc converter will be larger than P_{in}, and $\boldsymbol{v}_{\text{ref1}}$ is opposite in phase to $\boldsymbol{v}_{\text{ref2}}$. By regulating the proportion k, P_1 for the decomposed ac–dc converter can remain constant as required, and P_2 for the AIPB can track power pulsations P_r.

Due to the presence of P_r, V_2 exhibits pronounced pulsations at double or higher-order grid frequencies. A notch filter [33] with stopbands at these frequencies is therefore incorporated into V_2 control loop, alongside a PI controller to regulate the

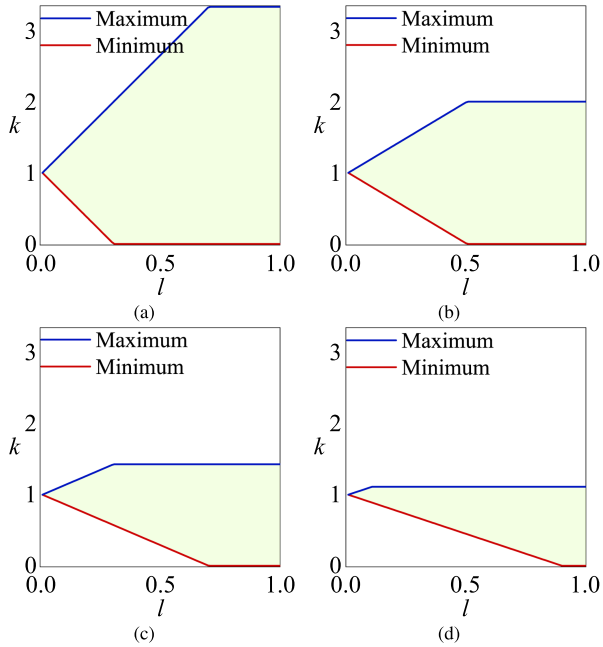

Fig. 7. Controllable range of k under different l. (a) $m = 0.3$. (b) $m = 0.5$. (c) $m = 0.7$. (c) $m = 0.9$.

average value of V_2. The output of the PI controller is used to modify parameter k, and the resulting value is then applied to decompose $\boldsymbol{v}_{\text{ref}}$. Therefore, the decomposed reference voltage vectors for the two decomposed converters are given by

$$\begin{cases} \boldsymbol{v}_{\text{ref1}} = (k - \Delta k)\boldsymbol{v}_{\text{ref}} \\ \boldsymbol{v}_{\text{ref2}} = (1 - k + \Delta k)\boldsymbol{v}_{\text{ref}}. \end{cases} \tag{16}$$

Then, $\boldsymbol{v}_{\text{ref1}}$ and $\boldsymbol{v}_{\text{ref2}}$ are directly fed into the modulation stages of the decomposed ac–dc converter and AIPB, respectively, for duty cycle calculation, as detailed in [27].

D. Active Power Regulation Range Analysis

Since the active power regulation range of the proposed converter depends on the decomposed voltage vectors, it is necessary to discuss the range of proportion k. In the linear modulation range, reference voltage vectors generated by decomposed converters should satisfy the following limitations:

$$\begin{cases} 0 \le |\boldsymbol{v}_{\text{ref1}}| = |k\boldsymbol{v}_{\text{ref}}| \le \frac{V_1}{\sqrt{3}} \\ 0 \le |\boldsymbol{v}_{\text{ref2}}| = |(1-k)\boldsymbol{v}_{\text{ref}}| \le \frac{V_2}{\sqrt{3}}. \end{cases} \tag{17}$$

According to (17), the controllable range of k can be solved by

$$A = \left\{ k \mid \max\left(0, \frac{m-l}{m}\right) \le k \le \min\left(\frac{1}{m}, \frac{m+l}{m}\right) \right\} \tag{18}$$

where l ($l = V_2/V_1$) represents the ratio of the voltage across the buffering capacitor to the voltage across the dc load, and m ($m = \sqrt{3}|\boldsymbol{v}_{\text{ref}}|/V_1$) represents the modulation index.

Fig. 7 illustrates the controllable range of k for different values of l when $m = 0.3$, 0.5, 0.7, and 0.9, respectively. It is evident that the range A expands as m decreases or l increases. Hence,

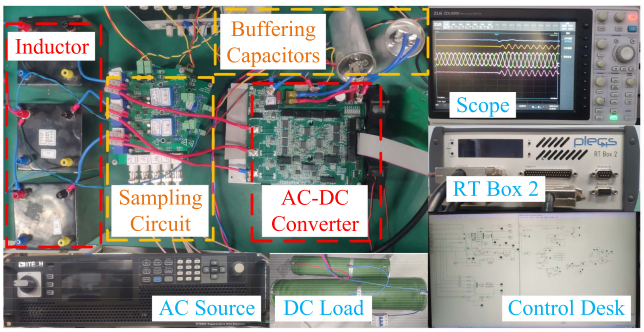

Fig. 8. Experimental prototype of the proposed AC–DC converter.

TABLE I
EXPERIMENTAL PARAMETERS

Parameters	Value	Parameters	Value
Grid voltage (RMS)	55 V	DC load voltage	200 V
Grid frequency	50 Hz	Switching frequency	10 kHz
DC load resistance	80 Ω	Filter inductance	5 mH
Buffering capacitor	120 μF	DC bus capacitor	150 μF

decreasing m or increasing l provides a viable option to broaden the active power regulation range of the proposed converter.

By combining (7) and (15), the desired range of k can be expressed as

$$B = \left\{ k \,|\, \frac{P_0}{P_0 + P_m} \le k \le \frac{P_0}{P_0 - P_m} \right\}. \tag{19}$$

When $B \subseteq A$, the active power P_1 can successfully track P_0 in every control period, thereby ensuring the desired power buffering. Based on (18) and (19), the following two constraints should be satisfied:

$$\begin{cases} \max\left(0, \frac{m-l}{m}\right) \le \frac{P_0}{P_0+P_m} \\ \frac{P_0}{P_0-P_m} \le \min\left(\frac{1}{m}, \frac{m+l}{m}\right). \end{cases} \tag{20}$$

According to (20), the maximum permissible power pulsation magnitude $P_{\max}$ can be calculated as

$$P_{\max} = \begin{cases} \frac{lP_0}{m+l}, & m < 1-l \\ (1-m)\,P_0, & 1-l \le m \le l \\ \min\left(1-m, \frac{l}{m-l}\right) P_0, & m > l \text{ and } m \ge 1-l. \end{cases} \tag{21}$$

As long as the magnitude P_m remains below $P_{\max}$, the power pulsations can be effectively buffered.

IV. EXPERIMENTAL VERIFICATION UNDER UNBALANCED GRID VOLTAGE APPLICATIONS

To verify the effectiveness of the proposed converter, an experimental prototype, as shown in Fig. 8, is built. The specifications of the experimental prototype are summarized in Table I, where the film capacitor, known for its tolerance to large voltage variations and long lifespan [34], is employed as the buffering capacitor C_2. The control algorithm is executed by the PLECS RT Box 2. Since the focus of this article is power control rather than voltage control, the voltage reference $V_{2\text{ref}}$ is set as half of the voltage reference $V_{1\text{ref}}$. During experimental tests, power

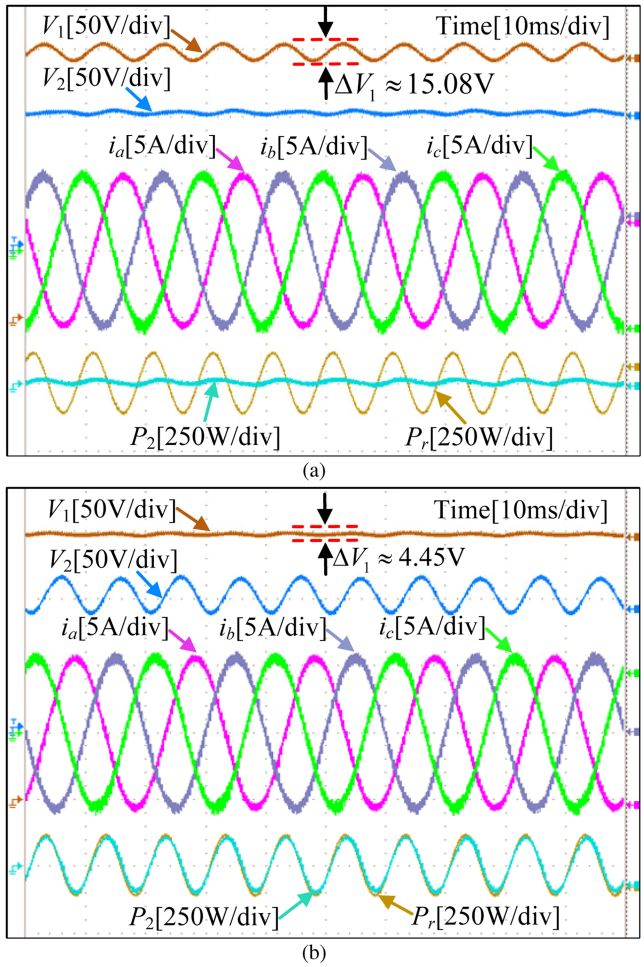

Fig. 9. Experimental results of the proposed converter under a 50% voltage dip in phase a. From top to bottom: DC load voltage V_1, buffering capacitor voltage V_2, three-phase grid currents i_{abc}, buffered active power P_2, and power pulsations P_r. (a) Disabling active power buffering. (b) Enabling active power buffering.

pulsations arise from the unbalanced grid voltage condition, which is achieved by configuring voltage dips or angle shifts in the output channels of the programmable ac source (IT7900).

A. Performance Evaluation of Power Buffering

To verify the power buffering performance of the proposed converter, steady-state experiments are conducted first by disabling and then enabling active power buffering under a 50% voltage dip in phase a. The test results are shown in Fig. 9, where active power buffering is disabled by setting the proportion parameter k equal to 1. It can be seen that balanced grid currents are obtained in both test results, indicating the effectiveness of balanced current control. However, in the absence of active power buffering, substantial voltage pulsations ($\Delta V_1 \approx$ 15.08V) appear in the dc load voltage V_1, as shown in Fig. 9(a). Conversely, upon activation of active power buffering, voltage pulsations in V_1 are reduced to 4.45V, as shown in Fig. 9(b). This reduction is achieved because the AIPB successfully buffers the power pulsations P_r induced by the unbalanced grid voltage. During the buffering process, the buffering capacitor voltage V_2

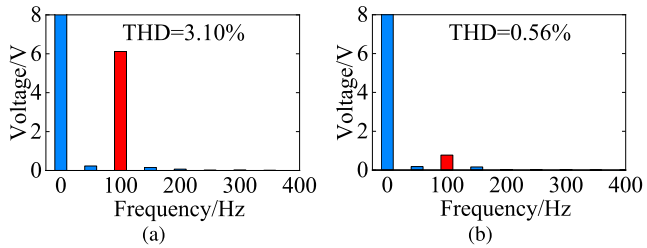

Fig. 10. FFT analysis of DC load voltage V_1 a 50% voltage dip in phase a. (a) Disabling active power buffering. (b) Enabling active power buffering.

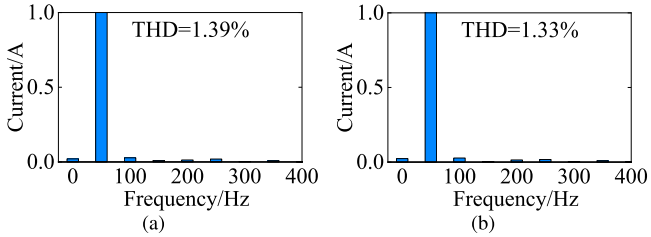

Fig. 11. FFT analysis of phase-a current under a 50% voltage dip in phase a. (a) Disabling active power buffering. (b) Enabling active power buffering.

pulsates at twice the grid frequency, enabling the capacitor to dynamically compensate for the power imbalance between the instantaneous input power and the desired output power, thereby stabilizing V_1. These results verify that the proposed converter can effectively perform active power buffering while achieving balanced grid current injection.

To further evaluate the power buffering performance of the proposed converter, the Fast Fourier Transformation (FFT) analysis of the dc load voltage is conducted, and the results are presented in Fig. 10. As shown, the second-order harmonic component is significantly reduced from 6.12 to 0.77 V after enabling active power buffering, and the total harmonic distortion (THD) of the dc load voltage decreases from 3.10% to 0.56%. In addition, FFT analysis of the phase-a grid current is conducted and presented in Fig. 11. The analysis reveals that the grid current THD remains low in both cases, measured at 1.39% without active power buffering and 1.33% with buffering enabled. These results confirm that the proposed converter can implement effective power buffering while injecting low-harmonic grid currents.

To further evaluate the buffering capability of the proposed converter under diverse unbalanced grid conditions, its steady-state performance is examined in two representative scenarios, including a two-phase voltage dip and an angle shift with a one-phase voltage dip. Fig. 12(a) shows the performance during a two-phase voltage dip, where the power pulsation magnitude remains below the permissible value. As a result, effective power buffering is achieved, and the dc load voltage fluctuation is constrained to 4.17 V. Under angle shift and single-phase voltage dip conditions, as depicted in Fig. 12(b), the dc load voltage also remains well regulated, with a pulsation amplitude of only 4.05 V. These experimental results validate that the proposed ac–dc converter achieves flexible operation under diverse unbalanced grid conditions.

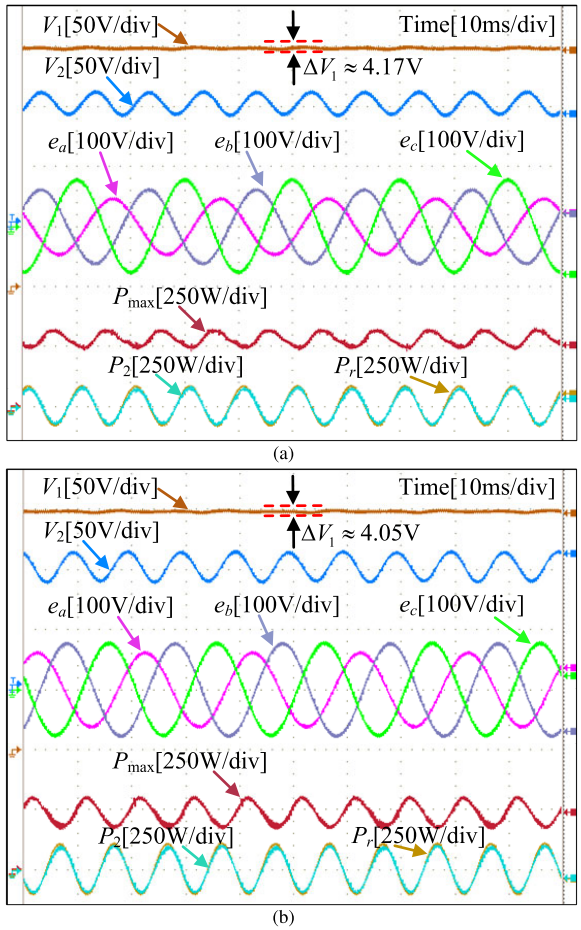

Fig. 12. Steady-state experimental results for the proposed AC-DC converter under various unbalanced grid conditions. From top to bottom: DC load voltage V_1, buffering capacitor voltage V_2, three-phase grid voltages, maximum permissible power pulsation magnitude $P_{\max}$, buffered active power P_2, and power pulsations P_r. (a) Unbalanced grid condition I: two-phase voltage dip ($e_a = 33\angle 0°, e_b = 44\angle -120°, e_c = 55\angle 120°$). (b) Unbalanced grid condition II: angle shift and one-phase voltage dip ($e_a = 33\angle 0°, e_b = 55\angle -100°, e_c = 55\angle 120°$).

B. Experimental Validation of Autonomous Buffering Capability

To verify the autonomous power buffering capability of the proposed converter, a comparative experimental evaluation is conducted under a 50% voltage dip in phase a. As shown in Figs. 13 and 14, the performance of the conventional PR-controller-based power buffering scheme [22], [23], [24] is compared with that of the autonomous power buffering scheme.

As shown in Fig. 13(b) and Fig. 14(b), at the nominal grid frequency $\omega_g = 314$ rad/s, both schemes successfully regulate the active power P_2 to track pulsations injected into input active power P_{in}, thereby maintaining a stable dc load voltage. However, when the grid frequency deviates from its nominal value, the PR-controller-based power buffering scheme suffers from degraded buffering performance, with P_2 failing to accurately track power pulsations, causing noticeable voltage pulsations on the dc load. This degradation is mainly attributed to the frequency sensitivity of the PR controller, which is tuned for

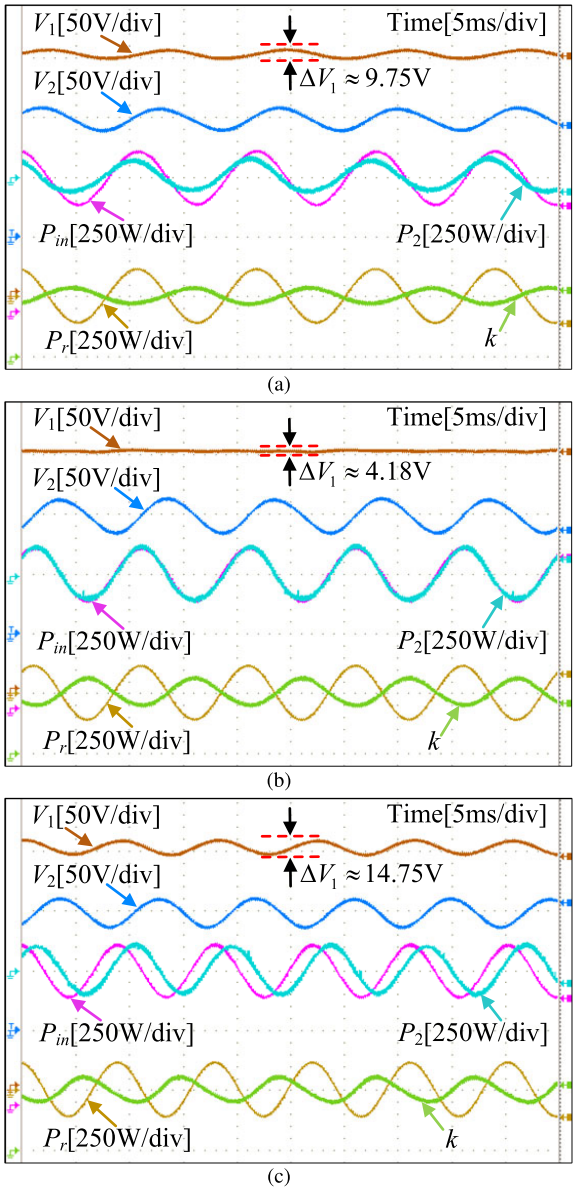

Fig. 13. Steady-State experimental results of the proposed converter with PR-controller-based power buffering scheme under a 50% voltage dip in phase a. Waveforms from top to bottom are DC load voltage V_1, buffering capacitor voltage V_2, input active power P_{in}, buffered active power P_2, power pulsations P_r, and proportion parameter k. (a) ω_g =283 rd/s. (b) ω_g =314 rd/s. (c) ω_g =346 rd/s.

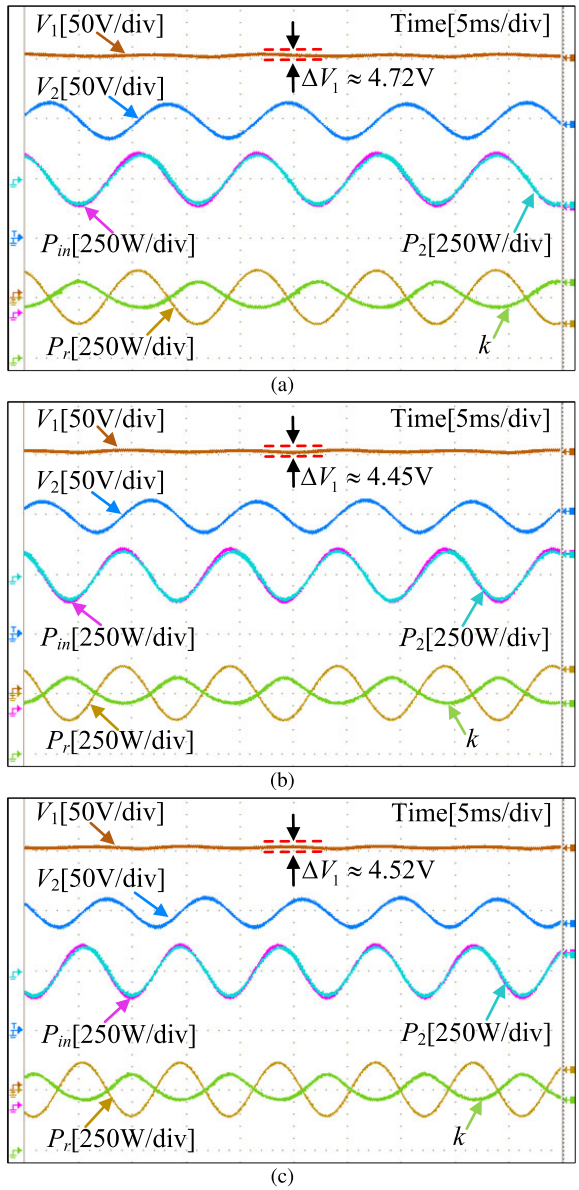

Fig. 14. Experimental results of the proposed converter with the autonomous power buffering scheme under a 50% voltage dip in phase a. Waveforms from top to bottom are DC load voltage V_1, buffering capacitor voltage V_2, input active power P_{in}, buffered active power P_2, power pulsations P_r, and proportion parameter k. (a) ω_g =283 rd/s. (b) ω_g =314 rd/s. (c) ω_g =346 rd/s.

nominal grid frequency and lacks robustness to frequency variations. In contrast, the autonomous power buffering scheme achieves power buffering through simple proportion parameter regulation without relying on the resonant gain at a fixed frequency, thereby exhibiting enhanced robustness to grid frequency deviations. By dynamically adjusting the proportion parameter k, the voltage across the AIPB pulsates adaptively at double-line frequency, indicating that the AIPB autonomously buffers the power imbalance between the input and output of the proposed converter. The above experimental results demonstrate that the proposed converter features autonomous power buffering capability with stable performance across various grid frequencies, without the need for dedicated or frequency-tuned control loops.

C. Dynamic-State Performance

To verify the stability of the proposed converter under varying grid voltage conditions, a step transition from a balanced to an unbalanced grid condition, caused by a 50% voltage dip in phase a, is applied. As shown in Fig. 15(a), both the V_1 and V_2 remain stable under the balanced grid condition. Upon the injection of power pulsations under the unbalanced grid condition, V_2 begins to oscillate at twice the grid frequency, indicating that the AIPB successfully absorbs the power pulsations. Throughout

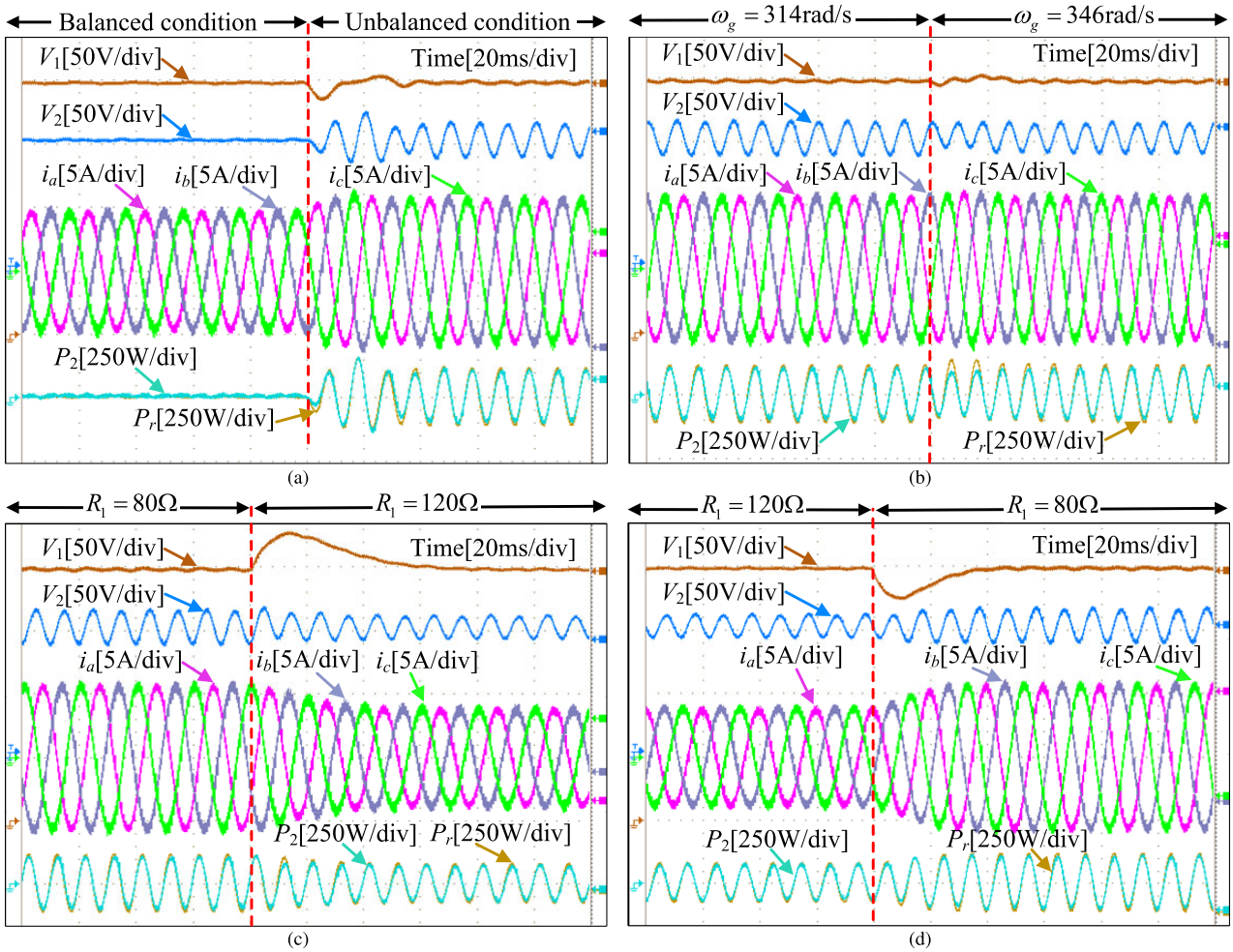

Fig. 15. Dynamic-State experimental results of the proposed converter. Waveforms from top to bottom are DC load voltage V_1, buffering capacitor voltage V_2, three-phase grid currents i_{abc}, buffered active power P_2, and power pulsations P_r. (a) Response to a step transition from a balanced to an unbalanced grid condition caused by a 50% voltage dip in phase a. (b) Response to a step variation in grid angular frequency under a 50% voltage dip in phase a. (c) Response to a sudden load increase under a 50% voltage dip in phase a. (d) Response to a sudden load decrease under a 50% voltage dip in phase a.

the steady-state process, the grid currents remain balanced and sinusoidal due to the applied balanced current control, and V_1 continues to exhibit stable regulation. These results demonstrate that the proposed converter effectively buffers dc-side power pulsations and maintains stable operation even under grid voltage imbalance.

To verify the stability of the proposed converter under grid frequency deviations, a step change in the grid angular frequency is applied during a 50% voltage dip in phase a. As depicted in Fig. 15(b), when the grid angular frequency experiences a step change from 314 rd/s to 346 rd/s, the pulsation frequency of the injected power component P_r increases accordingly. The active power P_2 promptly adapts to frequency variations, automatically synchronizing with the updated pulsation frequency while continuously compensating for low-frequency power imbalances. These experimental results validate that the proposed converter maintains stable operation despite grid frequency deviations and confirm that the AIPB provides robust power buffering performance under dynamic conditions.

To verify the stability of the proposed converter under dc load fluctuations, a step change in the dc load resistance is applied during a 50% voltage dip in phase a. As shown in Fig. 15(c) and (d), the system experiences abrupt load variations, including both load increases and decreases. The active power P_2 adaptively tracks the varying power demand, ensuring uninterrupted regulation of the dc load voltage. These results demonstrate that the proposed converter can maintain voltage stability and provide reliable power buffering under sudden load disturbances.

To further evaluate the power buffering flexibility of the ac–dc converter, the dynamic response to a sudden step change in the buffering capacitor voltage reference $V_{2\text{ref}}$ is investigated under a deep grid voltage dip, with an 80% voltage drop in phase a, as shown in Fig. 16. When $V_{2\text{ref}}$ is set to 60 V, the power pulsation magnitude surpasses the permissible limit during several control cycles. Fortunately, increasing the voltage ratio provides a straightforward means to enhance the buffering capability. As illustrated in Fig. 16, doubling $V_{2\text{ref}}$ increases both the average voltage ratio and average value of $P_{\max}$, ensuring that the power pulsation magnitude remains within the allowable range. These experimental results are in good agreement with the analysis in Section III-D, thereby confirming that the power buffering

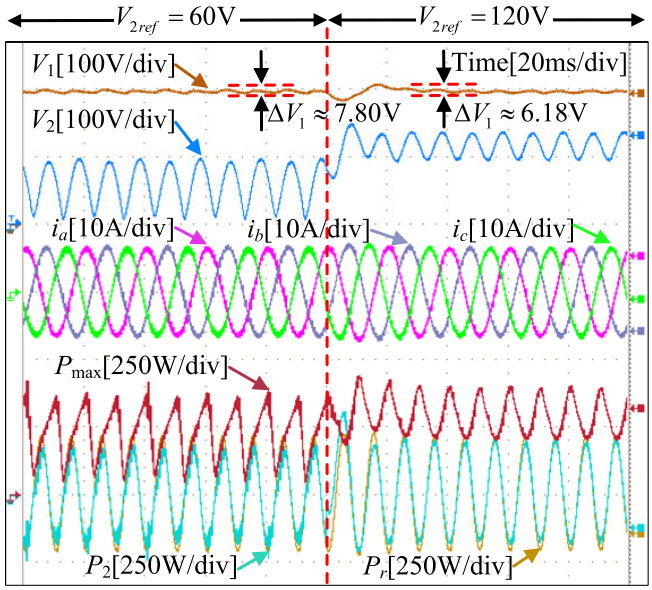

Fig. 16. Dynamic response to a sudden change in the buffering capacitor voltage reference $V_{2\text{ref}}$ from 60 to 120V under an 80% single-phase voltage dip in phase a. From top to bottom: DC load voltage V_1, buffering capacitor voltage V_2, three-phase grid currents, maximum permissible power pulsation magnitude $P_{\max}$, buffered active power P_2, and power pulsations P_r.

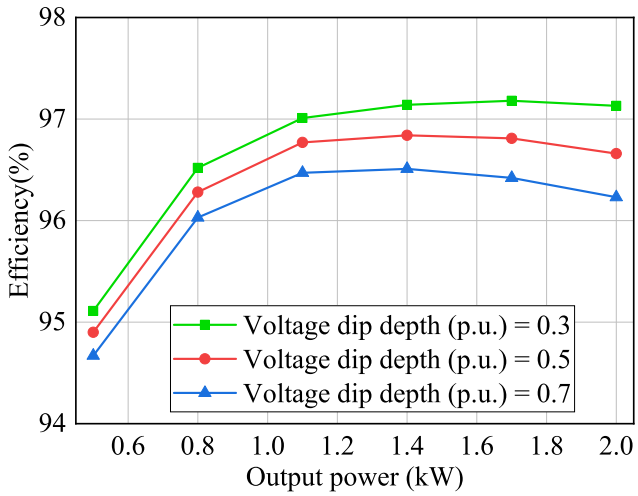

Fig. 17. Measured efficiencies of the proposed AC–DC converter under different output power and different voltage dip depth.

capability of the AIPB can be flexibly enhanced by increasing the average voltage ratio.

D. Efficiency Evaluation of the Proposed Converter

The measured efficiency curves under various output power levels and voltage dip depths are presented in Fig. 17. It can be observed that the efficiency progressively decreases as the dip depth increases, primarily due to aggravated power pulsations. These pulsations impose elevated voltage and current stresses on the converter, thereby increasing conduction and switching losses in the semiconductor devices as well as equivalent series resistance (ESR) losses in the buffering capacitor and filter inductors. To alleviate these adverse effects, efficiency can be improved by employing advanced semiconductor devices such as GaN MOSFETS, adopting low-loss modulation strategies like discontinuous pulsewidth modulation, and optimizing component design.

V. Conclusion

Active power buffering has become an essential function in modern power electronic systems, enabling the suppression of low-frequency power pulsations and ensuring stable dc-link voltage regulation. This article proposes a grid-connected ac–dc converter with an AIPB, which enables effective power pulsation suppression without relying on external buffering components or complex power buffering control. The AIPB shares the existing filter inductor and active switches of the grid-connected ac–dc converter, resulting in a compact and hardware-efficient implementation. In addition, its power buffering function is self-regulated by leveraging the three-port nature of the proposed converter, thereby eliminating the need for frequency-sensitive controllers and enhancing robustness against grid frequency variations. Experimental validation under unbalanced grid voltage conditions demonstrates the capability of the proposed converter to suppress dc-side power pulsations and maintain stable operation. Owing to its straightforward implementation, the converter can be readily extended to other power buffering scenarios.

Future research will focus on extending the autonomous buffering concept to other multilevel converter architectures and exploring its applicability to two-level systems. Moreover, comprehensive investigations into soft switching and fault-tolerant control will be conducted to further improve efficiency and ensure long-term reliability.

Appendix A

The main focus of the AIPB is on active power regulation. For completeness, the design of V_2 control loop and the considerations for the buffering capacitor C_2 are presented in the Appendix to support the implementation of the AIPB. In addition, the computational complexity associated with the proportional parameter k is also discussed.

A. Design of V_2 Control Loop

Combining (4), (8), (14), and (16), dynamic behavior of the buffering capacitor voltage V_2 can be described by

$$\frac{C_2}{2}\frac{dV_2^2}{dt} = (1+\Delta k)P_{\text{out}} - P_0 \tag{22}$$

where the right-hand side of (22) represents the instantaneous power flowing into AIPB.

Assuming that Δk varies slowly compared to output power P_{out}, the averaged dynamics are given by

$$\frac{C_2}{2}\frac{d\langle V_2^2\rangle}{dt} = (1+\Delta k)\langle P_{\text{out}}\rangle - \langle P_0\rangle. \tag{23}$$

Noting that $\langle P_{\text{out}} \rangle = P_0$ and $\langle P_0 \rangle = P_0$, the average dynamic of V_2 can be simplified as

$$\frac{C_2}{2}\frac{d\overline{V}_2^2}{dt} = \Delta k P_0 \tag{24}$$

where $\overline{V}_2$, obtained via a notch filter, is the average value of V_2.

To analyze the average dynamic behavior under small disturbances, the system variables in (24) are expressed as the sum of their equilibrium values and small perturbations

$$\overline{V}_2 = V_{2,\text{eq}} + \widetilde{\overline{V}}_2 \tag{25}$$

$$\Delta k = 0 + \widetilde{\Delta k}. \tag{26}$$

Substituting (25) and (26) into (24), the linearized small-signal model of the V_2 voltage control loop is approximated as follows:

$$C_2 V_{2,\text{eq}} \frac{d\widetilde{\overline{V}}_2}{dt} \approx P_0 \widetilde{\Delta k}. \tag{27}$$

Equation (27) reveals that the average value of V_2 is regulated by adjusting Δk. Since V_2 voltage control loop generates the bias term Δk to achieve voltage regulation of the AIPB, its output dynamics can be approximated as follows:

$$\widetilde{\Delta k} \approx -\left(K_P + \frac{K_I}{s}\right)\widetilde{\overline{V}}_2. \tag{28}$$

Substituting (28) into the plant model (27) in the Laplace domain yields

$$C_2 V_{2,\text{eq}} s \widetilde{\overline{V}}_2 = -P_0\left(K_P + \frac{K_I}{s}\right)\widetilde{\overline{V}}_2. \tag{29}$$

Dividing both sides of (29) by $\widetilde{\overline{V}}_2$ gives the characteristic equation:

$$s^2 + \frac{P_0 K_P}{C_2 V_{2,\text{eq}}} s + \frac{P_0 K_I}{C_2 V_{2,\text{eq}}} = 0. \tag{30}$$

Equation (30) corresponds to a canonical second-order system, whose natural frequency ω_n and damping ratio ζ are defined as

$$\begin{cases} \omega_n = \sqrt{\frac{P_0 K_I}{C_2 V_{2,\text{eq}}}} \\ \zeta = \frac{K_P}{2}\sqrt{\frac{P_0}{C_2 V_{2,\text{eq}} K_I}}. \end{cases} \tag{31}$$

The PI controller parameters of V_2 control loop are designed based on the canonical second-order system response defined by ω_n and ζ in (31). To ensure that V_1 voltage loop responds significantly slower than the power control loop, ω_n is selected well below $2\omega_g$. The damping ratio is constrained to $0.7 < \zeta < 1.2$ to achieve an acceptable settling time. In addition, the PI gains are assigned with sufficient margin to maintain effective buffering under potential reductions in C_2 or variations in $V_{2,\text{eq}}$, thereby preserving V_2 loop performance.

B. Design Considerations for the Buffering Capacitor C_2

Based on (9), the minimum of V_2 can be obtained as

$$V_{2\min} = \sqrt{V_{2\max}^2 - \frac{2P_m}{C_2\omega_g}}. \tag{32}$$

According to (32), the decoupling capacitor C_2 can be expressed as

$$C_2 = \frac{2P_m}{\omega_g(V_{2\max}^2 - V_{2\min}^2)} = \frac{P_m}{\omega_g \Delta V_2 V_{2\text{ave}}} \tag{33}$$

where $\Delta V_2 = V_{2\max} - V_{2\min}$ is the voltage pulsations across C_2, $V_{2\text{ave}} = (V_{2\max} + V_{2\min})/2$ denotes the average voltage of C_2.

As (33) indicates, increasing the allowable voltage pulsations ΔV_2 reduces the required capacitance C_2, but at the expense of higher voltage stress on the buffering capacitor. Conversely, decreasing ΔV_2 necessitates a larger C_2, which increases the cost and volume of the buffering capacitor. Therefore, the selection of C_2 is the comprehensive consideration of buffering performance, voltage stress, and cost.

C. Computational Complexity of the Proportion Parameter k

By combining (10) and (14), the proportion parameter k for power buffering can be reformulated as

$$k = \frac{i_{\alpha\text{ref}} e_\alpha^+ + i_{\beta\text{ref}} e_\beta^+}{i_\alpha v_\alpha + i_\beta v_\beta} = \frac{i_{\alpha\text{ref}} e_\alpha^+ + i_{\beta\text{ref}} e_\beta^+}{i_{\alpha\text{ref}} v_\alpha + i_{\beta\text{ref}} v_\beta} \tag{34}$$

where $i_{\alpha\text{ref}}$ and $i_{\beta\text{ref}}$ originate from the external voltage control loop, e_α^+ and e_β^+ are obtained from the DSOGI-PLL, and v_α and v_β are outputs of the current control loop.

As indicated in (34), computing the proportion parameter k requires four multiplications, two additions, and one division per control cycle. In grid-connected ac–dc converters, the PLL as well as the current and external voltage control loops are inherent parts of the control architecture. With appropriate design, these loops can attenuate the detrimental effects of harmonics and measurement noise, thereby ensuring accurate and robust computation of k. In scenarios involving stronger distortions or higher uncertainty, advanced methods such as disturbance-observer-based control [35] or algebraic estimation technique [36] can be employed to further improve robustness. However, these methods inevitably increase computational complexity, resulting in a tradeoff between improved noise immunity and implementation burden.

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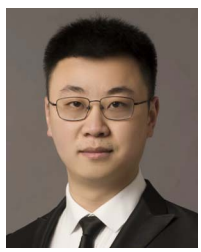

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