# A Five-Level Common-Ground Buck-Boost Inverter With Capacitor Voltage Balance

Vinh-Thanh Tran, Anh-Tuan Nguyen-Phan, Duc-Tri Do, *Member, IEEE*, and Khai M. Nguyen

***Abstract*—A new five-level common-ground buck-boost inverter (5L-CG-BBI) topology is presented in this article. The 5L-CG-BBI can eliminate common-mode voltage by the dc source and ac load sharing the same ground. To regulate the introduced 5L-CG-BBI, a space-vector modulation (SVM) approach has been presented. In this scheme, neutral-point voltage is balanced by using the proper medium voltage vectors in the switching sequences. The proposed inverter can buck and boost ac output voltage from a single dc input source in two-stage power conversion, where the modulation index of the inverter side and the duty ratio of the dc–dc stage are controlled independently. Consequently, the component voltage ratings of the introduced inverter are improved compared to existing 5L-CG inverters. The proposed inverter and SVM scheme are validated by a 900-W experimental prototype.**

***Index Terms*—Buck-boost inverter, common-ground (CG), common-mode voltage (CMV), leakage current (LC), neutral-point voltage (NPV) balance.**

## I. Introduction

CONVENTIONAL H-bridge inverter is widely adopted in transformer-less photovoltaic (PV) applications. However, it only generates a three-level output voltage. In order to enhance numbers of output voltage levels, some five-level inverters (5LIs) have been presented [1], [2]. Because the switching devices of the inverters operate under high switching frequency, high *dv*/*dt* common-mode voltage (CMV) between negative point of the input source and the ground is generated. High CMV causes high leakage current (LC) going through stray capacitors between the input source and the ground [3], [4], [5]. Moreover, the LC causes electromagnetic interference noise and safety concern [3]. So, in transformer-less inverters, LC and CMV are considered to be mitigated.

H5, H6, and HERIC topologies have been presented to mitigate CMV and LC [6], [7]. In H5 topology, one extra switch has been installed in series with dc-link rail, which is between the input source and H-bridge circuit. In active modes, this switch is gated on, however, in freewheeling mode, it is gated off to create galvanic isolation between the dc source and the ac grid. Consequently, the CMV and LC in H5 topology are mitigated. The same way is also applied to H6 topology to mitigate LC. The H6 topology uses two more active switches and two more diodes than conventional full-bridge inverter [8], [9]. The HERIC configuration installed a bi-directional switch in parallel with output load to implement freewheeling mode [7], [10]. It helps to reduce conduction loss compared to the H5 and H6 topologies. However, LC in these topologies is not completely eliminated.

Half-bridge inverters are considered as inverters with a constant CMV and a very small LC [11], [12]. In these topologies, the CMV remains fixed at half of the dc-link voltage. However, half-bridge inverters only have a maximum voltage gain of 0.5. To enhance the voltage gain of these inverters to 1, switched-capacitor (SC) circuit has been adopted before the inverter side to increase the dc-link voltage to twice that of input voltage [11]. However, with this voltage gain value, the inverters just operate in buck mode, where the dc input source's voltage is greater than the ac output voltage. To increase the voltage gain, a dc–dc boost converter is placed at the front end of the inverter to enhance the dc-link voltage [13]. Neutral-point voltage (NPV) unbalance is an important issue of these inverters, which must be addressed to ensure high quality of output voltage/current.

SC-based inverters with common-ground (CG) feature have attracted much attention from researchers because they can obtain zero CMV/LC by connecting negative points of input voltage and output load [14], [15], [16], [17], [18]. The basic concept of these SC-based CG inverters is that the virtual dc-link capacitors are charged in medium positive voltage levels or zero output voltage level. Then, these virtual dc-link capacitors are employed to feed the output and generate negative voltage levels. In some configurations, flying capacitors are adopted to create more output voltage levels [17], [18]. Moreover, the SC structures help the inverters to boost the dc-link voltage. However, the boost factor is not flexible to be controlled, which is fixed to 2 or 3. Moreover, when connecting two capacitors in parallel, it generates high charging currents going through capacitors and switches. This leads to significant switching and conduction losses in the inverter.

The work in [13] presented a single-stage 5L-CG boost-type active neutral-point-clamped (5L-CGBT-ANPC) inverter, which can buck-boost output voltage from a single dc input source in single stage power conversion. The work in [13] can produce a five-level output voltage with only seven switches. However, the duty ratio of switches of dc–dc stage is greater than $2M - 1$,

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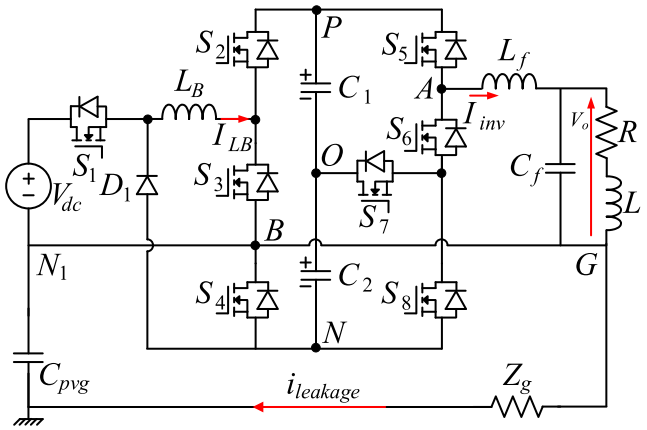


Fig. 1. Topology of the proposed 5L-CG-BBI.

where $M$ is modulation index of inverter stage. So, this inverter produces very high component voltage ratings. The works in [19], [20] have the same drawback such as [13], where duty ratio $D$ is not smaller than modulation index $M$. The literature in [21] presented a switched-boost dual T-type 5L inverter with CG feature, which have uncoupled $D$ and $M$. Hence, modulation index $M$ can theoretically be maximized to 1. Consequently, the component voltage ratings are reduced, significantly.

The work in [22] presented a combination of a quadratic dc–dc cell and dc–ac inverter cell with CG feature. Inheriting high-gain feature of quadratic cell, Oppong et al. [22] have a high boost factor of about $1/(1\text{-}D)^2$. However, the inductors of [22] operate in discontinuous conduction mode, which generates high current ratings of devices. A step-up/down 5L CG inverter was presented in [23]. This topology can limit the charging currents of capacitors by adopting a small inductor attached in series with input dc source. Similar to SC based inverters, this inverter only boosts the ac output voltage to twice dc input source. The literature in [24] presented a new topology which integrates one extra active switch to the mid-point of the conventional two-stage T-Type inverter. This extra switch helps to increase boost factor to twice that in conventional inverter. A combination of quasi-Z-source (qZS) network and a virtual dc bus cell in [25] brings benefits of voltage boosting and CG feature. DC–DC boosting operating is ensured by qZS circuit. However, coupled $D$ and $M$ is existing limitation of [24], [25]. Oppong et al. [26] integrated a coupled inductor to enhance boost factor for PV applications. However, the energy of leakage inductance must be managed to reduce voltage spikes. Agrawal et al. [27] introduced a topology of five-level CG inverter with fault-tolerance characteristic. In [27], some extra redundant switches were integrated with the main inverter to recovery the operating of the inverter under open-circuit fault. It increases the reliability of the inverter. However, it also increases the cost and component voltage ratings.

The topology of a 5L-CG buck-boost inverter (5L-CG-BBI) is presented in this article, which eliminates CMV by adopting CG feature. The 5L-CG-BBI is capable of producing a five-level output voltage. The introduced inverter can buck/boost ac output voltage from a single dc source in two stage power conversion. As a result, there is no coupling between the modulation index $M$ and the duty ratios of the dc–dc boost circuit. Therefore, component voltage ratings of the proposed inverter are improved compared to existing 5L-CG inverters. The proposed inverter is controlled using a space vector modulation (SVM) technique. In this approach, medium voltage vectors are correspondingly selected to balance NPV. An experimental prototype is adopted to test the proposed inverter and SVM scheme. The rest of this article consists of seven sections. Section II introduces topology of the proposed inverter and its operating principle. Section III presents the proposed SVM method to balance NPV. Design guidelines and comparison analysis are presented in Sections IV and V. In Section VI, the power loss analysis is provided. Experimental results are provided in Section VII. Section VIII concludes this article.

## II. Proposed 5L-CG-BBI Topology

In Fig. 1, the 5L-CG-BBI topology is depicted. It is composed of an inverter side circuit and a dc–dc circuit to convert dc-source to ac output load. Three switches $S_2$, $S_3$, and $S_4$ are used for dc–dc boost circuit and dc–ac side circuit. Beside these three switches, the dc–dc circuit includes one inductor $L_B$, two capacitors $C_1$, $C_2$, one switch $S_1$ and one diode $D_1$. The inverter side circuit employs seven switches ($S_2 - S_8$) to convert the dc-link voltage $V_{PN}$ into an ac output voltage. With these seven switches, the inverter can generate a five-level voltage at output voltage $V_{AB}$. Both dc–ac and dc–dc operating modes are independently controlled by the proposed inverter's operating principle. The operating modes of the introduced inverter have been detailed as follows.

The CMV in single-phase inverter is defined as voltage between negative points $G$ of output load and $N_1$ of dc input source. As shown in Fig. 1, these terminals are directly connected. It results in constant zero values of CMV and LC. This is the reason why the proposed inverter and any CG inverters can eliminate CMV.

### A. Operating Principle of Inverter Side Circuit

Fig. 2 shows the introduced inverter's operating modes. The proposed inverter is capable of generating five distinct output voltage levels $\pm V_{PN}$, $\pm V_{PN}/2$, and 0 V as illustrated in Fig. 2, where $V_{PN}/2 = V_{C1} = V_{C2}$, and $V_{PN} = V_{C1} + V_{C2}$. When the output voltage $V_{AB}$ equals $+V_{PN}$, as presented in Fig. 2(a), the switches $S_4$, $S_5$, and $S_7$ are turned ON, while $S_6$ and $S_8$ are turned OFF. In this condition, the full dc-link voltage $V_{PN}$ is applied across the output voltage. In Fig. 2(b), the switches $S_4$, $S_6$, and $S_7$ are turned ON, while $S_5$ and $S_8$ are turned OFF. In this state, the capacitor $C_2$ supplies energy to the load and the output voltage $V_{AB}$ equals to $V_{C2} = V_{PN}/2$. The $V_{AB}$ equals 0-V when the switches $S_4$, $S_6$, and $S_8$ or $S_2$, $S_3$, $S_5$, and $S_7$ are turned ON, as presented in Fig. 2(c), (d). In this condition, terminals $A$ and $B$ of output voltage are directly connected. In order to produce value $-V_{PN}/2$ at the output voltage $V_{AB}$, the switches $S_2$, $S_3$, $S_6$, and $S_7$ are turned ON, while $S_4$, $S_5$, and $S_8$ are turned OFF. In this state, node $A$ is connected to the negative terminal of capacitor $C_1$, whereas node $B$ is connected to positive terminal of $C_1$ which results in $V_{AB} = -V_{C1} = -V_{PN}/2$. When the output voltage $V_{AB}$ equals $-V_{PN}$, the $S_2$, $S_3$, $S_6$, $S_8$ are turned ON, while $S_4$, $S_5$, and $S_7$ are turned OFF, as shown in Fig. 2(f).

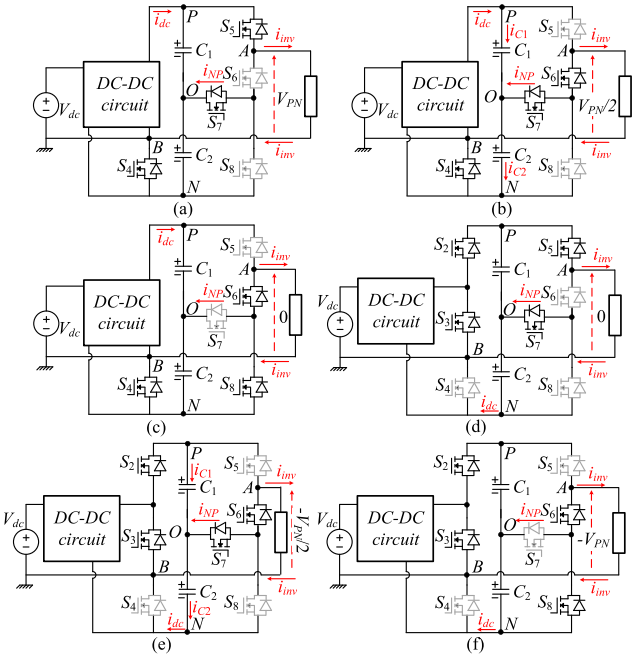


Fig. 2. Operating modes of the inverter side. (a) Vector [PN]. (b) Vector [ON]. (c) Vector [NN]. (d) Vector [PP]. (e) Vector [OP]. (f) Vector [NP].

It can be seen that branch *A* of the inverter side can generate a three-level output voltage at output pole voltage $V_{AO}$, which are states *P*, *O*, and *N* corresponding to values $+V_{PN}/2$, 0 V, and $-V_{PN}/2$. Because branch *B* has only three switches, at output pole voltage $V_{BO}$, it is unable to produce a three-level voltage. Instead, it generates two states *P* and *N* at $V_{BO}$. It should be defined that a vector is a combination of one state of $V_{AO}$ and one state of $V_{BO}$. For example, when the inverter operates under vector [*PN*], the output pole voltage $V_{AO}$ is $+V_{PN}/2$ and $V_{BO}$ is $-V_{PN}/2$. Consequently, the output voltage $V_{AB}$ is $+V_{PN}$, as depicted in Fig. 2(a). When the inverter produces vectors [ON], [NN], [PP], [OP], [NP], the $V_{AB}$ is $+V_{PN}/2$, 0 V, 0 V, $-V_{PN}/2$, and $-V_{PN}$, respectively, as shown in Fig. 2(b)–(f).

### B. Operating Principle of DC–DC Circuit

Switches $S_1$–$S_4$ together with diode $D_1$ are employed to control the dc–dc stage of the inverter. When the output voltage $V_{AB}$ is positive, the inverter side operates under vectors [PN], [ON], and [NN]. Modes 1 and 2 of the dc–dc circuit are utilized to step up the dc-link voltage from a dc input voltage. In these modes, switches $S_1$ and $S_4$ are always gated ON. It results in reverse biasing diode $D_1$. When switch $S_3$ is turned ON and switch $S_2$ is turned off, mode 1 presented in Fig. 3(a) is activated. Now, the boost inductor $L_B$ is charged by input voltage and capacitors $C_1$ and $C_2$ are discharged by inverter side current. The following equations are obtained

$$\begin{cases} v_{LB} = L_B \cdot di_{LB}/dt = V_{\rm dc} \\ i_{C1} = i_{C2} = C_1 dv_{C1}/dt = C_2 dv_{C2}/dt = -I_{PN} \end{cases} \tag{1}$$

where $I_{PN}$ is equivalent current of inverter side.

In mode 2 shown in Fig. 3(b), switch $S_2$ is gated ON, whereas switch $S_1$ is triggered OFF. As a result, inductor $L_B$ and input

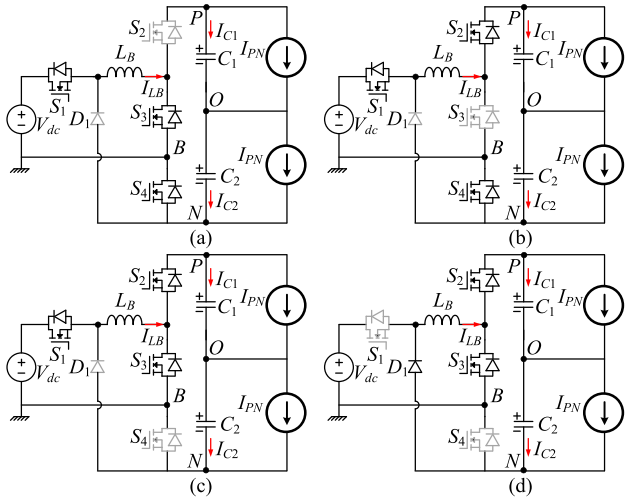


Fig. 3. Operating modes of dc–dc circuit. (a) and (b) Modes 1, 2 under vectors [PN], [ON], [NN]. (c) and (d) Modes 3, 4 under vectors [PP], [OP], [NP].

voltage charge for two capacitors. The expressions for the inductor voltage and capacitor currents are derived as follows

$$\begin{cases} v_{LB} = L_B \cdot di_{LB}/dt = V_{\rm dc} - V_{C1} - V_{C2} = V_{\rm dc} - V_{PN} \\ i_{C1} = i_{C2} = C_1 dv_{C1}/dt = C_2 dv_{C2}/dt = I_{LB} - I_{PN} \end{cases}. \tag{2}$$

When $V_{AB}$ operates in negative half cycle, the inverter side adopts vectors [PP], [OP], [NP]. Now, the dc–dc circuit utilizes modes 3 and 4 to boost dc-link voltage. In these modes, switches $S_2$ and $S_3$ are always triggered ON, as illustrated in Fig. 3(c) and (d). In mode 3, switch $S_1$ is gated ON to store energy to inductor $L_B$. Two capacitors are discharged by inverter side current. Equation (1) describes the voltage of inductor $L_B$ and capacitor currents in this mode. In mode 4, switch $S_1$ is turned OFF, which forward-biases diode $D_1$, as presented in Fig. 3(d). The inductor $L_B$ charges for two capacitors, as expressed in the following equation:

$$\begin{cases} v_{LB} = L_B \cdot di_{LB}/dt = -V_{C1} - V_{C2} = -V_{PN} \\ i_{C1} = i_{C2} = C_1 dv_{C1}/dt = C_2 dv_{C2}/dt = I_{LB} - I_{PN} \end{cases}. \tag{3}$$

## III. Proposed SVM Method to Balance NPV

In Fig. 4, the space vector diagram (SVD) of the proposed SVM approach is presented. This SVD has two zero vectors [PP] and [NN], two medium vectors [ON] and [OP], two large vectors [PN] and [NP]. For large vectors [PN] in Fig. 2(a) and [NP] in Fig. 2(f), the neutral current $i_{\rm NP}$ is 0 A, the capacitor currents $I_{C1}$ and $I_{C2}$ are equal and $I_{C1} = I_{C2} = i_{\rm dc} - i_{\rm inv}$, where $i_{\rm dc}$ and $i_{\rm inv}$ are output currents of dc–dc circuit and inverter circuit, respectively. For zero vectors [PP] and [NN] in Fig. 2(c) and (d), the capacitor currents are $I_{C1} = I_{C2} = i_{\rm dc}$. The capacitor currents in the large vectors and zero vectors are found to be equal, so these vectors do not affect the difference between these capacitor voltages. However, there is a difference between two capacitor currents in medium vectors. As presented in Fig. 2(b) and (e), when the inverter operates under vectors [OP] and [ON], terminal *A* is directly connected to neutral point *O*. Now, the neutral current

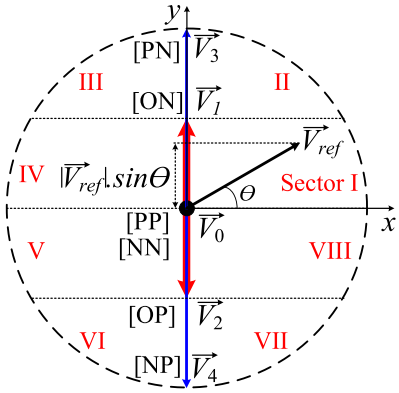


Fig. 4. SVD of the proposed SVM method.

$i_{\rm NP}$ is -$i_{\rm inv}$. Two capacitor currents are expressed as follows:

$$\begin{cases} i_{C1} = C_1 \frac{dv_{C1}}{dt} = i_{\rm dc} \\ i_{C2} = C_2 \frac{dv_{C2}}{dt} = i_{\rm dc} + i_{NP} = i_{\rm dc} - i_{\rm inv} \end{cases} \text{for [ON]}$$

$$\text{and} \begin{cases} i_{C1} = C_1 \frac{dv_{C1}}{dt} = i_{\rm dc} - i_{NP} = i_{\rm dc} + i_{\rm inv} \\ i_{C2} = C_2 \frac{dv_{C2}}{dt} = i_{\rm dc} \end{cases} \text{for [OP].} \quad (4)$$

Because of the difference between $I_{C1}$ and $I_{C2}$ in medium vectors, these vectors affect the capacitor voltage difference. For example, when $i_{\rm inv} < 0$ and $C_1 = C_2$, current of capacitor $C_2$ is larger than that of capacitor $C_1$. Consequently, capacitor $C_2$ voltage is increased faster than capacitor $C_1$ voltage. So, in case of $V_{C1} > V_{C2}$, these medium vectors can balance capacitor voltages. In contrast, in case of $V_{C1} < V_{C2}$, these medium vectors increase the capacitor voltage difference which makes the capacitor voltage unbalance issue worse. Similarly, when $i_{\rm inv} > 0$, current of capacitor $C_2$ is smaller than that of capacitor $C_1$. As a result, capacitor $C_1$ voltage is increased faster than capacitor $C_2$ voltage. So, in case of $V_{C2} > V_{C1}$, these medium vectors can balance capacitor voltages. However, when $V_{C2} < V_{C1}$, these medium vectors make the capacitor voltage unbalance issue worse. It can be concluded that, the NPV can be balanced by choosing appropriate medium vectors.

### A. Proposed SVM Method

The SVD is separated into eight sectors (I–VIII), as shown in Fig. 4. The analysis of the proposed method is carried out by considering sectors I and II as examples. In conventional SVM methods, two nearest vectors will be selected to synthesize the reference vector$\vec{V}_{\rm ref}$. For example, in sector I, two vectors [ON] and [NN] are adopted in switching sequence. However, in the proposed method, candidate voltage vectors will be selected based on capacitor voltages to balance NPV.

If the reference vector is located in Sector I, based on actual capacitor voltages, candidate voltage vectors will be selected to balance NPV. In case 1, when $V_{C1} < V_{C2}$, if $i_{\rm inv} > 0$, vector [ON] helps to balance NPV. So, two vectors [ON] and [NN] are adopted to synthesize output voltage. The following equations

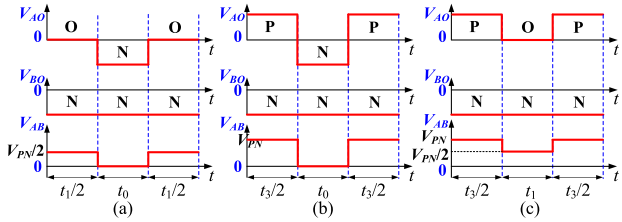


Fig. 5. Switching sequences for proposed method in (a) and (b) sector I, (c) sector II. (a) $V_{C1} < V_{C2}$, $i_{\rm inv} > 0$ or $V_{C1} > V_{C2}$, $i_{\rm inv} < 0$, (b) $V_{C1} > V_{C2}$, $i_{\rm inv} > 0$ or $V_{C1} < V_{C2}$, $i_{\rm inv} < 0$.

are obtained

$$|\vec{V}_{\rm ref}| \sin\theta \cdot T = |\vec{V}_0| \cdot t_0 + |\vec{V}_1| \sin(\pi/2) \cdot t_1 \text{ and } T = t_0 + t_1 \quad (5)$$

where $T$ is switching period, $t_0$, $t_1$ are dwell times of vectors $\vec{V}_0$ and $\vec{V}_1$, respectively.

The $|\vec{V}_{\rm ref}|$, $|\vec{V}_0|$, $|\vec{V}_1|$ are expressed as follows:

$$|\vec{V}_{\rm ref}| = MBV_{\rm dc}; |\vec{V}_0| = 0; |\vec{V}_1| = BV_{\rm dc}/2 \quad (6)$$

where $M$ is modulation index ($M \leq 1$), $B$ is boost factor.

Substituting (6) into (5), the calculation of dwell times for the candidate voltage vectors is given by

$$t_1 = 2M \sin(\theta)T; \text{ and } t_0 = (1 - 2M \sin\theta)T. \quad (7)$$

In case 2, when $V_{C1} > V_{C2}$, if $i_{\rm inv} > 0$, two medium vectors cannot be adopted in switching sequence because they increase the difference between two capacitor voltages. So, zero vector [NN] and large vector [PN] are selected to synthesize output voltage. These vectors can maintain the difference between $V_{C1}$ and $V_{C2}$. The following equations are obtained

$$|\vec{V}_{\rm ref}| \sin\theta \cdot T = |\vec{V}_0| \cdot t_0 + |\vec{V}_3| \sin(\pi/2) \cdot t_3 \text{ and } T = t_0 + t_3 \quad (8)$$

where $t_3$ is dwell time of vector $\vec{V}_3$. $|\vec{V}_3|$ is expressed as follows:

$$|\vec{V}_3| = BV_{\rm dc}. \quad (9)$$

The on-times of candidate vectors are expressed as follows:

$$t_3 = M \sin\theta T \text{ and } t_0 = (1 - M \sin\theta)T. \quad (10)$$

The switching sequences for case 1 and case 2 are [ON]-[NN]-[ON] and [PN]-[NN]-PN], as presented in Fig. 5(a) and (b). In cases 3, when $V_{C1} < V_{C2}$ and $i_{\rm inv} < 0$, the switching pattern in Fig. 5(b) is selected, whereas the switching sequence in Fig. 5(a) is adopted to balance NPV when $V_{C1} > V_{C2}$ and $i_{\rm inv} < 0$ (case 4).

In case the reference vector falls within Sector II, two vectors [ON] and [PN] are adopted. The relationship between these vectors and vector$\vec{V}_{\rm ref}$ are expressed as follows:

$$\begin{cases} |\vec{V}_{\rm ref}| \sin\theta \cdot T = |\vec{V}_1| \sin(\pi/2) \cdot t_1 + |\vec{V}_3| \sin(\pi/2) \cdot t_3 \\ T = t_1 + t_3 \end{cases}. \quad (11)$$

The on-times of the candidate vectors can be obtained as

$$t_3 = (2M \sin\theta - 1)T; \text{ and } t_1 = (2 - 2M \sin\theta)T. \quad (12)$$

In Fig. 5(c), the switching sequence for sector II is [PN]-[ON]-[PN]. Table I summarizes the dwell-time calculations

TABLE I
DWELL-TIME CALCULATIONS AND SWITCHING SEQUENCE SELECTIONS

| Sector | | $I_{inv}$ | Dwell-times | Switching sequences |
|---|---|---|---|---|
| I, IV | $V_{C1} < V_{C2}$ | $> 0$ | $t_1 = 2M\sin\theta T;\ t_0 = (1-2M\sin\theta)T$ | [ON]-[NN]-[ON] |
| | $V_{C1} > V_{C2}$ | $< 0$ | | |
| | $V_{C1} > V_{C2}$ | $> 0$ | $t_3 = M\sin\theta T;\ t_0 = (1-M\sin\theta)T$ | [PN]-[NN]-[PN] |
| | $V_{C1} < V_{C2}$ | $< 0$ | | |
| II, III | – | – | $t_3 = (2M\sin\theta-1)T;\ t_1 = (2-2M\sin\theta)T$ | [PN]-[ON]-[PN] |
| V, VIII | $V_{C1} < V_{C2}$ | $> 0$ | $t_2 = -2M\sin\theta T;\ t_0 = (1+2M\sin\theta)T$ | [PP]-[OP]-[PP] |
| | $V_{C1} > V_{C2}$ | $< 0$ | | |
| | $V_{C1} > V_{C2}$ | $> 0$ | $t_4 = -M\sin\theta T;\ t_0 = (1+M\sin\theta)T$ | [PP]-[NP]-[PP] |
| | $V_{C1} < V_{C2}$ | $< 0$ | | |
| VI, VII | – | – | $t_4 = (-2M\sin\theta-1)T;\ t_2 = (2+2M\sin\theta)T$ | [OP]-[NP]-[OP] |

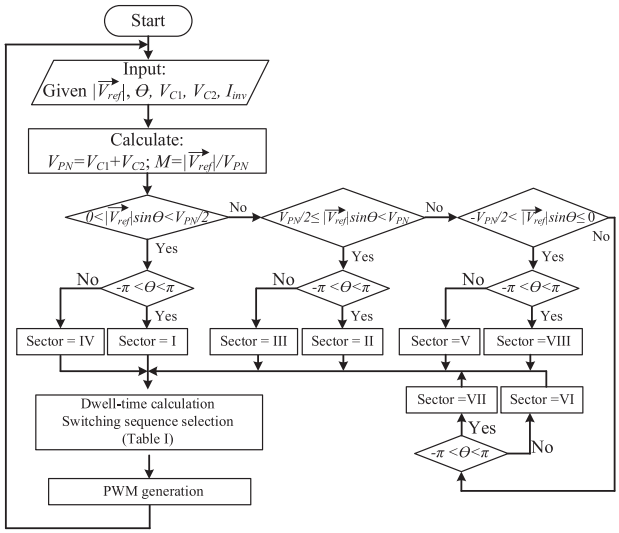


Fig. 6. Flowchart of the proposed SVM method in any switching period $T$.

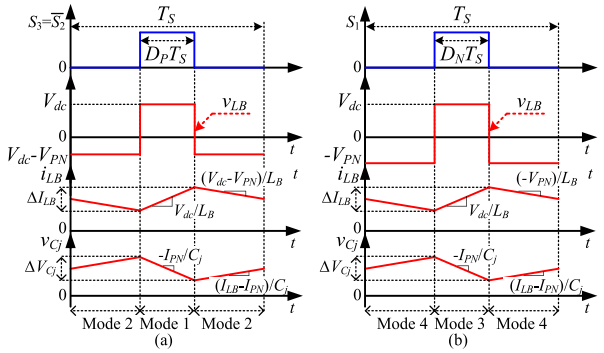


Fig. 7. Key waveforms of the introduced 5L-CG-BBI under (a) positive half cycle of $V_{AB}$ and (b) negative half cycle of $V_{AB}$.

and switching sequence selections for the other sectors. The flowchart of the proposed SVM method is depicted in Fig. 6.

## B. Steady-State Analysis

Fig. 7 illustrates the key waveforms of the proposed inverter during the positive and negative half cycles of the output voltage. In positive half cycle, duty ratio of mode 1 is $D_P$, whereas duty ratio of mode 2 is (1 - $D_P$), as shown in Fig. 7(a). Applying the volt–second balance principle to inductor $L_B$, the capacitor

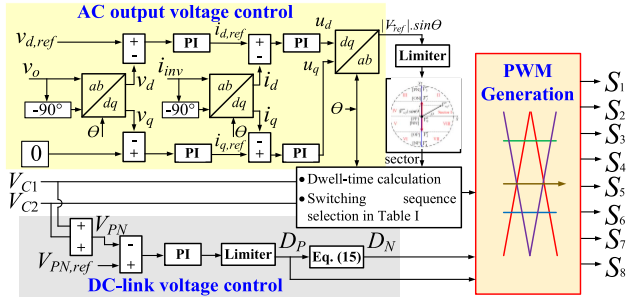


Fig. 8. Control block diagram of the proposed method.

voltages $V_{C1}$ and $V_{C2}$ are expressed as follows:

$$V_{C1} = V_{C2} = V_{PN}/2 = V_{\rm dc}/[2(1-D_P)]. \tag{13}$$

Similarly, in negative half cycle, the duty ratio of mode 3 is $D_N$, while duty ratio of mode 4 is $(1-D_N)$. Based on (1), (3), and voltage-second balanced principle of inductor $L_B$, the capacitor voltages are calculated as follows:

$$V_{C1} = V_{C2} = V_{\rm PN}/2 = V_{\rm dc}D_N/[2(1-D_N)]. \tag{14}$$

Now, the following equation presents boost factor $B$:

$$B = V_{PN}/V_{\rm dc} = 1/(1-D_P) = D_N/(1-D_N). \tag{15}$$

The amplitude of output voltage $\hat{V}_O$ is the magnitude of reference vector, which is calculated as follows:

$$\hat{V}_O = MBV_{\rm dc} = MV_{\rm dc}/(1-D_P) = MV_{\rm dc}D_N/(1-D_N). \tag{16}$$

The voltage gain $G$ of the inverter is given as follows:

$$G = \hat{V}_O/V_{\rm dc} = MB = M/(1-D_P) = MD_N/(1-D_N). \tag{17}$$

## C. DC-Link Voltage and AC Output Voltage Regulations

Fig. 8 presents the control block diagram designed to maintain a constant dc-link voltage and generate an ac output voltage at the load. It should be noted that the dc-link voltage regulation and the ac output voltage control are carried out independently. First, two capacitor voltages, $V_{C1}$ and $V_{C2}$, are fed back to the controller to regulate the dc-link voltage. The $V_{C1}$ and $V_{C2}$ are added up to determine the dc-link voltage. The actual value of $V_{PN}$ is compared with desire dc-link voltage to generate error signal. As illustrated in Fig. 8, a proportional integral (PI) controller is

adopted to minimize this error signal. Duty ratio $D_P$ is the PI controller's output. Equation (15) is used to compute duty ratio $D_N$. The values $D_P$ and $D_N$ are employed to control the dc–dc stage of the introduced inverter.

The ac output voltage regulation is carried out by providing feedback signals of $V_O$ and $I_{\rm inv}$ to the controller. Then PI controllers are adopted to calculate value $|\vec{V}_{\rm ref}|\sin\theta$, as presented in Fig. 8. The limiter of ac output voltage control loop limits the $|\vec{V}_{\rm ref}|\sin\theta$ to no greater than dc-link voltage $V_{\rm PN}$. This value is used to determine sector of reference vector, shown in Fig. 6. Then, the dwell-time calculation and switching sequence selection are done by using capacitor voltages, phase angle $\theta$ and the help of Table I. It should be noted that two capacitor voltages are used to determine switching sequence to balance NPV. The switching sequence is then used to generate control signal to switches.

## IV. Component Selections

### A. Inductor and Capacitor Selections

Based on (15), the coefficient $D_P$ is calculated by the duty ratio $D_N$ as: $D_P = (2D_N - 1)/D_N$, with $0.5 \le D_N \le 1$. It can be seen that duty ratio $D_P$ is always less than duty ratio $D_N$. As a result, inductor current ripple $\Delta I_{LB}$ calculated by $D_N$ is larger than the current ripple calculated by $D_P$. Therefore, the inductor current ripple based on $D_N$ is used to select inductor $L_B$. The $\Delta I_{LB}$ is expressed as follows:

$$\Delta I_{LB} = V_{\rm dc} D_N T_S / L_B. \tag{18}$$

When the output voltage $V_{AB}$ is positive, the $L_B$ is directly attached to the input voltage. While, in negative cycle of $V_{AB}$, it is connected to input source in $D_N T_S$ in any switching period. So, the average current of inductor $L_B$ is expressed as $I_{LB} = 2P_O/[V_{\rm dc}(1 + D_N)]$, where $P_O$ is output power.

The inductor is selected in term of $\Delta I_{LB} \le k_L\% I_{LB}$, where $k_L\%$ is inductor current factor

$$L_B \ge V_{\rm dc}^2 D_N (1 + D_N) T_S / (2k_L\% P_O). \tag{19}$$

The capacitor voltage ripple $\Delta V_{Cj}$ $(j = 1, 2)$ are expressed by duty ratio $D_N$ as follows:

$$\Delta V_{Cj} = I_{PN} D_N T_S / C_j. \tag{20}$$

The capacitor $C_j$ is selected in term of $\Delta V_{Cj} \le k_C\% B V_{\rm dc}/2$, where $k_C\%$ is capacitor voltage factor

$$C_j \ge 2 I_{PN} D_N T_S / (k_C\% B V_{\rm dc}). \tag{21}$$

If the proposed inverter is extended to apply for grid connected PV application, one input capacitor $C_P$ has been added in parallel to the PV input voltage $V_{\rm PV}$ to prevent $2\omega$ power from flowing into the PV panel [28]. The capacitance of $C_P$ is expressed as follows [28]:

$$C_P \ge P_m / (2\omega k_V\% V_{\rm PV}^2) \tag{22}$$

where $P_m$ is designed power of the inverter, $k_V\%$ is acceptable percentage of PV input voltage ripple which is usually $5\% \div 10\%$, $\omega$ is line frequency of ac grid.

### B. Semiconductor Device Selections

The voltage ratings of switches $S_2$–$S_5$ are dc-link voltage $V_{PN}$, while the switch $S_6$–$S_8$ voltage rating are half of dc-link voltage $V_{PN}/2$. Switch $S_1$ and diode $D_1$ block the sum of the input voltage and the dc-link voltage, $V_{\rm dc} + V_{PN}$. Three switch $S_1$–$S_3$, and diode $D_1$ transfer inductor current $I_{LB}$, while other switches are designed to carry inverter side current $I_{\rm PN}$.

## V. Comparison Study

The proposed inverter can bring some benefits such as:

1) eliminating LC by adopting CG characteristic;
2) reducing component voltage ratings with uncoupled *M* and *D* feature; and
3) reducing cost of semiconductor devices.

Moreover, because the proposed inverter does not use SC structure, it does not generate high inrush currents through capacitors and semiconductor devices. In order to highlight these advantages, some single-phase 5LIs have been compared with the introduced 5L-CG-BBI, as listed in Table II.

First, the numbers of component counts have been compared between the proposed inverter and others. In general, the numbers of switches used in these topologies are approximately the same. The topologies in [16] and [17] employ one fewer active switch than the proposed inverter; however, they require one additional diode compared to the proposed topology. The proposed 5L-CG-BBI can save one active switch compared to [18], [20] and two switches compared to [21] and conventional two stage 5L-ANPC inverter mentioned in [13]. The topology in [19] requires one fewer diode than the proposed inverter. The work in [13] uses smallest numbers of switching devices, which only uses seven switches and zero diode.

The [16] and [18] use SC structure to boost the dc-link voltage. When capacitors of these works are connected in parallel, they generate high inrush charging currents through capacitors and switches because of small parasitic resistances of devices in charging paths. However, the proposed inverter acts like a conventional 2-stage buck-boost inverter, so it can limit the charging currents of capacitors to no more than inductor current. Consequently, the introduced topology does not generate high inrush charging currents through capacitors and switches.

Topology in [16] does not have a constant CMV, so it generates high LC through parasitic capacitors between source and load. The works in [19] and [20] directly connect the positive point of dc input source to the negative point of load, while the conventional two-stage 5L-ANPC inverter establishes a direct connection between the load negative point and the dc-link neutral point. So, they generate constant CMVs and near zero LCs. The proposed inverter, the works reported in [13], [17], [18], and [21] adopt a CG connection for both the input source and the output load. Hence, they create zero CMVs and zero LCs.

The efficiency of the proposed inverter and others has been listed in Table II. It can be seen that the efficiency reported in Table II varies from 95% to 97%. The proposed inverter can obtain efficiency of 95.4% in buck mode and 95% in boost mode. It is close to existing inverters.

The component voltage ratings of the proposed inverter have been compared with the others in terms of total capacitor voltage

TABLE II
OVERALL COMPARISON BETWEEN PROPOSED TOPOLOGY AND EXISTING BUCK-BOOST INVERTERS

| | Sw. | Di. | Ind. | Cap. | ($D$) | $I_{CC}$ | ($B$) | ($G$) | TCV | TSV | TDV | CMV/ LC | Cost of Semi | $\eta$ @ Power |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| [16] | 7 | 2 | 0 | 2 | NA | High | 2 | 2$M$ | 2 | 11 | 2 | High/high | $128.65 | 95.2% @ 1kW |
| [17] | 7 | 2 | 2 | 2 | 0.5 | Low | 2 | 2$M$ | 3 | 12 | 4 | Zero/zero | $140.51 | NA |
| [18] | 9 | 0 | 0 | 2 | NA | High | 2 | 2$M$ | 2 | 13 | NA | Zero/zero | $129.07 | 97% @ 1kW (buck) 96.2%@1kW (boost) |
| [21] | 10 | 0 | 1 | 2 | Uncoupled | No | 2/(1-$D$) | $MB$ | $B$ | 7.5$B$ | NA | Zero/zero | $148.6 | NA |
| [13] | 7 | 0 | 1 | 2 | $D \geq 2M$-1 | No | 1/(1-$D$) | $MB$ | 1.5$B$ | 6$B$ | NA | Zero/zero | $118.03 | NA |
| [19] | 8 | 0 | 1 | 2 | $D \geq M$ | No | 1/(1-$D$) | $MB$ | 1.5$B$ | 7$B$ | NA | $V_{dc}$/0 | $137.56 | 95.9%@170W |
| [20] | 9 | 0 | 1 | 2 | $D \geq M$ | High | 2/(1-$D$) | $MB$ | $B$ | 6.5$B$ | NA | -$V_{dc}$/0 | $175.77 | NA |
| 2-Stage 5L-ANPC | 10 | 0 | 1 | 3 | Uncoupled | No | 1/(1-$D$) | $MB$/2 | 1.5$B$ | 6$B$ | NA | $V_{PN}$/2/0 | $120.58 | NA |
| Proposed | 8 | 1 | 1 | 2 | Uncoupled | No | $D$/(1-$D$) | $MB$ | $B$ | 6.5$B$+1 | $B$+1 | Zero/zero | $106.77 | 95.4% @ 900W (buck) 95% @ 900W (boost) |

$I_{CC}$: Capacitor charging current.

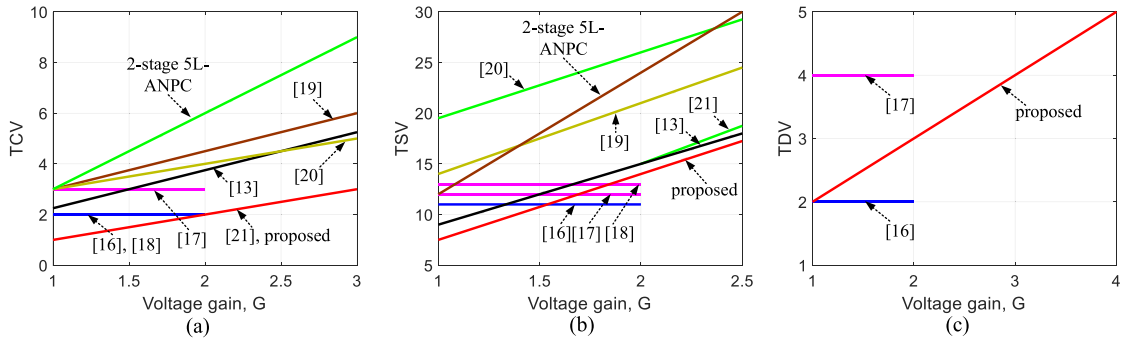


Fig. 9. Comparison between the proposed inverter and others. (a) TCV stress versus voltage gain. (b) TSV stress versus voltage gain. (c) TDV stress versus voltage gain.

(TCV) stress, total switch voltage (TSV) stress, total diode voltage (TDV) stress. The parameters are defined as follows:

$$\begin{cases} \text{TCV} = \frac{1}{V_{\text{dc}}} \sum_{i=1}^{C} V_{C,i};\ \text{TSV} = \frac{1}{V_{\text{dc}}} \sum_{j=1}^{S} V_{\text{SW},j}; \\ \text{TDV} = \frac{1}{V_{\text{dc}}} \sum_{k=1}^{D} V_{\text{diode},k} \end{cases}. \quad (23)$$

Fig. 9 presents comparison results about TCV, TSV, TDV between the proposed inverter and others. It should be noted that modulation index $M$ of the works [21], two-stage 5L-ANPC, and the proposed inverter is maximized to be 1 in these comparisons because $M$ and duty ratios of boost circuit are uncoupled. It can be seen that the inverters in [16], [17], and [18] have larger TCV than the proposed inverter and [21] in the range $G < 2$ because they have constant boost factor as 2 whereas the boost factor of the proposed inverter and [21] are $B = G/M = G$. Assume that the inverters in [13], [19], [20], and [21], two-stage 5L-ANPC, and the proposed inverter operate with the same value of $G$, the works in [13], [19], and [20] have boost factor of $B = G/M$ whereas the boost factor of the two-stage 5L-ANPC is $B = 2G/M = 2G$. As shown in Table II, the modulation index $M$ of [13], [19], [20] is smaller than 1 because $1 > D \geq 2M$-1 and $1 > D \geq M$. As a result, [13], [19], [20], and the two-stage 5L-ANPC have larger boost factor and TCV than the proposed inverter and [21]. Similarly, the proposed inverter also has better TSV than [13], [19], [20], [21], two-stage 5L-ANPC, as shown in Fig. 9(b). In the rage $G < 1.5$ and $G > 2$, the proposed inverter also has smallest TSV compared to others, as shown in Fig. 9(b). When $1.5 \leq G \leq 2$, the introduced inverter presents moderate value of TSV, which is larger than the works in [16], [17], and [18] and smaller than others. The proposed inverter also introduces moderate value of TDV when comparing with [16] and [17], as shown in Fig. 9(c).

The proposed inverter brings benefit of component voltage rating reduction which leads to reduce the cost of semiconductor devices. In order to highlight this benefit, the cost of the proposed inverter has been compared with the others as follows. Table III shows parameters of MOSFETs and diodes of Onsemi used to design these inverters. The proposed inverter and others are designed to operate with the input voltage varying from 200 to 400 V. The dc-link voltage and output load voltage of the proposed inverter are controlled at 400 V and 220 $V_{\text{RMS}}$, respectively. At 400-V input voltage, the voltage stresses of switch $S_1$ and diode $D_1$ of the proposed inverter reach value 800 V, while the voltage ratings of switches $S_2$–$S_5$ are 400 V and the voltage ratings of switches $S_6$–$S_8$ are 200 V. As a result, switch $S_1$ and diode $D_1$ are selected as 1200 V MOSFET and

TABLE III
UNIT PRICES OF SEMICONDUCTOR DEVICES

| Devices | Unit Price ($) @ www.mouser.com |
|---|---|
| MOSFET (1200 V) Onsemi: UJ3C120080K3S | $19.53 |
| MOSFET (650 V) Onsemi:NTH4L060N065SC1 | $10.19 |
| Diode (1200 V) Onsemi: FFSH30120A-F155 | $15.91 |
| Diode (650 V) Onsemi: FFSH3065B-F085 | $9.98 |

TABLE IV
EXPERIMENTAL PARAMETERS

| Parameters/ Components | | Values |
|---|---|---|
| DC source | $V_{dc}$ | 200–400 V |
| AC output voltage | $V_{O,RMS}$ | 220$V_{RMS}$ |
| Output frequency | $f_O$ | 50 Hz |
| Switching frequency | $f_s$ | 10 kHz |
| Boost inductor | $r_{LB}$, $L_B$ | 0.4 Ω, 3 mH/20 A |
| DC-link capacitors | $r_{ESR}$, $C_1$, $C_2$ | 0.05 Ω, 1 mF/400 V |
| LC filter | $L_f$ and $C_f$ | 3 mH and 10 μF |
| RL load | $R$-$L$ | 76 Ω - 50 mH |
| $S_1$–$S_8$ | C3M0075120D (1200-V, 75-mΩ) | |
| $D_1$ | UJ3D1250K2 (1200-V, 50-A) | |

1200 V diode. While, switches $S_2$–$S_8$ are designed as 650 V MOSFETs. Because the proposed inverter has smaller component voltage ratings than others, the proposed inverter can be designed with fewer 1200 V IGBTs/MOSFETs than others. For example, at 400-V input voltage, the work in [19] has the minimum value of dc-link voltage of 711 V in theory by applying $D = M = 0.4374$. The topology in [19] has six switches blocking dc-link voltage and two switches blocking half of dc-link voltage. As a result, the topology in [19] are designed with six 1200 V switches and two 650 V switches. The same way can be applied to design other topologies. The result is that the proposed inverter uses only one 1200 V MOSFET, while the works in [16], [17], and [18] use four 1200 V switches, the works in [13], [21] use five 1200 V switches, the study in [19] and [20] use six and nine 1200 V switches, respectively. Consequently, the proposed inverter has smallest total cost of semiconductors than others, as shown in Table II.

## VI. POWER LOSS DISTRIBUTION

The system parameters used for power loss estimation are presented in Table IV. The power loss calculations are performed in four cases. In case 1, the input voltage and dc-link voltage are set to 200 and 400 V, the modulation index $M$ and duty ratio $D_N$ are selected as 0.78 and 0.67, respectively. In case 2, the buck mode operation is tested with 400 V input voltage and 400 V dc-link voltage. The values of $M$ and $D_N$ are respectively 0.78 and 0.5. In case 3, dc-link voltage is boosted to 500 from 200 V input voltage, the $M$ and $D_N$ are 0.62 and 0.71. In case 4, 400-V input voltage and 500-V dc-link voltage are adopted with $M = 0.62$ and $D_N = 0.56$. The output load voltage is controlled at 220 $V_{RMS}$, and rated output power of 900 W. The power loss distribution of the 5L-CG-BBI topology at different $M$ and $D_N$ values are illustrated in Fig. 10. The results indicate that the minimum total loss of 22.71 W occurs at case 4, while

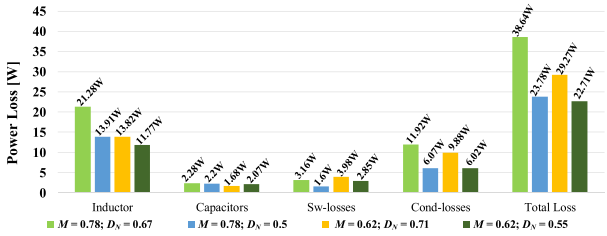


Fig. 10. Power loss distribution under 900-W output power.

the maximum total loss of 38.64 W is observed at case 1. The efficiency of the inverter corresponding four cases are 95.7%, 97.4%, 96.7%, and 97.5%, respectively. It can be observed that the proposed topology achieves relatively high efficiency, ranging from 95.7% to 97.5%. When $D_N$ is set at higher values (0.67–0.71), it leads to a large boost factor $B$ (2–2.5), causing higher current through the inductor. Consequently, inductor loss, and conduction losses of semiconductor devices increase, which reduces the efficiency of the inverter to about 95.7%–96.7%. In contrast, at lower $D_N$ values with a moderate boost factor (1–1.25), the total losses are reduced which allows the higher efficiency of 97.4% and 97.5%. The power losses are mainly concentrated in the inductor, which accounts for approximately 51.8%–55% of the total loss. The conduction losses are around 26.5%–30.8%. Meanwhile, switching losses and the capacitors losses account for the smallest percentages in the total loss.

## VII. EXPERIMENTAL RESULTS AND DISCUSSIONS

The experimental results are conducted in order to validate:
1) the operating of the proposed inverter under buck and boost modes,
2) reactive power capability,
3) capacitor voltage balance capability, and
4) responds of the proposed inverter under varying loads and input voltages with the proposed controllers.

In order to verify buck-boost operation of the proposed inverter, the input voltage is selected in the range from 200 to 400 V. This is the commonly range of input voltage for PV-grid connected applications [3], [4], [18], [21]. Resistive-inductive (RL) loads are adopted to verify the operating of the inverter with reactive power capability. It should be noted that the RL loads are those available in the laboratory. The 30 Ω-50 mH and 76 Ω-50 mH are adopted in experiment. With these values of RL loads, the power factor of the load is 0.886 for 30 Ω-50 mH RL load and 0.98 for 76 Ω-50 mH RL load. Fig. 11 provides an illustration of the experimental setup. Control signals of all switches are created by microcontroller DSP TMS320 F28335. Voltage sensors HV25 and current sensors ACS712 are adopted to measure capacitor voltages, output voltage and current. Parameters of the experiment are listed in Table IV. The low-pass filter (3 mH-10 $\mu$F) designed with a cut-off frequency of 900 Hz is utilized to mitigate high-frequency harmonics of the output voltage/current.

First, the proposed inverter is tested under boost mode with 200 V input voltage. Fig. 12(a)–(f) shows the experimental

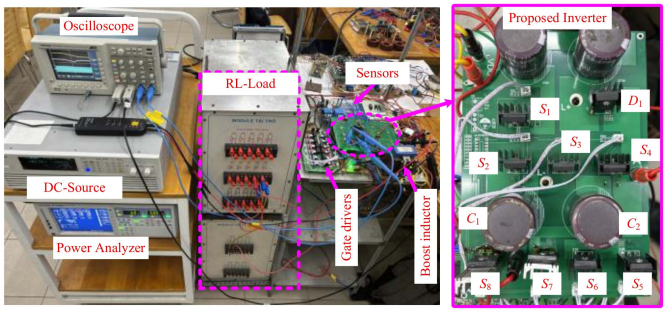


Fig. 11. Experimental setup.

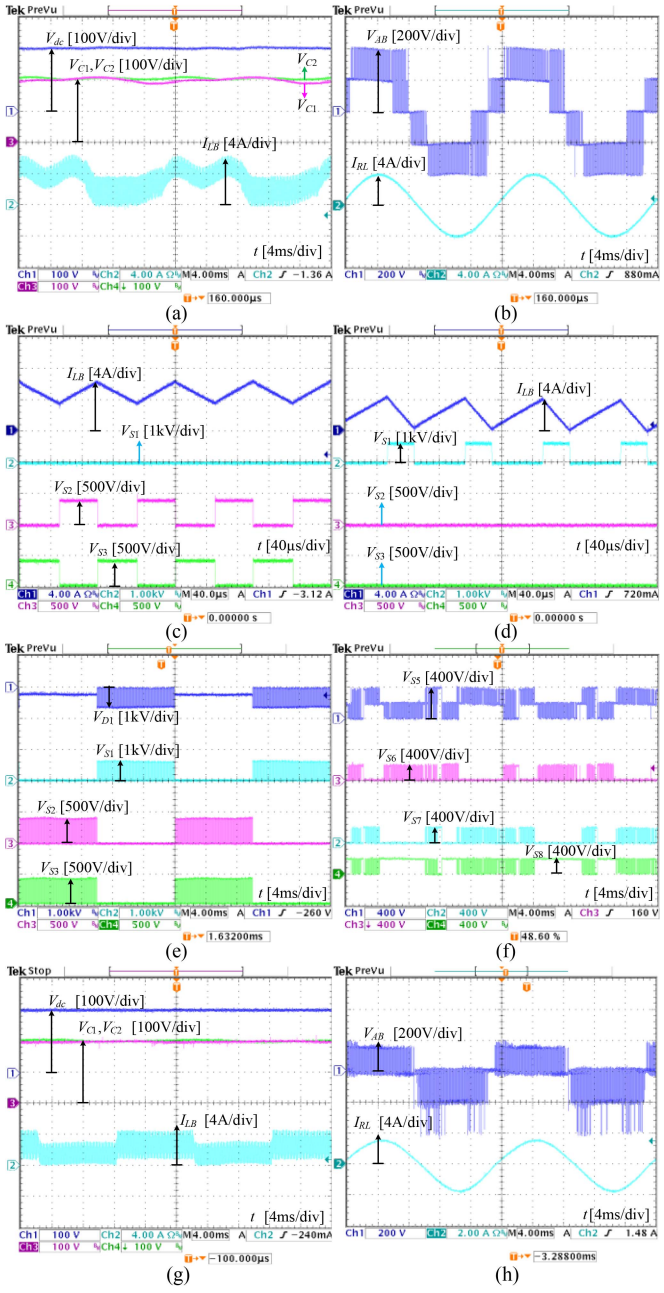


Fig. 12. Experimental results under 200-V input voltage. (a)–(f) $M = 0.78$, $B = 2$, (g), and (h) $M = 0.39$, $B = 2$.

TABLE V
SUMMARY OF EXPERIMENTAL RESULTS

| | $V_{C1}$ | $V_{C2}$ | $V_{O,RMS}$ | $I_{RL,RMS}$ | THD$_{IRL}$ |
|---|---|---|---|---|---|
| $V_{dc} = 200\ V$ | 198 V | 203 V | 217 V | 2.8 A | 2.45% |
| $V_{dc} = 400\ V$ | 203 V | 205 V | 218 V | 2.82 A | 2.22% |

results for boost mode operation. The 76 Ω-50 mH RL load is adopted in this experiment. From 200-V input voltage, capacitor $C_1$ and $C_2$ voltages are boosted to 198 and 203 V, respectively, as shown in Fig. 12(a). The dc-link voltage is approximately 400 V. The two capacitor voltages exhibit a difference of 5 V, which represents 1.25% of the dc-link voltage. The average input inductor current is 3.18 A, the inductor waveform is illustrated in Fig. 12(a). The output voltage $V_{AB}$ has five voltage levels: ±400 V, ±200 V and 0 V, as depicted in Fig. 12(b). The waveform of output load current $I_{RL}$ is sinusoidal. Its rms current value is 2.8 A. As a result, the output load voltage obtains 217 $V_{RMS}$. The THD of output current is 2.45%. The zoom-in waveforms of inductor current, drain-source voltages of $S_1$, $S_2$, and $S_3$ in positive and negative half cycles output voltage $V_{AB}$ are shown in Fig. 12(c) and (d), respectively. In positive half cycle of $V_{AB}$, Fig. 12(c), the inductor $L_B$ stores energy when switch $S_3$ is gated ON. It should be noted that $S_1$ is always gated on during positive half cycle of $V_{AB}$. In negative half cycle of $V_{AB}$, Fig. 12(d), two switches $S_2$ and $S_3$ are both gated ON. The inductor $L_B$ stores energy when switch $S_1$ is triggered ON. The drain-source voltages of switches $S_1$–$S_8$ and anode-cathode voltage of diode $D_1$ are shown in Fig. 12(e) and (f). It shows that the voltage stresses of $D_1$ and $S_1$ are the sum of input voltage and dc-link voltage, which are approximately 600 V. The voltage stresses of $S_2$, $S_3$, and $S_5$ are dc-link voltage, while they are half of dc-link voltage for switches $S_6$, $S_7$, and $S_8$. The proposed inverter is also tested under small modulation index, $M = 0.39$, as shown in Fig. 12(g) and (h). In this case, capacitor voltages are also boosted to 199 and 202 V, respectively. During almost the output voltage cycle, the output voltage $V_{AB}$ has three voltage levels: ±200 and 0 V, as depicted in Fig. 12(h). It is because the inverter operates in sectors I, IV, V, VIII due to a small modulation index ($M < 0.5$). In these sectors, the inverter operates mostly at the medium and zero vectors. The waveform of output load current $I_{RL}$ is sinusoidal. Its rms current value is 1.37 A. As a result, the output load voltage obtains 107 $V_{RMS}$. The THD of output current is 2.78%. The proposed inverter is also tested under buck mode with 400 V input voltage. The experimental results for buck mode are listed in Table V.

Second, the proposed NPV balance scheme has been tested. In order to generate unbalanced capacitor voltage conditions, an additional resistor have been connected to $C_1$ or $C_2$. In case 1, one additional 2-kΩ resistor has been connected in parallel to capacitor $C_2$ to make $V_{C1}$ greater than $V_{C2}$, as shown in Fig. 13(a). When the proposed NPV balanced method is enabled, two capacitor voltages are balanced even though additional resistor is still connected in parallel to $C_2$. In case 2, an additional 2-kΩ resistor is connected in parallel to $C_1$ to generate $V_{C2} > V_{C1}$, as depicted in Fig. 13(b). The voltage difference between two capacitors is also decreased to zero by applying the

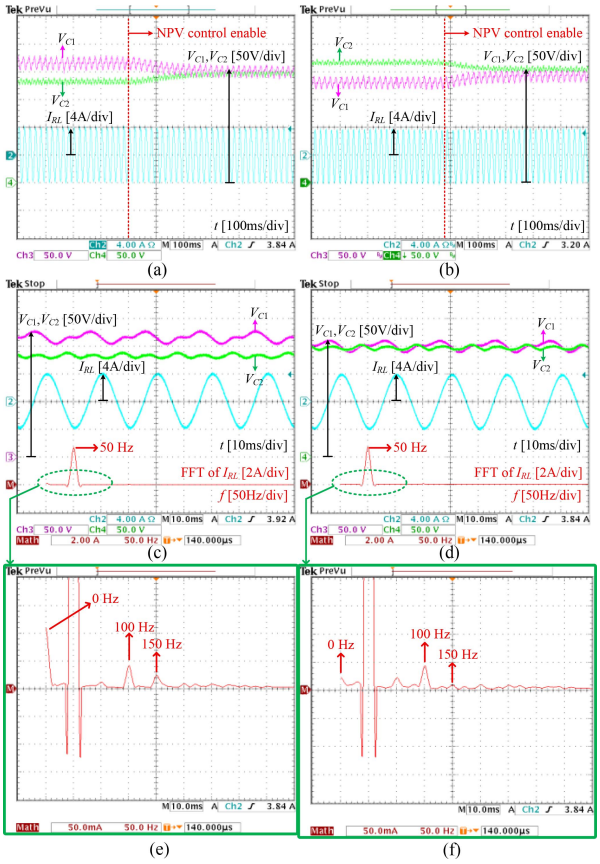


Fig. 13. Experimental results for validating the proposed NPV balance scheme. (a) $V_{C1} > V_{C2}$. (b) $V_{C1} < V_{C2}$. (c), (d) FFT spectra of IRL under unbalanced and balanced NPV, (e), (f) zoom-in waveforms of FFT spectra of $I_{RL}$.

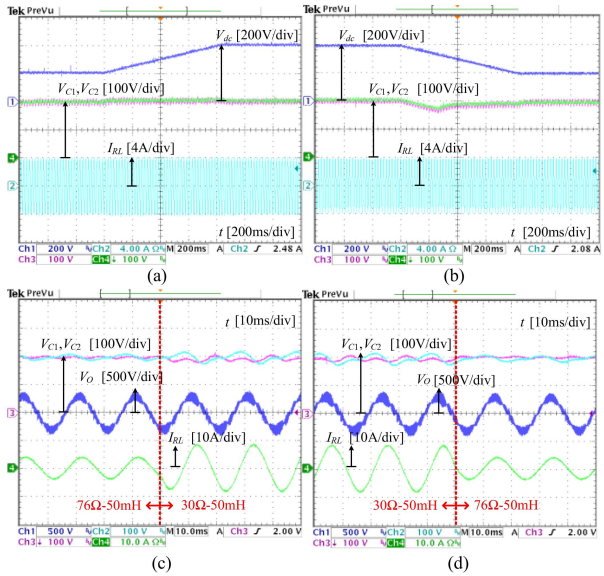


Fig. 14. Experimental results under (a) and (b) variation of input voltage, and (c) and (d) variation of output load.

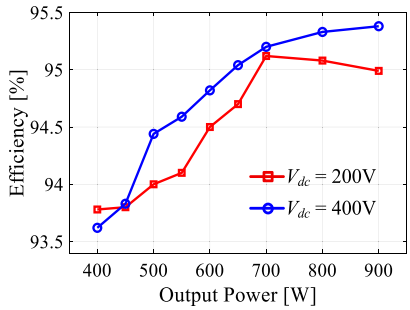


Fig. 15. Efficiency of the proposed inverter.

proposed method, as illustrated in Fig. 13(b). Fig. 13(c) and (d) shows the waveforms of capacitor voltages, output current and its FFT spectra under unbalanced and balanced NPV. Fig. 13(c) shows that unbalanced NPV condition generates high amplitude harmonics at 0, 100, and 150 Hz of output current. However, the proposed method helps to balance capacitor voltages and reduce amplitude of harmonics of output current, as shown in Fig. 13(d). These results demonstrate the effectiveness of the proposed NPV balance scheme.

Fig. 14 illustrates the experimental results for both dc-link voltage regulation and ac output voltage control. First, the proposed closed-loop controllers are tested under variation of input source. The $V_{\rm dc}$ changes from 200 to 400 V in Fig. 14(a) and from 400 to 200 V in Fig. 14(b). In both cases, two capacitor voltages are controlled at 200 V with small undershoot, which ensures 400 V of dc-link voltage. The ac output voltage is controlled at 220 $V_{\rm RMS}$, approximately, which generates 2.8 $A_{\rm RMS}$ of output current, as shown in Fig. 14(a) and (b). Next, the proposed controllers are also tested under change of load. In Fig. 14(c), the output load is changed from 76 Ω-50 mH to 30 Ω-50 mH, the output load current is increased. However, the capacitor voltages and output load voltage are still maintained as 200 V and 220 $V_{\rm RMS}$. Similarly, the change of load from 30 Ω-50 mH to 76 Ω-50 mH does not affect the dc-link voltage and ac output load voltage with the help of the proposed controllers.

The efficiency of the proposed inverter has been measured with the help of power analyzer Yokogawa WT3000E. The results of efficiency are drawn in Fig. 15. The inverter's efficiency is measured under 200 and 400 V of input voltage. An increase in input voltage leads to higher efficiency, which results from the decrease in input current. It results in reducing conduction losses of the inverter. At 900 W of output power, the proposed inverter obtains 95.4% at 400 V of $V_{\rm dc}$ and 95% at 200 V of $V_{\rm dc}$, as shown in Fig. 15.

## VIII. Conclusion

This article has presented a new topology of 5L-CG-BBI, which can obtain some advantages as:

1) completely eliminates CMV by adopting CG feature,
2) balances NPV, and
3) two-stage power conversion enabling both step-up and step-down control of the ac output voltage.

The SVM method has been presented to control the proposed inverter. The medium vectors and large vectors have been appropriately selected in the switching sequence to balance NPV. In this topology, the dc–dc stage and dc–ac stage have been controlled separately. As a result, the modulation index of the dc–ac stage can be maximized to 1 in theory, which

helps to reduce component voltage ratings compared to existing CG inverters. The comparative analysis and experimental setup have been presented to demonstrate the benefits and verify the operating of the proposed inverter. To summarize, the introduced inverter is suitable for grid-connected PV systems.

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