A Family of Symmetrical Integrated Synchronizations for Grid-Following and Grid-Forming Inverters

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***Abstract*—Grid-following and grid-forming inverters are usually synchronized with the phase-locked loop and the power synchronization control, respectively, and they exhibit complementary characteristics in the grid strength adaptability. How to make the best of two synchronization approaches and endow the system with superior grid strength adaptivity and transient stability remains a significant yet unsolved challenge. Based on their structural similarity and duality, this article proposes a family of novel integrated synchronizations, which are in a symmetric and elegant form. The interaction between the integrated synchronization and other control parts is described by evolving the complex system into a simple single-input-single-output model. On its basis, comprehensive small-signal and transient stability analysis reveals that the proposed synchronization methods can ensure the robust operation of inverters and enhance their tolerance to severe faults.**

***Index Terms*—Grid-following (GFL), grid-forming (GFM), robustness, stability, synchronization.**

I. Introduction

ELECTRICAL power systems are transitioning from large-scale, fossil fuel-based synchronous generators (SGs) to inverter-interfaced renewables [1], [2]. Nowadays, the majority of grid-interfacing inverters employ the grid-following (GFL) control, which follows the grid voltage and frequency via a phase-locked loop (PLL). Its stable operation relies on a stiff power grid [3]. With the increasing penetration of renewables, the grid strength is inevitably weakened. This makes the grid-forming (GFM) inverter, which self-synchronizes and flexibly creates a stable ac voltage, envisioned to be the cornerstone of future power systems [4], [5], [6].

Along with flexible behaviors dominated by control algorithms, they impose new sets of dynamics which may induce instability under severe grid conditions [7], [8], [9]. An intriguing finding is drawn that, although the dynamics of GFL and GFM inverters are irrelevant, they have complementary characteristics in the grid strength adaptability. Specifically, GFL inverters are vulnerable to a weak grid [10], whereas GFM inverters are vulnerable to a stiff grid [11].

Focusing on the instability mechanism and stability enhancement, extensive studies have been performed separately on GFL or GFM inverters [12], [13], [14]. It reveals that the PLL introduces negative damping, which interacts with the power grid. This interaction becomes obvious when grid impedance increases [15], [16]. Such interaction is exactly the root cause of oscillation in the GFL inverter under weak grid conditions [16]. As for the GFM inverter, the dominant part for its instability issue under stiff grid conditions is the power synchronization control (PSC), which also introduces negative damping and interacts with the power grid [17]. These limitations of PLL and PSC constrain the safe and reliable operation of modern power systems. Associate incidents, such as the oscillation witnessed at the wind farms in the Electric Reliability Council of Texas, USA [14], and Hami, Xinjiang, China [15], have been frequently reported. It is, thus, urgent and critically important to develop improved synchronization schemes with enhanced small-signal and transient stability.

Considering their complementary grid strength adaptability, Liu and Wang [18] directly add the PLL into the PSC-based GFM inverter. The added PLL essentially acts to emulate the damper winding of SGs and thus improves system stability. In addition to simply superposing PLL and PSC, a few researchers have devoted themselves to further revealing their potential relations, intriguing dualities, or similarities. Zhong and Boroyevich revealed the structural resemblance between PLL and PSC in 2016 [19]. Furthermore, Harnefors et al. pointed out that the typical GFL and GFM inverters have structural similarities in their control units, not only limited to synchronization parts

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[20]. Later, by revisiting the characteristics of GFL and GFM inverters, Green et al. revealed their duality in [21]. These findings bridge the gap between the two basic inverter types and are stimulating further integration. Jiang et al. [22] recently proposed the current-synchronization control for GFM inverters, which is compatible with the direct current limiter, operates as a PSC under normal conditions to provide synthetic inertia, and behaves as a PLL during severe grid faults with enhanced synchronization stability. Through proper integration, it is expected to make the best of PLL and PSC. However, the research on the control integration is still in its infancy, and the integration mechanism remains unclear.

Motivated by the challenges and building upon prior research on the connection between PLL and PSC, this article is devoted to exploring their further integration and proposes a family of integrated synchronization strategies for GFL and GFM inverters, achieving improved synchronization stability. The main contributions of this work are summarized in the following.

1) Leveraging the duality of PLL and PSC, a family of symmetrical integrated synchronizations is proposed, including current-based, voltage-based, and power-based types. It enables robust control without altering control parameters or detecting the grid strength.
2) By analyzing interaction characteristics between the synchronization and the other parts, the proposed synchronization strategies are proven to provide phase compensation, rendering inverters operate stably even under ultraweak and ultrastiff grid conditions.
3) A comprehensive transient stability analysis is conducted for inverters employing the proposed methods. Suitable current limiter designs are also discussed to enhance system fault ride-through capability and transient performance.

The rest of this article is organized as follows. Section II proposes the symmetrical integrated synchronization based on duality properties. Section III presents the SISO model, and Section IV studies the small-signal grid-synchronization stability and transient behaviours. Section V provides experimental verification. Finally, Section VI concludes this article.

II. Duality-Based Symmetrical Integrated Synchronizations for GFL and GFM Inverters

A. System Description of GFL and GFM Inverters

Fig. 1 depicts the typical configurations of GFL and GFM inverters, where V_{dc} and $\boldsymbol{v}_g$ represent the dc-side voltage and the grid voltage, respectively. The inductor L_f and the capacitor C_f form the LC filter. L_{T} represents the transformer inductance. The power grid is modeled as an ideal voltage source v_g in series with grid impedance. To present the worst case, a pure inductance L_g is considered here.

Basically, GFL inverters inject current into an existing grid voltage to which it synchronizes (typically using a PLL), while GFM inverters form a voltage-source grid from which current flows out. In essence, the GFL inverter acts as a constant internal current source in parallel with the inverter output admittance in the subtransient timeframe, whereas the GFM inverter behaves as a constant internal voltage source in series with the output impedance in the subtransient timeframe [23], as illustrated in Fig. 2.

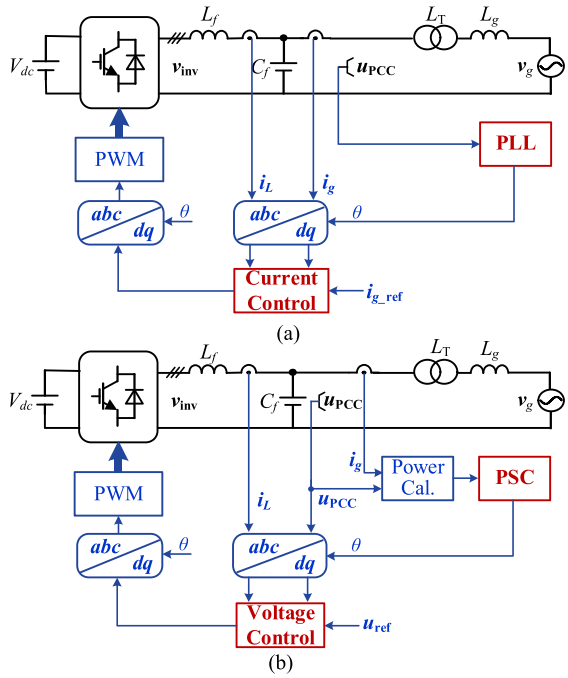

Fig. 1. Typical inverter configurations in synchronous dq frame. (a) GFL inverters with the PLL. (b) GFM inverters with the PSC.

There are many variations of both GFM and GFL control. The widely used current control and PLL structures in GFL inverters are shown in Fig. 2(a). The current controller G_i ensures accurate tracking of the reference i_{g_ref}. Decoupling of current loops is achieved via the feedforward with the gain of $\omega_n L_f$, while the capacitor current feedback with the gain of G_{ad} provides active damping [24]. Fig. 2(b) presents the typical control structure for a GFM inverter, featuring dual-loop voltage control with an outer voltage loop that generates the reference for the inner current loop. Voltage reference and frequency are typically set by Q-u and P-ω droop, respectively. Additional feedforward and compensation terms—such as voltage feedforward, current decoupling, and filter capacitor current compensation [25]—may also be included.

B. Duality of PLL and PSC

As shown in Fig. 2(a), the phase angle is estimated by regulating u_{q} to $u_{\mathrm{q\_ref}} = 0$ via the regulator $G_{\mathrm{uq}}(\mathrm{s})$ in PLL, yielding the synchronization dynamics shown as follows:

$$\widetilde{\theta}_{\mathrm{PLL}} = \widetilde{u}_{\mathrm{q}} G_{\mathrm{uq}}/s \tag{1}$$

where values with the tilde symbol "$\sim$" represent perturbed values.

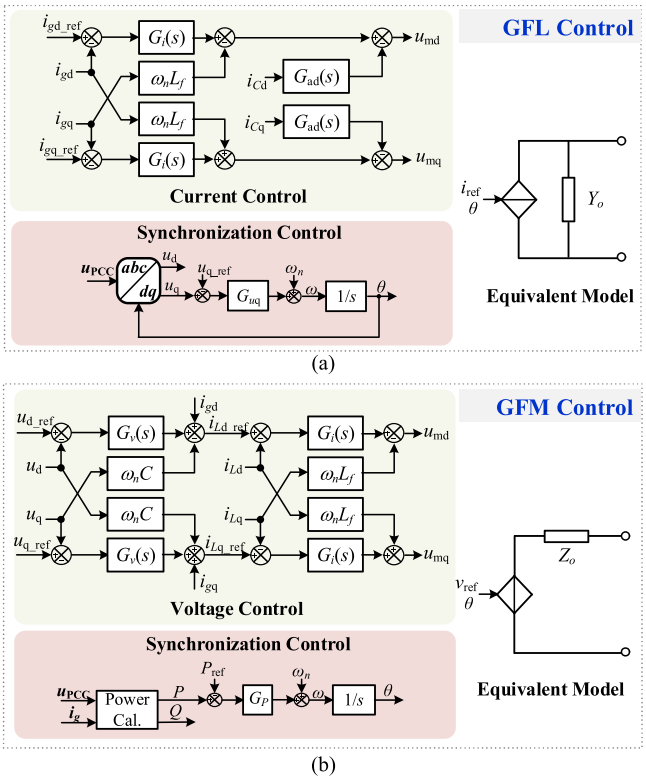

Fig. 2. Control structure and equivalent model of (a) GFL control and (b) GFM control.

We recall that $Q = 1.5(u_{\mathrm{q}}i_{\mathrm{gd}} - u_{\mathrm{d}}i_{\mathrm{gq}})$, impose perturbations to each variable in this equation and neglect high-order small-signal terms, yielding

$$\tilde{Q} \approx 1.5(\underbrace{I_{\mathrm{gd}}\tilde{u}_{\mathrm{q}}}_{(1)} + \underbrace{U_{\mathrm{q}}\tilde{i}_{\mathrm{gd}}}_{(2)} - \underbrace{U_{\mathrm{d}}\tilde{i}_{\mathrm{gq}}}_{(3)} - \underbrace{I_{\mathrm{gq}}\tilde{u}_{\mathrm{d}}}_{(4)}). \tag{2}$$

The reactive power perturbation consists of four terms, each representing a perturbation in either voltage or current multiplied by its corresponding steady-state value. Given that $U_{\mathrm{q}} = u_{\mathrm{q\_ref}} = 0$, the second term can be neglected. Considering that the bandwidth of the inner current loop is usually designed much higher than that of the outer loops [26], the current can be assumed to accurately track its reference, allowing the current disturbance—and thus the third term— to be ignored. Moreover, the fourth term can be approximately zero under certain conditions, such as when the q-axis current reference is set to be zero (which is common in GFL inverters with MPPT), or when an outer loop adjusts the current reference toward zero under stiff grid conditions (i.e., $I_{\mathrm{gq}} = i_{\mathrm{gq\_ref}} \approx 0$). Under these assumptions, (1) can be approximated as follows:

$$\widetilde{\theta}_{\mathrm{PLL}} \approx \frac{\widetilde{Q}}{1.5I_{\mathrm{gd}}} \cdot \frac{G_{uq}}{s} \tag{3}$$

and the u_{q}-based PLL can evolve into the Q-ω droop in the GFL inverter, as shown in Fig. 3(a1)–(a3). The well-known PSC is based on P-ω droop, as shown in Fig. 3(b). Comparing Fig. 3(a3) and (b), the variants of PLL and PSC exhibit duality. Note that this is only valid within the current-loop bandwidth and with a zero reference for the q-axis current.

Besides the abovementioned variants of PLL, the duality can also be observed from the variants of PSC in the GFM inverter. The PSC regulates the active power via the P-ω droop, as illustrated in Fig. 2(b). The synchronization dynamics are expressed as follows:

$$\widetilde{\theta}_{\mathrm{PSC}} = \widetilde{P} \cdot G_P \Big/ s. \tag{4}$$

Similarly, recalling $P = 1.5(u_{\mathrm{d}}i_{\mathrm{gd}} + u_{\mathrm{q}}i_{gq})$, the active power perturbation is given by

$$\tilde{P} \approx 1.5(\underbrace{U_{\mathrm{d}}\tilde{i}_{\mathrm{gd}}}_{(1)} + \underbrace{I_{\mathrm{gd}}\tilde{u}_{\mathrm{d}}}_{(2)} + \underbrace{U_{\mathrm{q}}\tilde{i}_{gq}}_{(3)} + \underbrace{I_{\mathrm{gq}}\tilde{u}_{\mathrm{q}}}_{(4)}). \tag{5}$$

In the GFM control, the inner voltage loop has a much higher bandwidth than the outer loops. Thus, while studying synchronization dynamics, the voltage can be assumed to accurately track its reference, i.e., $U_{\mathrm{d}} = E_{\mathrm{ref}}$ and $U_{\mathrm{q}} = 0$. This allows the third term to be neglected, and voltage disturbances can be omitted, leading to the omission of the second and fourth terms as well. Then the synchronization dynamics are dominated by the d-axis current disturbance, i.e.,

$$\widetilde{\theta}_{\mathrm{PSC}} = 1.5E_{\mathrm{ref}}\widetilde{i}_{\mathrm{gd}} \cdot G_P \Big/ s. \tag{6}$$

Thus, the P-ω droop can be regarded as i_{d}-based PLL in the GFM inverter, as shown in Fig. 4(a1)–(a3), dual to the u_{q}-based PLL shown in Fig. 4(b). Note that this is only valid within the voltage-loop bandwidth of the GFM inverter and with a zero reference for q-axis voltage.

C. Duality-Based Integrated Synchronizations

As mentioned, PLL and PSC endow inverters with complementary grid strength adaptability. A natural idea is to integrate them so as to harvest the robustness against variable grid strength. Motivated by this idea and inspired by the duality of PSC and PLL, the integrated synchronization is proposed.

As reported in Section II-B, the PLL can equivalently evolve into the Q-ω droop control. Naturally, integrating it with the PSC (i.e., P-ω droop) yields the power-based integrated synchronization shown in Fig. 5(a), where $G_P(s)$ and $G_Q(s)$ are the gains of the P-ω and Q-ω droop loops, respectively. Following the similar transformation procedure in Section II-B, we can also derive variant forms of the power-based symmetrical integrated synchronization, as shown in Fig. 5(b) and (c), named as the voltage-based integrated synchronization and the current-based integrated synchronization, respectively. These three types are in a symmetric and elegant form.

Different from the conventional PLL, which regulates u_{q} to $u_{\mathrm{q\_ref}} = 0$ in GFL inverters, the proposed voltage-based integrated synchronization regulates the d-axis and q-axis components of the PCC voltage to $u_{\mathrm{d\_ref}} = U_{\mathrm{PCC}}$ and $u_{\mathrm{q\_ref}} = 0$ simultaneously. At the steady state, the d-axis of the rotating dq frame aligns with the vector $\boldsymbol{u}_{\mathbf{PCC}}$, as shown in Fig. 6. Assuming a small disturbance causing $\boldsymbol{u}_{\mathbf{PCC}}$ behind the d-axis,

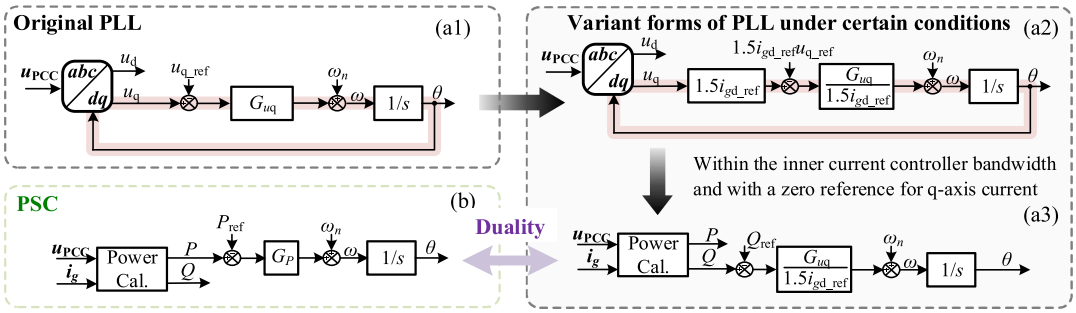

Fig. 3. Variant forms of PLL in the GFL inverter. (a) Original PLL and its variant forms. (b) Representation of its duality with PSC.

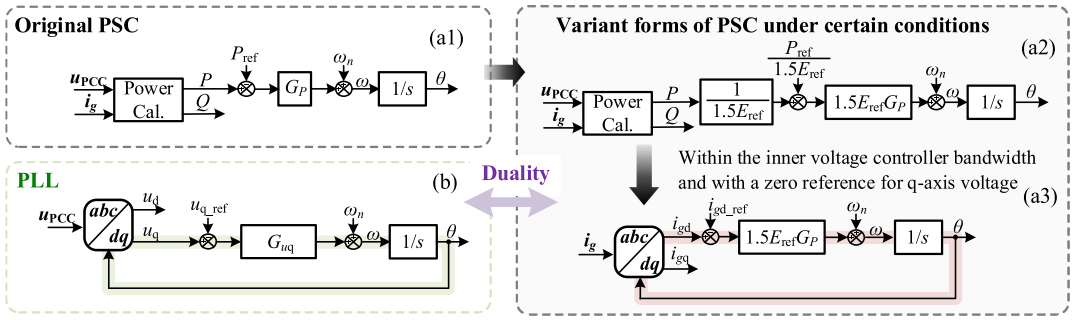

Fig. 4. Variant forms of PSC in the GFM inverter. (a) Original PSC and its variant forms. (b) Representation of its duality with PLL.

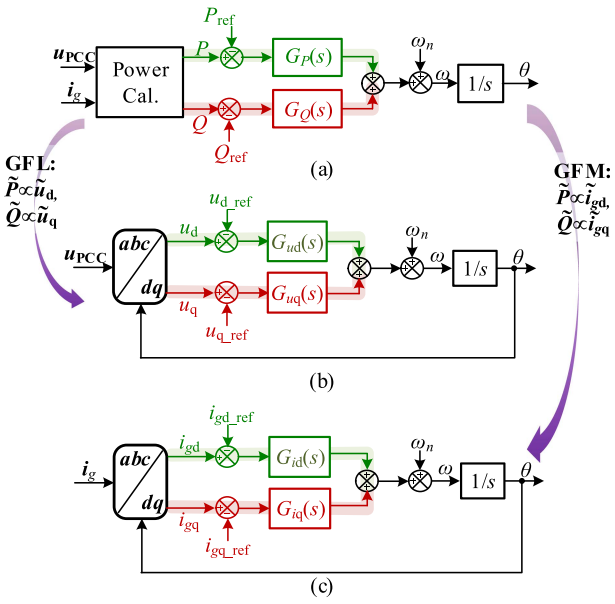

Fig. 5. Integrated synchronizations. (a) Power-based integrated synchronization. (b) Voltage-based integrated synchronization. (c) Current-based integrated synchronization.

the synchronization control will push ω to decrease, which decelerates the rotating dq frame and makes it aligned with $\boldsymbol{u}_{\mathbf{PCC}}$ again.

The conventional PSC in GFM inverters regulates P to its reference P_{ref}, thereby determining the corresponding phase angle of the rotating dq frame. Given that the time scale of the inner voltage control loop is far smaller than that of the outer power control loops, we can assume that u_{d} and u_{q} have already reached their references. By setting $u_{\mathrm{d\_ref}} = E_{\mathrm{ref}}$ and $u_{\mathrm{q\_ref}} = 0$ as an illustrative example, and based on $P = 1.5(u_{\mathrm{d}} i_{\mathrm{gd}} + u_{\mathrm{q}} i_{\mathrm{gq}})$ and $Q = 1.5(u_{\mathrm{q}} i_{\mathrm{gd}} - u_{\mathrm{d}} i_{\mathrm{gq}})$, the steady-state d-axis and q-axis components of the grid current can be derived as follows:

$$i_{\mathrm{gd}} = P_{\mathrm{ref}}/(1.5E_{\mathrm{ref}}) \tag{7}$$

$$i_{\mathrm{gq}} = -Q_{\mathrm{ref}}/(1.5E_{\mathrm{ref}}). \tag{8}$$

In the current-based integrated synchronization, i_{gd} and i_{gq} are directly regulated to reach the results shown in (7) and (8). Consequently, at the steady state, the rotating dq frame is consistent with the conventional PSC-based dq frame, as shown in Fig. 7. Consider a small disturbance that causes the current vector $\boldsymbol{i}_{\boldsymbol{g}}$ to deviate from its reference vector. In this scenario, the synchronization responds to tune the rotating angular frequency of the dq-frame and ultimately realigns the current components with their respective references.

Therefore, compared with the conventional PLL or PSC, the proposed voltage-based and current-based integrated synchronizations yield the identical dq-frame phase angle at the steady state; Meanwhile, these methods decompose the control variable into two separate variables, introducing an additional degree of freedom. Thereby, the system stability performance can be enhanced without losing the synchronization accuracy. To maintain control simplicity, the controller form of the added control loops employs a simple proportional controller.

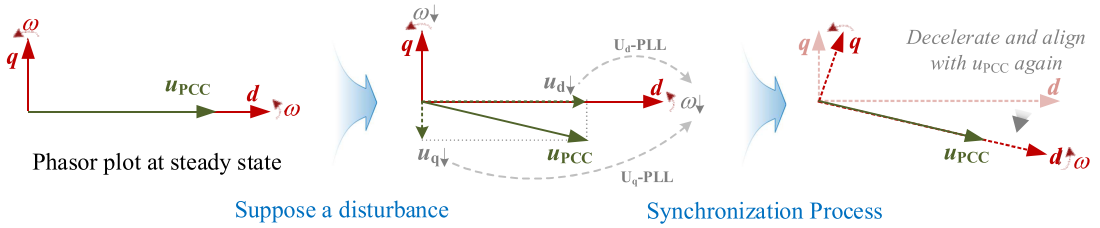

Fig. 6. Synchronization principle of the voltage-based integrated synchronization method for GFL inverters.

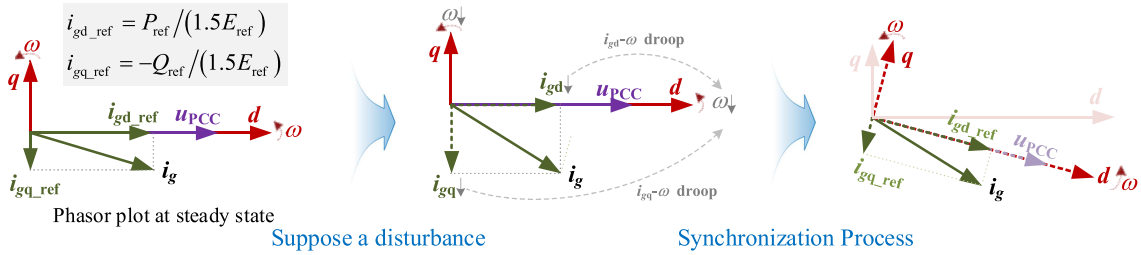

Fig. 7. Synchronization principle of the current-based integrated synchronization method for GFM inverters.

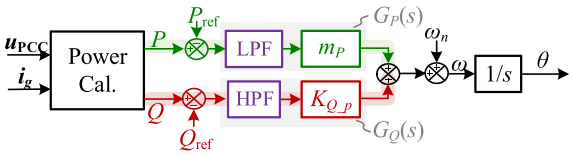

Fig. 8. Detailed control block of power-based integrated synchronization for GFM inverters.

Depending on the inverters' application and function configuration, these three types of integrated synchronization have different priorities. For example, if the inverter is expected to possess both GFL and GFM modes, the power-based integrated synchronization is preferred owing to its compatibility. Otherwise, the voltage-based or current-based integrated synchronization may be preferred, avoiding the power calculation part.

Remark 1: In the power-based integrated synchronization, to avoid the unwanted influence of the Q-θ path on the droop characteristics, a high-pass filter (HPF) is embedded in $G_{\mathrm{Q}}(s)$ to block the component at 0 Hz and eliminate the resulting power bias. The HPF-based path functions similarly to a virtual inductance. Furthermore, a low-pass filter (LPF) is usually added to the P-ω droop to emulate virtual inertia. These modifications result in the updated power-based integrated synchronization depicted in Fig. 8. The cutoff frequency of the HPF is suggested to set as 2 Hz, so that it nearly does not affect the possible stability enhancement in the sub-/super-synchronization frequency bands, and the dc gain of the HPF should be adaptively adjusted based on the estimated line's R/X in scenarios with complex line characteristics.

Remark 2: To prevent conflicts between synchronization and control loops, the inner and synchronization loops must control different electrical variables, and the inner loop bandwidth should be much higher than that of the outer loop to reduce their dynamic coupling.

III. Small-Signal SISO Modeling of Inverters With Integrated Synchronizations

Different from the conventional MIMO model, we take the phase angle as the output. The decoupled SISO model is built via proper coordinate transformation and transfer function rearrangement in this section, allowing for an intuitive analysis of its interaction with other control blocks.

Since the small-signal synchronization stability entails the ability to maintain grid synchronism under small perturbations, we linearize system dynamics around an equilibrium point, where the equivalent transformation shown in Fig. 5 is valid. Consequently, GFL inverters with the power-based and voltage-based integrated synchronization share identical linearized models, as do GFM inverters with the power-based and current-based integrated synchronizations. For clearer comparison with the conventional u_{q}-PLL and P-ω droop methods, we specifically model: (1) GFL inverters with the voltage-based integrated synchronization, and (2) GFM inverters with the power-based integrated synchronization.

A. SISO Model of GFL Inverters With Voltage-Based Integrated Synchronization

Based on Fig. 2(a), the inverter bridge voltage $\boldsymbol{v}_{\mathbf{inv}}$ is

$$\boldsymbol{v}_{\mathrm{inv}} = K_{\mathrm{PWM}} G_{\mathrm{d}}(s) \cdot [G_i(s)(\boldsymbol{i}_{g\_\mathrm{ref}} - \boldsymbol{i}_g) - G_{\mathrm{ad}}(s)\boldsymbol{i}_c + \frac{j\omega_n L_f}{K_{\mathrm{PWM}}}\boldsymbol{i}_g] \tag{9}$$

and the dynamics of the LC filter are represented as follows:

$$\boldsymbol{v}_{\mathrm{inv}} - \boldsymbol{u}_{\mathrm{PCC}} = (sL_f + j\omega L_f)\boldsymbol{i}_L \tag{10}$$

$$\boldsymbol{i}_L - \boldsymbol{i}_g = (sC_f + j\omega C_f)\boldsymbol{u}_{\mathrm{PCC}}. \tag{11}$$

Therein, $K_{\mathrm{PWM}} = V_{dc}/(2V_{\mathrm{tri}})$ is the PWM gain with V_{tri} being the magnitude of the triangular carrier, and $G_{\mathrm{d}}(s) = e^{-1.5sTs}$ is the control delay. ω is the angular frequency of the inverter's rotating dq-frame, and ω_n is its nominal value.

By imposing a small-signal disturbance to ω and state variables in Fig. 1, we have

$$\omega = \omega_n + \tilde{\omega}, x = X + \tilde{x} \tag{12}$$

where ω_n and X are the nominal values, and the values with the tilde symbol "$\sim$" present perturbed values. Combining (10)–(12) yields (13)

$$\begin{aligned}\tilde{v}_{\mathrm{inv}} = (sL_f + j\omega_n L_f)\left[(sC_f + j\omega_n C_f)\tilde{u}_{\mathrm{PCC}} + j\tilde{\omega}C_f U_{\mathrm{PCC}} + \tilde{i}_g\right] \\ + j\tilde{\omega}L_f[(sC_f + j\omega_n C_f)U_{\mathrm{PCC}} + I_g] + \tilde{u}_{\mathrm{PCC}}.\end{aligned} \tag{13}$$

With the reference calculation unit, $\boldsymbol{i_{g\_ref}}$ is expressed as follows:

$$\begin{bmatrix} i_{\mathrm{gd\_ref}} \\ i_{\mathrm{gq\_ref}} \end{bmatrix} = \begin{bmatrix} G_{\mathrm{dref}}(s)(P_{\mathrm{ref}} - P) \\ G_{\mathrm{qref}}(s)(u_{\mathrm{d}} - E_{\mathrm{ref}}) \end{bmatrix}. \tag{14}$$

Imposing perturbations to the state variables in (14) yields

$$\begin{aligned}\begin{bmatrix} \tilde{i}_{\mathrm{gd\_ref}} \\ \tilde{i}_{\mathrm{gq\_ref}} \end{bmatrix} = \begin{bmatrix} -1.5I_{\mathrm{gd}}G_{\mathrm{dref}}(s) & -1.5I_{\mathrm{gq}}G_{\mathrm{dref}}(s) \\ G_{\mathrm{qref}}(s) & 0 \end{bmatrix} \begin{bmatrix} \tilde{u}_{\mathrm{d}} \\ \tilde{u}_{\mathrm{q}} \end{bmatrix} \\ + \begin{bmatrix} -1.5U_{\mathrm{d}}G_{\mathrm{dref}}(s) & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_{\mathrm{gd}} \\ \tilde{i}_{\mathrm{gq}} \end{bmatrix}.\end{aligned} \tag{15}$$

Imposing perturbations to state variables in (9), combining (13) and (15), gives

$$\boldsymbol{A}\begin{bmatrix} \tilde{u}_{\mathrm{d}} \\ \tilde{u}_{\mathrm{q}} \end{bmatrix} = \boldsymbol{B}\begin{bmatrix} \tilde{i}_{\mathrm{gd}} \\ \tilde{i}_{\mathrm{gq}} \end{bmatrix} \tag{16}$$

and the output admittance, denoted as $\boldsymbol{Y_{GFL}}$, is written as follows:

$$\boldsymbol{Y}_{\mathrm{GFL}} = \begin{bmatrix} \tilde{i}_{\mathrm{gd}} \\ \tilde{i}_{\mathrm{gq}} \end{bmatrix} \begin{bmatrix} \tilde{u}_{\mathrm{d}} \\ \tilde{u}_{\mathrm{q}} \end{bmatrix}^{-1} = \boldsymbol{B}^{-1}\boldsymbol{A} \tag{17}$$

where the simplified expressions of the matrices $\boldsymbol{A}$ and $\boldsymbol{B}$ are given in the Appendix, as shown in (A1) and (A2).

Recalling Fig. 1, the relation of $\boldsymbol{u_{PCC}}$ and $\boldsymbol{v_g}$ is given by

$$\boldsymbol{u_{PCC}} - \boldsymbol{v_g} = (R_g + sL_g + j\omega L_g)\boldsymbol{Y_{GFL}}\boldsymbol{u_{PCC}}. \tag{18}$$

Note that the model is built in the inverter's own rotating dq-frame, so that the synchronization dynamics should be considered to transform the grid voltage into the rotating dq-frame. Perform linearization to the grid voltage $\boldsymbol{v_g}$, giving

$$\boldsymbol{v_g} = V_g e^{-j\delta} \Rightarrow \begin{bmatrix} \tilde{v}_{\mathrm{gd}} \\ \tilde{v}_{\mathrm{gq}} \end{bmatrix} = \begin{bmatrix} -V_g \sin\delta_0 \\ -V_g \cos\delta_0 \end{bmatrix} \tilde{\delta}. \tag{19}$$

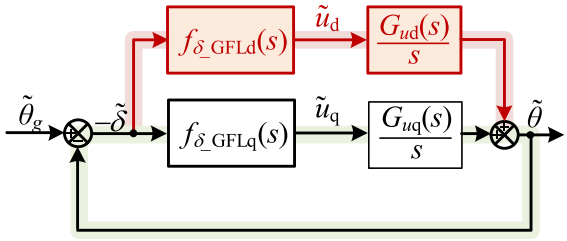

Fig. 9. Closed-loop SISO model of the GFL inverter with voltage-based integrated synchronization.

where δ_0 and $\tilde{\delta}$ are the nominal and perturbed values of the power angle δ, respectively. The power angle δ is the phase angle between the inverter's dq frame and the grid voltage, also called "load angle," expressed as $\delta = \theta - \theta_g$.

Imposing small-signal perturbations to ω, $\boldsymbol{u_{PCC}}$, and $\boldsymbol{v_g}$ in (18), and substituting (17) and (19) into it, yields (20) shown at the bottom of this page. From (20), the d-axis and q-axis components of $\boldsymbol{u_{PCC}}$ can be expressed as follows:

$$\begin{cases} \tilde{u}_{\mathrm{d}} \approx [1 \quad 0]\boldsymbol{F_{\delta\_GFL}}(\boldsymbol{s}) \cdot (-\tilde{\delta}) \triangleq f_{\boldsymbol{\delta\_GFLd}}(\boldsymbol{s}) \cdot (-\tilde{\delta}) \\ \tilde{u}_{\mathrm{q}} \approx [0 \quad 1]\boldsymbol{F_{\delta\_GFL}}(\boldsymbol{s}) \cdot (-\tilde{\delta}) \triangleq f_{\boldsymbol{\delta\_GFLq}}(\boldsymbol{s}) \cdot (-\tilde{\delta}) \end{cases} \tag{21}$$

where $f_{\delta\_\mathrm{GFLd}}(s)$ and $f_{\delta\_\mathrm{GFLq}}(s)$ denote the angle-input-voltage-output (AIVO) functions in d-axis and q-axis frames, respectively.

With the voltage-based integrated synchronization shown in Fig. 5(b), $\tilde{\theta}$ can be expressed as follows:

$$\tilde{\theta} = \frac{G_{uq}(s)}{s}\tilde{u}_{\mathrm{q}} + \frac{G_{ud}(s)}{s}\tilde{u}_{\mathrm{d}}. \tag{22}$$

Combining (21) and (22) gives the closed-loop diagram shown in Fig. 9. The corresponding open-loop transfer function $L_{\mathrm{GFL}}(s)$ and closed-loop transfer function $\Phi_{\mathrm{GFL}}(s)$ are

$$L_{\mathrm{GFL}}(s) = f_{\delta\_\mathrm{GFLd}}(\boldsymbol{s})\frac{\mathrm{G}_{ud}(s)}{s} + f_{\boldsymbol{\delta}\_\mathrm{GFLq}}(s)\frac{\mathrm{G}_{uq}(s)}{s} \tag{23}$$

$$\Phi_{\mathrm{GFL}}(s) = \frac{f_{\boldsymbol{\delta}\_\mathrm{GFLd}}(\boldsymbol{s})\,\mathrm{G}_{ud}(s) + f_{\boldsymbol{\delta}\_\mathrm{GFLq}}(s)\mathrm{G}_{uq}(s)}{s + f_{\boldsymbol{\delta}\_\mathrm{GFLd}}(\boldsymbol{s})\,\mathrm{G}_{ud}(s) + f_{\boldsymbol{\delta}\_\mathrm{GFLq}}(s)\mathrm{G}_{uq}(s)}. \tag{24}$$

B. SISO Model of GFM Inverters With Power-Based Integrated Synchronization

According to Fig. 2(b), the inverter bridge voltage $\boldsymbol{v_{inv}}$ of the GFM inverter can be expressed as follows:

$$\boldsymbol{v_{inv}} = K_{\mathrm{PWM}}G_{\mathrm{d}}(s)\left[G_i(s)(\boldsymbol{i_{Lref}} - \boldsymbol{i_L}) + \frac{j\omega_n L_{f1}}{K_{\mathrm{PWM}}}\boldsymbol{i_g}\right] \tag{25}$$

$$\begin{bmatrix} \tilde{u}_{\mathrm{d}} \\ \tilde{u}_{\mathrm{q}} \end{bmatrix} \approx \left(\begin{bmatrix} R_g + sL_g & -\omega_n L_g \\ \omega_n L_g & R_g + sL_g \end{bmatrix}\boldsymbol{B}^{-1}\boldsymbol{A} - \boldsymbol{E} - \begin{bmatrix} G_{ud}(s)L_g I_{gq} & G_{uq}(s)L_g I_{gq} \\ -G_{ud}(s)L_g I_{gd} & -G_{uq}(s)L_g I_{gd} \end{bmatrix}\right)^{-1} \cdot \begin{bmatrix} -V_g \sin\delta_0 \\ -V_g \cos\delta_0 \end{bmatrix} \cdot (-\tilde{\delta})$$
$$\triangleq \boldsymbol{F}_{\delta\_\mathbf{GFL}}(\boldsymbol{s}) \cdot (-\tilde{\delta}). \tag{20}$$

where

$$\boldsymbol{i_{Lref}} = G_v(s)(\boldsymbol{u_{ref}} - \boldsymbol{u_{PCC}}) + \boldsymbol{i_g} + j\omega_n C_f \boldsymbol{u_{PCC}}. \quad (26)$$

The grid voltage reference $\boldsymbol{u_{ref}}$ is

$$\begin{bmatrix} u_{\mathrm{d\_ref}} \\ u_{\mathrm{q\_ref}} \end{bmatrix} = \begin{bmatrix} E_{\mathrm{ref}} + G_{nq}(Q_{\mathrm{ref}} - Q) \\ 0 \end{bmatrix}. \quad (27)$$

Combining (25)–(27) and considering the *LC* filter dynamics in (10) and (11), the output impedance of the GFM inverter, denoted as $\boldsymbol{Z_{GFM}}$, is derived as follows:

$$\boldsymbol{Z_{GFM}} = \begin{bmatrix} \tilde{u}_{\mathrm{d}} \\ \tilde{u}_{\mathrm{q}} \end{bmatrix} \begin{bmatrix} \tilde{i}_{gd} \\ \tilde{i}_{gq} \end{bmatrix}^{-1} = \boldsymbol{C}^{-1}\boldsymbol{D}. \quad (28)$$

The expressions of the matrices $\boldsymbol{C}$ and $\boldsymbol{D}$ are shown in the Appendix, as shown in (A3) and (A4).

Similar to (18), the relation of the inverter output voltage to the grid voltage remains

$$\begin{aligned} \boldsymbol{u_{PCC}} - \boldsymbol{v_g} &= (R_g + sL_g + j\omega L_g)\boldsymbol{i_g} \\ &= (R_g + sL_g + j\omega L_g)\boldsymbol{u_{PCC}}\boldsymbol{Z_{GFM}^{-1}}. \end{aligned} \quad (29)$$

Imposing small-signal perturbations to ω, $\boldsymbol{u_{PCC}}$, and $\boldsymbol{v_g}$ in (29), and substituting (19) and (28) into it, yields (30) shown at the bottom of this page. From (30), the d-axis and q-axis components of $\boldsymbol{i_g}$ can be expressed as follows:

$$\begin{cases} \tilde{i}_{gd} = [1 \quad 0]\boldsymbol{F_{\delta\_GFM}}(\mathbf{s}) \cdot (-\tilde{\delta}) \triangleq f_{\boldsymbol{\delta\_GFMd}}(\mathbf{s}) \cdot (-\tilde{\delta}) \\ \tilde{i}_{gq} = [0 \quad 1]\boldsymbol{F_{\delta\_GFM}}(\mathbf{s}) \cdot (-\tilde{\delta}) \triangleq f_{\boldsymbol{\delta\_GFMq}}(\mathbf{s}) \cdot (-\tilde{\delta}) \end{cases} \quad (31)$$

where $f_{\delta\_\mathrm{GFMd}}(s)$ and $f_{\delta\_\mathrm{GFMq}}(s)$ denote the angle-input-current-output (AICO) functions of the GFM inverter.

The power-based integrated synchronization results in

$$\begin{aligned} \tilde{\theta} = \frac{G_P(s)}{s}\tilde{P} + \frac{G_Q(s)}{s}\tilde{Q} &\approx \frac{1.5U_{\mathrm{d}}G_P(s)}{s}\tilde{i}_{gd} - \frac{1.5U_{\mathrm{d}}G_Q(s)}{s}\tilde{i}_{gq} \\ &\triangleq \mathrm{PSC}(s)\tilde{i}_{gd} + \mathrm{QSC}(s)\tilde{i}_{gq}. \end{aligned} \quad (32)$$

The closed-loop SISO diagram can then be depicted in Fig. 10. The corresponding open-loop transfer function $L_{\mathrm{GFM}}(s)$ and closed-loop transfer function $\Phi_{\mathrm{GFM}}(s)$ are given by

$$L_{\mathrm{GFM}}(s) = f_{\delta\_\mathrm{GFMd}}(s)\mathrm{PSC}(s) + f_{\delta\_\mathrm{GFMq}}(s)\mathrm{QSC}(s) \quad (33)$$

$$\Phi_{\mathrm{GFM}}(s) = \frac{f_{\delta\_\mathrm{GFMd}}(s)\mathrm{PSC}(s) + f_{\delta\_\mathrm{GFMq}}(s)\mathrm{QSC}(s)}{1 + f_{\delta\_\mathrm{GFMd}}(s)\mathrm{PSC}(s) + f_{\delta\_\mathrm{GFMq}}(s)\mathrm{QSC}(s)}. \quad (34)$$

IV. Grid-Synchronization Stability Analysis

The grid-synchronization stability involves two categories: a) small-signal stability, which focuses on whether the inverter has strong robustness against the grid strength variation; b) transient stability (or called large-disturbance stability), which focuses on whether the inverter can move from the original equilibrium to a new one during transients.

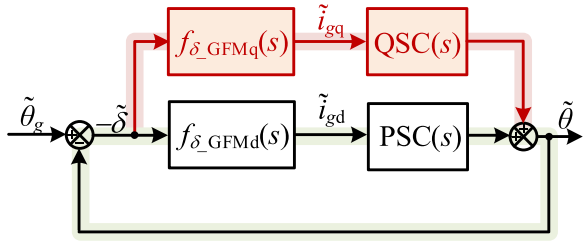

Fig. 10. Closed-loop SISO model of the GFM inverter with the power-based integrated synchronization.

A. Small-Signal Grid-Synchronization Stability Analysis

As for the GFL inverter with the integrated voltage synchronization, its transfer function shown in (23) can be rewritten as follows:

$$L_{\mathrm{GFL}}(\boldsymbol{s}) = f_{\boldsymbol{\delta\_GFLq}}(\boldsymbol{s}) \cdot f_{\boldsymbol{syn\_GFL}}(\boldsymbol{s}) \quad (35)$$

where

$$f_{\boldsymbol{syn\_GFL}}(\boldsymbol{s}) = \frac{G_{\mathrm{uq}}(\boldsymbol{s})}{s} + \frac{f_{\boldsymbol{\delta\_GFLd}}(\boldsymbol{s})}{f_{\boldsymbol{\delta\_GFLq}}(\boldsymbol{s})} \cdot \frac{G_{\mathrm{ud}}(\boldsymbol{s})}{s}. \quad (36)$$

So that $L_{\mathrm{GFL}}(s)$ is formulated as a product of the AIVO function $f_{\delta\_\mathrm{GFLq}}(s)$ and the synchronization function $f_{\mathrm{syn\_GFL}}(s)$. Consequently, the synchronization stability can be examined by analyzing the interaction between $f_{\mathrm{syn\_GFL}}(s)$ and $f_{\delta\_\mathrm{GFLq}}(s)$, similar to the well-known impedance-based stability analyses [27], [28]. Essentially, it shares the same fundamental philosophy as the multiplicative perturbation approach [29].

Based on (35), the following criterion holds: The system is stable if and only if the phase difference between the synchronization function $f_{\mathrm{syn\_GFL}}(s)$ and the inverse of the AIVO function $1/f_{\delta\_\mathrm{GFLq}}(s)$ remains within $\pm 180°$ at the gain crossover frequency (i.e., the frequency where their magnitude intersects in the Bode diagram). This criterion aligns fundamentally with the Nyquist stability criterion, while providing a more intuitive interpretation of the impact mechanism on synchronization stability.

Prior to investigating the integrated synchronization stability, we first analyze the instability mechanism of the GFL inverter with the conventional PLL in a weak grid. Referring to (36) and setting $G_{\mathrm{ud}}(s) = 0$, the frequency responses of $f_{\mathrm{syn\_GFL}}(s)$ and $1/f_{\delta\_\mathrm{GFLq}}(s)$ with PLL can be depicted in Fig. 11. As shown, as L_g increases, a distinct resonance peak emerges in

$$\begin{bmatrix} \tilde{i}_{gd} \\ \tilde{i}_{gq} \end{bmatrix} = \left(\begin{bmatrix} R_g + sL_g & -\omega_n L_g \\ \omega_n L_g & R_g + sL_g \end{bmatrix} - \boldsymbol{Z_{GFM}} - 1.5 \begin{bmatrix} G_P(s)U_{\mathrm{d}}L_g I_{gq} & -G_Q(s)U_{\mathrm{d}}L_g I_{gq} \\ -G_P(s)U_{\mathrm{d}}L_g I_{gd} & G_Q(s)U_{\mathrm{d}}L_g I_{gd} \end{bmatrix} \right)^{-1} \cdot \begin{bmatrix} -V_g \sin\delta_0 \\ -V_g \cos\delta_0 \end{bmatrix} \cdot (-\tilde{\delta}) \triangleq \boldsymbol{F_{\delta\_GFM}}(\boldsymbol{s}) \cdot (-\tilde{\delta}). \quad (30)$$

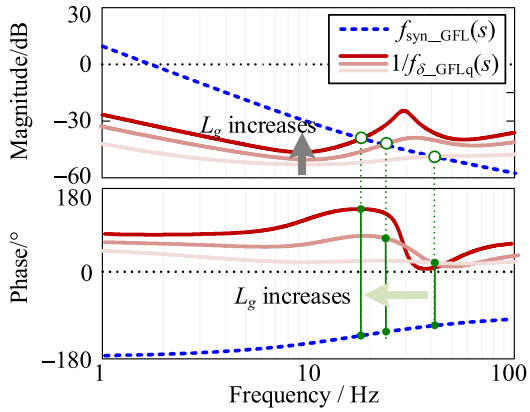

Fig. 11. Frequency responses of $f_{syn\_GFL}(s)$ and $1/f_{\delta\_GFLq}(s)$ with the conventional PLL.

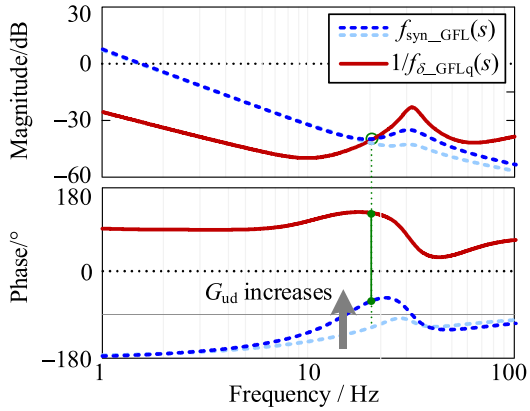

Fig. 12. Frequency responses of $f_{syn\_GFL}(s)$ and $1/f_{\delta\_GFLq}(s)$ with the proposed integrated synchronization.

the magnitude-frequency curve of $1/f_{\delta\_GFLq}(s)$, accompanied by a significant phase steepening in the corresponding frequency range. Consequently, as L_g increases, the intersection frequency of $f_{syn\_GFL}(s)$ and $1/f_{\delta\_GFLq}(s)$ becomes lower, and the corresponding phase difference tends to exceed 180°, leading to instability.

In comparison with the conventional PLL, the proposed integrated synchronization scheme introduces an additional term incorporating $1/f_{\delta\_GFLq}(s)$ into the synchronization function $f_{syn\_GFL}(s)$, as highlighted in purple color in (36). Consequently, the aforementioned frequency response variations of $1/f_{\delta\_GFLq}(s)$ induced by increasing L_g are inherently reflected in the frequency characteristics of $f_{syn\_GFL}(s)$, as shown in Fig. 12. This mechanism effectively compensates for the phase difference between $f_{syn\_GFL}(s)$ and $1/f_{\delta\_GFLq}(s)$, thereby enhancing system stability.

As for the GFM inverter with the integrated voltage synchronization, similarly, the loop gain shown in (33) can be rewritten as follows:

$$L_{GFM}(s) = f_{\delta\_GFMd}(s) \cdot f_{syn\_GFM}(s) \tag{37}$$

where

$$f_{syn\_GFM}(s) = \mathrm{PSC}(s) + \frac{f_{\delta\_GFMq}(s)}{f_{\delta\_GFMd}(s)} \cdot \mathrm{QSC}(s). \tag{38}$$

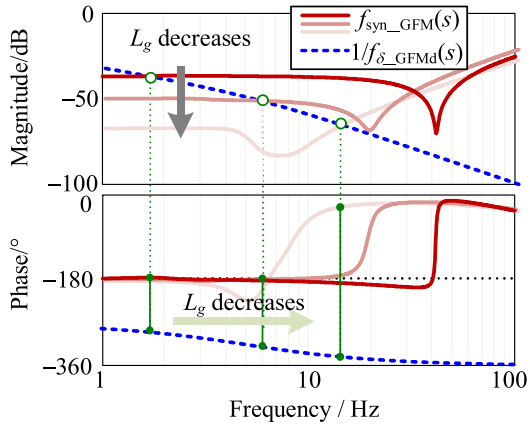

Fig. 13. Frequency responses of $f_{syn\_GFM}(s)$ and $1/f_{\delta\_GFMd}(s)$ with the conventional PSC.

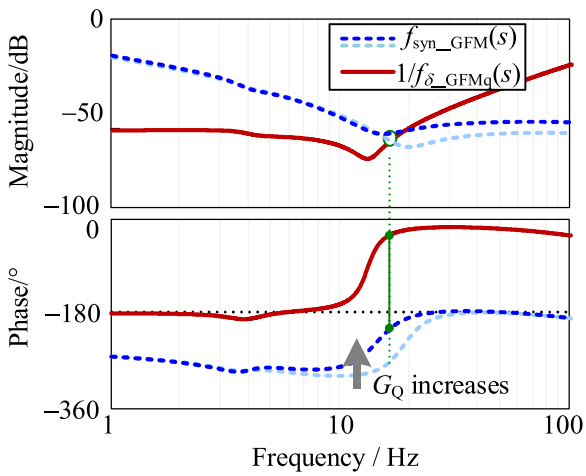

Fig. 14. Frequency responses of $f_{syn\_GFM(s)}$ and $1/f_{\delta\_GFMq(s)}$ with the proposed integrated synchronization.

The system is stable if and only if the phase difference between the synchronization function $f_{syn\_GFM}(s)$ and the inverse of the AICO function $1/f_{\delta\_GFMd}(s)$ is bounded within ±180° at their magnitude-curve intersection frequency. In contrast to GFL inverters, the phase difference tends to exceed 180° as L_g decreases, as shown in Fig. 13, aligning with the well-known instability phenomenon of GFM inverters under stiff grid conditions.

While applying the proposed integrated synchronization scheme, the frequency response variations of $1/f_{\delta\_GFMd}(s)$ induced by reduced L_g are also reflected in the frequency characteristics of $f_{syn\_GFM}(s)$, as shown in Fig. 14. This mutual compensation of their phase differences enhances the system stability, analogous to the stabilizing mechanism of the integrated synchronization scheme on GFL inverters.

B. Transient Grid-Synchronization Stability Analysis

While certain integrated synchronization schemes present similar small-signal stability characteristics, the aforementioned operational equivalences become invalid during the transient

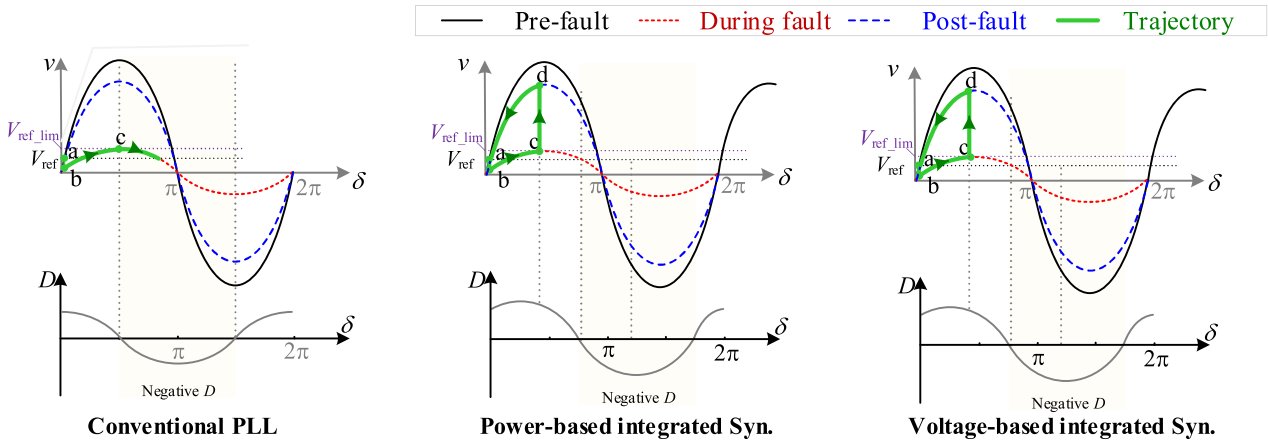

Fig. 15. Transient stability of GFL inverters with the priority-based current limiter ($\theta = 0°$).

process, leading to substantially divergent transient performances under grid contingencies. Besides, the compatible current limiting for protection would also be different for these three methods.

1) GFL Inverters With the Integrated Synchronization: GFL inverters commonly employ the direct current limiter, inserted before the inner current controller to directly restrain the fault current. Coordinated the direct current limiter, transient performances of GFL inverters with integrated synchronizations are studied as follows.

According to the synchronization principle, the large-signal models with three synchronization methods, including PLL, power-based integrated synchronization, and voltage-based integrated synchronization, can be readily derived as follows [30]:

$$\underbrace{\frac{1}{K_{uq\_i}}}_{H}\ddot{\delta} = -\underbrace{\frac{K_{uq\_p}}{K_{uq\_i}}v_g\cos\delta}_{D}\cdot\dot{\delta} + \underbrace{X_g i_g\cos\theta}_{v_{\rm ref}} - \underbrace{v_g\sin\delta}_{v}; \quad (39)$$

$$\underbrace{\frac{i_{gd\_\rm ref}}{i_g K_{Q\_i}}}_{H}\ddot{\delta} = -\underbrace{\left[\frac{K_{Q\_p}}{K_{Q\_i}}v_g\cos(\theta+\delta) + \frac{K_{P\_p}}{K_{Q\_i}}v_g\sin(\delta-\theta)\right]}_{D}\dot{\delta} + \underbrace{\left[X_g i_g - \frac{Q_{\rm ref}}{1.5 i_g}\right]}_{v_{\rm ref}} - \underbrace{v_g\sin(\theta+\delta)}_{v} \quad (40)$$

$$\underbrace{\frac{1}{K_{uq\_i}}}_{H}\ddot{\delta} = -\underbrace{\left[\frac{K_{uq\_p}}{K_{uq\_i}}v_g\cos(\delta) + \frac{K_{ud\_p}}{K_{uq\_i}}v_g\sin(\delta)\right]}_{D}\dot{\delta} + \underbrace{X_g i_g\cos\theta}_{v_{\rm ref}} - \underbrace{v_g\sin\delta}_{v}. \quad (41)$$

Referring to the swing equation of SG, H denotes the equivalent inertial coefficient, D is the equivalent damping coefficient, and $v_{\rm ref}$ is the equivalent voltage reference. As shown, these coefficients are also related to the value of θ. When the direct current limiter is triggered, the magnitude of the current reference is constant, while its phase θ may be adjusted with different rules (i.e., prioritizing the active power output or reactive power support) [31]. The priority-based current limiter with $\theta = 0°$ and $\theta = -90°$ are considered in the following.

According to (39)–(41), the v-δ and D-δ curves under $\theta = 0°$ and $\theta = -90°$ are plotted in Figs. 14 and 15, respectively. Therein, $v_{\rm ref\_lim}$ represents the equivalent voltage reference during fault, which can be obtained by substituting $i_g = i_{g\_\rm lim}$ and $\theta = 0°$ (or $-90°$) into the expressions of $v_{\rm ref}$ in (39)–(41). The system trajectory can be readily obtained, which is highlighted by the solid line with arrows in Figs. 15 and 16.

Priority-based current limiter with $\theta = 0°$ (see Fig. 15): Before fault, the system operates at the stable equilibrium point (SEP) a, which suddenly moves to the point b during fault. Then, the power angle starts to increase due to $v < v_{\rm ref\_lim}$, until reaching the point c. For the GFL inverter with the conventional PLL, (39) indicates that the damping coefficient at the point c is $D(\pi/2) = 0$ and becomes negative within the range $\delta \in (\pi/2, 3\pi/2)$. In comparison, (40) and (41) tell that the integrated synchronization not only contributes to a higher peak damping coefficient but also extends the upper boundary of δ below which damping remains positive. Consequently, when the operating point exceeds point c, the system with a conventional PLL is susceptible to loss of synchronization under negative damping effects [32], [33]. In contrast, the system with integrated synchronization exhibits enhanced transient stability due to sustained positive damping near point c.

Priority-based current limiter with $\theta = -90°$ (see Fig. 16): Different from Fig. 15, the condition of $v_{\rm ref\_lim} = 0$ holds for the system with PLL and voltage-based integrated synchronization. Accordingly, during a fault, the scenario of $v > v_{\rm ref\_lim}$ results in the decrease of δ, and thus the operating point leaves the point b and stops at the SEP c. In contrast, the system with the power-based integrated synchronization will suffer instability risk during a fault, since its point c falls into the negative damping region.

In summary, the voltage-based integrated synchronization demonstrates superior transient stability for GFL inverters.

2) GFM Inverters With the Integrated Synchronization: The priority-based current limiter turns inverters into current sources during overcurrent events to satisfy fault current requirements.

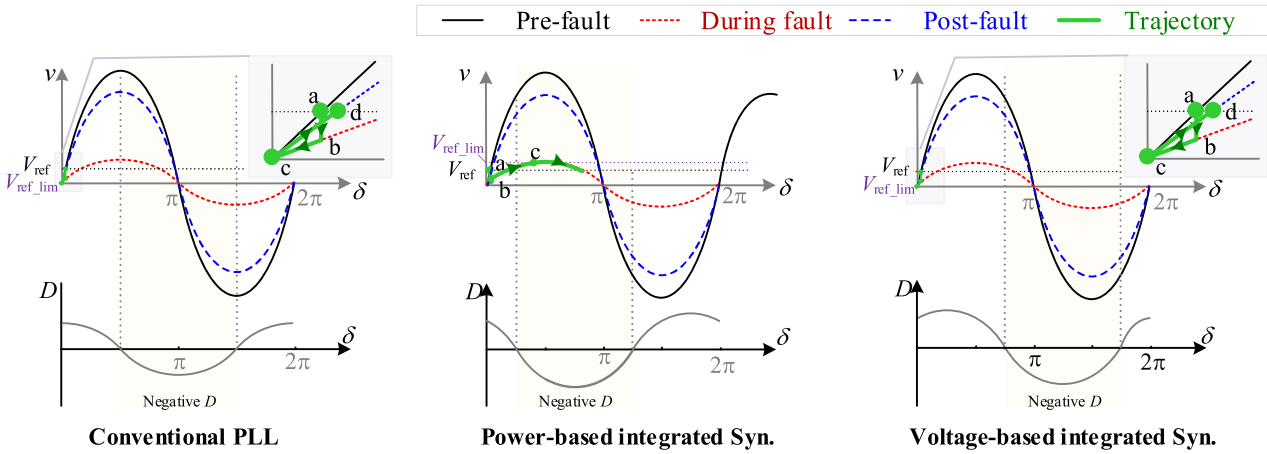

Fig. 16. Transient stability of GFL inverters with the priority-based current limiter ($\theta = -90°$).

In order to maintain its voltage source behavior and allow for automatic fault recovery, both circular current limiter (CCL) and virtual impedance limiter (VIL) are popularized for GFM inverters [34]. As reported in [35], the transient performances with CCL and VIL are similar, since CCL can be modeled as an equivalent resistor. Thus, the transient performances coordinated with the priority-based current limiter and the CCL are studied here.

Priority-based current limiter: As previously mentioned, in order to secure the power-sharing and drooping characteristics, the HPF is added in the Q-ω droop path. Accordingly, the transient performances with the power-based integrated synchronization and with the PSC are comparable. The corresponding swing equation during fault is [22]

$$\underbrace{\frac{1}{m_p\omega_p}}_{H}\ddot{\delta} = -\underbrace{\frac{1}{m_p}}_{D}\dot{\delta} + P_{\text{ref}} - \underbrace{1.5v_g i_{\text{lim}}\cos(\delta-\theta)}_{P_e}. \quad (42)$$

As for the GFM with the current-based integrated synchronization, its swing equation during a fault is written by

$$\underbrace{\frac{1}{K_{\text{id}}\omega_p}}_{H}\ddot{\delta} = -\underbrace{\frac{1}{K_{\text{id}}}}_{D}\dot{\delta} + i_{gd\_\text{ref}} - \underbrace{i_{\text{lim}}\cos\theta}_{i}. \quad (43)$$

As shown, the equivalent damping coefficient is a positive constant. Consequently, the aforementioned effect induced by negative damping will not occur in this case. The system trajectory is depicted as shown in Fig. 17. Note that inverters with priority-based current limiters are difficult to directly exit the current-limiting mode after fault clearance; hence, the postfault swing equation can be considered analogous to that during fault conditions.

As shown in Fig. 17, the operating point with the power-based integrated synchronization transitions from the prefault SEP a to the point b at the fault instant. Due to $P < P_{\text{ref}}$, the operating point accelerates and transitions along the P-δ curve until the fault clearance. In order to obtain the SEP during a fault, the adaptive power reference adjustment is usually required [36]. In contrast, as for the current-based integrated synchronization, if

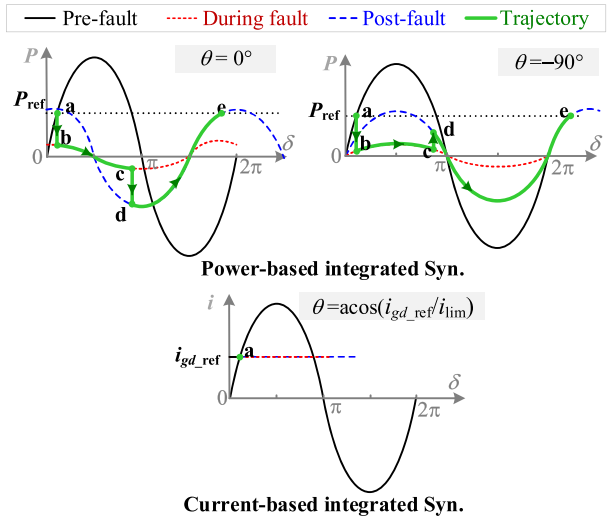

Fig. 17. Transient stability of GFM inverters with the priority-based current limiter.

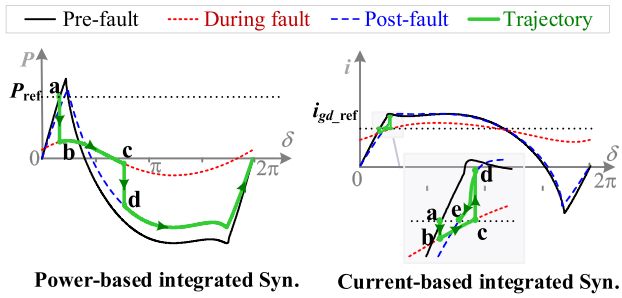

Fig. 18. Transient stability of GFM inverters with the circular current limiter.

$\theta = \arccos(i_{gd\_\text{ref}}/i_{\text{lim}})$ is set for the current limiter, the system will stay at the SEP a during fault and after fault clearance, while maintaining nearly invariant power angle throughout the transient process.

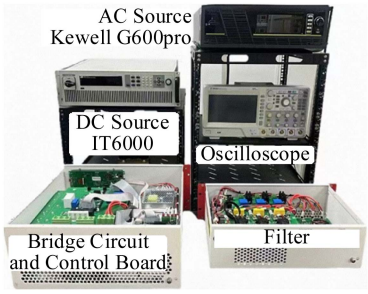

Fig. 19. Configuration of the experimental setup.

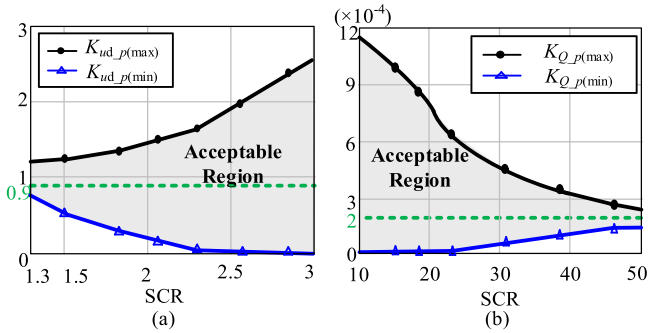

Fig. 20. Acceptable region of (a) K_{ud_p} and (b) K_{Q_p}.

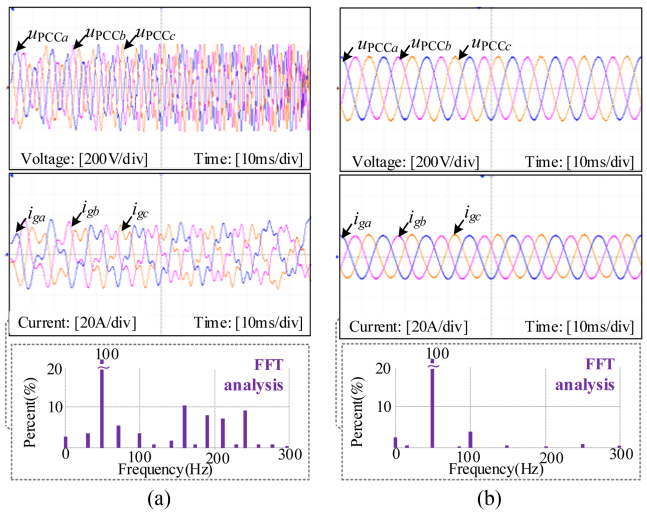

Fig. 21. Experimental results of the GFL inverter under SCR = 2.4. (a) Conventional PLL. (b) Proposed integrated synchronization.

Circular current limiter: When the circular current limiter is applied, the P-δ function with the power-based integrated synchronization during fault is expressed as follows [35]:

$$P = \frac{3}{2}\left[\frac{R_e\left(E_{\rm ref}^2 - E_{\rm ref} v_{\rm g}\cos\delta\right)}{R_e^2 + \left(X_g + X_f\right)^2} - R_e i_{\rm lim}^2 + \frac{\left(X_g + X_f\right) E_{\rm ref} v_{\rm g}\sin\delta}{R_e^2 + \left(X_g + X_f\right)^2}\right] \tag{44}$$

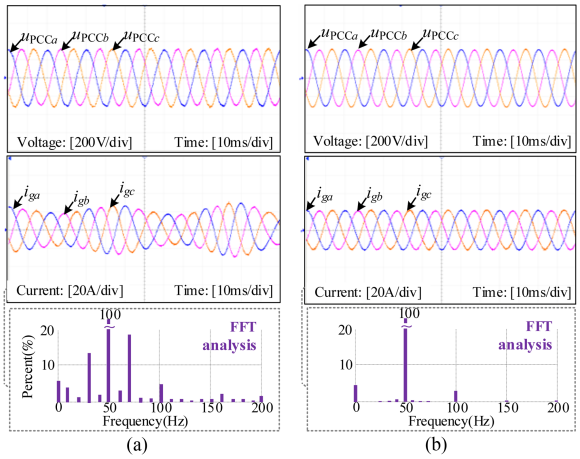

Fig. 22. Experimental results of the GFM inverter under SCR = 29. (a) Conventional PSC. (b) Proposed integrated synchronization.

where

$$R_e = \max\left\{0, \mathrm{Re}\left(\sqrt{\frac{E_{\rm ref}^2 - 2E_{\rm ref} v_{\rm g}\cos\delta + {v_{\rm g}}^2}{i_{\rm lim}^2} - \left(X_g + X_f\right)^2}\right)\right\} \tag{45}$$

and the i-δ function with the current-based integrated synchronization during fault is given by

$$i_{gd} = \frac{\left(E_{\rm ref} - v_{\rm g}\cos\delta\right) R_e + \left(X_g + X_f\right) v_{\rm g}\sin\delta}{{R_e}^2 + \left(X_g + X_f\right)^2}. \tag{46}$$

Based on (44) and (46), the P-δ and i-δ curves are plotted as shown in Fig. 18. As can be observed, the operation point of GFM inverters with the power-based integrated synchronization keeps accelerating during a fault, due to the absence of an equilibrium point. In contrast, GFM converters with the current-based integrated synchronization can directly transition to a faulted steady state when a fault occurs, and maintain a constant power angle until the fault is cleared. This is also consistent with the conclusion shown in [22].

In summary, while conventional PSC and the power-based integrated synchronization require adaptive power reference adjustment during faults to achieve SEP, the current-based synchronization with a circular current limiter can achieve stabilization within fault inception/clearance instants, demonstrating negligible power angle deviation with inherent transient superiority.

C. Physical Insights

The physical insights of the proposed integrated synchronization in improving system stability are summarized as follows.

The small-signal stability enhancement, as analyzed in Section IV-A, stems from the ability of the integrated synchronization schemes to reshape the frequency characteristics of the system loop gain. Essentially, it reshapes the inverter's output impedance so as to enhance the interactive stability between the inverter and the grid.

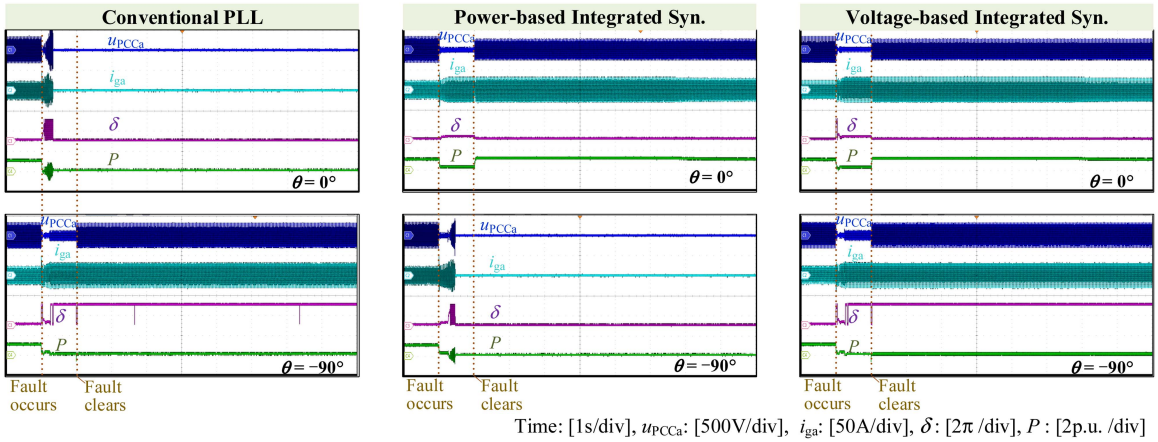

Fig. 23. Transient responses of the GFL inverter during symmetrical grid faults.

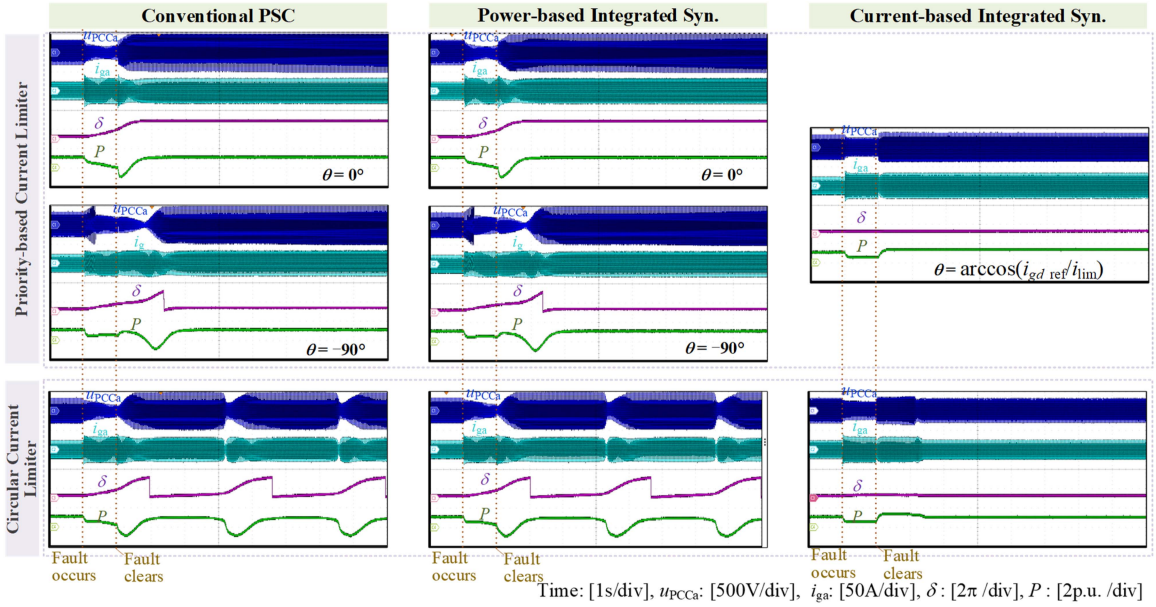

Fig. 24. Transient responses of the GFM inverter during symmetrical grid faults.

For transient stability improvement, the voltage-based scheme introduces additional damping by emulating the damper winding of SGs, as illustrated in (41). The current-based integrated synchronization ensures synchronization by increasing the maximum available electromagnetic power during faults, thereby strengthening the electrical braking capability to resynchronize after a disturbance, as reflected in (43).

V. Verification

To verify the abovementioned theoretical analyses, experiments are performed, whose main parameters are listed in Table I, and control parameters are elaborated in Section V-A. The configuration of the experimental setup is presented in Fig. 19. The single-phase inverter bridge is implemented with two IGBT modules (CM200DY-24NF), which are driven by M57962L. The control algorithm is implemented in DSP (TI TMS320C28346). The required currents and voltage are sensed by the current hall (LA55-P) and the voltage hall (LV25-P), respectively. The grid voltage and the grid impedance were emulated by a programmable ac source (Kewell G6000pro) and the external inductor and capacitor, respectively.

A. Parameter Determination

The design of current/voltage regulator parameters and the conventional u_q-PLL or P-ω droop coefficients can refer to [6] and [12]. The proportional gains in the additional loop of the integrated synchronization are determined with a detailed design procedure as follows.

Step 1: Initialize the SCR, draw the root locus of the open-loop model as the proportional gain varies from 0 to infinity.

Step 2: Based on the plotted root locus, determine the boundaries of the proportional gain under different SCR.

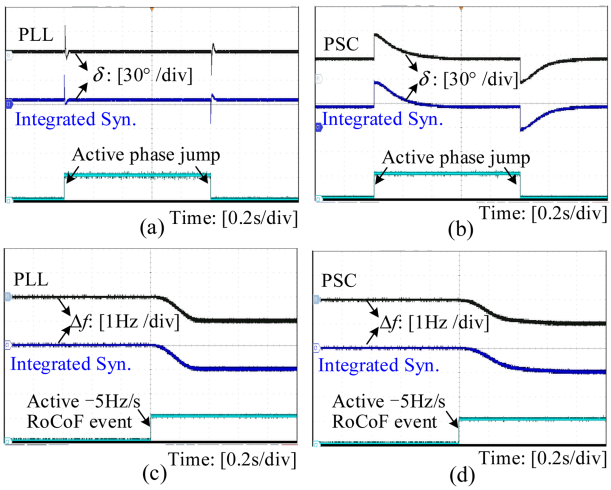

Fig. 25. Comparison of dynamics performances. (a) Dynamic responses of GFL inverters with PLL or integrated synchronization when subject to ±30° phase jumps. (b) Dynamic responses of GFM inverter with PSC or integrated synchronization when subject to ±30° phase jumps. (c) Dynamic responses of GFL inverter with PLL or integrated synchronization when subject to −5Hz/s RoCoF event. (d) Dynamic responses of GFM inverter with PSC or integrated synchronization when subject to −5Hz/s RoCoF event.

TABLE I
PARAMETERS FOR EXPERIMENTAL TESTS

System parameters			
Parameter	Value	Parameter	Value
DC-side voltage V_{dc}	700 V	Fundamental frequency f_o	50 Hz
Grid voltage V_g (RMS)	220 V	Switching frequency f_{sw}	20 kHz
Output power P_o	10 kW	Sampling frequency f_s	20 kHz
Inverter-side inductor L_f	3.2 mH	Grid-side inductor L_T	0.6 mH
Filter capacitor C_f	10 μF	Parasitic resistor R_f	0.046 Ω

Controller parameters			
GFL inverter		GFM inverter	
Parameters	Value	Parameters	Value
$G_{uq}(s)$	$0.727 + 82.28/s$	$G_P(s)$	$-0.00314\pi/(s+10\pi)$
$G_{dref}(s)$	$(0.5 + 40/s)/10000$	n_q	$-31.1/10000$
$G_{qref}(s)$	$(5 + 400/s)/311$	HPF	$s/(s+4\pi)$
$G_i(s)$	$0.094 + 9.42/s$	$G_v(s)$	$0.00264 + 0.99/s$
$G_{ad}(s)$	0.065	$G_i(s)$	$0.0654 + 1.31/s$

Step 3: Encircled by the maximum and minimum boundaries, the acceptable region can be obtained, from which the desired parameter can be easily selected.

Taking the main parameters in Table I as an illustration, the proportional gain of G_{ud} in the voltage-based integrated synchronization, i.e., K_{ud_p}, is determined. Assuming the minimum SCR is 1.3, the acceptable region of K_{ud_p} is drawn in Fig. 20(a). In order to ensure the stability under varying grid impedance, $K_{ud\_p} = 0.9$ is selected. Similarly, the proportional gain of G_Q for the power-based integrated synchronization in the GFM inverter is determined from Fig. 20(b), and $K_{Q\_p} = 0.0002$ is selected.

B. Verification of Integrated Synchronizations

Since the voltage-based and power-based integrated synchronization endows GFL inverters with the same performance, we take the former as an illustration, and the results with the power-based integrated synchronization are not repeated. Similarly, the experimental results with power-based integrated synchronization for GFM inverters are taken as an illustration, and the current-based ones are not repeated.

The first set of experiments was conducted to confirm the effectiveness of the proposed methods on the small-signal synchronization stability. Fig. 21 shows the waveforms of the GFL inverter with the conventional PLL and the proposed integrated synchronization under SCR = 2.4. As shown, the system is stable with the integrated synchronization, and the THDs of the output current are 2.5%; in contrast, the oscillation appears with the conventional PLL and the THDs reach 7.3%.

Fig. 22 shows the waveforms of the GFM inverter under SCR = 29. As shown, while using the conventional PSC, distortion components in the grid current exceed 10%; In contrast, the system with the proposed integrated synchronizations remains stable, and the THDs of the grid current are only 1.3%. The abovementioned quantitative comparison confirms that the integrated synchronization improves system adaptability against the grid strength variation.

The second set of experiments was conducted to confirm the transient stability. Fig. 23 shows the transient responses of the GFL inverter during symmetrical grid faults (V_g drops to 0.2 p.u., which lasts 1 s and recovers to 0.8 p.u.). The oscillation in the output power and power angle can be clearly observed in the conventional PLL operating with the priority-based current limiter ($\theta = 0°$) and the power-based integrated synchronization with the priority-based current limiter ($\theta = -90°$), indicating LOS. In contrast, the GFL inverter with the integrated synchronization can ride through a grid fault, demonstrating its superiority in transient stability, which agrees with theoretical analyses in Section IV.

Fig. 24 shows the transient responses of the GFM inverter during symmetrical grid faults. As can be observed, the power-based integrated synchronization shows compatible transient performance as the conventional PSC. This is because the inserted HPF prevents the effect of Q-ω droop. Compared with the power-based integrated synchronization, the current-based integrated synchronization coordinating with the priority-based current limiter or circular current limiter can directly transition to a faulted steady state when a fault occurs, and maintain a constant power angle until the fault is cleared. Moreover, the circular current limiter can automatically exit the current limiting mode after fault clearance, while endowing the system with the voltage source characteristics in the whole process. The results match well with the theoretical analyses in Section IV.

The third set of experiments was conducted to evaluate the dynamic performance of the proposed integrated synchronization schemes. For comparison, the results with traditional approaches are also presented. Fig. 25(a) and (b) show the dynamic responses of GFL and GFM inverter when subject to ±30° phase

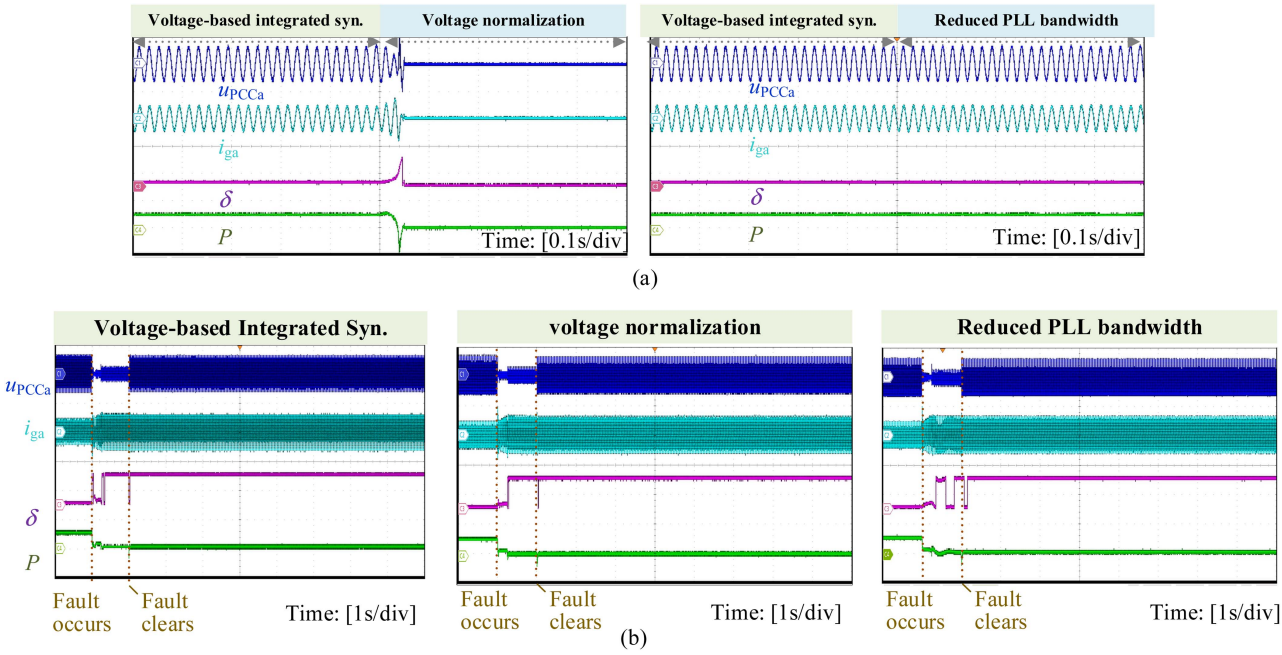

Fig. 26. Comparison of the proposed voltage-based integrated synchronization to the voltage normalization and the reduced PLL bandwidth approach for GFL inverters. (a) Small-signal stability comparison. (b) Transient stability comparison. (u_{PCCa}: [500V/div], i_{ga}: [50A/div], δ: [2π /div], P: [2p.u. /div]).

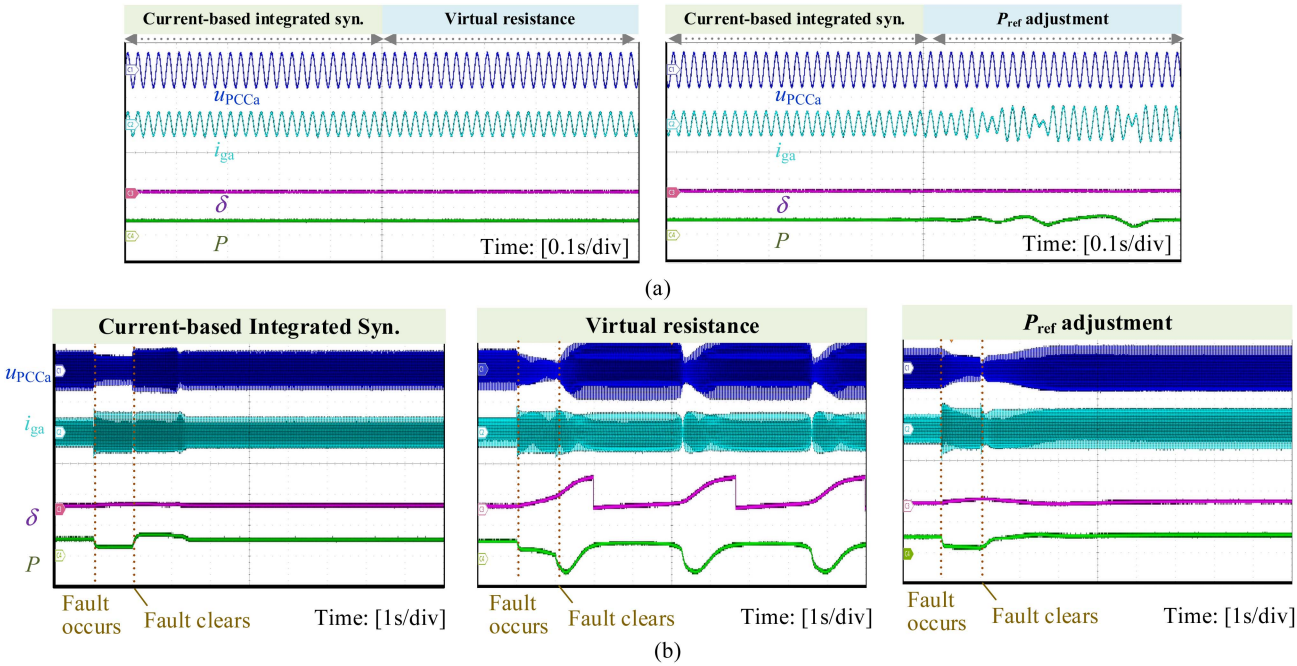

Fig. 27. Comparison of the proposed current-based integrated synchronization to the virtual resistance and the active power reference adjustment approach for GFM inverters. (a) Small-signal stability comparison. (b) Transient stability comparison. (u_{PCCa}: [500V/div], i_{ga}: [50A/div], δ: [2π/div], P: [2p.u. /div]).

jumps, respectively, and Fig. 25(c) and (d) show the dynamic responses of GFL and GFM inverter when subject to -5 Hz/s RoCoF event of the power grid that lasts 0.2 s. As shown, the proposed schemes offer comparable response speed and accuracy to conventional control schemes.

The fourth set of experiments was conducted to compare the proposed methods with existing advanced synchronization approaches, including the voltage normalization approach and reduced PLL bandwidth for GFL inverters, and virtual resistance control or power reference adjustment for GFM inverters. Compared with the voltage normalization approach, as shown in Fig. 26, the proposed method exhibits comparable transient stability performance while offering superior adaptability to a weak grid; when compared to the reduced PLL bandwidth approach, both methods effectively improve system stability, but the proposed method avoids significant degradation

$$\boldsymbol{A} \approx K_{\mathbf{PWM}} G_{\mathbf{d}}(s) \left\{ G_i(s) \begin{bmatrix} -1.5 I_{g\mathbf{d}} G_{\mathbf{dref}}(s) & -1.5 I_{g\mathbf{q}} G_{\mathbf{dref}}(s) \\ G_{\mathbf{qref}}(s) & 0 \end{bmatrix} - G_{\mathbf{ad}}(s) \begin{bmatrix} sC_f & -\omega_n C_f \\ \omega_n C_f & sC_f \end{bmatrix} \right\} - E - \begin{bmatrix} sL_f & -\omega_n L_f \\ \omega_n L_f & sL_f \end{bmatrix} \begin{bmatrix} sC_f & -\omega_n C_f \\ \omega_n C_f & sC_f \end{bmatrix} \tag{A1}$$

$$\boldsymbol{B} = K_{\mathrm{PWM}} G_{\mathrm{d}}(s) \left\{ G_{\mathrm{ad}}(s) \begin{bmatrix} sC_f & -\omega_n C_f \\ \omega_n C_f & sC_f \end{bmatrix} \begin{bmatrix} sL_T & -\omega_n L_T \\ \omega_n L_T & sL_T \end{bmatrix} - G_i(s) \begin{bmatrix} -1.5 U_{\mathrm{d}} G_{\mathrm{dref}}(s) - 1 & 0 \\ 0 & -1 \end{bmatrix} \right\} + \begin{bmatrix} sL_f & 0 \\ 0 & sL_f \end{bmatrix} + \begin{bmatrix} sL_f & -\omega_n L_f \\ \omega_n L_f & sL_f \end{bmatrix} \begin{bmatrix} sC_f & -\omega_n C_f \\ \omega_n C_f & sC_f \end{bmatrix} \begin{bmatrix} sL_T & -\omega_n L_T \\ \omega_n L_T & sL_T \end{bmatrix} \tag{A2}$$

$$\boldsymbol{C} \approx K_{\mathrm{PWM}} G_{\mathrm{d}}(s) G_i(s) G_v(s) \left(1.5 G_{nq}(s) \begin{bmatrix} -I_{g\mathrm{q}} & I_{g\mathrm{d}} \\ 0 & 0 \end{bmatrix} + E \right) + \begin{bmatrix} sL_f & 0 \\ 0 & sL_f \end{bmatrix} \begin{bmatrix} sC_f & -\omega_n C_f \\ \omega_n C_f & sC_f \end{bmatrix} + E + K_{\mathrm{PWM}} G_{\mathrm{d}}(s) G_i(s) \begin{bmatrix} sC_f & 0 \\ 0 & sC_f \end{bmatrix} \tag{A3}$$

$$\boldsymbol{D} = 1.5 G_{nq}(s) K_{\mathrm{PWM}} G_{\mathrm{d}}(s) G_i(s) G_v(s) \begin{bmatrix} 0 & U_{\mathrm{d}} \\ 0 & 0 \end{bmatrix} - K_{\mathrm{PWM}} G_{\mathrm{d}}(s) \begin{bmatrix} sL_f & 0 \\ 0 & sL_f \end{bmatrix}. \tag{A4}$$

in dynamic performance. Besides, Fig. 27 tells that both VR and current-based integrated synchronization ensure stability of GFM inverters in a stiff grid, while the latter has better transient stability. Compared with the active power reference adjustment approach, both methods can effectively improve transient stability, while the current-based integrated method also contributes to enhancing adaptability to stiff grids. The abovementioned results demonstrate that the proposed integrated synchronization has comprehensive performance improvements compared to these typical control strategies.

VI. Conclusion

Inspired by the structural similarity and duality properties of the conventional PLL and PSC, a family of integrated synchronization schemes is proposed for GFL/GFM inverters to make the best of them. The derived integrated synchronization schemes are in a symmetric and elegant form. Compared with existing methods, the integrated synchronization has the following merits. (1) The integration enables the robust operation of GFL or GFM inverters under the extra weak and stiff grid conditions, while does not require alter control parameters or detect the grid strength; (2) The voltage-based and current-based integration enables the system to directly transition to a faulted steady state, maintaining a constant power angle until fault clearance, thereby enhancing its tolerance to severe faults. Experimental results confirmed the abovementioned advantages of the integrated synchronization methods.

Appendix

The expressions of the matrices $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$, and $\boldsymbol{D}$ are shown in the Appendix, they are: shown at the top of this page.

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