A Decoupled Model of Multielement Resonance for Synchronous Rectification in Bidirectional High-Voltage SiC CLLC Converters

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***Abstract*—Hardware detection synchronous rectification (SR) methods are unsuitable for high-frequency/ high-voltage CLLC operations due to the high *dv/dt*. Because of the multielement resonance in CLLC converters, it is difficult to derive analytical solutions for SR switching instants in existing time-domain models. Consequently, they typically adopt fitting formulas or approximation approaches, resulting in compromised SR accuracy. This article proposed a digital CLLC SR control by a unified decoupled model of multielement resonance. By decoupling both the resonant inductors and resonant capacitors between primary and secondary sides, the SR analytical solutions are derived in a unified coordinate system. In the above-resonance region, the delay time is derived by the proposed decoupled model to determine the SR turn-ON and turn-OFF instants. In the below-resonance region, the SR ON-time is calculated to determine the SR turn-OFF instant with fixed SR turn-ON instant. With the proposed decoupled model, the analytical solutions of SR switching instants can be derived, which supports the online calculations. A 6.6-kW 300-kHz SiC-based bidirectional CLLC prototype was built. With the proposed SR, the CLLC efficiencies are up to 98.19% and 98.20% in the forward and reverse modes at full load, respectively. Compared to the conventional time-domain SR method, the forward efficiency increment is as high as 0.63% and the reverse efficiency increment is 0.45% .**

***Index Terms*—Bidirectional, CLLC converter, SiC, state-plane analysis, synchronous rectification (SR), time-domain model.**

I. Introduction

CLLC resonant converters feature a symmetric architecture for bidirectional power transfer, achieving soft switching under nearly all load conditions and inherent galvanic isolation [1], [2]. These characteristics make it extensively adopted in electric vehicle charging systems and renewable energy integration systems [3], [4].

Synchronous rectification (SR) is crucial for enhancing the efficiency of CLLC converters by replicating the conduction behavior of the secondary-side MOSFET body diode to minimize conduction losses [5], [6], [7]. In CLLC converters, resonant components and transformers occupy significant volume, which can be reduced by increasing the switching frequency to enhance power density [8]. Due to their high-frequency capability and high voltage tolerance, SiC MOSFETs are well-suited for high-frequency and high-voltage applications such as EV charging and renewable energy systems [9]. However, their body diode exhibits a significantly higher forward voltage drop compared to Si devices, making the implementation of SR essential for efficiency improvement. Existing SR strategies can be categorized into two main approaches: 1) high-frequency signal detection methods and 2) model-based methods.

A. High-frequency Signal Detection Methods

Table I provides existing SR methods. For high-frequency signal detection, conventional methods typically sense the resonant tank voltage/current or the drain-source voltage of SR MOSFETs. A method for determining secondary-side current direction through resonant inductor voltage detection was proposed [10]. It effectively mitigates the SRs false trigger issues induced by current oscillations, but it increases circuit complexity.

A Rogowski coil-based current sensing approach is employed for detecting high-frequency resonant currents in both primary and secondary windings [11]. The acquired current signals are processed as pulse waveforms and fed into the microcontroller unit for SR control. Nevertheless, additional space requirements and cost are introduced due to the Rogowski coil. A resonant current detection method based on a current transformer (CT) was proposed [12]. The ac current signal obtained by the CT is rectified to the dc signal. The processed signals are then compared with a fixed threshold, so that the SR driving signals are subsequently generated. Nevertheless, the two methods both increased the size and cost of the CLLC converter.

A body-diode-conduction extraction method is introduced [13]. It uses absorption diodes and series combination of blocking diode to solve the high *dv/dt* issue, which typically causes

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TABLE I
COMPARISONS OF SR METHODS

Category	Implementation approaches	Ref	Cost	Noise immunity	Versatility	Complexity	Accuracy
High-frequency Signal Detection Methods	Resonant inductance voltage sensing	[10]	Medium	Medium	Medium	High	Medium
	Resonant current sensing	[11]	High	Medium	High	Medium	Low
		[12]	High	Low	Medium	Medium	Low
	SR drain-source voltage sensing	[13]	Medium	High	Medium	High	Medium
Model-based Mathematical Computation Methods	Fundamental harmonic approximation	[14]	Low	High	High	Medium	Low
	Extended harmonic approximation	[15]	Low	High	Low	High	High
	Three-order fitting model	[16]	Low	High	High	Medium	High
	Time-domain model	[17]	Low	High	Medium	High	Low
	Fixed SR based on parameter design	[18]	Low	High	Low	High	High
	Time-domain fitting formulas	[20][21]	Low	High	High	High	High
	Three-dimensional polynomial fitting	[22]	Low	High	Low	High	High
	Standard quadratic-root formula	[23]	Low	High	Medium	High	High
	Quantitative state trajectory model	[24]	Low	High	High	High	High
	Time-domain-based neural network training	[25]	Medium	High	Medium	High	Medium
Proposed decoupled model			**Low**	**High**	**High**	**Low**	**High**

conventional drain-source voltage sensing ICs to fail. However, this method increases implementation costs.

These methods generally require additional sensing components and compensation circuits, which increases the converter volume and are unsuitable for high-frequency/ high-voltage SiC applications.

B. Model-Based Mathematical Computation Methods

In the frequency domain, the fundamental harmonic approximation (FHA) method is employed to calculate the phase shift angle between the primary-side driving signals and secondary-side resonant current in a CLLC converter [14]. Although FHA approach can be implemented easily, the SR accuracy is limited because it neglects the high-order harmonics.

An extended harmonic approximation method was developed to calculate the SR phase shift angle between primary-side and secondary-side switching signals [15]. Since it neglects discontinuous conduction mode (DCM) operation, its applicability is limited. A frequency-domain SR method was proposed using a three-order fitting model, but the SR accuracy can be further improved caused by the fitting errors [16].

In the time domain, a comprehensive time-domain model for CLLC converters was developed in [17]. However, the state equations involve complex general solutions of differential equations, which cause a significant computational burden on the digital controller. A SR method based on the resonant tank parameters matching was proposed [18]. Its predefined battery charging profiles are aligned with resonant tank parameters to achieve nearly fixed SR conduction time. However, this method is only effective under constrained load variations. As the dynamic response happens, the fixed SR conduction time can hardly be regulated correspondingly causing high conduction loss.

A state-plane model of CLLC is established in [19]. Two decoupled sets of equations were given based on change of variables. However, four complex coefficients are generated in the two decoupled *LC* resonators. Two pairs of state variables have to be calculated in two coordinate systems. These processes complicate the analysis. Besides, it neglects the two switching states where the magnetizing inductor participates in the resonance and only the continuous conduction mode is considered but the DCM is not. Therefore, using this method is hard to obtain the SR switching instants.

A CLLC time-domain model was established in [20] and [21]. This method solves the fifth-order differential equations and obtains the SR switching instants through numerical iteration. Due to the numerous calculations, fitting approximation has to be adopted resulting in low SR accuracy. A digital SR algorithm based on a time-domain model was proposed, utilizing hybrid modulation combining pulse frequency modulation (PFM) and phase-shift modulation (PSM) [22]. The method leverages polynomial fitting for mode boundary recognition under PFM and a simplified resonant tank model under PSM to calculate SR timing. All these methods employ the fitting approach, which limits the SR accuracy.

In [23], the SR method approximates the secondary-side current as a piecewise sinusoidal-linear waveform to enable computational simplicity. However, the simplification neglects higher-order harmonics and nonlinear dynamics inherent in the resonant current, which results in reduced accuracy. In [24], a switching delay SR strategy is proposed. This method delays the turn-ON instant of secondary-side switches to ensure ZVS by fully charging or discharging the output capacitors. However, the resonant capacitors are approximated as fixed dc sources during dead time, so that the accuracy can be further improved.

The contribution of this article is to propose a decoupled model for SR in high-voltage SiC CLLC converters. The analytical solutions of SR switching instants are derived to enable online calculations with high accuracy and high immunity.

The rest of this article is organized as follows. Section II presents the proposed SR. Section III derives the decoupled model. Section IV elaborates on the proposed SR. Section V presents simulations and tolerances analysis. Section VI presents experimental results and discussion. Finally, Section VII concludes this article.

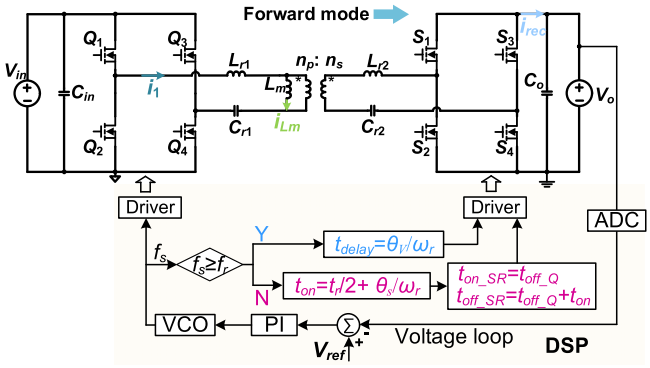


Fig. 1. Proposed SR strategy in forward operation.

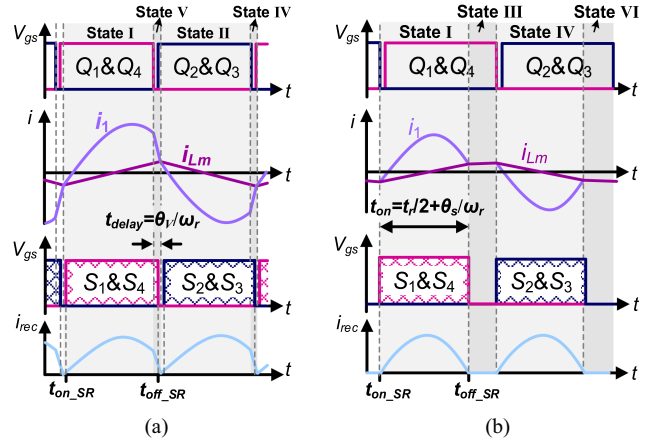


Fig. 2. Waveforms of proposed SR strategy in forward operation. (a) In the above-resonance region. (b) In the below-resonance region.

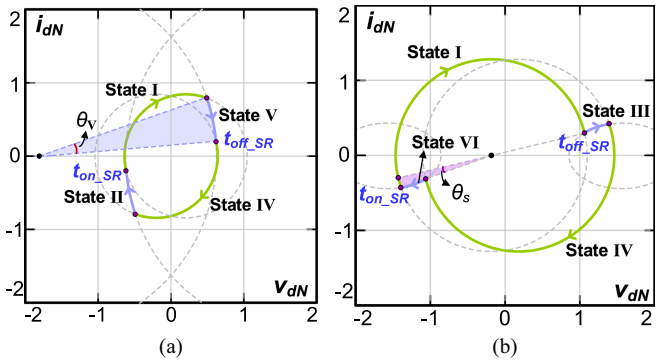


Fig. 3. State-plane diagrams. (a) Above-resonance region. (b) Below-resonance region.

II. Proposed SR Strategy Based On Decoupled Model Using State-Plane Analysis

Fig. 1 shows the proposed SR strategy using the decoupled model of multielement resonance for the SiC CLLC in the forward mode. Fig. 2 illustrates the CLLC waveforms. As shown in Fig. 3, the decoupled model is derived in the state plane to calculate the SR switching instants. In the above-resonance region, the delay time t_{delay} is calculated to determine the SR turn-ON and turn-OFF instants. In the below-resonance region, the SR turn-OFF instant is determined by the SR ON-time t_{ON} and the SR turn-ON instant is synchronized with the turn-OFF instant of the primary-side switch. In practical operation, dead time is considered for the SR driving signals.

Due to the high-voltage and high-frequency capabilities, SiC MOSFETs are used in the bidirectional CLLC converter to achieve a resonant frequency of 300 kHz in the 6.6-kW application. However, the forward voltage of SiC MOSFETs body diode may be six times higher than Si MOSFETs, which will increase the conduction losses largely. Thus, SR is essential in the SiC power devices applications.

The conventional CLLC state-plane model in [19] has four complex coefficients in the two decoupled *LC* resonators. Two pairs of state variables have to be calculated in two coordinate systems. In contrast, the proposed method derives a unified decoupled *LC* resonator that only needs a coordinate system without any coefficient. In [21], due to the numerous calculations, fitting approximation has to be adopted resulting in low SR accuracy. The proposed SR method derives the analytical solutions of SR switching instants, enabling high-precision online computation in a digital signal processor (DSP).

In the reverse operation, the SR strategy remains consistent with the forward operation due to the symmetric CLLC topology.

The advantages of the proposed SR control are as follows.

1) The proposed SR utilizes a decoupled model for geometric calculations in the state plane, which significantly reduces the body diode conduction losses and improves the efficiency.
2) The analytical solutions of SR switching instants are derived from the proposed decoupled model, supporting online calculations and enabling rapid response when the load changes.
3) The proposed SR is calculated in the DSP and no additional hardware is required, which enhances immunity to high *dv/dt* switching noise and eliminates SR false triggering.

III. Proposed Decoupled Model of Multielement Resonance in CLLC Converters

Because there are five resonant elements in CLLC converter, the analytical solutions of SR are difficult to be obtained by the conventional models. This section will derive a unified decoupled model based on time-domain analysis and present the corresponding state-plane equations. All state variables and their normalized values are systematically listed in Table II.

A. Operation Mode in Above-Resonance Region

Fig. 4 shows the CLLC converter and waveforms. Due to the symmetry between positive and negative half-cycle operations, the subsequent analysis will concentrate on the positive half-cycle. In the above-resonance region, as shown in Fig. 4(b), the operation of the CLLC converter within one switching cycle is divided into four states: 1) State I, 2) State II, 3) State IV, and 4) State V.

[t_1, t_2]: This interval corresponds to State I. At t_1, i_1 intersects with i_{Lm}. Afterward, since $i_1 > i_{Lm}$, i_2 flows through the body

TABLE II
CLLC STATE VARIABLES AND NORMALIZATION

Parameters	Symbol	Normalized variable
Input voltage	V_{in}	$V_{inN} = 1$
Output voltage	V_o	$V_{oN} = V_o/V_{in}$
Primary resonant inductor current	i_1	$i_{1N} = i_1 Z_1/V_{in}$
Secondary resonant inductor current	i_2	$i_{2N} = i_2 Z_1/V_{in}$
Primary resonant capacitor voltage	v_1	$v_{1N} = v_1/V_{in}$
Secondary resonant capacitor voltage	v_2	$v_{2N} = v_2/V_{in}$
Magnetizing inductor current	i_{Lm}	$i_{LmN} = i_{Lm} Z_1/V_{in}$
Magnetizing inductor voltage	v_{Lm}	$v_{LmN} = v_{Lm}/V_{in}$
Resonant capacitor voltage difference	$v_d = v_1 - nv_2$	$v_{dN} = v_d/V_{in}$
Resonant inductor current difference	$i_d = i_1 - i_2/n$	$i_{dN} = i_d Z_1/V_{in}$
Switching frequency	f_s	$f_N = f_s/f_r$
Resonant frequency	$f_r = 1/2\pi\sqrt{L_{r1}C_{r1}}$	-
Resonant angular frequency	$\omega_r = 1/\sqrt{L_{r1}C_{r1}}$	-
Characteristic impedance	$Z_1 = \sqrt{L_{r1}/C_{r1}}$	-
Second characteristic impedance	$Z_2 = \sqrt{(L_{r1}+L_m)/C_{r1}}$	-

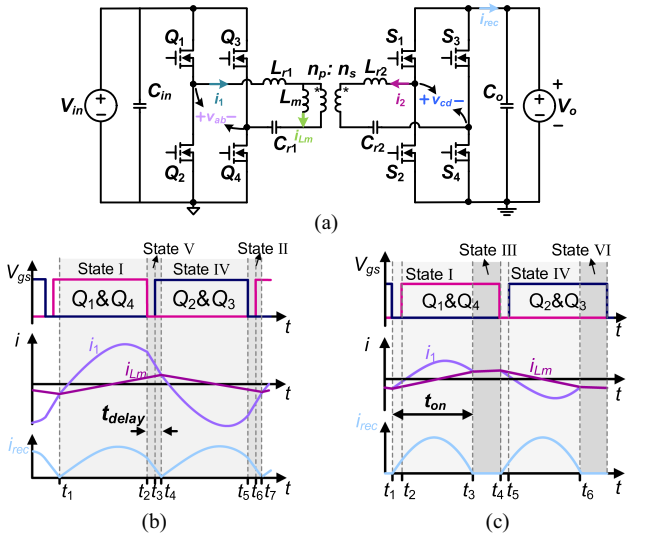


Fig. 4. CLLC converter and waveforms in forward mode. (a) CLLC converter. (b) In the above-resonance region. (c) In the below-resonance region.

diodes of S_1 and S_4. During this state, v_{ab} is equal to $V_{\rm in}$, and v_{cd} is V_o. L_{r1}, C_{r1}, L_{r2}, and C_{r2} are involved in resonance.

[t_2, t_4]: This interval corresponds to State V. At t_2, Q_1 and Q_4 are turned OFF. As i_1 is still greater than i_{Lm}, i_2 continues flowing through the body diodes of S_1 and S_4 and v_{cd} remains at V_o. At t_3, Q_2 and Q_3 turn ON. i_1 flows through the channels of Q_2 and Q_3 and continues to decrease. This state ends when i_1 intersects with i_{Lm} again. In this state, L_{r1}, C_{r1}, L_{r2}, and C_{r2} participate in resonance.

The ideal SR ON-time during the positive half-cycle is from t_1 to t_4. t_1 is the moment when the delay time $t_{\rm delay}$ occurs after the turn-OFF instant of Q_2 and Q_3. Similarly, t_4 is the moment when the delay time $t_{\rm delay}$ occurs after the turn-OFF instant of

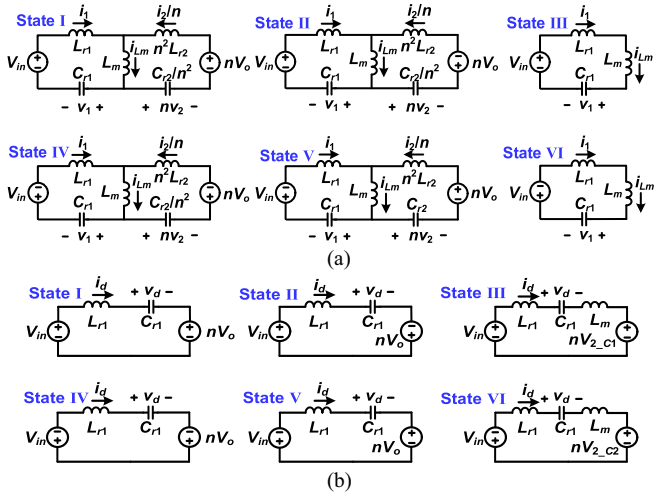


Fig. 5. Circuit diagrams for each state. (a) Equivalent circuits. (b) Decoupled circuits.

Q_1 and Q_4. By calculating $t_{\rm delay}$, the SR drive signal in the above-resonance region can be obtained.

B. Operation Mode in Below-Resonance Region

In the below-resonance region, as shown in Fig. 4(c), the CLLC operation within one switching cycle is divided into four states: 1) State I, 2) State III, 3) State IV, and 4) State VI.

[t_1, t_3]: This interval corresponds to State I. In this state, i_1 is higher than i_{Lm}, so i_2 flows through the body diodes of S_1 and S_4 and v_{cd} is equal to V_o. At t_1, Q_2 and Q_3 turn OFF. Since i_1 is negative, it flows through the body diodes of Q_1 and Q_4 causing v_{ab} to switch to $V_{\rm in}$. At t_2, Q_1 and Q_4 turn ON and i_1 flows through the channels of Q_1 and Q_4. In this state, L_{r1}, C_{r1}, L_{r2}, and C_{r2} participate in the resonance.

[t_3, t_4]: This interval corresponds to State III. At t_3, i_1 and i_{Lm} intersect and i_2 becomes 0. In this state, L_{r1}, C_{r1}, and L_m participate in the resonance. Since i_2 is 0, v_2 remains unchanged on the secondary side.

The ideal SR turn-ON instant is t_1, which is the moment when Q_2 and Q_3 turn OFF. By calculating $t_{\rm ON}$, the SR turn-OFF instant (t_3) can be obtained.

C. Derivation of Decoupled Model and State-Plane Equations

From the abovementioned analysis, the SR switching instants can be obtained through $t_{\rm delay}$ and $t_{\rm ON}$. However, the calculation using conventional time-domain models is highly intricate and is hard to derived the SR analytical solutions. Therefore, a decoupled model is proposed shown in Fig. 5. With the proposed decoupled model using state-plane analysis, the SR analytical solutions can be derived easily with high accuracy.

For States I, II, IV, and V, the resonance involves L_{r1}, C_{r1}, L_{r2}, and C_{r2} and their equivalent circuits are shown in Fig. 5(a). In the CLLC design, L_{r1} is equal to $n^2 L_{r2}$ and C_{r1} is equal to C_{r2}/n^2. Therefore, taking State I as an example, the following

can be derived through KVL:

$$\begin{cases} V_{in} = L_{r1} \cdot \frac{di_1(t)}{dt} + L_m \cdot \frac{d(i_1(t)+i_2(t)/n)}{dt} + v_1(t) \\ i_1(t) = C_{r1} \cdot \frac{dv_1(t)}{dt} \\ nV_o = n^2 L_{r2} \cdot \frac{d(i_2(t)/n)}{dt} + L_m \cdot \frac{d(i_1(t)+i_2(t)/n)}{dt} + nv_2(t) \\ i_2(t) = C_{r2} \cdot \frac{dv_2(t)}{dt}. \end{cases} \tag{1}$$

From (1), it can be obtained that

$$\begin{cases} v_d(t) = v_1(t) - nv_2(t) \\ i_d(t) = i_1(t) - i_2(t)/n \\ V_{\text{in}} - nV_o = L_{r1} \cdot \frac{di_d(t)}{dt} + v_d(t) \\ i_d(t) = C_{r1} \cdot \frac{dv_d(t)}{dt}. \end{cases} \tag{2}$$

From (2), the decoupled model for State I is established, as shown in Fig. 5(b), as well as other states. Since the switching states exhibited by i_d and v_d are consistent with i_1, i_2, v_1 and v_2, i_d, and v_d can be effectively utilized to obtain the SR timings in the state plane. From (2) the trajectory expression of State I can be derived as

$$(v_{dN} - 1 + nV_{oN})^2 + i_{dN}^2 = (V_{d0N} - 1 + nV_{oN})^2 + I_{d0N}^2. \tag{3}$$

The state trajectory expressions for State II, IV, and V are

$$(v_{dN} - 1 - nV_{oN})^2 + i_{dN}^2 = (V_{d0N} - 1 - nV_{oN})^2 + I_{d0N}^2 \tag{4}$$

$$(v_{dN} + 1 - nV_{oN})^2 + i_{dN}^2 = (V_{d0N} + 1 - nV_{oN})^2 + I_{d0N}^2 \tag{5}$$

$$(v_{dN} + 1 + nV_{oN})^2 + i_{dN}^2 = (V_{d0N} + 1 + nV_{oN})^2 + I_{d0N}^2 \tag{6}$$

where I_{d0_N} and V_{d0_N} denote the normalized initial resonant inductor current difference and resonant capacitor voltage difference for each state, respectively. From (3) to (6), the state-plane trajectory of the decoupled model in the above-resonance region can be established.

For State III and State VI, L_{r1}, C_{r1}, and L_m participate in the resonance, while i_2 remains at zero and v_2 maintains a constant value. Therefore, taking State III as an example, the circuit equation can be expressed as

$$\begin{cases} V_{in} = (L_m + L_{r1}) \cdot \frac{di_1(t)}{dt} + v_1(t) \\ i_1(t) = C_{r1} \cdot \frac{dv_1(t)}{dt} \\ v_2(t) = V_{2\_C1} \\ i_2(t) = 0 \end{cases} \tag{7}$$

where V_{2_C1} represents the resonant capacitor voltage on the secondary side during State III. From (7), it can be obtained that

$$\begin{cases} v_d(t) = v_1(t) - nv_2(t) \\ i_d(t) = i_1(t) - i_2(t)/n \\ V_{in} - nV_{2\_C1} = (L_m + L_{r1}) \cdot \frac{di_d(t)}{dt} + v_d(t) \\ i_d = C_{r1} \cdot \frac{dv_d(t)}{dt}. \end{cases} \tag{8}$$

Therefore, the trajectory equations of State III and State VI is

$$(v_{dN} - 1 + nV_{2N\_C1})^2 + \left(\frac{i_{dN}}{Z_1/Z_2}\right)^2$$

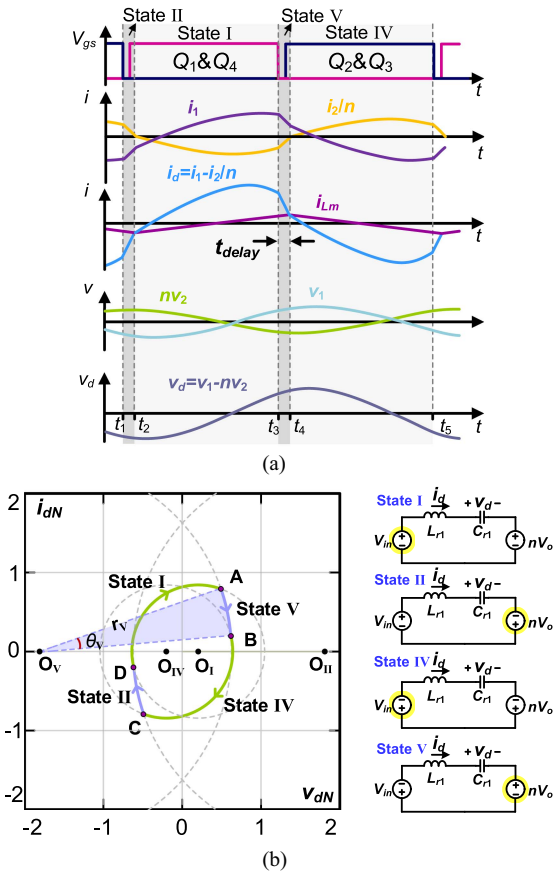


Fig. 6. SR model using proposed decoupled model in above-resonance region. (a) SR waveforms. (b) State-plane trajectory diagram and decoupled circuits.

$$= (V_{d0N} - 1 + nV_{2N\_C1})^2 + \left(\frac{I_{d0N}}{Z_1/Z_2}\right)^2 \tag{9}$$

$$(v_{dN} + 1 + nV_{2N\_C2})^2 + \left(\frac{i_{dN}}{Z_1/Z_2}\right)^2$$

$$= (V_{d0N} + 1 + nV_{2N\_C2})^2 + \left(\frac{I_{d0N}}{Z_1/Z_2}\right)^2 \tag{10}$$

where $V_{2\_N\_C1}$ and $V_{2\_N\_C2}$ denote the normalized resonant capacitor voltage on the secondary side during State III and State VI. From (3), (5), (9), and (10), the state-plane trajectory of the decoupled model in the below-resonance region can be established.

IV. Calculations of SR Switching Instants Based on Proposed Decoupled Model

In this section, the SR analytical solutions are derived. The proposed SR considered the operations above and below the resonance regions, ensuring the accuracy of SR when the operating frequency deviates from the resonant frequency.

A. Calculations of SR Delay Time in Above-Resonance Region

A coordinate system is established with v_{dN} as the x-axis and i_{dN} as the y-axis. The state-plane diagram and the corresponding waveforms are shown in Fig. 6. In the state-plane diagram, O_I,

$O_{\rm II}$, $O_{\rm IV}$, and $O_{\rm V}$ represent the centers of the state trajectories I, II, IV, and V, respectively. x_{OV} is the x-coordinate of $O_{\rm V}$. $\theta_{\rm V}$ is the central angle corresponding to the state trajectory V and $r_{\rm V}$ represents the radius of state trajectory V.

The delay time can be derived as

$$t_{\rm delay} = \theta_{\rm V}/\omega_r. \tag{11}$$

Using geometric principles, $\theta_{\rm V}$ is expressed as

$$\begin{aligned}\theta_{\rm V} = &\arccos\left[\left(V_{dNA} - x_{OV}\right)/r_{\rm V}\right] \\ &- \arccos\left[\left(V_{dNB} - x_{OV}\right)/r_{\rm V}\right]\end{aligned} \tag{12}$$

where V_{dNA} and V_{dNB} denote the normalized resonant capacitor voltage difference at points A and B, respectively.

By substituting the state variables at points A, B, and D into (3) and (6), it can be obtained that

$$\begin{cases}\left(V_{dNA}+1+nV_{oN}\right)^2+I_{dNA}^2=\left(V_{dNB}+1+nV_{oN}\right)^2+I_{dNB}^2 \\ \left(V_{dNA}-1+nV_{oN}\right)^2+I_{dNA}^2=\left(V_{dND}-1+nV_{oN}\right)^2+I_{dND}^2\end{cases}. \tag{13}$$

Points B and D are symmetrical with respect to the origin. Thus, it can be obtained from (13) that

$$nV_{oN} = V_{dNA}/V_{dNB}. \tag{14}$$

I_{oN} can be calculated from the primary side as

$$I_{oN} = \left(nf_N/\pi\right)\int_{t_2}^{t_4}\left[i_{1N}(t) - i_{LmN}(t)\right]dt = 2nf_N V_{1NB}/\pi \tag{15}$$

where $V_{1\ NB}$ denotes the primary resonant capacitor voltage at t_4.

$I_{o\ N}$ can also be calculated from the secondary side as

$$I_{oN} = -\left(f_N/\pi\right)\int_{t_2}^{t_4} i_{2N}(t)dt = -2f_N V_{2NB}/\pi \tag{16}$$

where $V_{2\ NB}$ represents the secondary-side resonant capacitor voltage at t_4. From (15) and (16), V_{dNB} is

$$V_{dNB} = I_{oN}\pi(n+1/n)/\left(2f_N\right). \tag{17}$$

Based on the voltage second balance principle, I_{dNB} is

$$I_{dNB} = Z_1 V_{LmN}/\left(4f_s L_m\right) \tag{18}$$

where V_{LmN} is approximated as nV_{oN}. Thus, I_{dNB} is

$$I_{dNB} = nZ_1 V_{oN}/\left(4f_s L_m\right). \tag{19}$$

$r_{\rm V}$ can be derived as

$$r_{\rm V} = \sqrt{\left(V_{dNB} - x_{OV}\right)^2 + I_{dNB}^2}. \tag{20}$$

By (11), (12), (14), (17), (19), and (20), the SR delay time can be obtained.

B. SR On-Time Calculations in Below-Resonance Region

The state-plane diagram and the corresponding waveforms in the below-resonance region are shown in Fig. 7. In this case, the state-plane trajectory can be divided into four states: 1) State I, 2) State III, 3) State IV, and 4) State VI. In the state-plane

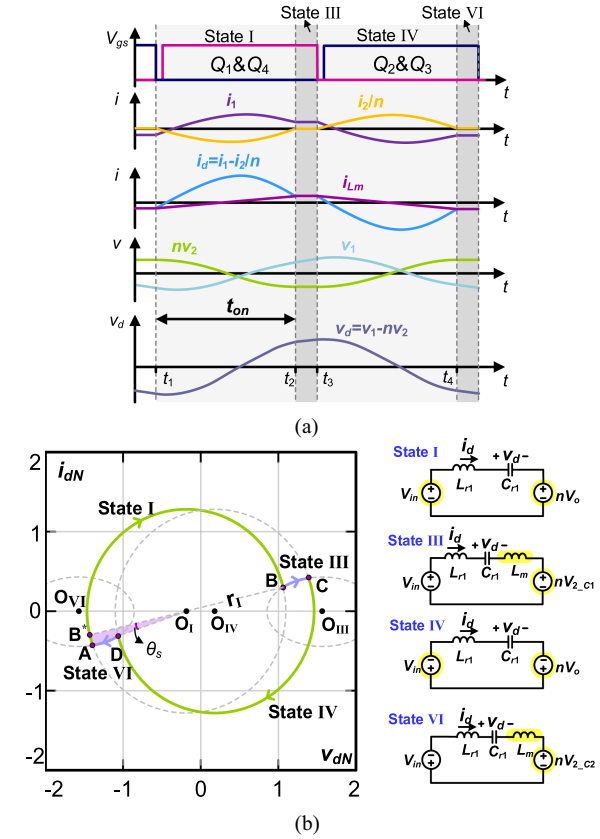


Fig. 7. SR model using proposed decoupled model in below-resonance region. (a) SR waveforms. (b) State-plane trajectory diagram and decoupled circuits.

diagram, point $B*$ is the reflection of point B with respect to point $O_{\rm I}$.

The SR ON-time $t_{\rm ON}$ is

$$t_{\rm on} = 0.5t_r + t_{\theta s} \tag{21}$$

where t_r represents the resonant period and $t_{\theta\ s}$ corresponds to the time from point A to point $B*$ along state trajectory I. $t_{\theta s}$ is

$$t_{\theta s} = \theta_s/\omega_r. \tag{22}$$

It should be noted that $B*$ and B are symmetric about $O_{\rm I}$. Thus, by geometric principles, θ_s can be expressed as

$$\theta_s = \arccos\left[\left(x_{OI} - V_{dNA}\right)/r_{\rm I}\right] - \arccos\left[\left(V_{dNB} - x_{OI}\right)/r_{\rm I}\right] \tag{23}$$

where $r_{\rm I}$ denotes the radius of State I. By substituting the variables at points A, B, and C into (3) and (9), it can be obtained

$$\begin{cases}\left(V_{dNA}-1+nV_{oN}\right)^2+I_{dNA}^2=\left(V_{dNB}-1+nV_{oN}\right)^2+I_{dNB}^2 \\ \left(V_{dNB}-1+nV_{2N\_C1}\right)^2+\left(\frac{I_{dNB}}{Z_1/Z_2}\right)^2 \\ \qquad =\left(V_{dNC}-1+nV_{2N\_C1}\right)^2+\left(\frac{I_{dNC}}{Z_1/Z_2}\right)^2 \\ \left(V_{dNB}-1+nV_{oN}\right)^2+I_{dNB}^2=r_{\rm I}^2\end{cases} \tag{24}$$

where $V_{dN\ C}$ represents the normalized resonant capacitor voltage difference at point C. I_{dNA}, I_{dNB}, and I_{dNC} represent the normalized resonant inductor current difference at points A, B, and C, respectively. Z_1 and Z_2 represent the first and second

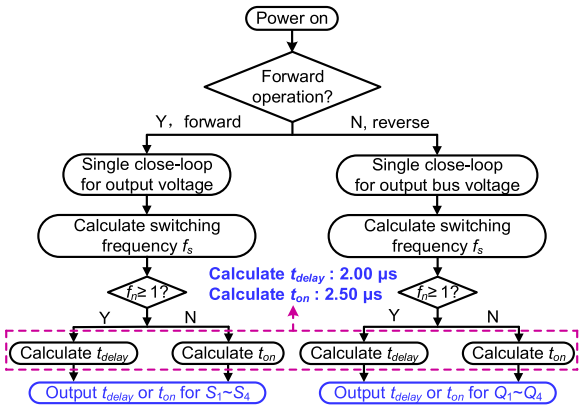


Fig. 8. Flowchart of the proposed SR control algorithm.

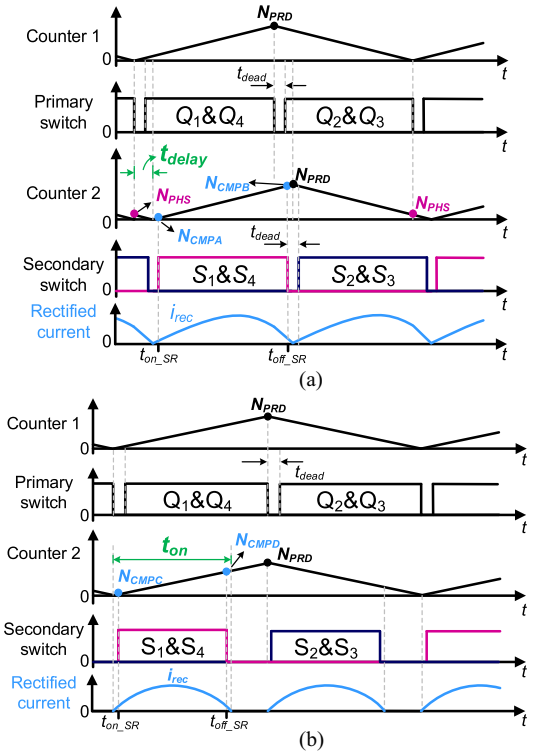


Fig. 9. Detailed CLLC SR driving signals in forward mode. (a) In the above-resonance region. (b) In the below-resonance region.

characteristic impedances, respectively. $V_{2\ N\ C1}$ represents the normalized secondary-side capacitor voltage at t_2.

Since the secondary-side capacitor voltages at points A and B are equal in magnitude but opposite in sign, I_{oN} can be calculated from the secondary side as

$$I_{oN} = -\frac{f_N}{\pi}\int_{t_1}^{t_2} i_{2N}(t)dt = -\frac{f_N}{\pi}\cdot(V_{2NB}-V_{2NA}) = -\frac{2f_N}{\pi}V_{2N\_C1}. \quad (25)$$

Thus, $V_{2\ N\ C1}$ can be substituted into (24) as a known quantity.

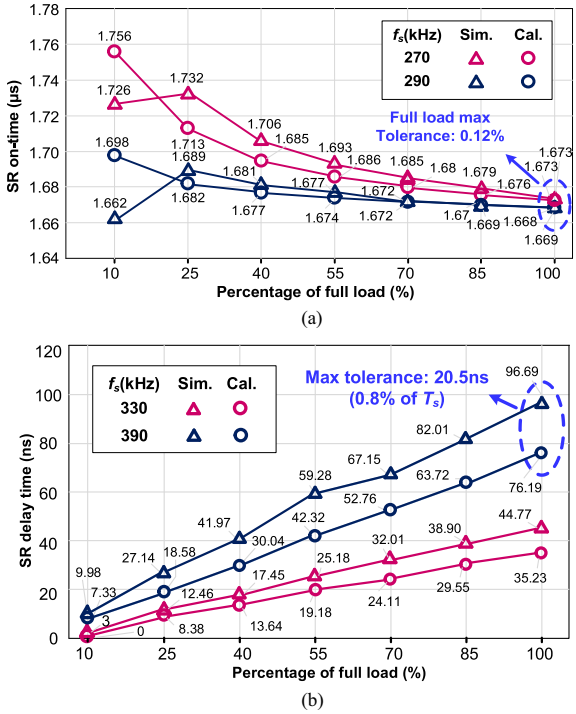


Fig. 10. SR time parameters. (a) Forward operation below f_r: $v_o = 400$ V. (b) Reverse operation above f_r: $v_{bus} = 500$ V.

To solve (24), variables a and b are introduced and expressed as

$$\begin{cases} a = V_{dNB} + V_{dNA} \\ b = V_{dNB} - V_{dNA} \end{cases}. \quad (26)$$

Therefore, solving (24) gives

$$a = \frac{(2nV_{oN}-2)\cdot b}{(Z_1/Z_2)^2\cdot(b-2+2nV_{2NB})-b}. \quad (27)$$

i_{Lm} can be considered constant in State III and State VI. I_{oN} is calculated from the primary side as

$$I_{oN}/n = (f_N/\pi)\int_{t_1}^{t_2}[i_{1N}(t) - i_{LmN}(t)]dt = (f_N/\pi)\cdot(V_{1NB}-V_{1NA}) \quad (28)$$

where $V_{1\ NB}$ and $V_{1\ NA}$ denote the normalized primary-side resonant capacitor voltage at t_2 and t_1, respectively. I_{dNB} can be obtained

$$I_{dNB} = nZ_1V_{oN}/(4f_rL_m). \quad (29)$$

Through (25) and (28), it can be obtained

$$\left(\frac{1}{n}+n\right)I_{oN} = \frac{f_N}{\pi}\cdot(V_{dNB}-V_{dNA}). \quad (30)$$

Herin, b is

$$b = \frac{\pi I_{oN}}{f_N}\cdot\left(\frac{1}{n}+n\right). \quad (31)$$

Through (26), (27), and (31), V_{dNA} and V_{dNB} can be get. Then, by (21), (22), (23) (24), and (29), the SR ON-time can be derived.

Due to the symmetrical topology of the CLLC converter, the aforementioned method is also applicable to the reverse operation.

C. Implementation of Proposed SR

The proposed SR control algorithm is implemented on the TMS320F280049C DSP and the flowchart is depicted in Fig. 8. The SR calculation time is less than 3 μs so the proposed SR can achieve rapid dynamic response.

Taking the forward operation as an example, Fig. 9 illustrates the implementation of proposed SR in the DSP enhanced pulse width modulation (ePWM) module. The ePWM clock f_{clk} is 100 MHz. N_{PRD} corresponding to the switching period (T_s) is

$$N_{\mathrm{PRD}} = T_s f_{clk}. \tag{32}$$

In the above-resonance region, the SR driving signals exhibit a delay time t_{delay} relative to the primary-side driving signals. To lag the phase of Counter 2, N_{PHS} is expressed as

$$N_{\mathrm{PHS}} = t_{\mathrm{delay}} f_{clk}. \tag{33}$$

To prevent the short circuit, t_{dead} is inserted into the SR signals. Thus, N_{CMPA} corresponding to $t_{\mathrm{ON\_SR}}$ is

$$N_{\mathrm{CMPA}} = 0.5 t_{\mathrm{dead}} f_{clk} \tag{34}$$

where N_{CMPB} corresponding to $t_{\mathrm{OFF\_SR}}$ is

$$N_{\mathrm{CMPB}} = N_{\mathrm{PRD}} - 0.5 t_{\mathrm{dead}} f_{clk}. \tag{35}$$

In the below-resonance region, to prevent the short circuit when the f_s is close to f_r, the dead time is also inserted into the SR signals. Thus, N_{CMPC} corresponding to $t_{\mathrm{ON\_SR}}$ is

$$N_{\mathrm{CMPC}} = 0.5 t_{\mathrm{dead}} f_{clk} \tag{36}$$

where N_{CMPD} corresponding to $t_{\mathrm{OFF\_SR}}$ is

$$N_{\mathrm{CMPD}} = t_{\mathrm{on}} f_{clk} - 0.5 t_{\mathrm{dead}} f_{clk}. \tag{37}$$

V. Simulations and Tolerances Analysis

The SR time parameters calculated by the proposed decoupled model shows excellent agreement with simulation results. Tolerance analysis of circuit parameters reveals minimal deviations, further validating the SR implementation.

A. Comparisons Between Simulations and Proposed SR

Fig. 10 depicts the comparative results between the simulations and the proposed SR. The proposed SR can support the maximum switching frequency 390 kHz. The maximum tolerance is as low as 0.12% at full load in the forward mode and 0.8% in the reverse mode. Therefore, the proposed decoupled model simplifies the computational process while maintaining high SR accuracy.

B. Analysis of Parameter Tolerances

Fig. 11 shows the SR delay time tolerances caused by component variations in the forward above-resonance operation. A 10% tolerance in the primary resonant inductance L_{r1} causes 18.33 ns

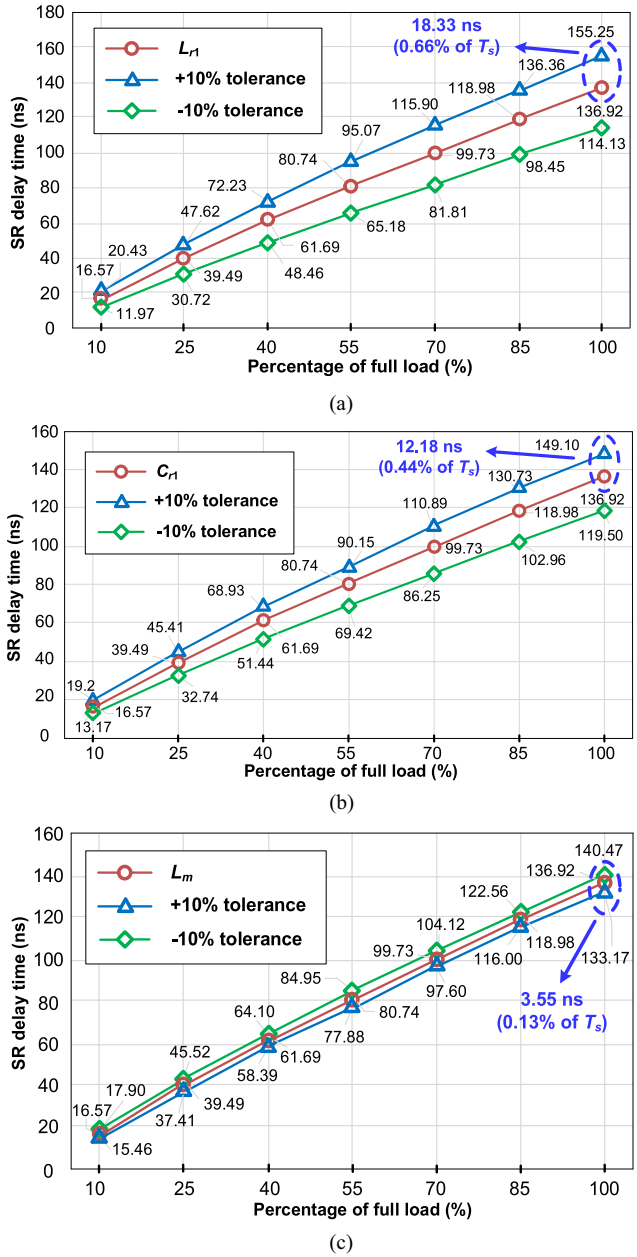


Fig. 11. Tolerances in forward operation: v_o = 400 V, f_s = 360 kHz. (a) Primary resonant inductor. (b) Primary resonant capacitor. (c) Magnetizing inductor.

deviation (0.66% of 2.778 μs period), while 10% tolerances in the resonant capacitance C_{r1} and magnetizing inductance L_m yield 12.18 ns (0.44%) and 3.55 ns (0.13%) deviations, respectively. Thus, the impact of circuit element tolerances is negligible.

Fig. 12 shows the SR ON-time tolerances in the reverse below-resonance operation. With 10% tolerances, the secondary resonant inductance L_{r2} causes 2.6% variation, resonant capacitance C_{r2} 2.9%, and secondary-side magnetizing inductance L_{m1} only 0.07%, demonstrating the robustness of the proposed SR method.

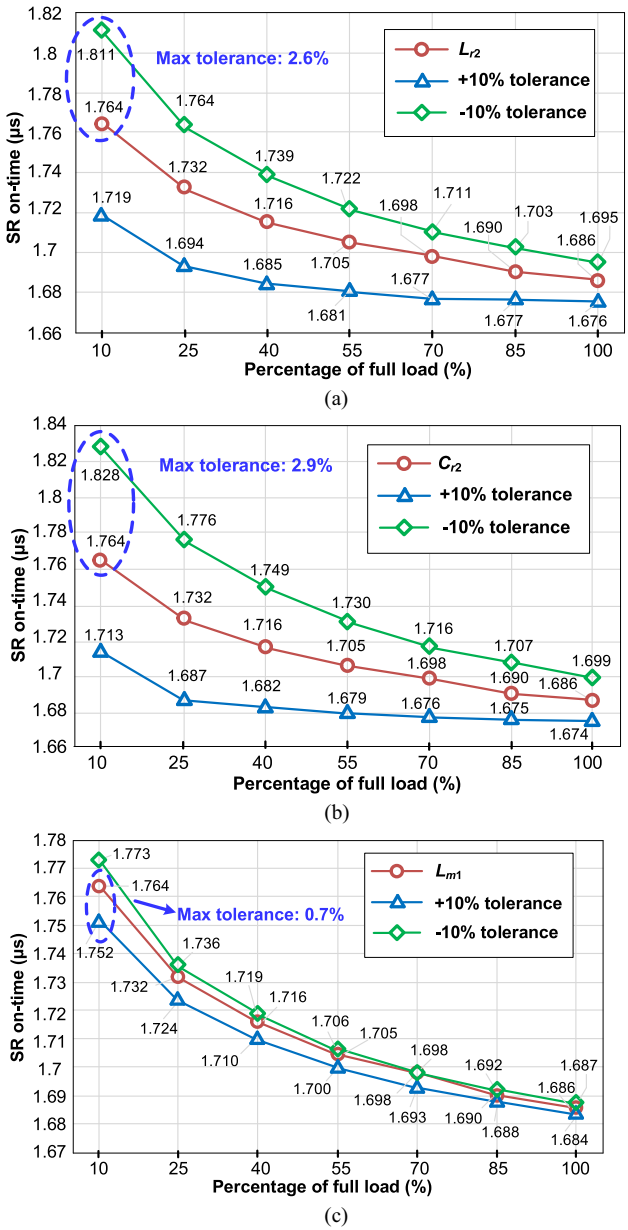


Fig. 12. Tolerances in reverse operation: $v_{bus} = 500$ V, $f_s = 280$ kHz. (a) Secondary resonant inductor. (b) Secondary resonant capacitor. (c) Secondary magnetizing inductor.

C. CLLC Power Loss Analysis

The CLLC power losses at different operating frequencies are shown in Fig. 13. In Fig. 13(a), when the CLLC operates at the resonant frequency (300 kHz), the total loss is minimum. Compared with the power loss at the switching frequency of 360 kHz, the turn-OFF losses of the primary-side switches Q_1–Q_4 are reduced significantly. In Fig. 13(b), the total loss is also minimum when the CLLC converter operates at 300 kHz.

VI. Experimental Results and Discussion

A. Experimental Prototype

To validate the proposed SR strategy, a bidirectional full-SiC CLLC charger prototype was built shown in Fig. 14.

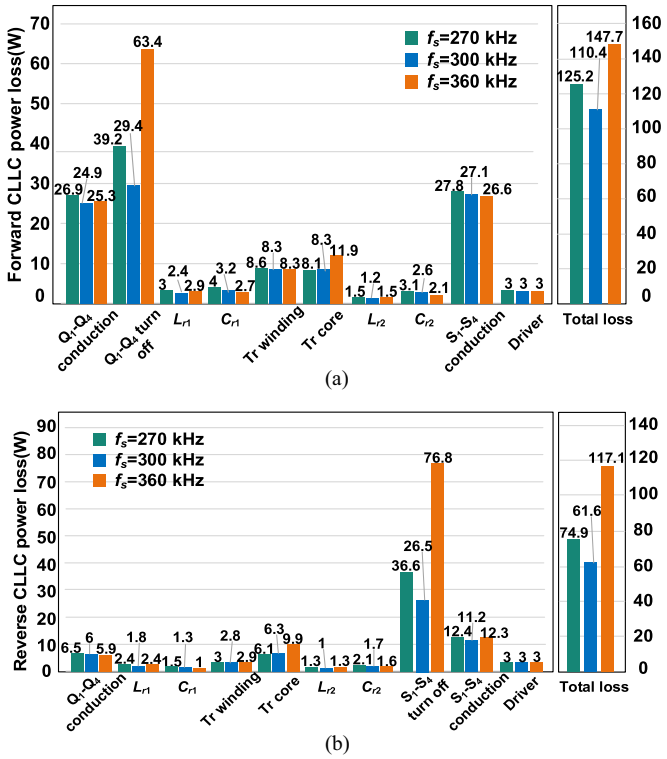


Fig. 13. Power loss analysis. (a) Forward operation: $v_{bat} = 400$ V, $P_o = 6.6$ kW. (b) Reverse operation: $v_{bus} = 400$ V, $P_o = 3.3$ kW.

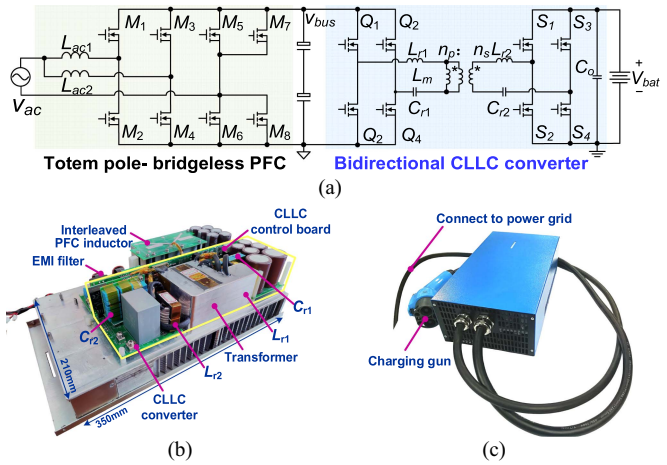


Fig. 14. 6.6-kW bidirectional charger. (a) Topology. (b) PCB structure. (c) Assembled prototype.

Observed from Fig. 14, the charger integrates a totem pole bridgeless PFC converter as the ac–dc stage and a CLLC resonant converter as the dc–dc stage. 1200-V 30-mΩ SiC MOSFETs are used in the primary side and 650-V 20-mΩ SiC MOSFETs are adopted in the secondary side. The key parameters are summarized in Table III.

B. Proposed SR in Forward Mode

Fig. 15 illustrates the proposed SR in the forward mode. From Fig. 15(a) and (b), S_1 leads and lags the primary-side switch Q_1 when f_s is 340 kHz in the above-resonance region. In the

TABLE III
SPECIFICATIONS OF SIC BIDIRECTIONAL CLLC CHARGER

Item	Values
Operating conditions	V_{bus}: 380 V-700 V, V_{bat}: 200 V-500 V P_{charge}: 6.6 kW, $P_{discharge}$: 3.3 kW
Resonant inductor L_{r1}	Core: EC50A3, DMR96 (DMEGC) Inductance: 8.7 μH
Resonant inductor L_{r2}	Core: EC33A, DMR96 (DMEGC) Inductance: 4.3 μH
Transformer T	Core: EE70, DMR96 (DMEGC) Turns ratio: 10:7 Magnetizing inductor L_m: 36.9 μH
Resonant capacitor C_{r1}	B32652A2152, 1.5 nF × 21 (film, TDK)
Resonant capacitor C_{r2}	B32652A2222, 2.2 nF × 29 (film, TDK)
Primary SiC devices Q_1-Q_4	IMW120R030M1H 30 mΩ @ V_{GS} = 18 V, I_D = 56 A, T_J = 25 °C Reverse diode forward voltage: V_{SD} = 4.1 V@ I_{SD} = 25 A, T_J = 25 °C
Secondary SiC devices S_1-S_4	IMW65R020M2H 20 mΩ @ V_{GS} = 18 V, I_D = 46.9 A, T_J = 25 °C Reverse diode forward voltage: V_{SD} = 4.3 V@ I_{SD} = 46.9 A, T_J = 25 °C
Resonant frequency f_r	300 kHz
Switching frequency f_s	260 kHz-390 kHz
DSP	TMS320F280049C (TI)

below-resonance region at 275 kHz under full load, precise SR is also achieved to validate the proposed SR control. In Fig. 16, the full-load maximum of the SR ON-time tolerance is only 1.52%, validating the accuracy of proposed SR.

Fig. 17 demonstrates the loads step up from 1 kW to 5 kW by using the proposed SR control. The delay time calculated from the proposed decoupled model varies with load changes, which confirms the effectiveness of the proposed SR method during dynamic transitions.

C. Proposed SR in Reverse Mode

Fig. 18 illustrates the SR waveform during reverse operation. In the below-resonance region, as the load ranges from 25% to 100% of full load, the proposed SR maintains effective operation. In the above-resonance region at full load, the proposed SR is also to achieve precise control at 340 kHz. In Fig. 19, the maximum tolerance of the SR delay time is only 0.4%, validating the accuracy of proposed SR in the reverse mode.

Fig. 20 shows the reverse operation under consecutive load step-changes from 3 kW to 1 kW and back to 3 kW. In Fig. 20(b) and (c), the SR ON-time adaptively tracks the load changes. Therefore, the proposed SR strategy achieves accurate SR in the dynamic response.

D. Efficiency Measurements and Comparisons: Figs. 21 and 22 present the measured CLLC efficiencies using the YOKOGAWA WT1800 power analyzer at 300 kHz. The proposed SR achieves 98.19% at 6.6 kW (v_{bat} = 400 V) in the forward mode and 98.20% at 3.3 kW (v_{bus} = 400 V) in the reverse mode. The efficiency improvements are up to 0.63% and 0.45% over [9] in the forward and reverse modes. Additionally, the light-load (0.8 kW) efficiency at 400 V of the bus voltage is improved by 2.15% in the reverse mode.

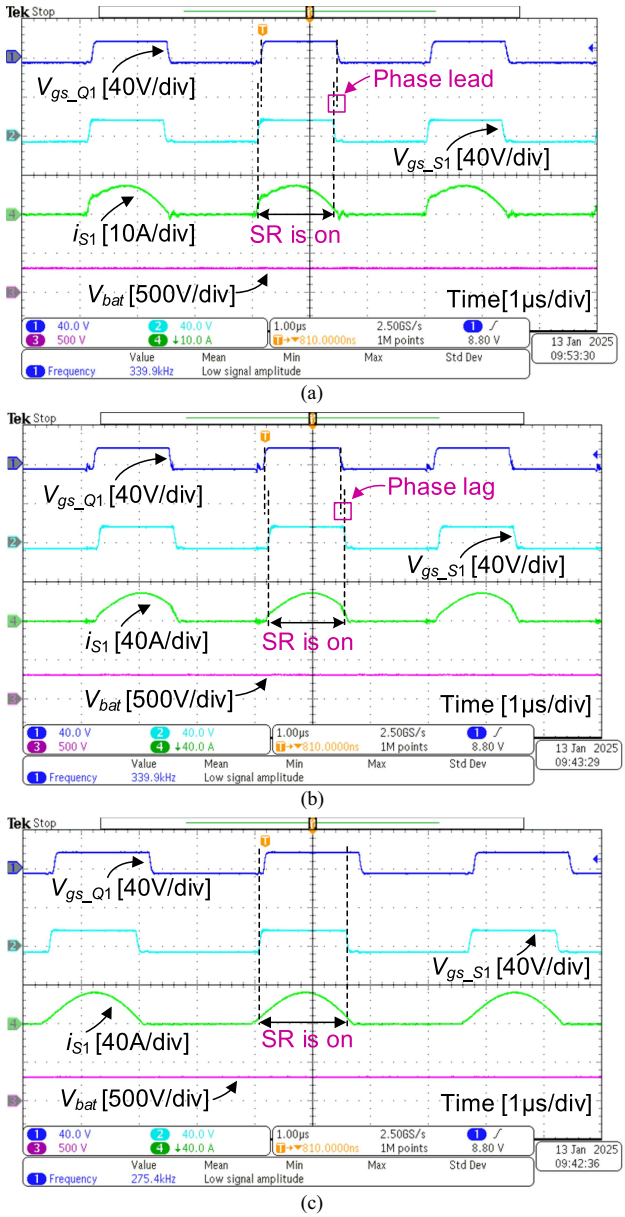


Fig. 15. Forward SR. (a) 25% of full load: v_{bat} = 320 V, f_s = 340 kHz. (b) Full load: v_{bat} = 320 V, f_s = 340 kHz. (c) Full load: v_{bat} = 320 V, f_s = 275 kHz.

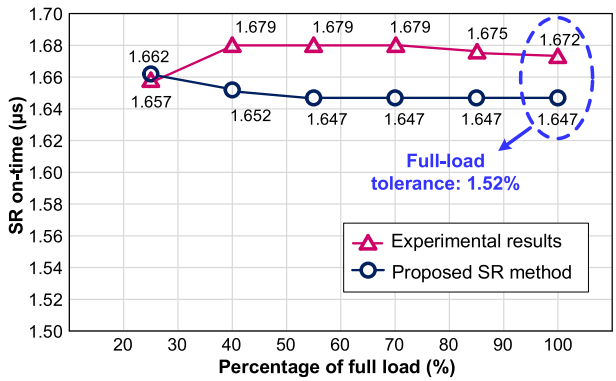


Fig. 16. Comparison of SR conduction time in forward mode.

TABLE IV
COMPARISONS OF CLLC SR METHODS

Ref	Implementation approaches	Extra components	Resonant frequency	Charging efficiency		Discharging efficiency
				Full load	Peak efficiency	
[9]	Time-domain analytical model	None	300 kHz	97.56%@6.6 kW	97.73%@4.6 kW	97.75%@3.3 kW
[10]	Inductance voltage sensing	Voltage sensing coil	110 kHz	96.47%@3 kW	97.1%@1.4 kW	-
[12]	Resonant current sensing	Diodes and sensors	73 kHz	97.25%@7.5 kW	-	97%@6.6 kW
[18]	Fixed SR based on parameter design	None	69.5 kHz	97.14%@0.88 kW	97.58%@0.59 kW	-
[20]	Time-domain fitting formulas	None	50 kHz	96.68%@2 kW	97.15%@1.5 kW	-
[22]	Polynomial fitting	None	65 kHz	97%@1.2 kW	97.2%@0.6 kW	97.2%@0.6 kW
[24]	Quantitative state trajectory model	None	70 kHz	97.08%@0.6 kW	97.43%@0.4 kW	-
Proposed	Decoupled model	None	**300 kHz**	**98.19%@6.6 kW**	**98.35%@4.6 kW**	**98.20%@3.3 kW**

The significance of bold values to emphasize the index of proposed method in this article.

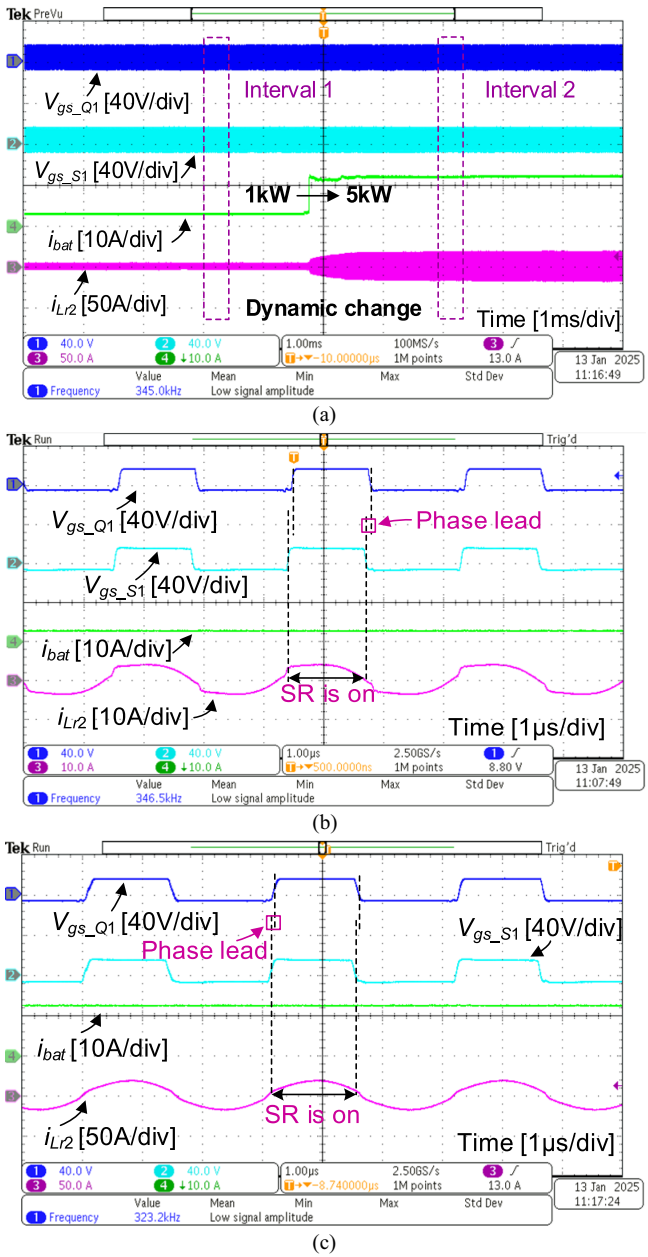


Fig. 17. Load change in forward mode: $v_{bat} = 400$ V. (a) From 1 kW to 5 kW. (b) Zoomed-in interval 1. (c) Zoomed-in interval 2.

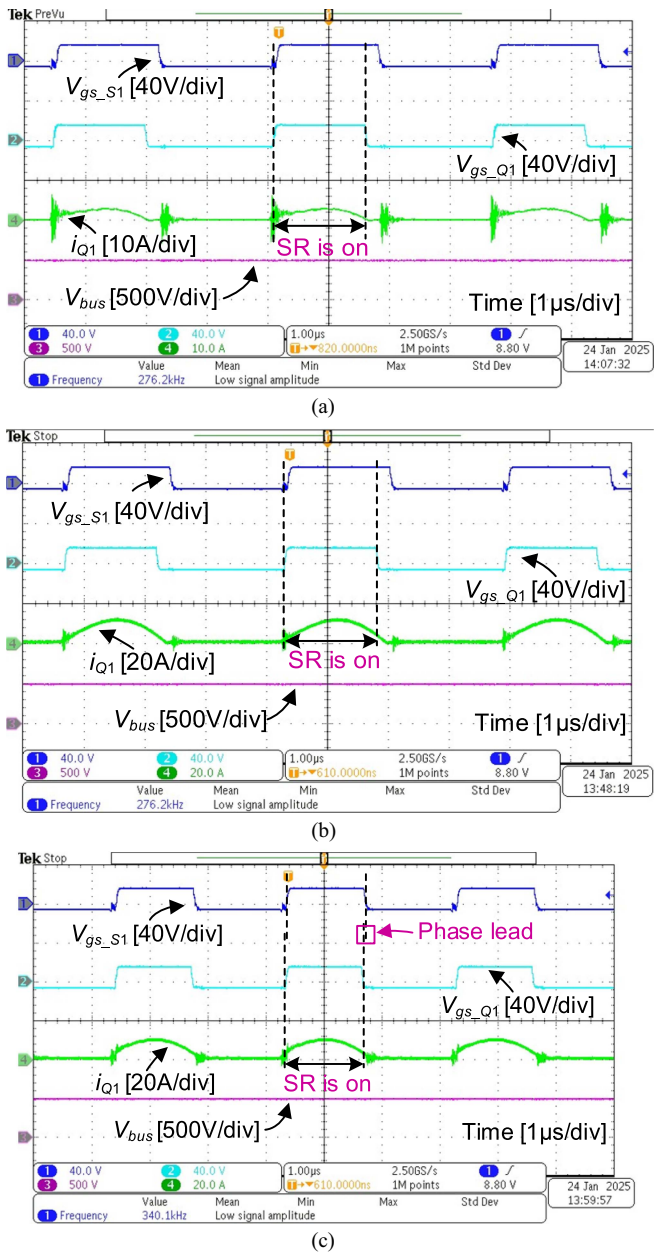


Fig. 18. Reverse SR. (a) 25% of full load: $v_{bus} = 500$ V, $f_s = 276$ kHz. (b) Full load: $v_{bus} = 500$ V, $f_s = 276$ kHz. (c) Full load: $v_{bus} = 320$ V, $f_s = 340$ kHz.

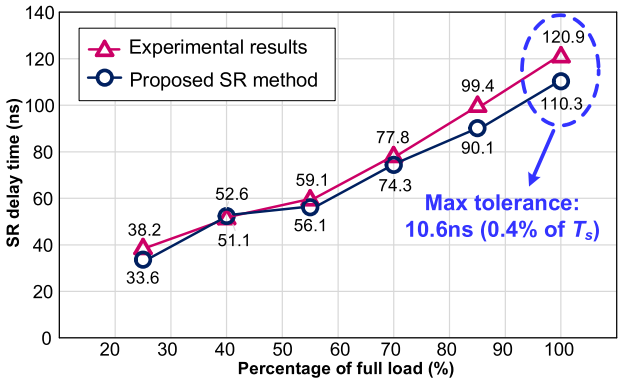


Fig. 19. Comparison of SR delay time in reverse mode.

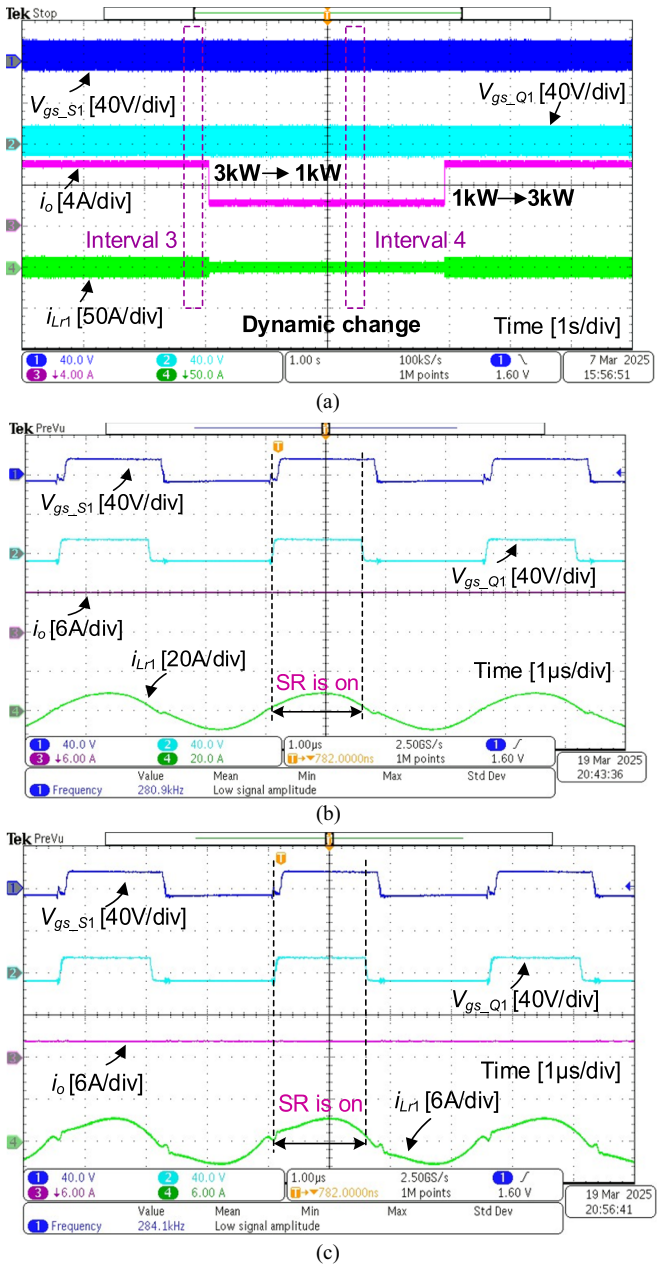
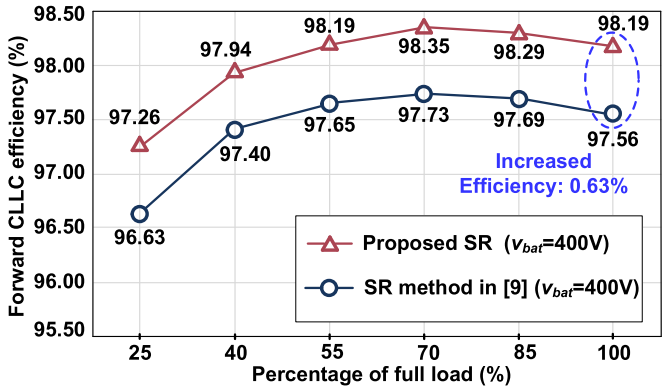
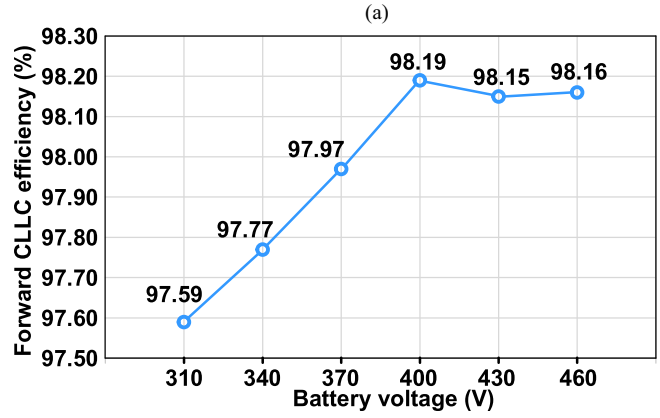


Fig. 20. Dynamic load change in reverse mode: $v_{bus} = 400$ V. (a) From 3 kW to 1 kW and back to 3 kW. (b) Zoomed-in interval 3. (c) Zoomed-in interval 4.



(a)



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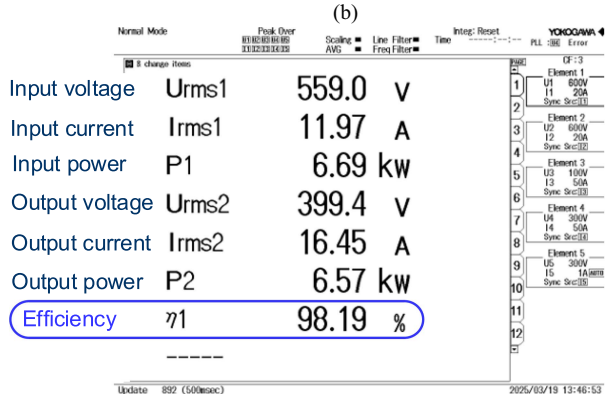


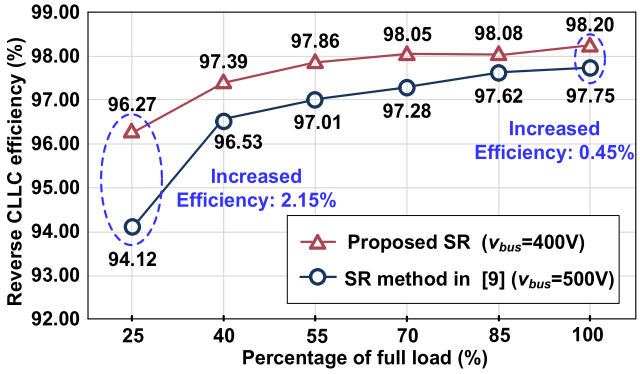
(c)

Fig. 21. Measured forward efficiency: $f_s = 300$ kHz. (a) $v_{bat} = 400$ V. (b) Different output battery voltages: $P_o = 6.6$ kW. (c) Power analyzer image at 6.6 kW.

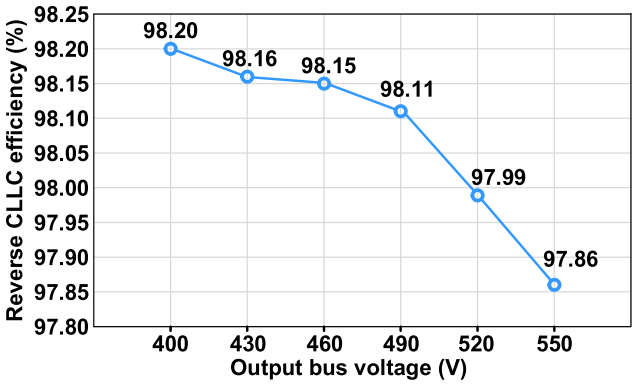
Table IV gives the comparisons of the CLLC SR methods. Compared to existing SR methods, the proposed SR is implemented easily and can achieve higher efficiency without additional sensing components.

VII. Conclusion

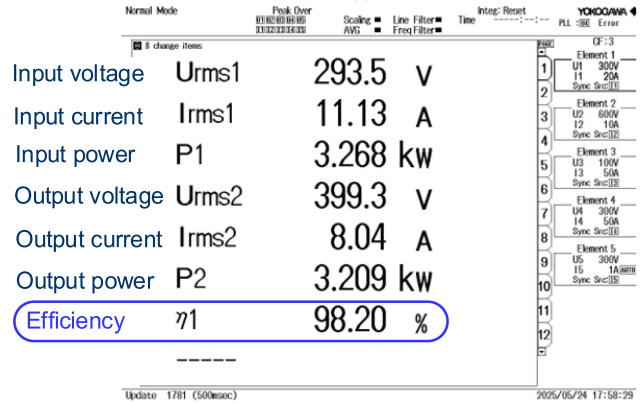
This article proposed a decoupled model of multielement resonance for SR utilizing state-plane analysis in bidirectional high-voltage SiC CLLC converters. In the above-resonance region, the SR control is implemented using the delay time calculated from the proposed decoupled model. In the below-resonance region, the SR turn-OFF instant is controlled by the SR ON-time and the SR turn-ON instant is synchronized with the turn-OFF



(a)



(b)



(c)

Fig. 22. Measured reverse efficiency: $f_s = 300$ kHz. (a) Different loads. (b) Different output bus voltages: $P_o = 3.3$ kW. (c) Power analyzer image at 3.3 kW.

instant of primary-side switches. The proposed method achieves precise SR with low computational complexity. Furthermore, the analytical solutions are derived from the proposed decoupled model, facilitating the online calculations, which enables robust performance under dynamic operations.

The proposed SR utilizes existing dc measurements (input/output voltage/current), which eliminates high-frequency signal detection requirements and demonstrates high noise immunity compared to conventional methods. In contrast to existing model-based approaches, the proposed method developed a decoupled model to reduce the computational burden caused by the five resonant elements in CLLC converters. The proposed SR can be implemented online with high accuracy.

Through the parameter tolerance analysis, the SR tolerance is as low as 0.13% with 10% parameter variations. With the proposed SR at full load, the forward CLLC efficiency is up to 98.19% and the reverse CLLC efficiency is 98.20% . Compared to the conventional time-domain SR method, the efficiency improvements are as high as 0.63% and 0.45% in the forward and reverse modes, respectively.

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