A Current-Efficient Fast-Transient PMOS LDO With Aux-Path Push-Pull Buffer and Shaped-Hybrid-Bias Technique Achieving 8.15 ps FoM

Xin-Ce Gong, *Student Member, IEEE*, Jian-Jun Kuang, *Student Member, IEEE*, Xin Ming, *Member, IEEE*, Shi-Ting Hu, Zheng-Hao Liu, Zhi-Yi Lin, *Member, IEEE*, Mo Huang, *Senior Member, IEEE*, and Bo Zhang, *Senior Member, IEEE*

***Abstract*—A current-efficient and fast-transient p-channel metal-oxygen-semiconductor (PMOS) low-dropout regulator designed for high-speed high-current load transient in mobile applications is presented. A low-power aux-path push-pull buffer is applied to provide both high push and pull current for gate-capacitance (C_{gP}) of power field-effect transistor (FET), hence significantly suppressing both undershoot and overshoot, and the aux-path further accelerates the transient response. Meanwhile, a shaped-hybrid-bias (SHB) circuit, implementing a novel hybrid scheme, regulates the range of error amplifier's bias current and combines the advantage of adaptive bias and dynamic bias. DC accuracy and stability under heavy load are well-maintained. Thus, a higher mirror ratio can be utilized, which contributes to achieving higher bandwidth and response speed. This circuit was implemented in a 0.18-μm CMOS process and occupies a silicon area of 400 $\times$ 250 μm^2. With a 1 μF output capacitor and 18 μA quiescent current, load transient test results with 200 mV V_{DROP} show that it features 19/14 mV of undershoot/overshoot at load transient under 270 mA load step (t_{edge} = 300 ns).**

***Index Terms*—Adaptive bias, current clamp techniques, dynamic bias, fast transient low-dropout (LDO), push-pull buffer.**

I. Introduction

THE demand for fast transient response low-dropout (LDO) with low quiescent current is increasing, driven by the development of mobile devices. To meet this demand under stringent efficiency constraints, numerous research efforts have focused on low-quiescent-current LDO design techniques [1], [2], [3], [4], [5]. N-channel metal-oxygen-semiconductor (NMOS) LDO shows good transient performance [1], [3], [6], however, it typically requires a larger dropout voltage compared with p-channel metal-oxygen-semiconductor (PMOS) LDO [7] or requires extra charge pump [1], [8]. Fig. 1 shows the typical structure of PMOS LDO with off-chip capacitor [3], where the buffer is used to drive the large gate capacitance (C_{gP}) of power field-effect transistor (FET) (M_P) and isolates the error amplifier (EA)'s output from C_{gP} for wideband design [9]. Adaptive bias is often employed for EA to provide high transconductance and increase the bandwidth of LDO under heavy load conditions while keeping high current-efficiency under light load. Consequently, effective design hinges on addressing two key points.

1) For conventional buffer design, drive capability of buffer is proportional to quiescent current [3], [10], demanding high slew-rate typically entails high static current consumption in the buffer, leading to low current efficiency, which is not desired in portable device. A common source circuit with diode load can be used as buffer [11], but the performance is not satisfactory. While Zhao et al. [5] proposed a high slew-rate efficiency low-impedance transient current enhanced (LTE) buffer, however, the LDO consumes a high quiescent current of 48 μA. The authors in [12], [13], [14], [15], and [16] used super source follower as buffer to drive the gate capacitance and push gate pole to high frequency with inner feedback loop of their buffer, however, these buffer's positive slew rate is restricted by the biasing

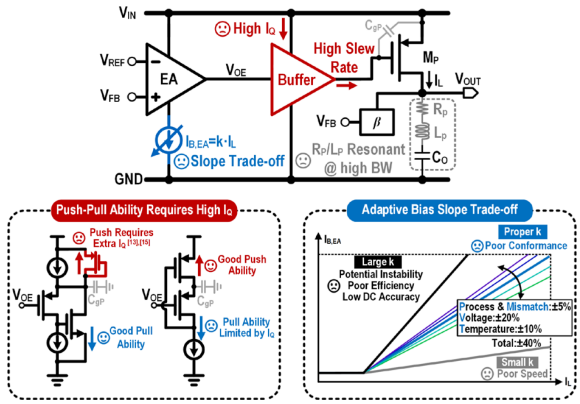

Fig. 1. Typical structure of PMOS LDO with a bucky off-chip capacitor.

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Xin-Ce Gong, Jian-Jun Kuang, Shi-Ting Hu, Zheng-Hao Liu, Zhi-Yi Lin, and Bo Zhang are with the State Key Laboratory of Electronic Thin Films and Integrated Devices, UESTC, Chengdu 611731, China.

Xin Ming is with the State Key Laboratory of Electronic Thin Films and Integrated Devices, UESTC, Chengdu 611731, China, also with the Shenzhen Institute for Advanced Study, UESTC, Shenzhen 518000, China, and also with the Engineering Research Center of Advanced Power and RF Devices and Integration, Ministry of Education, Chengdu 611731, China (e-mail: mingxin@uestc.edu.cn).

Mo Huang is with the Institute of Microelectronics, Department of Electrical and Computer Engineering (ECE), Faculty of Science and Technology (FST), University of Macau, Macao 999078, China.

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condition, specifically the limited current available for sourcing the gate capacitance during a downward load transient. Though adaptive bias for buffer can relieve this issue [14], [15], [16], the adaptive bias in buffer will deteriorate the inner loop stability due to changes in the loop gain dynamics as the bias currents adapt abruptly. Park et al. [17] presented a push-pull buffer, but voltage headroom is sacrificed due to the requirement of stacking transistor in translinear loop. Wang and Mercier [18] used digital-like structure to achieve fast transient response, but results in significant output voltage ripple. The authors in [14] and [19], presented LDO with flipped-voltage-follower (FVF)-liked output stage, with the high bandwidth local feedback loop, the response speed is satisfactory, but it requires extra current to build the local FVF feedback loop. Yang et al. [20] presented a design of close-loop unit-gain buffer, however the structure suffers from complexity and imposes a substantial quiescent current. Consequently, designing a buffer capable of delivering high slew rate with low quiescent current, while maintaining stability and minimizing voltage headroom loss, remains a significant challenge.

2) Adaptive bias technology can significantly enhance current efficiency under light load by regulating the quiescent current to nanoampere (nA) level [2], [21]. The design challenge lies in selecting the optimal current mirror ratio k (defined as the ratio of bias current and load current). If k is excessively large, as shown in Fig. 1(c), although the adaptive bias circuits can expend the EA's bandwidth [3], [4], [10], [22], they introduce risk of potential instability due to poor control of range of the EA's bias current as well as loop unit-gain bandwidth (UGB). Moreover, with excessive large k, the current efficiency deteriorates, and dc accuracy degrades due to reduced loop gain. Conversely, an insufficiently small k results in negligible adaptive effect and provides minimal acceleration to the transient response. Therefore, optimizing k is nontrivial. Even with careful selection, process, voltage and temperature (PVT) and mismatch variations inevitably impair performance predictability and circuit robustness. The drift of the mirror ratio mainly comes from PVT and mismatch. Among them, the impact of process corner and mismatch is generally contained within 5%, and the impact of temperature is moderate (±10%). The biggest source of error is voltage difference, which is because the $V_{\rm DS}$ of the mirror FET and the power FET are not the same; and under heavy load, the power FET of LDO with compact size often works in the linear region, which makes the mirror ratio error larger. Among these factors, the changes in corner and mismatch are random, and the total contribution after superposition is small, while the effects of temperature and voltage can be superimposed. Consequently, considering the combined effects, k can vary up to ±40% under worst-case.

This work proposed an LDO with aux-path push-pull (AP^3) buffer and shaped-hybrid-bias (SHB) EA schemes to cope with design issues mentioned above. It can deliver up to 270-mA load current with 5 V devices and features good transient performance for both light-to-heavy (L-H) and heavy-to-light (H-L) load transient, where the quiescent current is only 18 μA This regulator incorporates two important techniques.

1) An AP^3 buffer is proposed to extend bandwidth to 4- times higher. The proposed AP^3 buffer is based on a close-looped push-pull scheme and can push the gate pole to two times higher compared with conventional super source followers. The HPF-based aux-path technique doubles the gain and extends bandwidth. With the aux-path techniques and push-pull techniques, the bandwidth is extended to four times higher, respectively, with the same quiescent current.
2) A SHB technique is proposed to balance speed and loop stability by regulating the range of bias current. It combines the advantages of adaptive bias and dynamic bias techniques, achieving both high bandwidth under heavy load condition and fast response during load transient. A current shaper circuit is proposed to resolve the PVT and mismatch problem and guarantee the loop gain and stability under heavy load conditions.

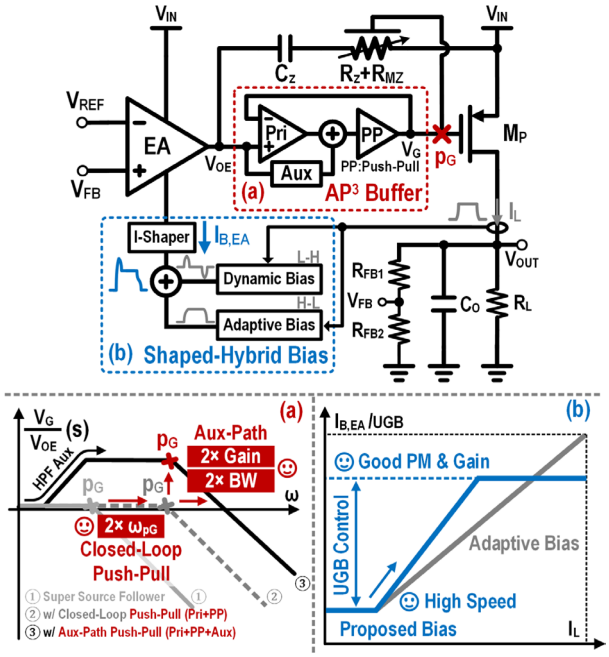


Fig. 2. Proposed LDO simplified system structure, (a) effect of AP^3 buffer and (b) conception of proposed shaped-hybrid-bias technique.

The rest of this paper is organized as follows. Section II describes the concept and design of the proposed LDO regulator and performance validation result. Section III shows the experimental result and method, as well as chip photo. Finally, Section IV concludes this article.

II. Design of Proposed LDO

Fig. 2 shows the structure of the proposed fast load transient LDO with low quiescent current. As shown in Fig. 2(a), an AP^3 buffer is employed to drive the power FET and extend the bandwidth of LDO. From the perspective of frequency domain, the proposed current-efficient push-pull techniques drive the gate pole $p_{\rm G}$ to high-frequency and the HPF based aux-path techniques extend the bandwidth of LDO to two times higher with the same quiescent current. From the perspective of time domain, the proposed current-efficient techniques provide the push-pull ability at the gate of power FET and improve the transient response ability of LDO.

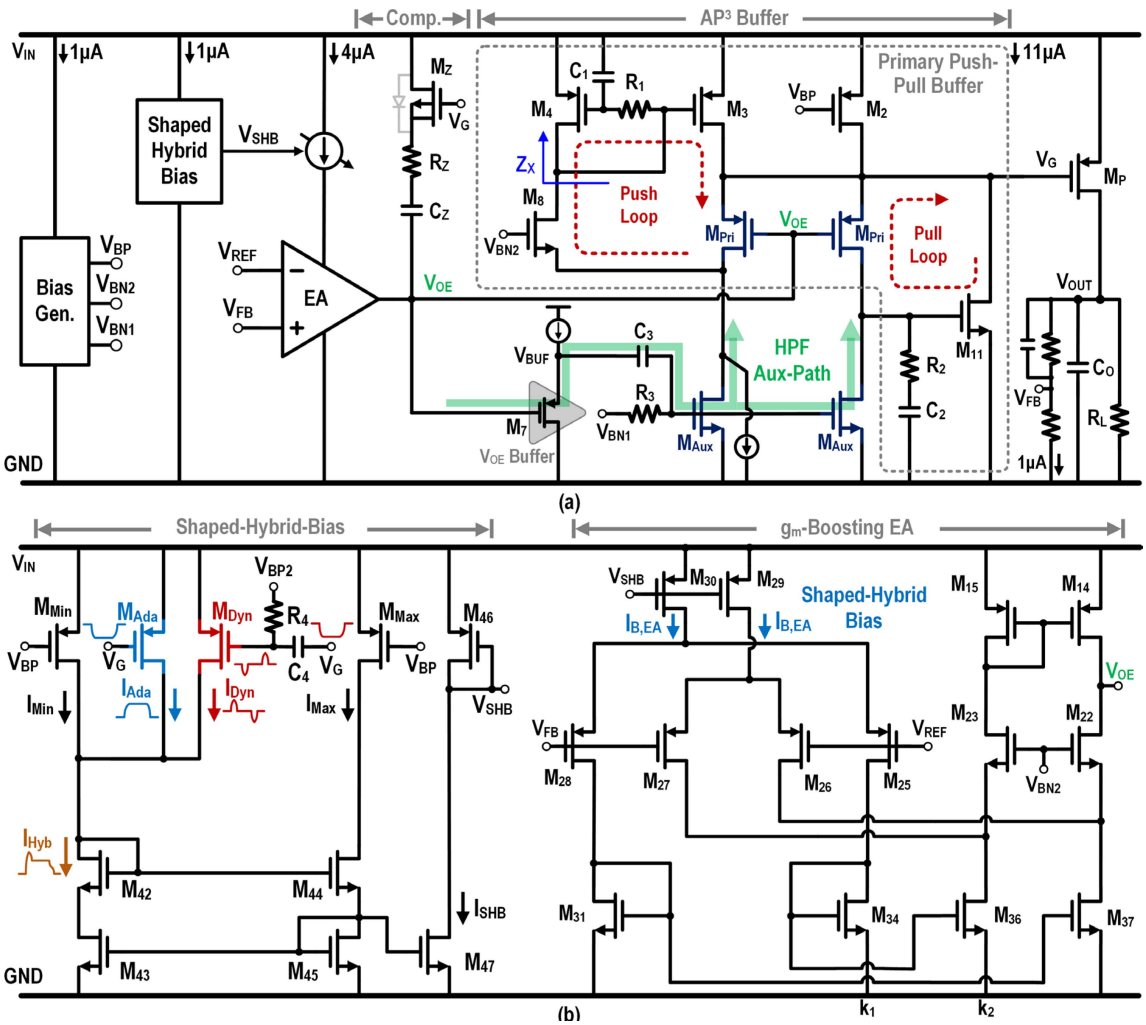


Fig. 3. (a) Schematic of proposed LDO with AP³ buffer. (b) Schematic of proposed SHB circuit and g_m-boosting EA.

As shown in Fig. 2(b), an SHB circuit senses the output current and combines the advantages of conventional adaptive bias scheme and dynamic bias scheme where EA's bias current is proportional to load current and slope of load current, respectively. Process variations make it challenging to maintain an optimal adaptive bias ratio (k). Conventional schemes suffer from unpredictable and potentially excessive variations in LDO bandwidth over PVT corners. A salient feature of the proposed bias circuit is the maximum bias current is automatically controlled to the preset values. During the L-H load transient, the hybrid bias circuit will response with low delay time and suppress the undershoot voltage. Furthermore, it ensures sufficient bias current and maintains loop bandwidth during H-L load transient to limit output overshoot.

An adaptive Type-II compensator is applied for loop stability under wide load current range, and it will precharge the compensation capacitor after H-L load transient with the reverse-connected body diode of M_Z. With these techniques, an LDO with low quiescent current and fast transient response is achieved. Fig. 3 shows the detailed schematic of proposed LDO [23]. The C_Z and R_Z are 1.5 pF and 150 kΩ, respectively. $C_1 \sim C_3$ are 1 pF and $R_1 \sim R_3$ are 500 kΩ. The C_{gP} is around 47 pF.

A. AP³ Buffer

Buffer design mainly focuses on high slew rate and bandwidth with low quiescent current. These determine the output voltage variation during load transient and response time after load transient, respectively.

Conventional design of fast transient buffer is hard to balance the quiescent current and drive ability. Several optimizations are proposed in prior work to resolve this problem. The authors in [12], [15] uses adaptive bias to improve the bandwidth and pull ability under heavy load condition. However, this technique also increases the bias current under heavy load and decreases the current efficiency. [3] uses two class-AB source followers to provide push and pull ability under different load condition, however the mode switch is not smooth and will generate a drive dead zone. Duong et al. [5] used an ac-coupled push transistor to provide the push ability of buffer, however the output impedance of push buffer is not satisfactory.

Thus, a closed-loop scheme-based band extended buffer with push pull ability is proposed to resolve these problems. The top-right of Fig. 3 shows the detailed circuit of the AP³. The proposed buffer consists of two techniques, which are current efficient

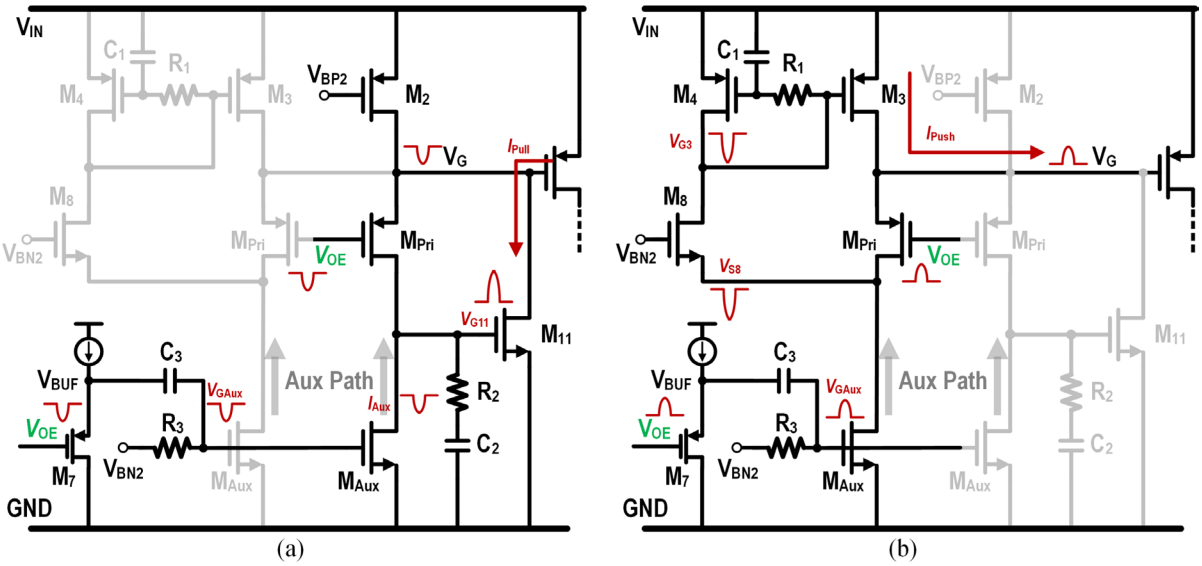


Fig. 4. Large signal response of AP^3 buffer. (a) Load current increases. (b) Load current decreases.

push pull techniques and bandwidth extended techniques called aux-path techniques.

As shown in Fig. 2(b), the push and pull loops are connected in parallel at $V_{\rm G}$ and form the primary push-pull buffer. This part can be considered as a unit gain closed-loop buffer. The pull loop is composed of $\rm M_{Pri}$ and $\rm M_{Aux}$ on the right and $\rm M_{11}$. $\rm M_{11}$ provides the pull capability during transients, and R_2 C_2 compensates the loop. The working principle of pull loop is like that of a super source follower. The push loop is composed of $\rm M_{Pri}$, $\rm M_{Aux}$ on the left, $\rm M_3$, $\rm M_4$, and $\rm M_8$. The $\rm M_3$ provides push capability during transients. The push loop works like a flipped-voltage-follower. $\rm M_4$ and R_1 C_1 form an active-inductor and boost the bandwidth. The output of EA is buffered by a small source follower and connected to a high pass filter that is composed of R_3 C_3. Then, the signal at output of EA will be fed directly into the feedback loop. The large signal and small signal analysis are as follows.

The large signal response of the AP^3 buffer is shown in Fig. 4 and illustrates as follows. When the load current of LDO switches from a small load current to a large load current, also known as L-H load transient, the undershoot voltage of $V_{\rm OUT}$ is amplified by EA and then transmitted to the gate of $\rm M_{Pri}$ and high pass coupled to the gate of $\rm M_{Aux}$, pulling down their gate voltage. At this time, the drain current of $\rm M_{Pri}$ will increase and the current flow through the $\rm M_{Aux}$ will decrease. These will pull up the gate of $\rm M_{11}$ jointly, and accelerate the slew rate of $V_{\rm G11}$, or the gate voltage of $\rm M_{11}$. Then, the current flows through the $\rm M_{11}$ increases immediately and generates $I_{\rm Pull}$.

When the load current of LDO switches from a large load current to a small load current, also known as H-L load transient, the overshoot voltage of $V_{\rm OUT}$ is amplified by EA and then transmitted to the gate of $\rm M_{Pri}$ and high-pass coupled to gate of $\rm M_{Aux}$, pulling up their gate. For this condition, the source voltage of $\rm M_8$ or $V_{\rm S8}$ is pulled down by the $\rm M_{Pri}$ and $\rm M_{Aux}$ jointly. And the R_1 and C_1 increase the impedance and the voltage variation of gate of $\rm M_3$, or $V_{\rm G3}$. Then, the current flow through $\rm M_3$ increases immediately then generates $I_{\rm Push}$.

With these techniques, the push ability of buffer during H-L load transient is satisfactory even without conventional adaptive bias. And the pull ability during L-H load transient is also satisfactory since the $\rm M_{Aux}$ increases the voltage variation of $V_{\rm G11}$ as well as $I_{\rm Pull}$.

From the small signal perspective, this buffer can be considered as two close-loop buffers that provide push and pull ability separately. The pull loop is based on super source follower, where R_2 and C_2 are used to ensure loop stability. The push loop is based on a flipped-voltage-follower scheme. An active inductor circuit is added to extend the bandwidth of push loop. Equivalent impedance of the active inductor is shown in the top-right of Fig. 5. The dynamic current of $\rm M_{Pri}$ in push loop flows through the active inductor scheme consisting of R_1, $\rm M_4$, and C_1, and finally injects to $V_{\rm G}$ for fast charging the gate capacitance, where $C_{\rm g3}$ is the gate parasitic capacitance of $\rm M_3$, the boosting impedance at moderate frequency effectively improves the transient response performance during overshoot period.

The small signal model of proposed AP^3 buffer is shown in Fig. 5, where $g_{\rm mPri}$ is the transconductance of $\rm M_{Pri}$, $R_{\rm Pri}$, and $R_{\rm Aux}$ are the output resistance of $\rm M_{Pri}$ and $\rm M_{Aux}$, $C_{\rm g11}$ is the gate parasitic capacitance of $\rm M_{11}$, respectively. With a fast push loop and a slow pull loop connected in parallel, a zero is shown in the whole loop of buffer. As shown in Fig. 6, the slow pull loop and fast push loop meet at $g_{\rm m4}/2C_1$, generates a zero and the bandwidth of buffer is doubled. The loop transfer function of proposed buffer can be expressed as follows:

$$T_{\rm LF}(s) = 1/2 \cdot g_{m11}\left(R_{\rm Aux}||R_{\rm Pri}\right) \times \frac{s \cdot R_2C_2 + 1}{\left[s \cdot \left(R_{\rm Pri}||R_{\rm Aux}\right)C_2 + 1\right]\left(s \cdot C_{\rm gP}/g_{\rm mPri} + 1\right)}$$

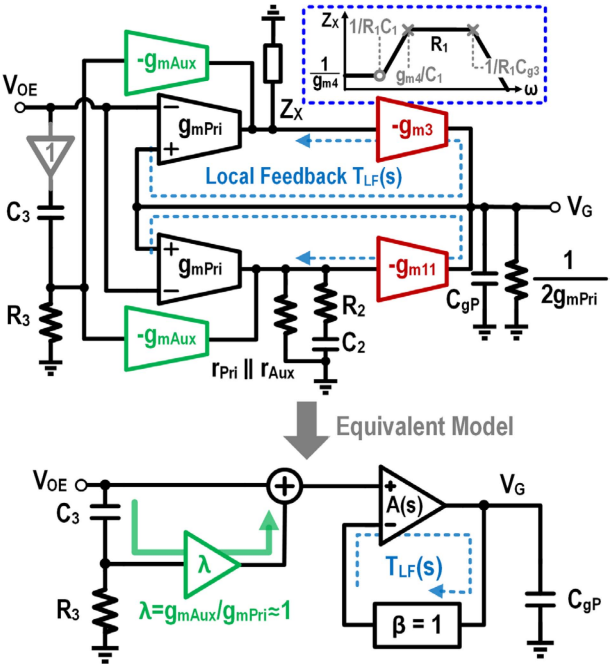


Fig. 5. Small signal model and equivalent model of AP^3 buffer.

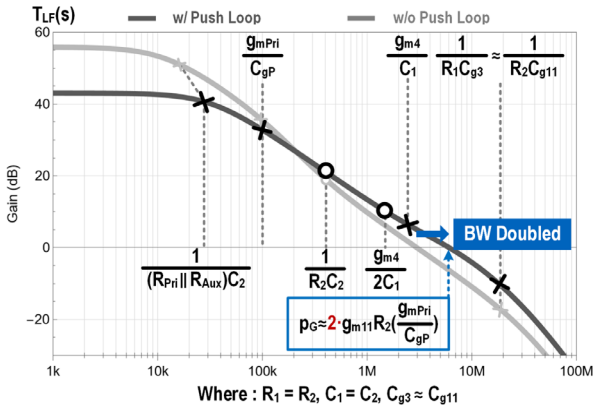


Fig. 6. Bode plot of primary push-pull buffer's loop frequency response, $T_{\mathrm{LF}}(s)$.

$$\times \frac{s \cdot 2C_1/g_{m4} + 1}{[s \cdot R_1 C_{g3} + 1]\,(s \cdot C_1/g_{m4} + 1)}. \tag{1}$$

And the output impedance of AP^3 buffer, or R_{OB} at low frequency and middle frequency can be expressed as (2). It is worth noting that the inner loop bandwidth of buffer as well as the location of gate pole is doubled compared with pull loop only, as shown in Fig. 6, which facilitates wide band design.

$$R_{\mathrm{OB}}|_{\mathrm{DC}} = \frac{1}{g_{\mathrm{mPri}} \cdot g_{m11} R_{\mathrm{Aux}} || R_{\mathrm{Pri}}}$$
$$R_{\mathrm{OB}}|_{\omega > g_{m4}/C_1} = \frac{1}{2 g_{\mathrm{mPri}} \cdot g_{m11} R_2}. \tag{2}$$

To further extend the bandwidth of LDO with same quiescent current, an auxiliary path (aux-path) is proposed to provide extra

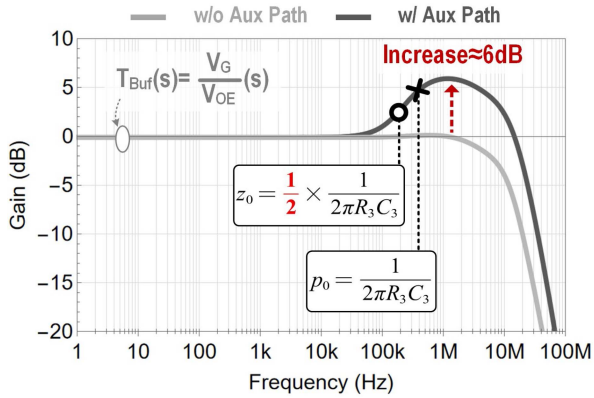


Fig. 7. Gain increases and bandwidth extends at middle frequency with the aux-path of AP^3 Buffer.

gain at middle to high frequency. As shown in Fig. 3, M_7 can directly feed V_{OE} to V_{G} at middle to high frequency. From a transient perspective, with the same variation of V_{OE}, buffer can output more current to adjust V_{G} and improve the transient performance. From small signal perspectives, referring to the simplified small-signal model at the bottom of Fig. 5, the aux-path provides additional signal at the input of the equivalent main close-loop buffer, as shown in Fig. 7, the moderate-frequency gain of buffer is doubled (Given that g_{mAux} is designed to be equal to the g_{mPri}), which can increase the UGB of LDO simultaneously.

Compared with previous push-pull buffer design, it can be found that the proposed AP^3 buffer does not apply an adaptive bias scheme to extend the bandwidth and drive ability of buffer, which increases current efficiency under heavy load conditions. Since during the H-L load transient, the output current of buffer is more likely to be a pulse current rather than a continuous high current, a push buffer that is based on dynamic bias scheme is enough for this application. And with the close loop feedback scheme, the p_{G} is also pushed to high frequency just like a buffer with adaptive bias scheme.

B. SHB Scheme

Adaptive bias technique is widely used in the design of LDO nowadays. This technique makes the bias current of EA proportional to load current, as shown in bottom of Fig. 8. The bandwidth of LDO under heavy load could be expressed as (3), where k_{gm} is the ratio of equivalent $g_{\mathrm{m,EA}}$ and g_{m} of input differential pair, this technique effectively improves the transient performance of LDO with low quiescent current and high current efficiency.

$$\begin{aligned} &\mathrm{UGB} \propto g_{\mathrm{m,EA}}/Cz \\ &g_{\mathrm{m,EA}} = k_{\mathrm{gm}} \cdot \tfrac{1}{2}\beta\sqrt{I_{\mathrm{B,EA}}}. \end{aligned} \tag{3}$$

However, conventional adaptive bias EA mainly faces two challenges: First is the adaptive bias circuit current mirror ratio suffers from ±40% variation across PVT corners and mismatch; second is that if the current mirror ratio is large enough, the transient response will be good but the stability, current efficiency,

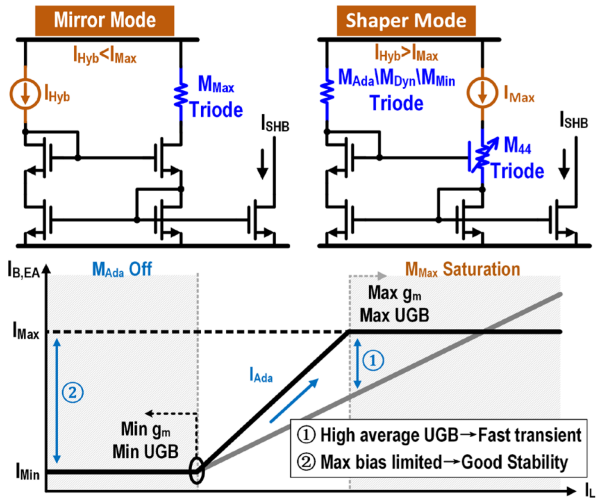


Fig. 8. Working principle of the SHB circuit.

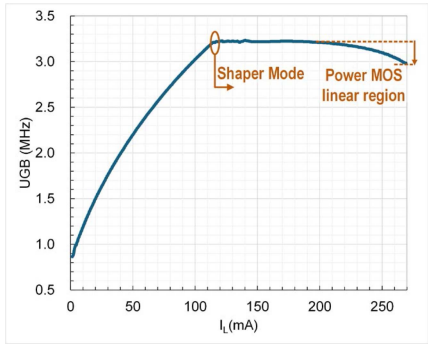


Fig. 9. Bandwidth control of LDO with proposed SHB under different load conditions ($V_{\mathrm{IN}} = 2.6$ V, $V_{\mathrm{OUT}} = 2.4$ V).

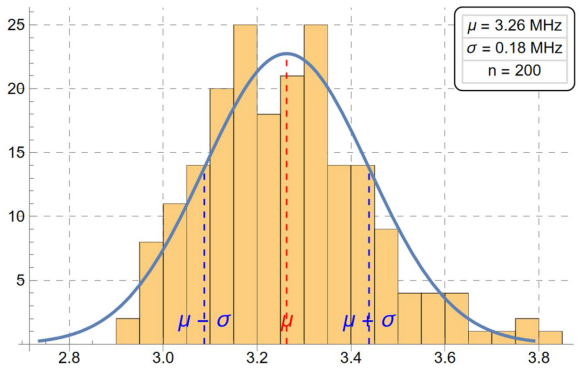


Fig. 10. Monte Carlo simulation of UGB of LDO under max I_{L} ($V_{\mathrm{IN}} = 2.6$ V, $V_{\mathrm{OUT}} = 2.4$ V).

and dc loop gain will be not satisfactory; if the current mirror ratio is small, the bandwidth of LDO will be limited and the transient performance will not be satisfactory.

This issue is resolved by proposing an SHB circuit. This innovative design ensures that the maximum biasing current of EA under heavy load conditions is automatically limited to the desired magnitude. In addition, for enhanced response speed, the SHB circuits incorporate dynamic bias currents.

As illustrated in Fig. 3, the SHB circuit consists of three current branches. The static current I_{Min} ensures optimal performance by setting a minimal $I_{\mathrm{B,EA}}$ to around 1μA. Adaptive bias current I_{Ada} and dynamic bias current I_{Dyn} are controlled by capacitively coupled V_{G}, overcoming the response latency of $\mathrm{M_{Ada}}$ and I_{Ada}. Summing current I_{Hyb} compares with I_{Max}, where the output current $I_{\mathrm{B,EA}}$ will be set to either I_{Hyb} or I_{Max} based on which is smaller.

The current shaper of proposed SHB circuit has two operational modes as shown in Fig. 8:

1) Mirror Mode: This is the working mode of shaper during light to middle load condition. During this mode, the $\mathrm{M_{Max}}$ will be pushed into triode region due to the bias current is not large enough. And become the resistor load of current mirror. The bias current can be expressed as follows:

$$I_{\mathrm{B,EA}} = I_{\mathrm{Hyb}} = I_{\mathrm{Min}} + I_{\mathrm{Ada}} + I_{\mathrm{Dyn}}. \tag{4}$$

2) Shaper Mode: $\mathrm{M_{Ada}}$ to $\mathrm{M_{Min}}$ will be pushed into triode region under heavy load condition. At this condition, I_{Hyb} will exceed I_{max}, and the $I_{\mathrm{B,EA}}$ will depend on I_{max}, which is around 3 μA in this design. In this mode, the bias current can be expressed as follows:

$$I_{\mathrm{B,EA}} = I_{\mathrm{Max}}. \tag{5}$$

Compared with conventional adaptive bias, proposed hybrid bias techniques can effectively control the bandwidth of LDO under heavy load conditions. Fig. 9 demonstrates the bandwidth of LDO is clamped within 3.3 MHz over 270 mA load range. The bandwidth will decrease a little due to the power FET is driven to triode regions under heavy load, and the gain of power is also decreased. With this technique, the gain and dc accuracy is also guaranteed under heavy load. And the maximum bandwidth of LDO is also under control to against mismatch, a Monte Carlo simulation result is shown in Fig. 10. The mean maximum bandwidth of 200 points sample is 3.3 MHz with a 175 kHz 1-σ value.

The small signal circuit analysis when the bias current works in the mirror mode is shown in Fig. 11. The loop characteristics are close to a simple single-pole loop, showing good loop stability. Since the parasitic capacitor of the entire loop is small, the loop bandwidth is high and reaches 80 MHz. This guarantees the speed of bias current mirror and ensures that the response speed of LDO will not be affected by proposed current shaper.

The transient response of the proposed bias circuit is shown in Fig. 12. For conventional adaptive bias, due to the large gate capacitance of power FET, there is a response lag of adaptive bias current, which will increase the undershoot voltage during L-H load transient but suppress the overshoot voltage during H-L load transient. With the proposed hybrid-bias techniques, as shown in Fig. 12, for L-H load transients, I_{Dyn} pulls up $I_{\mathrm{B,EA}}$ quickly while I_{Ada} responds later due to $\mathrm{M_{Ada}}$'s response latency. The bandwidth of the LDO increases rapidly, reducing the voltage drop. During H-L load transients, I_{Dyn} drops slightly and I_{Ada} maintains its original value for a short period due to response lag. This helps maintain high bandwidth during load transient edge

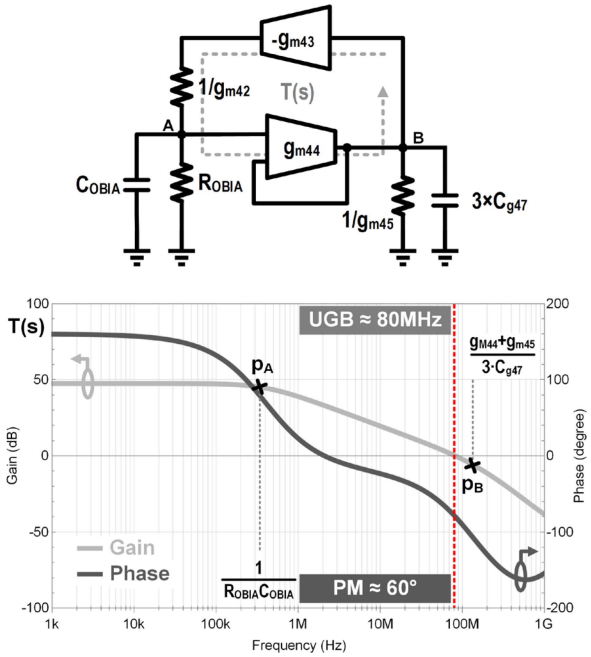


Fig. 11. Small signal model of SHB circuit under mirror mode.

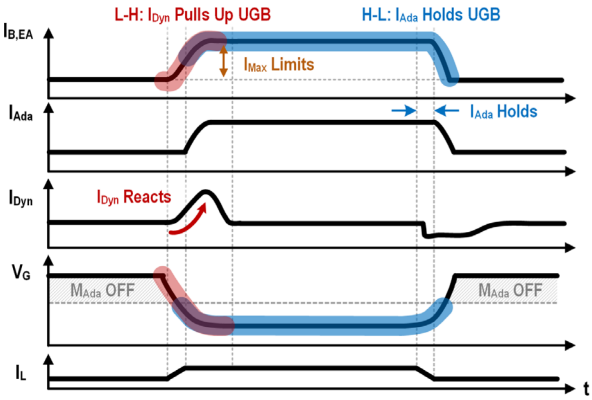


Fig. 12. Transient waveform of SHB under load transient.

and suppresses overshoot. Thus, the overshoot and undershoot will be suppressed together. The ratio of dynamic current to adaptive current is set that when the maximum transient load occurs, the dynamic current can generate a dynamic current twice the peak value of the adaptive current to ensure that the circuit reaches a high-bandwidth state as quickly as possible.

C. Error Amplifier and Loop Stability Design

To ensure the stability of LDO under wide load conditions, Type-II compensation technique is applied to proposed LDO.

In the conventional Type-II compensation technique, after the H-L load transition, there will be a response dead zone. This is because after the H-L load transition, the power FET must provide a current smaller than the load current to allow the output voltage to drop back to the steady-state voltage. This means that the V_{GS} of $\mathrm{M_P}$ will be overdriven to less than V_{th} and the $\mathrm{M_P}$

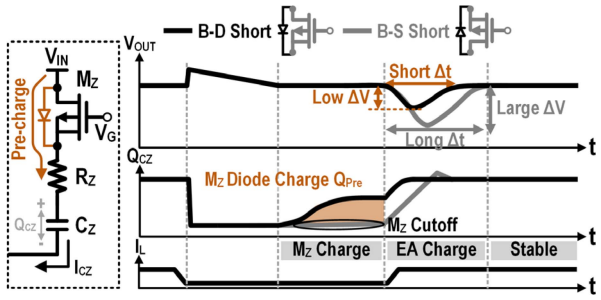


Fig. 13. Working principle of C_{Z}-precharged Type-II compensation.

will enter cut-off region. This requires EA to supply more charge to compensate for this part of the charge when L-H load transient happens, which will significantly increase the response time of the LDO.

In fact, when the load switches at a low frequency, since the time between the two loads transition is long enough, $\mathrm{C_Z}$ can be slowly charged by the leakage current of $\mathrm{M_Z}$, and no obvious performance degradation will be seen. However, when a high-frequency load transient occurs, EA must supply extra charge, thus the transient performance is degraded.

The C_{Z}-precharged compensator is thus proposed to be used in NMOS LDO [24], the proposed B-D shorted C_{Z}-precharged circuit can clamp the voltage of top plate of C_{Z} after H-L load transient. For PMOS LDO, as shown in Fig. 13, the clamp circuit precharges C_{Z} during "$\mathrm{M_Z}$ charge" stage through body diode of $\mathrm{M_Z}$, providing most of the charge required by C_{Z} (Q_{Pre}). If L-H load transient happens at that time, EA only provides a tiny part of the required charge during "EA charge" stage. However, based on conventional B-S short adaptive compensation, $\mathrm{M_Z}$ is cutoff during this process. Therefore, during "$\mathrm{M_Z}$ charge" stage, $\mathrm{M_Z}$ cannot charge C_{Z} quickly enough. It means that EA must supply extra charge to C_{Z} during "EA charge" stage, which will increase response time and undershoot at V_{OUT}. With the C_{Z}-precharged adaptive compensation, EA provides much less charge compared with B-S short cases. Response time of EA will be short, and the performance degradation is ignorable. The simulation result of C_{Z}-precharged compensator is shown in Fig. 14. As can be seen, the proposed C_{Z}-precharged reduces the undershoot voltage during L-H load transient. And the $\mathrm{C_Z}$ charging time also reduces from 600 μs to 16 μs.

The proposed LDO applies a g_{m}-boosting EA. As shown in Fig. 3, $\mathrm{M_{25}}$ and $\mathrm{M_{28}}$ convert the error voltage into error current and transmit to the current mirror. $\mathrm{M_{26}}$ and $\mathrm{M_{27}}$ work as an input differential pair of folded-cascode OTA and feed another ac current to the output of EA. With this technique, the equivalent transconductance can be expressed as follows:

$$g_{\mathrm{mEA}} = \left(1 + \frac{k_2}{k_1}\right) g_{\mathrm{m25}}. \tag{6}$$

With this technique, the transconductance and slew rate of EA is enhanced, thus the UGB of LDO is also improved with same quiescent current. The output resistance of EA, or R_{OE}, can be expressed as (7), where R_{O14} and R_{O22} is output resistance of $\mathrm{M_{14}/M_{15}}$ and $\mathrm{M_{22}/M_{23}}$, respectively. The $\mathrm{g_{m22}}$ is the

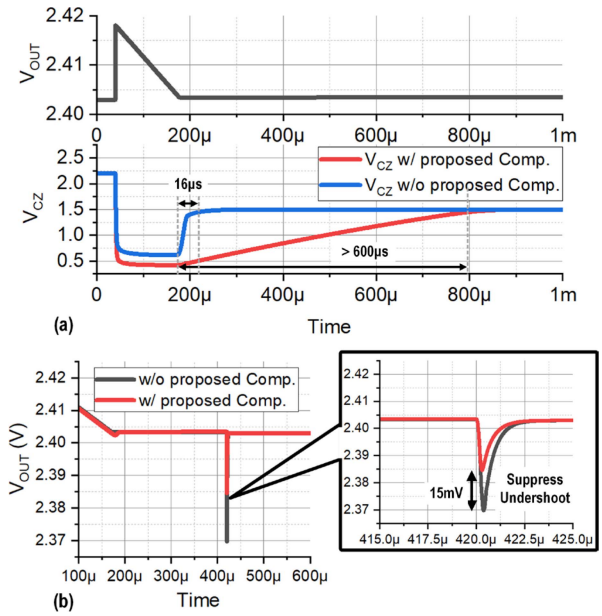


Fig. 14. Simulated load transient comparison of w/ and w/o C_Z-precharged Type-II compensation ($V_{IN} = 2.6$ V, $V_{OUT} = 2.4$ V, 100 μA-to-270 mA).

transconductance of M_{22}/M_{23}.

$$R_{OE} = \frac{R_{O14} \cdot g_{m22} R_{O22} R_{O37}}{R_{O14} + g_{m22} R_{O22} R_{O37}} \approx R_{O14}. \tag{7}$$

The small signal model of proposed LDO is shown in Fig. 15(a). For ensuring the loop stability of LDO over wide load range, A Q_Z-precharged adaptive Type-II compensation circuit is applied at the output of EA to create a tracking zero z_C for improving phase margin and compensating the first nondominate pole. The z_C can be expressed as follows, where R_{MZ} is the on-resistance of M_Z:

$$z_C = \frac{1}{(R_{MZ} + R_Z) \cdot C_Z}. \tag{8}$$

The AP^3 buffer is regarded as a block with pole-zero pair provided by aux-path as mentioned before. The parasitic effect of C_O is ignored due to the UGB is well controlled within f_{CO} by proposed SHB scheme. Fig. 15(b) shows the frequency compensation scheme of LDO. From light to medium load, the dominant pole is the output pole p_{OUT}, which can be expressed as follows:

$$p_{OUT} = \frac{1}{R_L \cdot C_O}. \tag{9}$$

At heavy load, output pole of EA, or p_{EA} becomes the dominant pole, which can be expressed as follows:

$$p_{EA} = \frac{1}{(R_{OE} + R_Z + R_{MZ}) \cdot C_Z}. \tag{10}$$

The zero-pole pair that is provided by aux-path technique can be expressed as (11), as can be found, this zero-pole pair effectively improves the bandwidth of proposed LDO.

The gate pole of power FET in LDO, or p_G, can be expressed as (12), where R_{OB} is the output impedance of AP^3 buffer as shown in (2).

$$z_0 = \frac{1}{2R_3C_3} \quad p_0 = \frac{1}{R_3C_3} \tag{11}$$

$$p_G \approx 2 \cdot g_{m11} R_2 \frac{g_{mPri}}{C_{gP}}. \tag{12}$$

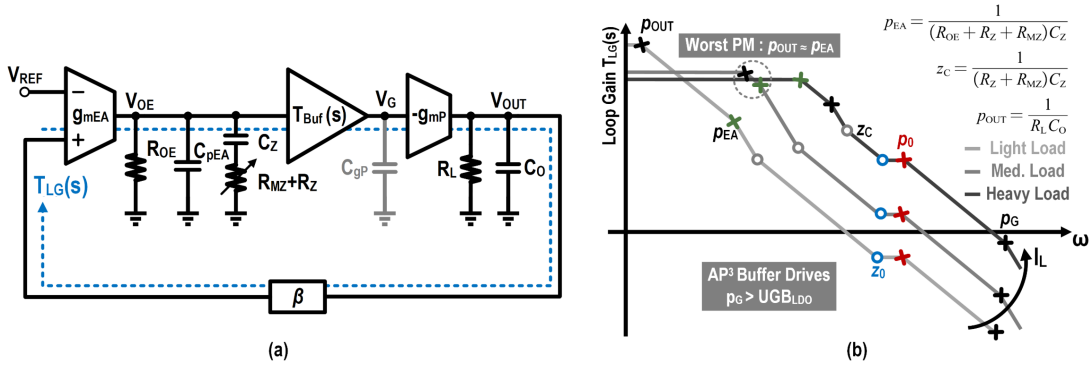
The worst stability is the case when the p_{OUT} meets p_{EA} at medium load condition (~10 mA). The loop transfer function of LDO, or $T_{LG}(s)$, is given as Fig. 15(c), where β is output voltage feedback factor, g_{mEA} is the equivalent transconductance of EA, R_{OE} is the equivalent output resistance of EA, R_{OB} is the output impedance of AP^3.

D. Performance Validation

Fig. 16 shows the simulated loop frequency response considering f_{CO} and parasitic parameters of C_O (f_{CO}~10 MHz, with $C_O = 1$ μF, $L_P = 300$ pH, and $R_P = 10$ mΩ) under different load conditions. As can be seen, the maximum of LDO is well controlled to about 3.3 MHz and keeps proper margin to f_{CO}. On the bandwidth other hand, the tracking zero z_C gradually moves to low frequency and compensates for the first nondominant pole with load decreasing, which guarantees the minimum phase margin of 60° over full load range. Monte Carlo and PVT result of phase margin under worst stability load condition ($I_L = 10$ mA) are also performed. As shown in Fig. 17, the worst PM is larger than 30° over PVT variation. Since the dc gain is larger than 60 dB over full load range, the differential voltage that applied on input of EA is less than 1 mV.

A time-domain transient simulation is conducted to assess the effect of the proposed techniques, as illustrated in Fig. 18. When each of the proposed techniques is incorporated into an LDO in a sequential manner, it becomes quite evident that proposed techniques have a profound impact on load transient.

As previously discussed in detail, the aux-path technique proves to be quite beneficial. It can extend the bandwidth of the LDO while maintaining the same quiescent current, which is a significant advantage. On the other hand, the push-pull technique also plays a crucial role. It can effectively drive the gate capacitor of the power FET, accelerating the load transient response. There is a 20% suppression of overshoot voltage and a 74% suppression of undershoot voltage after AP^3 technique is applied. Furthermore, the hybrid bias technique has an extraordinary effect. It not only accelerates the LDO response speed but also suppresses the overshoot voltage to 77%. When compared with the conventional adaptive bias, the proposed SHB technique mainly focuses on improving the L-H load transients. Therefore, optimizing the overshoot voltage is not its primary objective. However, it still offers improvements in other aspects. A Monte Carlo simulation is also performed to show the performance under mismatch and across different process corners, as shown in Fig. 19. It can be found that the proposed technique shows stable performance. The average undershoot is 19 mV with a 2.2 mV standard deviation and the average overshoot is 16 mV with a 1.4 mV standard deviation. From the simulation results, it can be found that the proposed techniques show good stability across different corners.



$$(c)\ T_{LG}(s) = -\beta g_{mEA} R_{OE} \cdot g_{mP} R_L \cdot \frac{s\cdot(R_Z+R_{MZ})C_Z+1}{[s\cdot R_L C_O+1]\,[s\cdot(R_{OE}+R_Z+R_{MZ})C_Z+1]\,[s\cdot R_{OB}C_{gP}+1]} \cdot \frac{s\cdot 2R_3C_3+1}{s\cdot R_3C_3+1}$$

Fig. 15. Small signal analysis of proposed LDO (a) small signal model, (b) pole zero and bode plot, and (c) transfer function.

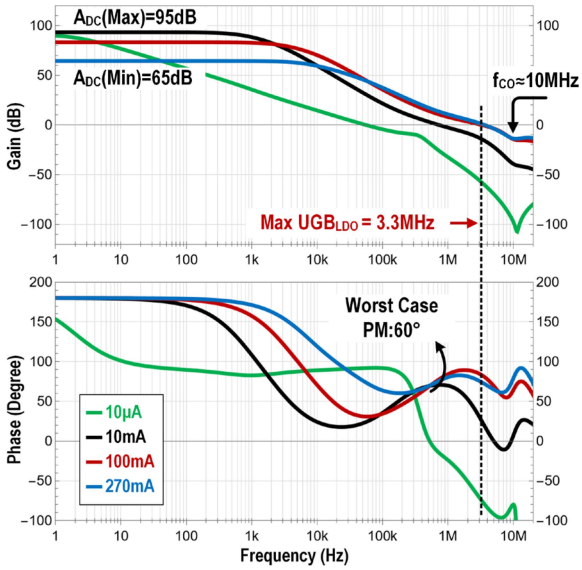


Fig. 16. Simulated bode plot of proposed LDO under different load (V_{IN} = 2.6 V, V_{OUT} = 2.4 V).

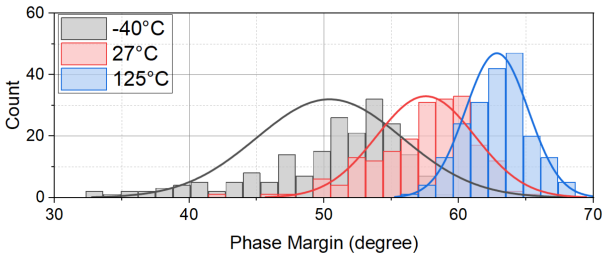


Fig. 17. Monte Carlo and PVT result of worst stability condition (I_L = 10 mA, V_{IN} = 2.6 V, V_{OUT} = 2.4 V).

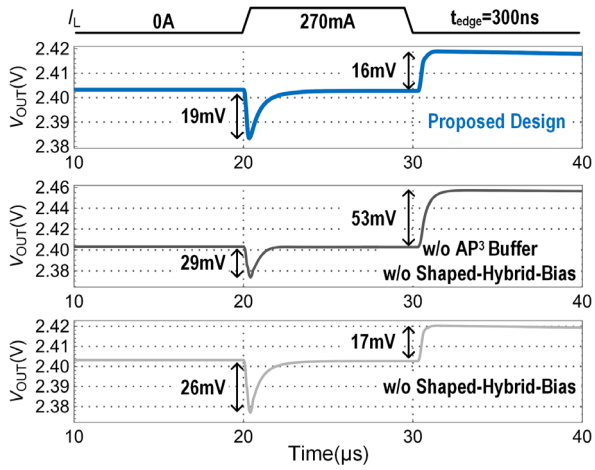


Fig. 18. Load transient simulation of LDO w/o and w/ proposed techniques.

III. Experimental Results and Discussion

This work was fabricated in a 180 nm CMOS process with 5 V devices. The minimum length of 5 V devices is 500 nm for both NMOS and PMOS. The die-shot and floorplan of chip is shown in Fig. 20. A kelvin connect V_{OFB} pin is added for better load regulation performance. The active region of proposed LDO is 400 μm in length and 250 μm in width.

Load transient tests are performed to confirm the effect of proposed AP³ buffer and SHB scheme. The test PCB and circuit is shown in Fig. 21. A 2N7002 with small C_{oss} from Onsemi is used as the load transistor. For PCB layout, a horizontal conducted current sense resistor is used for smallest load loop parasitic inductance.

Fig. 22 shows the load transient test result with 200 mV dropout voltage and C_O = 1 μF. For the load-transient test, as shown in Fig. 22(a), when I_L switches between 0 mA to 270 mA with 300 ns edge time, the overshoot and undershoot are 19 mV and 14 mV, respectively. When I_L switches between 1 mA to 270 mA with 300 ns edge time, as shown in Fig. 22(b), the overshoot and undershoot voltages are 18 mV and 13 mV, respectively. The load transient test result shows the good performance of proposed AP³ buffer. And it can be found that there is no visible oscillation in voltage response procedure, which shows the good loop stability with the proposed SHB technique.

The load regulation test result is also shown in Fig. 23, it can be found that within the whole load range, from 0 mA-to-270 mA,

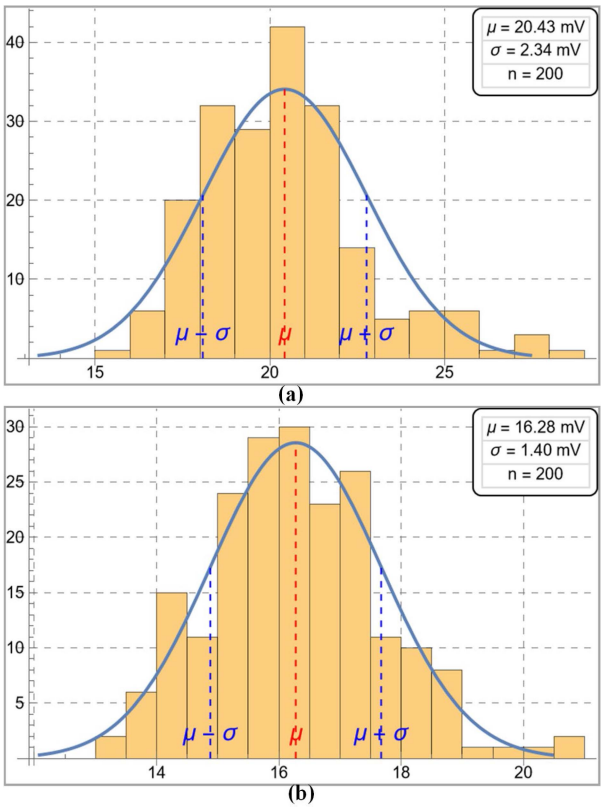


Fig. 19. Monte Carlo result of (a) undershoot and (b) overshoot voltage.

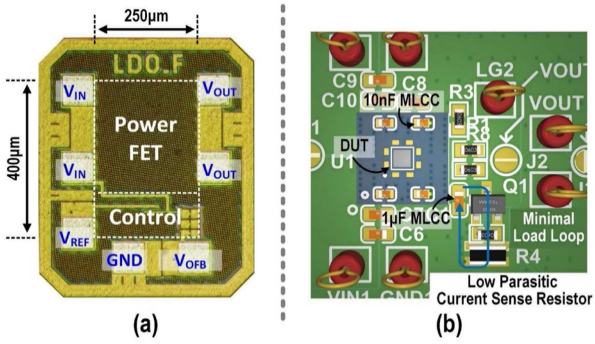


Fig. 20. (a) Chip micrograph (b) Testbench PCB.

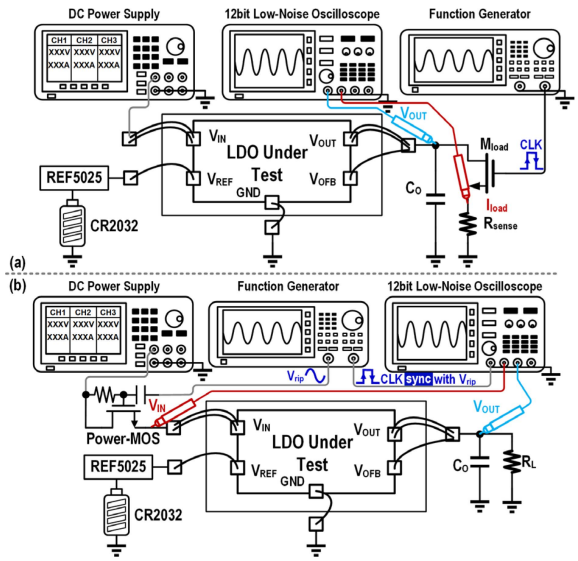


Fig. 21. Testbench for (a) load transient and (b) Power supply rejection ratio (PSRR)/line transient.

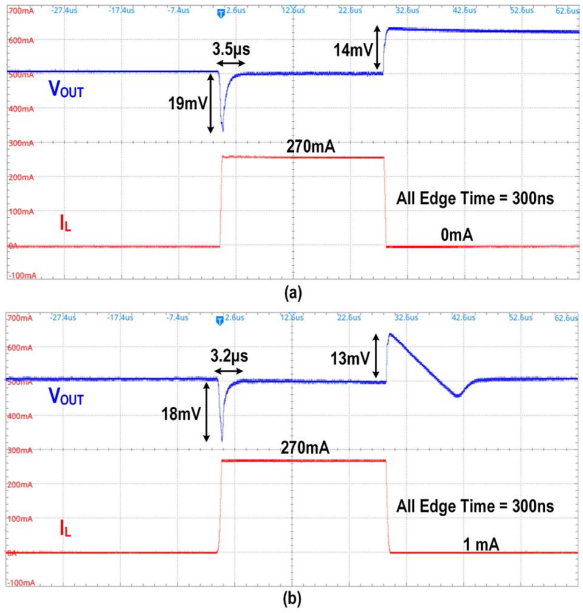


Fig. 22. Measured load transient under $V_{IN} = 2.6V/V_{OUT} = 2.4$ V with (a) light load is 0 mA and (b) light load is 1 mA.

the output voltage only varies less than 1.5 mV, which shows the high loop gain and effect of kelvin connection. In case of line regulation, with the 200 mV input voltage variation, the output voltage variation is less than 200 μV.

For PSR measurements, a line injector is applied to provide the ripple of input voltage, there are serval different line injection circuits that are widely used in previous work. An LC HPF and a power amplifier are the most widely used scheme. However, the minimum inject frequency with the *LC* filter is not low enough and the input ripple voltage will be distorted under heavy load conditions due to the nonlinearity of *L* and *C*. The self-resonant of *LC* also limits high-frequency response. For the power amplifier solution, which is another widely used PSR injector circuit, the loop stability of amplifier with large output capacitor is also worrying. Thus, a source-follower-based line injector circuit is proposed. The circuit is shown in Fig. 21, a power-MOS with G-D connected is the core of the proposed circuit. HPF is used to feed the ac voltage signal to the gate of power-MOS. Since the power-MOS is connected as a source follower and provides high drive ability, the bandwidth of proposed line injector is very high even with large input capacitor (∼100 nF). The gain of proposed line injector is flat within 100 Hz to 10 MHz with less than 1 dB ripple with a 7 mA quiescent current.

When using time domain technique to measure the PSR, the injection voltage amplitude should be small enough to avoid

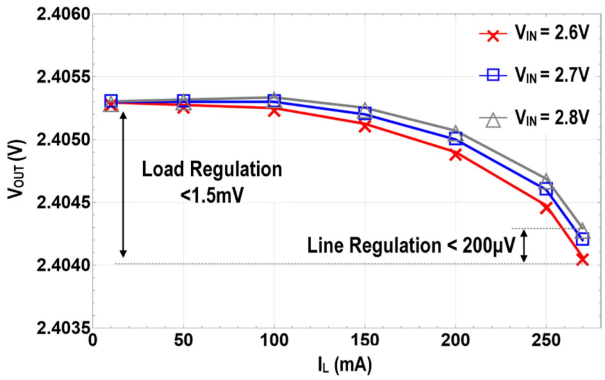


Fig. 23. Load regulation under different input voltage.

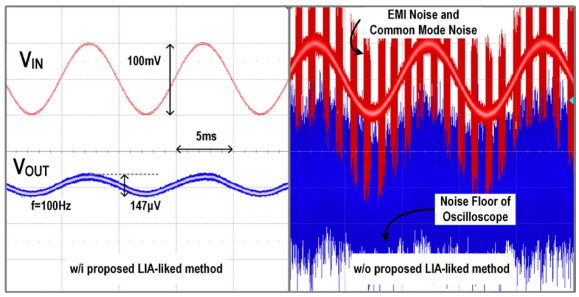


Fig. 24. PSR test waveform under $V_{IN} = 2.6$ V/$V_{OUT} = 2.4$ V w/ and w/o proposed LIA-liked method.

driving the LDO into nonlinear region. However, when measured high PSR with oscilloscope, low injected voltage means it will be easy to reach the limitation of noise floor of oscilloscope. Thus, a lock-in-amplifier-liked method is proposed. In addition to injecting the ripple voltage $V_{\rm rip}$ into the input of the LDO, a square wave clock signal that is synchronized with the ripple voltage and has the same frequency and phase is also sent to the oscilloscope to serve as the trigger source of the oscilloscope. In this way, only signals that are the same frequency or multiple of the injected ripple voltage can appear stably on the screen of the oscilloscope.

After that, the oscilloscope is set to average sampling mode. This operation constructs an equivalent low-pass filter. It is not difficult to find that the bandwidth of the constructed filter is inversely proportional to the number of averages. As shown in Fig. 24, this procedure selectively enhances the coherent signal component at the injected ripple frequency. Noncoherent components (including wide band noise and common mode interference) are suppressed to the level of equivalent input noise through integration averaging. This method not only improves the measurement range of the oscilloscope but also ensures that all nonlinear responses of the LDO are measured.

The PSR test result is shown in Fig. 25. The test condition of PSR is 270 mA load current with 1 μF output capacitor and 250 mV dropout voltage. An extra 50 mV dropout voltage is applied to avoid nonlinear response of LDO under 100 mV input ripple voltage. As shown in Fig. 25(a), the PSR at dc and low frequency is around 60 dB, while the worst PSR is 33 dB at 1 MHz. Competitive PSR performance shows that the

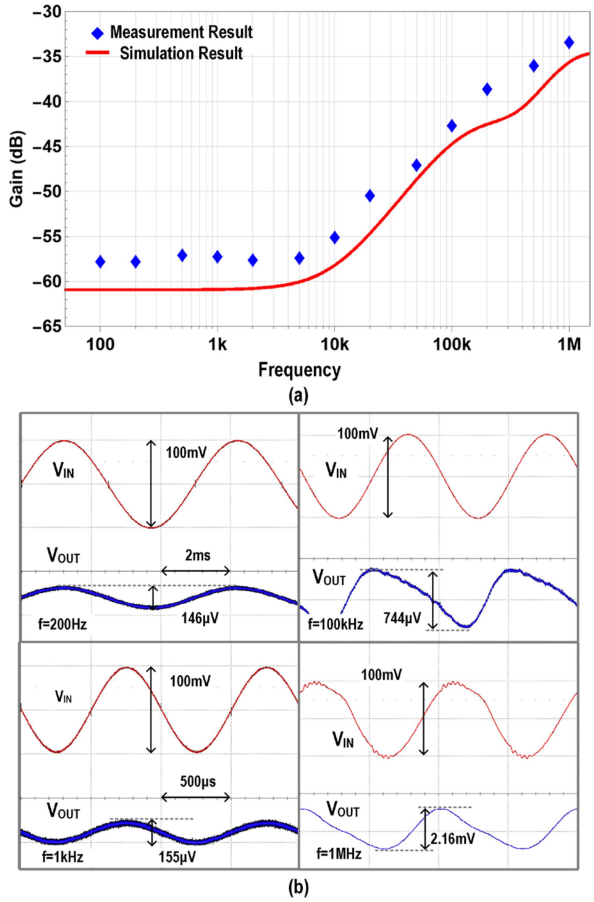


Fig. 25. PSR test result under $V_{IN} = 2.6$ V/$V_{OUT} = 2.4$ V cross frequency (a) and test waveform (b) under 250-mV dropout voltage and 270 mA load current.

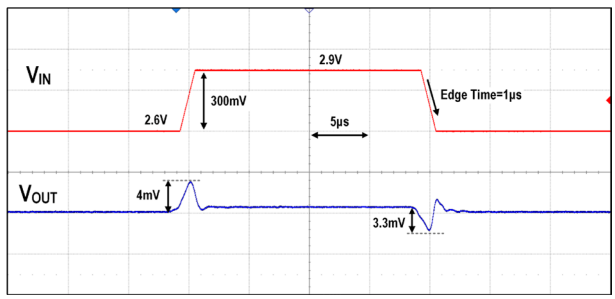


Fig. 26. Line transient test result with 270 mA load current.

proposed techniques will not deteriorate the PSR performance. A line transient test is also applied, and the result is shown in Fig. 26. The overshoot and undershoot voltage are 4 mV and 3.3 mV, respectively, with 300 mV line step and 1 μs edge time.

Performance comparison with other state-of-the-art works handing fast transient with low quiescent current ($I_{\rm LOADMAX} > 150$ mA) is given in Table I. Figures of merit (FoM) is utilized here to evaluate different current-efficiency designs for enhancing transient speed. With the help of AP^3 buffer and SHB scheme, the transient load performances are all guaranteed without large quiescent current consumption. In addition,

TABLE I
Comparison With Previous Published Works

Parameter	This Work	JSSC [1]	JSSC [10]	TPE [5]	JSSC [24]	TPE [22]	ASSCC [19]	ISSCC [7]
Year	2025	2018	2020	2022	2024	2022	2024	2025
Technology (μm)	0.18*	0.25	0.18	0.18	0.35	0.18	0.18	0.18
Chip area (mm^2)	0.100	0.108	0.126	0.088	0.1316	0.0296	0.047	0.047
Power FET Type	PMOS	NMOS	PMOS	PMOS	NMOS	PMOS	PMOS	PMOS
V_{IN} (V)	2.6-2.9	1.5-3.3	/	1.8-2.2	1.2-3	>1.8	1.8-2.3	1.0-1.4
V_{OUT} (V)	2.4	1.0-3.0	1.5-5.25	1.6	1	1.6	1.6	0.8
$I_{LOADMAX}$ (mA)	270	150	250	200	300	50	300	1200
V_{DROP} (mV)	200	240	178	200	200	200	200	200
C_O (μF)	1	1	2.2	1	1	1	1	4.7
I_q (μA)	18	1.24	5.6	48	8.2	2.5	27	15
Undershoot (mV)	19	135	36	30	68	30.75	35.8	16
Overshoot (mV)	14	65	29	46	36	20.5	24	95
ΔV_{OUT} (mV)	33.00	200.00	65.00	76.00	104.00	51.25	59.8	111
FoM (ps)	8.15	11.02	12.81	91.20	9.48	51.25	17.94	5.43

*0.18-μm 5V CMOS, L_{min}=0.5 μm ; FoM=$I_q \cdot \Delta V_{OUT} \cdot C_O / I_{LOADMAX}^2$

adaptive frequency compensation by using zero tracking makes the loop stable from zero to full load without ESR requirement. With the SHB scheme, good load regulation and line regulation are also guaranteed even under heavy load conditions and the power FET working under linear region. This work obtains the lowest FoM compared with other state-of-the-art works, except [7], which gets performance improvement with low voltage devices that have a minimum 180 nm channel length. This result demonstrates that the proposed regulator is a good candidate for mobile applications.

IV. Conclusion

This article proposes a current-efficient fast-transient PMOS LDO featuring a low-power AP^3 buffer and an SHB circuit. The AP^3 buffer effectively drives the gate capacitance of the power FET with high pull and push abilities, optimizing transient response with low quiescent current. The SHB circuit accurately controls the EA's bias current limits, ensuring the LDO's maximum bandwidth for loop stability, loop gain, and current efficiency. The circuit is implemented in a 0.18 μm 5 V CMOS process with a minimum 500 nm length for both NMOS and PMOS, the LDO achieves 19 mV undershoot and 14 mV overshoot with a 1 μF output capacitor during load transients from 0 A to 270 mA with 18 μA quiescent current, demonstrating excellent performance. The PSR performance of proposed LDO is also satisfactory. The experimental results validate the effectiveness of proposed techniques in enhancing LDO transient response while maintaining stability.

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Xin-Ce Gong (Student Member, IEEE) received the B.Sc. degree in microelectronics science and engineering from the School of Electronic Science and Engineering, University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2022, where he is currently working toward the Ph.D. degree in microelectronics and solid-state electronics with the Power Integration Technology Laboratory.

His current research interests include LDO and isolated dc-dc converter, etc.

Jian-Jun Kuang (Student Member, IEEE) received the B.Sc. degree in integrated circuit design and integration systems and M.Sc. degree in microelectronics and solid-state electronics from the School of Electronic Science and Engineering, University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2020 and 2023, respectively, where he is currently working toward the Ph.D. degree in electronic information.

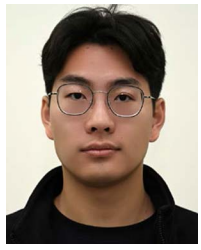
He is currently with Southchip Semiconductor Corporation Ltd. He has authored or coauthored high-quality papers in journals such as IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS, and IEEE JOURNAL OF SOLID-STATE CIRCUITS. His research interests include LDO, dc-dc converter, and analog circuit techniques.

Xin Ming (Member, IEEE) received the M.Sc. and Ph.D. degrees in microelectronics from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2007 and 2012, respectively.

From 2013 to 2014, he was a Visiting Scholar with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, USA, where his research activity was ripple-based control circuit design. He is currently a Full Professor with UESTC. His current research interests include GaN drivers, switching power supply, LDO, and isolated dc-dc converter, etc.

Shi-Ting Hu received the B.Sc. degree in microelectronics science and technology from the School of Electronic Science and Engineering, University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2024, where she is currently working toward the Ph.D. degree in integrated circuit science and engineering with the Power Integration Technology Laboratory.

Her current research interests include dc-dc converter and high power DrMOS technology, etc.



Zheng-Hao Liu received the B.Sc. degree in microelectronics science and technology from the School of Electronic Science and Engineering, University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2023, where he is currently working toward the Ph.D. degree in integrated circuit science and engineering with the Power Integration Technology Laboratory.

His current research interests include dc-dc converter and PoL converter, etc.

Zhi-Yi Lin (Member, IEEE) received the B.Sc. degree in integrated circuit design and integration systems and M.Sc. degree in microelectronics and solid-state electronics from the School of Electronic Science and Engineering, University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2020 and 2023, respectively, where he is currently working toward the Ph.D. degree in electronic information.

His current research interests include GaN drivers, dc–dc converters, LDO, etc.

Mo Huang (Senior Member, IEEE) received the Ph.D. degree in microelectronics and solid-state electronics from Sun Yat-sen University, Guangzhou, China, in 2014.

From 2008 to 2014, he was an IC Design Engineer and Project Manager with Rising Microelectronic Ltd., Guangzhou, China. From 2015 to 2016, he was a Postdoctoral Fellow with the University of Macau, China. From 2017 to 2019, he was an Associate Professor with the School of Electronic and Information Engineering, South China University of Technology, Guangzhou, China. In 2019, he joined the Institute of Microelectronics, University of Macau, Macau, China, where he is currently an Associate Professor. His current research focus on power management integrated circuits and systems.

Dr. Huang was a recipient of the ISSCC 2017 Takuo Sugano Award for Outstanding Far-East Paper, and the CICC 2025 Best Regular Paper. He was the Technical Program Committee member of ISSCC and CICC.

Bo Zhang (Senior Member, IEEE) received the B.Sc. degree in electronic engineering from the Beijing Institute of Technology, Beijing, China, in 1985, and the M.Sc. degree in electronic engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 1988.

From 1988 to 1996, he worked on power semiconductor devices research and development with UESTC. From 1996 to 1999, he was a Visiting Professor with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, where his research activities were modern power semiconductor devices. Since returning to UESTC, in November 1999, he has worked on power devices and smart power integrated circuits. He is currently a Full Professor with UESTC, where he is also the Director of the Center for Integrated Circuits. He holds more than 100 China or US patents. He has authored or coauthored and presented more than 500 technical papers in scientific journals and international conferences. His work has received more than 4000 citations, with an H-index of 31 and i10-index of 134 (Source: Google Scholar). His research interest has been focused on the power semiconductor technology since 1987, including power discrete devices, power management ICs, and power integrated technology.

Prof. Zhang was a Member of the IEEE EDS Power Devices and ICs Committee from 2014 to 2017 and a TPC Member of the International Symposium on Power Semiconductor Devices and ICs (ISPSD) from 2010 to 2015. He has been an IEEE Chengdu Section EXCOM Member and the Chair of the Technology Committee since 2006. He is also an Editor of IEEE TRANSACTIONS ON ELECTRON DEVICES.