A Carrier-Based DPWM Method With Dynamic Clamping State Selection for Neutral-Point Voltage Balance in Vienna Rectifier

Juyeon Lee, *Graduate Student Member, IEEE*, Young-Min Go, *Member, IEEE*, and June-Seok Lee, *Senior Member, IEEE*

***Abstract*—In the Vienna rectifier, a common issue of discontinuous pulsewidth modulation (DPWM) methods is that the clamping operations induce significant neutral-point (NP) voltage fluctuations that lead to distortion of the input current. In this article, a carrier-based DPWM method with dynamic clamping state selection (DCSS) for NP voltage balance is proposed. The proposed method selects a combination of a certain phase and switching state as a clamping operation to mitigate the NP voltage imbalance. The selection of the combination is determined based on the theoretically estimated NP voltage instead of the sensed one, which enables the proposed method to be implemented independent of the voltage sensor accuracy. In addition, an alternative PWM sequence is proposed to minimize additional switching losses by considering the operation of DCSS. The validity of the proposed method is verified through experiments.**

***Index Terms*—Discontinuous pulsewidth modulation (DPWM), neutral-point (NP) voltage balance, Vienna rectifier.**

I. Introduction

VIENNA rectifier, which is a nonregenerative three-level boost converter, offers several advantages, including low total harmonic distortion (THD) of the input current and high-power density. Furthermore, as the Vienna rectifier is composed of fewer switching devices compared to other three-level converters, it enables a reduction in manufacturing cost and system size. Thus, the Vienna rectifier is widely used in various applications, such as telecommunication systems, wind turbine systems, and electric vehicle chargers [1], [2], [3], [4], [5]. Fig. 1 shows the topology of the Vienna rectifier, where $V_{\rm dc}$, i_x, and e_x ($x = a$, b, and c), L_f, R_f, $C_{\rm top}$, and $C_{\rm bottom}$ denote the dc-link voltage, the phase current, the grid voltage, the input filter inductance, the parasitic resistance, the capacitances of the upper and lower capacitors in the dc-link, respectively.

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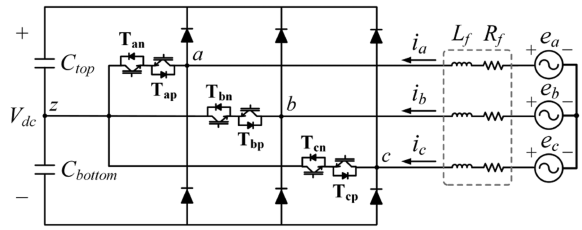

Fig. 1. Topology of the Vienna rectifier.

A recent trend in the industry is to increase the switching frequency of switching devices to reduce acoustic noise, filter size, and electromagnetic interference [1], [6]. However, this leads to an increase in switching losses and a decrease in power conversion efficiency. A discontinuous pulsewidth modulation (DPWM) method can relieve these negative effects of increasing switching frequency, as it is excellent at reducing switching losses by clamping the reference duty of a certain phase so that switching operations occur in only two of the three phases during each switching cycle. There are many previous studies on the DPWM method for two-level inverters [9], [10], [11]. Those methods clamp the reference voltage to $V_{\rm dc}/2$ (P-clamping) or $-V_{\rm dc}/2$ (N-clamping) with various modulation angles and modes, which can be selected depending on the phase current angle to minimize switching losses. However, these methods are not suitable for direct application to three-level converters, as they cannot utilize all the available vectors of three-level converters. One important consideration is that in the Vienna rectifier, which is a unidirectional converter, the pole voltage is determined depending on the switching state and the polarity of the phase current. Therefore, when the polarity of the reference voltage does not match that of the phase current, the desired pole voltage cannot be generated, leading to input current distortion—known as the zero-current distortion (ZCD) in Vienna rectifiers [12]. The space-vector DPWM (SVDPWM) method, which considers the ZCD in the Vienna rectifier, referred to as DPWMA, is proposed in [13]. This method involves an additional clamping state around the zero-crossing point of the phase current to avoid the ZCD, in which the reference voltage is clamped to 0 (O-clamping). In [14], a DPWM method is proposed, which is implemented based on a carrier-based DPWM (CB-DPWM) method. Although this method (called

CB-DPWMA hereafter in this article) shares the same clamping strategy as DPWMA, it has the advantage of being simple to implement by merely applying an offset voltage to achieve the clamping operation, without the computational complexity associated with SVDPWM. However, both the DPWMA and CB-DPWMA methods have a common issue that the clamping operation induces a large ac ripple in the neutral-point (NP) voltage, which has a frequency three times the fundamental one. Since this ripple component in the NP voltage not only causes distortion in the input current but also shortens the lifespan of the dc-link capacitors [15], it should be avoided.

Several CB-DPWM methods considering this issue are proposed in [16], [17], [18], [19], and [20]. The method presented in [16] modifies the reference duty signals, taking into account the actual value of the pole voltage. The pole voltage error caused by NP voltage imbalance is compensated by applying these methods, thereby effectively mitigating input current distortion even under NP voltage imbalance conditions. The DPWM method proposed in [17] considers the tradeoff between NP voltage ripple mitigation and switching loss reduction. This method maintains the clamping operation on the corresponding phase near the peak of the phase current while uniformly distributing the small vectors during the surrounding intervals to mitigate NP voltage fluctuation. In [18], [19], and [20], both advantages of eliminating the pole voltage error and mitigating the NP voltage fluctuation are adopted by applying the same approach as [16] and [17]. However, since all these methods do not regulate the NP voltage through real-time monitoring, they do not fundamentally resolve the NP voltage imbalance issue, including the voltage stress of switching devices and capacitors.

Several methods that regulate the NP voltage based on real-time monitored NP voltage are proposed in [21], [22], [23], [24], [25], [26], and [27]. The methods proposed in [21] and [22] perform NP voltage regulation by injecting an additional clamping offset component into the reference voltages of the conventional DPWM methods based on the monitored NP voltage. However, they cannot optimally reduce ac ripple of NP voltage, particularly depending on the modulation index (MI), because they utilize only a portion of the entire space vector diagram of each conventional DPWM method for NP voltage regulation. In addition, the ZCD is not addressed in [22]. The methods presented in [23] and [24] apply voltage vectors and utilize redundant small vectors to reduce the NP voltage based on the monitored NP voltage while clamping the switching state to mitigate switching losses. However, since they respectively stand on the basis of the SVDPWM and the duty-cycle predictive control with a cost function, the implementation is complex and entails significant computational burden. Moreover, they do not address additional switching losses that occur when the clamping states are frequently changed in almost every switching cycle to suppress NP voltage fluctuation. To manage the tradeoff between reduction of additional switching losses and NP voltage regulation, the CB-DPWM methods are proposed in [25], [26], and [27]. They introduce a hysteresis characteristic so that the NP voltage balancing control is activated only when the NP voltage exceeds a predefined allowable threshold. A hybrid CB-DPWM method is proposed in [28], which also considers the additional switching losses. It applies an NP voltage balancing approach similar to that in [25], [26], and [27], only when the NP voltage exceeds a predefined threshold. Otherwise, to reduce the phase current distortion under NP voltage imbalance, pole voltage error compensation is applied by modifying the reference voltages, following the same approach as [16]. However, these methods do not fundamentally resolve the issue of the additional switching losses. The SVDPWM method in [29] addresses the issue of additional switching losses by introducing a PWM sequence, which minimizes the switching state transitions between the clamping states. However, depending on the selected clamping mode, there still exist regions where additional switching losses occur. In [30], additional switching losses can be avoided in the entire clamping modes by applying an improved PWM sequence. However, its implementation involves high complexity and effort, since it requires frequent changes of carrier type, which entails modifying the digital signal processor (DSP) register.

Above all, the methods presented in [21], [22], [23], [24], [25], [26], [27], [28], [29], and [30] commonly monitor the NP voltage using the sensed voltages of C_{top} and C_{bottom} (V_{top} and V_{bottom}) obtained from voltage sensors. In practical environments, the sensed voltage signals contain significant noise, and to reduce its influence while ensuring proper dc-link voltage control, a low-pass filter (LPF) is applied to both the voltage sensing and analog-to-digital converter (ADC) circuits. However, while the dc components of V_{top} and V_{bottom} can be relatively accurately sensed, the ac ripple components—especially the fundamental triple-frequency or lower harmonics—are attenuated and phase-delayed due to the LPF, which makes accurate sensing difficult. As a result, those methods have a drawback in that the NP voltage balancing performance is highly dependent on the accuracy of voltage sensing, which, if inaccurate, can actually worsen the NP voltage fluctuation.

In this article, a CB-DPWM method with dynamic clamping state selection (DCSS) for the Vienna rectifier is proposed to mitigate NP voltage fluctuation. The proposed method selects the optimal clamping state based on the monitored NP voltage, where the monitoring is performed using the theoretically estimated NP voltage rather than the sensed one. This enables the proposed method to perform NP voltage balancing without being affected by the accuracy of voltage sensing. In addition, the proposed method applies the O-clamping during the interval where the polarities of the reference voltage and the phase current are different due to the input filter impedance and power factor. This allows the proposed method to reduce NP voltage fluctuation while preventing ZCD even under nonunity power factor. Furthermore, to prevent the additional switching losses caused by the application of DCSS, the proposed method introduces a modified switching pattern (MSP), which can be easily implemented compared to the methods proposed in [29] and [30], by simply modifying the reference duty signals. Moreover, since the impact of the MSP on the phase currents is considered in the proposed method, the increase in phase current THD can be minimized by applying an additional adjustment of the switching pattern. As a result, the proposed method achieves NP voltage balancing while retaining the switching loss reduction benefits of the DPWM method as much as possible, and also maintains the phase current THD at a desirable level. The

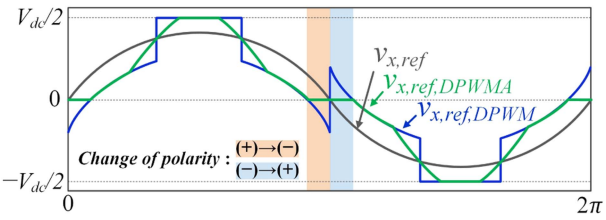

Fig. 2. Reference voltage according to the applied PWM method.

validity of the proposed method is verified through experimental results.

II. Conventional CB-DPWMA Method

A. Development of CB-DPWMA Method

The reference voltages of the three phases ($v_{x,\mathrm{ref}}$, $x = a$, b, and c) are defined as

$$\begin{aligned} v_{a,\mathrm{ref}} &= V_{\mathrm{mag}} \cos(\omega t) \\ v_{b,\mathrm{ref}} &= V_{\mathrm{mag}} \cos\left(\omega t - \frac{2}{3}\pi\right) \\ v_{c,\mathrm{ref}} &= V_{\mathrm{mag}} \cos\left(\omega t + \frac{2}{3}\pi\right), \end{aligned} \tag{1}$$

where V_{mag} is the magnitude of the reference voltage and ω is the angular frequency of e_x ($x = a$, b, and c). To minimize switching losses, the reference voltage of the phase with the largest current magnitude among the three phases should be clamped. As it can be assumed that the phase difference (θ_{diff}) between the reference voltage and the phase current is zero, the offset voltage (V_{offset}) for implementing the clamping operation is defined as

$$V_{\mathrm{offset}} = \begin{cases} V_{\mathrm{dc}}/2 - V_{\mathrm{max}}, & |V_{\mathrm{max}}| \geq |V_{\mathrm{min}}| \\ -V_{\mathrm{dc}}/2 - V_{\mathrm{min}}, & |V_{\mathrm{max}}| < |V_{\mathrm{min}}|, \end{cases} \tag{2}$$

where V_{max} and V_{min} denote the maximum and minimum values of $v_{x,\mathrm{ref}}$ among the three phases, respectively. The reference voltage applying V_{offset} ($v_{x,\mathrm{ref,DPWM}}$, $x = a$, b and c) is defined as

$$v_{x,\mathrm{ref,DPWM}} = v_{x,\mathrm{ref}} + V_{\mathrm{offset}} \quad (x = a,\ b,\ \text{and } c). \tag{3}$$

However, as shown in Fig. 2, there exists an interval where the polarity of $v_{x,\mathrm{ref,DPWM}}$ changes due to the application of V_{offset}, resulting in the occurrence of ZCD. Therefore, to prevent ZCD in the Vienna rectifier, the O-clamping operation is introduced during that interval by modifying V_{offset} to $V_{\mathrm{offset},VN}$, which is defined as

$$V_{\mathrm{offset},VN} = \begin{cases} V_{\mathrm{dc}}/2 - V_{\mathrm{max}}, & |V_{\mathrm{max}}| \geq |V_{\mathrm{min}}| \ \ \& \ \ V_{\mathrm{offset}} < -V_{\mathrm{mid}} \\ -V_{\mathrm{mid}}, & |V_{\mathrm{max}}| \geq |V_{\mathrm{min}}| \ \ \& \ \ V_{\mathrm{offset}} > -V_{\mathrm{mid}} \\ -V_{\mathrm{mid}}, & |V_{\mathrm{max}}| < |V_{\mathrm{min}}| \ \ \& \ \ V_{\mathrm{offset}} < -V_{\mathrm{mid}} \\ -V_{\mathrm{dc}}/2 - V_{\mathrm{min}}, & |V_{\mathrm{max}}| < |V_{\mathrm{min}}| \ \ \& \ \ V_{\mathrm{offset}} > -V_{\mathrm{mid}} \end{cases} \tag{4}$$

where V_{mid} denotes the median value of $v_{x,\mathrm{ref}}$ among the three phases. The reference voltage applying $V_{\mathrm{offset},VN}$

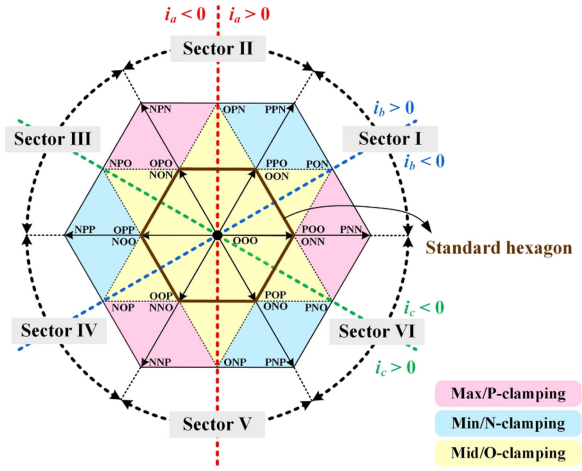

Fig. 3. Space vector diagram of the CB-DPWMA method.

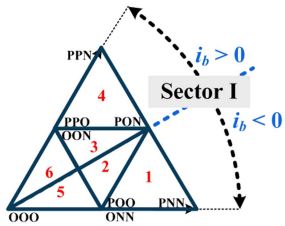

Fig. 4. Subsectors in Sector I.

($v_{x,\mathrm{ref,DPWMA}}$, $x = a$, b, and c) is defined as

$$v_{x,\mathrm{ref,DPWMA}} = v_{x,\mathrm{ref}} + V_{\mathrm{offset},VN} \quad (x = a,\ b,\ \textit{and } c). \tag{5}$$

In Fig. 2, it can be seen that $v_{x,\mathrm{ref,DPWMA}}$ is clamped to 0 during the interval where the polarity of $v_{x,\mathrm{ref,DPWM}}$ changes due to the application of V_{offset}. Fig. 3 illustrates the space vector diagram of the Vienna rectifier, where θ_{diff} is assumed to be 0. The shaded areas with pink, blue, and yellow represent each interval of max/P-clamping, min/N-clamping, and mid/O-clamping, where V_{max}, V_{min}, and V_{mid} are clamped to $V_{\mathrm{dc}}/2$, $-V_{\mathrm{dc}}/2$, and 0, respectively. It can be observed that the mid/O-clamping region is located near the boundary where the polarity of the phase current changes, and that the max/P-clamping and min/N-clamping regions appear at 60° intervals as the magnitude relationship among the reference voltages changes every 60°.

B. Analysis of NP Voltage Fluctuation in the DPWMA Method

The NP voltage fluctuates depending on the NP current (i_{NP}), which is determined by i_x ($x = a$, b, and c) and the corresponding switching duty ratio. Considering the exterior of the standard hexagon, as shown in Fig. 3, the applicable clamping states for DPWM operation are max/P-clamping, min/N-clamping, and mid/O-clamping. Fig. 4 depicts the subsectors of Sector I, where $i_a > i_b > i_c$. Note that $i_{\mathrm{max}} > 0$ and $i_{\mathrm{min}} < 0$ always hold, while the polarity of i_{mid} varies depending on the subsector. In Sector I, $i_{\mathrm{mid}} < 0$ ($|i_{\mathrm{max}}| > |i_{\mathrm{min}}|$) in subsectors 1 and 2, and $i_{\mathrm{mid}} > 0$ ($|i_{\mathrm{max}}| < |i_{\mathrm{min}}|$) in subsectors 3 and 4. Accordingly, the selected vectors to achieve DPWM operation in subsectors 1 and 2 are POO-PON-PNN and OON-PON-POO, respectively.

TABLE I
VARIATION OF NP VOLTAGE IN SECTOR I ACCORDING TO CLAMPING STATE

Sector	Relationship of i_x	Judgement		Sub-sector	Applicable clamping state	Variation of v_{neu}
I	$i_a>i_b>i_c$	$\lvert V_{max}\rvert>\lvert V_{min}\rvert$	$V_{max}-V_{min}>V_{dc}/2$		max/P-clamping	increase (+)
			$V_{offset}<-V_{mid}$	1	min/N-clamping	decrease (−)
					mid/O-clamping	increase (+)
			$V_{offset}>-V_{mid}$	2	min/N-clamping	decrease (−)
			$V_{max}-V_{min}<V_{dc}/2$		max/O-clamping	decrease (−)
			$V_{offset}>-V_{mid}$	5	mid/O-clamping	increase (+)
					min/O-clamping	increase (+)
		$\lvert V_{max}\rvert<\lvert V_{min}\rvert$	$V_{max}-V_{min}>V_{dc}/2$		mid/O-clamping	decrease (−)
			$V_{offset}<-V_{mid}$	3	max/P-clamping	increase (+)
					min/N-clamping	decrease (−)
			$V_{offset}>-V_{mid}$	4	max/P-clamping	increase (+)
			$V_{max}-V_{min}<V_{dc}/2$		max/O-clamping	decrease (−)
			$V_{offset}<-V_{mid}$	6	mid/O-clamping	decrease (−)
					min/O-clamping	increase (+)

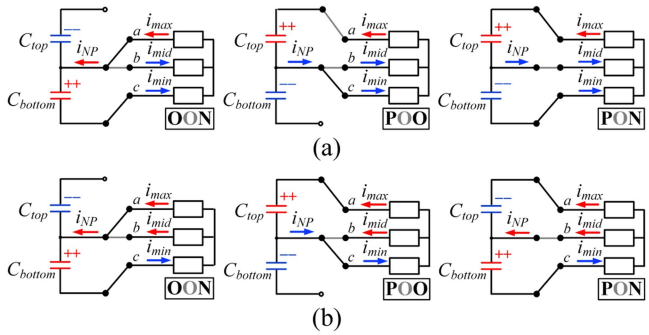

Fig. 5. Current path of i_{NP} and its effect on V_{top} and V_{bottom} for each vector in Sector I. (a) Subsector 2. (b) Subsector 3.

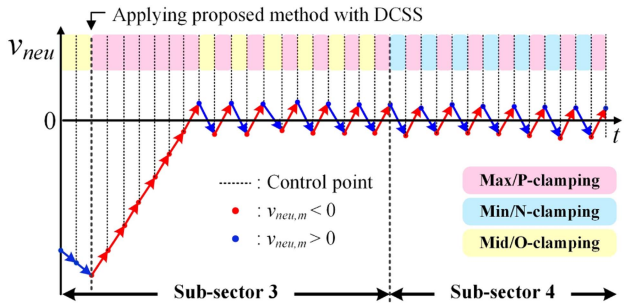

Fig. 6. NP voltage balancing through DCSS.

Likewise, those for subsectors 3 and 4 are OON-PON-POO and OON-PPN-PON, respectively. Fig. 5 illustrates the current path of i_{NP} and its effect on V_{top} and V_{bottom} according to the selected vector in subsectors 2 and 3. For subsector 2 in Fig. 5(a), i_{NP} has a positive polarity for OON, leading to charging C_{bottom}, and a negative polarity for POO and PON, leading to discharging C_{bottom}. Since the proportion of POO and PON is more dominant than that of OON in subsector 2, the NP voltage, which is defined as $V_{top}-V_{bottom}$, increases during this interval. For subsector 3 in Fig. 5(b), i_{NP} has a positive polarity for OON and PON, leading to charging C_{bottom}, and a negative polarity for POO, leading to discharging C_{bottom}. Since the proportion of OON and PON is more dominant than that of POO in subsector 3, the NP voltage decreases during this interval. Likewise, in subsectors 1 and 4, max/P-clamping and min/N-clamping are applied, respectively, and the phase current with the largest absolute value consistently flows through the same path. In subsector 1, C_{top} is charged, resulting in an increase in the NP voltage, whereas in subsector 4, C_{bottom} is charged, resulting in a decrease in the NP voltage. Other sectors can be generalized by classifying the three phases as *max*, *mid*, and *min* based on Fig. 3, allowing the NP voltage fluctuation to be analyzed in the same manner. As a result, when the conventional DPWMA method is applied, the NP voltage alternately increases and decreases almost every 30°, leading to large fluctuations at a frequency three times that of the fundamental.

III. PROPOSED DPWM METHOD WITH DCSS AND MSP

A. Development of DCSS Considering ZCD

Table I lists the NP voltage variation according to the applicable clamping states for each subsector of Sector I, derived from the same approach as the analysis presented in Section II-B. Since all sectors differ only in the magnitude relationship among the three phases, those of other sectors can also be easily derived. Subsectors 1–4 are located in the exterior of the standard hexagon, while subsectors 5 and 6 are located in the interior of the standard hexagon. Note that, under the condition where the MI (defined as $\sqrt{3}V_{mag}/V_{dc}$) is less than 0.5, the reference voltage vector always lies inside the standard hexagon, whereas under the condition for MI $>$ 0.58, it always lies outside the standard hexagon. From Table I, it can be observed that each subsector has two applicable clamping states, which have opposite effects on NP voltage variation. Accordingly, NP voltage balancing can be achieved by selecting and applying the appropriate clamping state that drives the NP voltage toward zero, based on its real-time monitored value. Fig. 6 depicts the NP voltage balancing process achieved through DCSS in subsectors 3 and 4 for Sector I, where v_{neu} is the actual NP voltage. Before applying DCSS, it can be observed that v_{neu} decreases due to the application of mid/O-clamping in subsector 3.

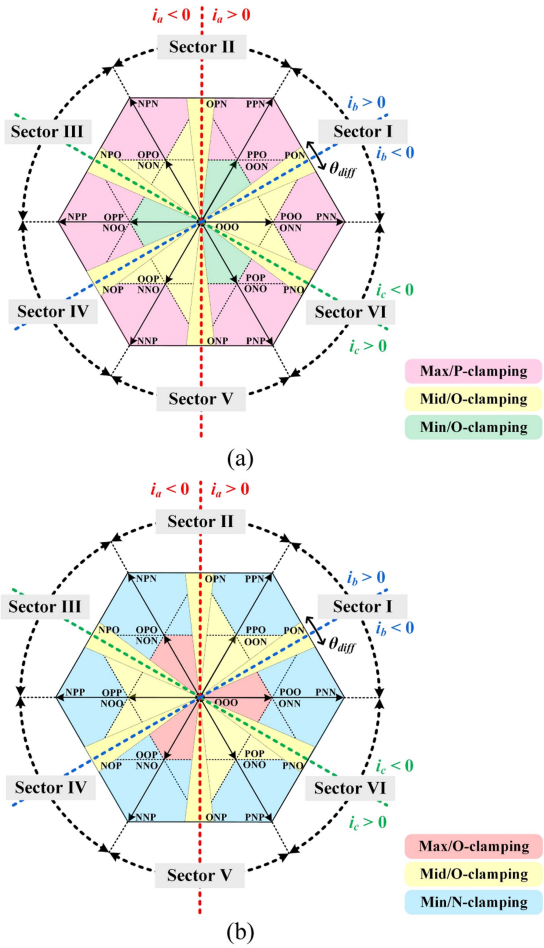

Fig. 7. Space vector diagram of the proposed DCSS method. (a) $v_{neu,m} < 0$. (b) $v_{neu,m} > 0$.

After applying DCSS, the polarity of the currently monitored NP voltage ($v_{neu,m}$) is detected at every control cycle, and the max/P-clamping state that can increase v_{neu} is consistently applied. As a result, v_{neu} gradually approaches zero. Once the polarity of $v_{neu,m}$ reverses, the mid/O-clamping is applied by DCSS to reduce v_{neu}, thereby maintaining it near zero. Similarly, in subsector 4, the mid/O-clamping and min/N-clamping states are alternately applied to keep v_{neu} close to zero. However, it should be noted that in practice, θ_{diff} is not zero. Therefore, to prevent ZCD, it is necessary to insert an additional mid/O-clamping interval around the zero-crossing of i_{mid}. However, since this interval is intentionally inserted irrespective of the monitored NP voltage, NP voltage balancing is not performed during this interval, and the NP voltage varies depending solely on the corresponding effect of the mid/O-clamping during this interval. Therefore, this interval should be minimized, which can be achieved by applying the mid/O-clamping state only during the phase difference interval determined by θ_{diff}. The term θ_{diff} can be derived from (6), as presented in [12]. θ_1 and θ_2 are the components of θ_{diff}, which are defined as (7), where θ_z and θ_{pf} denote the phase difference caused by the input filter impedance and the power factor (*pf*). The terms I_{qe}, I_{mag}, and E_{mag} denote the q-axis current in the synchronous reference frame and the magnitude of i_x and e_x, respectively.

$$\theta_{\text{diff}} = \theta_1 + \theta_2 \tag{6}$$

$$[\theta_1,\ \theta_2] = \begin{cases} [\theta_{pf},\ \theta_z] & (\text{for leading } pf) \\ [0,\ \theta_{pf}],\ (\theta_{pf} > \theta_z) \\ [0,\ \theta_z],\ (\theta_{pf} < \theta_z) & (\text{for lagging } pf) \end{cases} \quad \& \quad \left\{ \theta_{pf} = \cos^{-1}\left(\frac{I_{qe}}{I_{\text{mag}}}\right), \theta_z = \tan^{-1}\left(\frac{-I_{\text{mag}} \cdot \omega L_f}{E_{\text{mag}} - I_{\text{mag}} \cdot R_f}\right) \right\}. \tag{7}$$

Since the three phases can be classified into *max*, *mid*, and *min* for all Sectors, the clamping states can be determined in the same manner as shown for Sector I in Table I. Fig. 7(a) and (b) illustrates the space vector diagram with the clamping states selected for each Sector and subsector in the proposed DCSS method for both cases, where $v_{neu,m} < 0$ and $v_{neu,m} > 0$. It can be seen that the clamping state that increases v_{neu} is selected when $v_{neu,m} < 0$, whereas the one that decreases v_{neu} is selected when $v_{neu,m} > 0$. Consequently, the offset voltage ($V_{\text{offset,DCSS}}$) for implementing the proposed DCSS method considering ZCD is defined as (8) shown at the bottom of this page, where θ denotes the phase angle of e_a. As a result, the reference voltage of the proposed DPWM method with DCSS ($v_{x,\text{ref,DCSS}}, x = a,$

$$V_{\text{offset,DCSS}} = \begin{cases} V_{\text{dc}}/2 - V_{\max}, & v_{neu,m} < 0 \\ -V_{\text{dc}}/2 - V_{\min}, & v_{neu,m} > 0 \end{cases} \ \& \ |V_{\max}| \geq |V_{\min}| \ \& \ V_{\text{offset}} < -V_{\text{mid}}$$
$$\begin{cases} -V_{\text{mid}}, & v_{neu,m} < 0 \\ V_+, & v_{neu,m} > 0 \end{cases} \ \& \ |V_{\max}| \geq |V_{\min}| \ \& \ V_{\text{offset}} > -V_{\text{mid}}$$
$$\begin{cases} V_-, & v_{neu,m} < 0 \\ -V_{\text{mid}}, & v_{neu,m} > 0 \end{cases} \ \& \ |V_{\max}| < |V_{\min}| \ \& \ V_{\text{offset}} < -V_{\text{mid}}$$
$$\begin{cases} V_{\text{dc}}/2 - V_{\max}, & v_{neu,m} < 0 \\ -V_{\text{dc}}/2 - V_{\min}, & v_{neu,m} > 0 \end{cases} \ \& \ |V_{\max}| < |V_{\min}| \ \& \ V_{\text{offset}} > -V_{\text{mid}}$$
$$-V_{\text{mid}}, \quad \frac{n\pi}{3} - \theta_1 < \theta < \frac{n\pi}{3} + \theta_2, \quad (n = 0, 1, \ldots, 5)$$
$$\left(V_+ = \begin{cases} -V_{\text{dc}}/2 - V_{\min}, & (V_{\max} - V_{\min} > V_{\text{dc}}/2) \\ -V_{\max}, & (V_{\max} - V_{\min} < V_{\text{dc}}/2) \end{cases} \right.$$
$$\left. V_- = \begin{cases} V_{\text{dc}}/2 - V_{\max}, & (V_{\max} - V_{\min} > V_{\text{dc}}/2) \\ -V_{\min}, & (V_{\max} - V_{\min} < V_{\text{dc}}/2) \end{cases} \right) \tag{8}$$

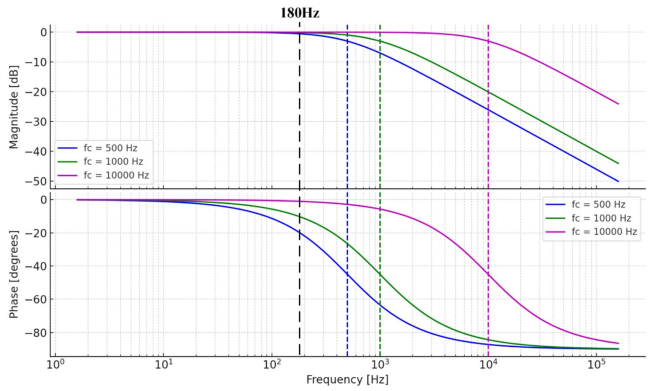

Fig. 8. Bode plots of first-order LPF with various f_c.

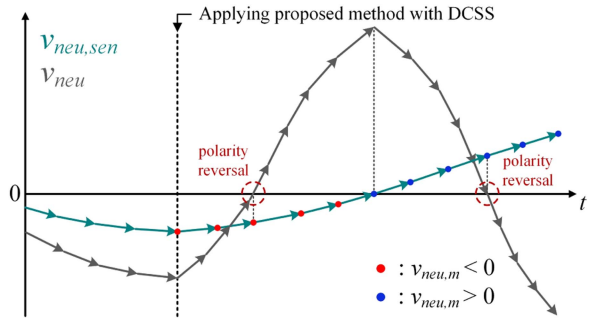

Fig. 9. Illustration of operating scenario of NP voltage balancing with DCSS based on $v_{neu,sen}$.

b, and c) is defined as (9).

$$v_{x,\mathrm{ref,DCSS}} = v_{x,\mathrm{ref}} + V_{\mathrm{offset,DCSS}}, \quad (x = a,\ b,\ and\ c)\,. \tag{9}$$

B. Introducing Model-Based Estimation of NP Voltage to Prevent Performance Degradation in NP Voltage Balancing With DCSS

Fig. 8 shows the Bode plots of a first-order LPF for cutoff frequencies (f_c) of 500 Hz, 1 kHz, and 10 kHz, respectively. It can be observed from the Bode plots that signals with frequencies above 180 Hz experience significant magnitude attenuation and phase delay. The frequency of v_{neu} appears at three times the fundamental (180 Hz) when the DPWMA method is applied, and it is expected to increase further when NP voltage balancing is applied. Thus, assuming that f_c typically applied to practical voltage sensor and ADC circuits is below 10 kHz, it is difficult to precisely sense the ac ripple component of v_{neu}, unlike its dc component. Therefore, the sensed NP voltage ($v_{neu,sen}$) cannot provide accurate information in monitoring the polarity of v_{neu} in real time, which is required for achieving effective NP voltage balancing. Fig. 9 shows a scenario where the proposed DCSS method fails to achieve immediate NP voltage balancing when NP voltage monitoring is performed using $v_{neu,sen}$. Note that $v_{neu,sen}$ is depicted with an arbitrary error relative to the actual v_{neu}, in order to reflect the effects of noise and the LPF. After applying NP voltage balancing, the DCSS operates to increase v_{neu}, as the polarity of $v_{neu,m}$ is detected as negative. Accordingly, v_{neu} continues to increase. However, when v_{neu} rises above zero and its polarity reverses to positive, $v_{neu,sen}$ still holds a negative value. Consequently, the polarity of $v_{neu,m}$ continues to be detected as negative, and DCSS keeps operating to increase v_{neu}, which leads to a large fluctuation in the positive direction. Similarly, once the polarity of $v_{neu,sen}$ changes, the DCSS operates to decrease v_{neu}, which then continuously decreases. Even after the polarity of v_{neu} becomes negative, $v_{neu,sen}$ still holds a positive value, causing the DCSS to continue operating in a manner that decreases v_{neu}. As a result, NP balancing with DCSS fails to regulate v_{neu} around zero, resulting in large fluctuations. To prevent the performance degradation of NP voltage balancing with DCSS caused by $v_{neu,sen}$, the proposed method introduces a model-based-estimated value of v_{neu} ($v_{neu,est}$) for monitoring v_{neu}. v_{neu} can be divided into an ac ripple component and a dc component. The ac ripple arises from the charging and discharging of C_{top} and C_{bottom} caused by i_{NP}, and the dc component is formed by the dc component of i_{NP}. i_{NP} is determined by the phase current and the switching state of the three phases. The average value of i_{NP} over one switching cycle (i_{neu}) is defined as

$$i_{neu} = -\sum\Big|_{x=a,b,c} \left(d_{x,\mathrm{ref,DCSS}} i_x\right), \quad \left(d_{x,\mathrm{ref,DCSS}} = \frac{v_{x,\mathrm{ref,DCSS}}}{V_{\mathrm{dc}}/2}\right), \tag{10}$$

where $d_{x,\mathrm{ref,DCSS}}$ denotes the reference duty when applying the proposed DPWM method with DCSS. Then, v_{neu} can be derived by integrating i_{neu}, based on the voltage–current relationship of the capacitor [31]. However, in practical digital implementation, $v_{neu,est}$ may exhibit a dc offset error if the value of v_{neu} at the start of integration (i.e., the initial value) is not properly reflected. Thus, it is necessary to separately derive the ac and dc components of v_{neu}. The ac component of $v_{neu,est}$ ($v_{neu,\mathrm{est,AC}}$) can be derived from the integration of i_{neu}. To eliminate the dc component in the integration result accumulated over time, the integrated value must be periodically reset to zero. If, however, $v_{neu,est}$ is unintentionally reset during NP voltage balancing, it may lead to inaccurate monitoring of v_{neu}. This issue can be addressed by resetting $v_{neu,est}$ only within the θ_{diff} interval, where NP voltage balancing is not active. Then, $v_{neu,\mathrm{est,AC}}$ is defined as

$$v_{neu,\mathrm{est,AC}} = \begin{cases} 0, & \left(\frac{n\pi}{3} - \theta_1 < \theta < \frac{n\pi}{3} + \theta_2,\ n = 0, 1, \ldots, 5\right) \\ \frac{1}{C_{\mathrm{dc}}} \int_{T_s} -i_{neu} dt, & (\mathrm{otherwise}) \end{cases}, \tag{11}$$

where C_{dc} is equal to C_{top} and C_{bottom} (assuming $C_{\mathrm{top}} = C_{\mathrm{bottom}}$), and T_s denotes the control period. The dc component of $v_{neu,\mathrm{est}}$ ($v_{neu,\mathrm{est,DC}}$) can be obtained from the difference between the dc components of V_{top} and V_{bottom}. As previously mentioned, unlike the ac component that has a specific frequency, the dc component, which has no frequency, is not affected by magnitude attenuation or phase delay by LPF. Therefore, it can be assumed that $v_{neu,sen}$ accurately reflects the dc component of v_{neu}. Accordingly, by applying a digital LPF to the sensed V_{top} and V_{bottom}, the pure dc components ($V_{\mathrm{top,LPF}}$

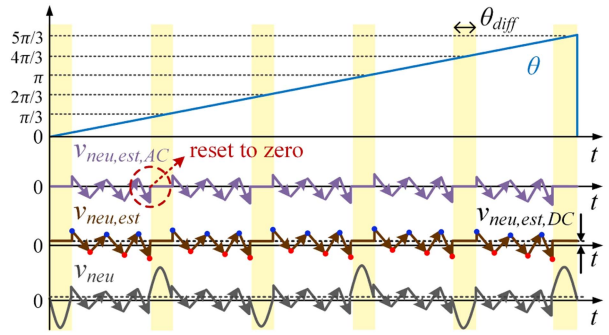

Fig. 10. Illustration of $v_{neu,est}$ and its components when NP voltage balancing with DCSS based on $v_{neu,\mathrm{est}}$ is applied.

and $V_{\mathrm{bottom,LPF}}$) can be extracted, where f_c of digital LPF is set sufficiently low to effectively eliminate the ac components. The term $v_{neu,\mathrm{est,DC}}$ is defined as (12). Finally, $v_{neu,est}$ is defined as (13).

$$v_{neu,\mathrm{est,DC}} = V_{\mathrm{top,LPF}} - V_{\mathrm{bottom,LPF}} \tag{12}$$

$$v_{neu,\mathrm{est}} = v_{neu,\mathrm{est,AC}} + v_{neu,\mathrm{est,DC}}. \tag{13}$$

Fig. 10 shows $v_{neu,\mathrm{est}}$ and its components when NP voltage balancing is applied based on $v_{neu,\mathrm{est}}$. It can be observed that $v_{neu,\mathrm{est}}$ consists of $v_{neu,\mathrm{est,AC}}$ and $v_{neu,\mathrm{est,DC}}$, where $v_{neu,\mathrm{est,AC}}$ is reset and maintained at zero during the interval of θ_{diff}.

C. Application of MSP to Avoid Additional Switching Losses

The switching state (S_x, x = *max*, *mid*, and *min*) of each phase in the Vienna rectifier is determined depending on the relationship between $d_{x,\mathrm{comp}}$ (x = *max*, *mid*, and *min*) and the carrier signal (V_{tri}), where $d_{x,\mathrm{comp}}$ denotes the level-shifted signal of $d_{x,\mathrm{ref,DCSS}}$ to be compared with V_{tri}, defined as

$$d_{x,\mathrm{comp}} = \begin{cases} d_{x,\mathrm{ref,DCSS}}, & (V_x \geq 0) \\ d_{x,\mathrm{ref,DCSS}} + 1, & (V_x < 0) \end{cases} \tag{14}$$

$$S_x = \begin{cases} 1, & (V_{tri} \geq d_{x,\mathrm{comp}}) \ \& \ (V_x \geq 0) \\ 0, & (V_{tri} < d_{x,\mathrm{comp}}) \ \& \ (V_x \geq 0) \\ 0, & (V_{tri} \geq d_{x,\mathrm{comp}}) \ \& \ (V_x < 0) \\ 1, & (V_{tri} < d_{x,\mathrm{comp}}) \ \& \ (V_x < 0) \end{cases}. \tag{15}$$

where the values of S_x "1" and "0" denote the turned-ON and turned-OFF states, respectively. Accordingly, the possible switching patterns that may occur when the proposed DPWM method with DCSS is applied are illustrated for each phase (x = *max*, *mid*, and *min*), as shown in Fig. 11. The terms $v_{x,z}$ and T_{sw} denote the pole voltage and the switching period, respectively. Fig. 11(a) shows the switching behavior in the *max* phase when max/P-clamping and other clamping states alternate every switching cycle. During the max/P-clamping interval, S_{max} remains in the "0" state, and in the subsequent switching cycle, the switching operation occurs internally without additional state transition. However, in the switching behavior of the *min* phase shown in Fig. 11(b), when min/N-clamping and other clamping states alternate, it can be observed that an additional switching transition occurs: S_{min} remains at "0" during the min/N-clamping interval, but switches to "1" at the transition to the next switching cycle. A similar switching transition occurs again when the clamping state returns to min/N-clamping in the following cycle. Fig. 11(c) and (d) show the switching behavior in the *mid* phase when mid/O-clamping and other clamping states alternate, where the conditions correspond to $V_{\mathrm{mid}} \geq 0$ and $V_{\mathrm{mid}} < 0$, respectively. In the same principle as *max* and *min* phase, it can be observed that in the *mid* phase, an additional switching transition occurs when $V_{\mathrm{mid}} \geq 0$, whereas no additional switching occurs when $V_{\mathrm{mid}} < 0$. Accordingly, Table II summarizes the phases in which additional switching transitions occur, depending on the clamping interval determined by the DCSS operation. Such switching behavior causes additional switching losses, which leads to degradation of the efficiency in the proposed DCSS method. This can be avoided by adjusting the switching pattern determined by (15), as shown in Fig. 12.

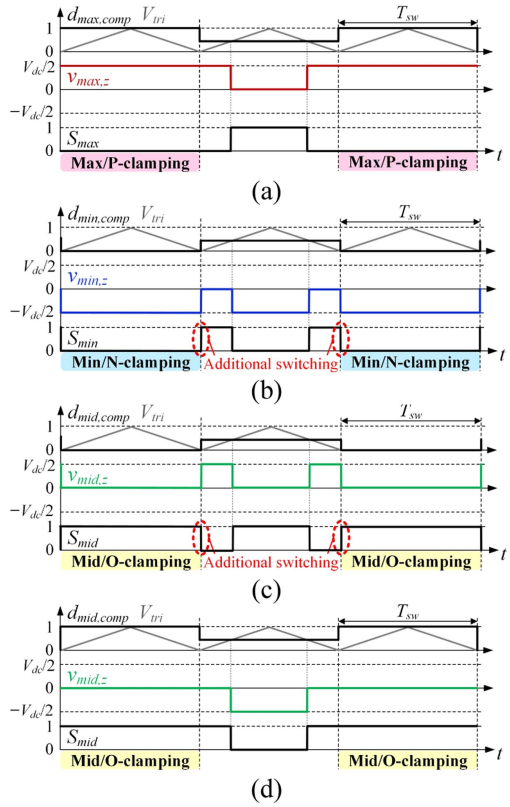

Fig. 11. Illustration of switching behaviors in each phase when the clamping states alternate due to the operation of DCSS (outside the standard hexagon). (a) *Max* phase. (b) *Min* phase. (c) *Mid* phase ($V_{\mathrm{mid}} \geq 0$). (d) *Mid* phase ($V_{\mathrm{mid}} < 0$).

TABLE II
CLAMPING ZONES AND CORRESPONDING PHASES WITH ADDITIONAL SWITCHING TRANSITIONS

Case	Zone	Condition	Clamping state	Phase
Exterior of standard hexagon	A	$\lvert V_{\mathrm{max}}\rvert \geq \lvert V_{\mathrm{min}}\rvert$ and $V_{\mathrm{offset}} < -V_{\mathrm{mid}}$	max/P, min/N	min
	B	$\lvert V_{\mathrm{max}}\rvert \geq \lvert V_{\mathrm{min}}\rvert$ and $V_{\mathrm{offset}} > -V_{\mathrm{mid}}$	mid/O, min/N	min
	C	$\lvert V_{\mathrm{max}}\rvert < \lvert V_{\mathrm{min}}\rvert$ and $V_{\mathrm{offset}} < -V_{\mathrm{mid}}$	max/P, mid/O	mid
	D	$\lvert V_{\mathrm{max}}\rvert < \lvert V_{\mathrm{min}}\rvert$ and $V_{\mathrm{offset}} > -V_{\mathrm{mid}}$	max/P, min/N	min
Interior of standard hexagon	B	$\lvert V_{\mathrm{max}}\rvert \geq \lvert V_{\mathrm{min}}\rvert$ and $V_{\mathrm{offset}} > -V_{\mathrm{mid}}$	mid/O, max/O	max
	C	$\lvert V_{\mathrm{max}}\rvert < \lvert V_{\mathrm{min}}\rvert$ and $V_{\mathrm{offset}} < -V_{\mathrm{mid}}$	min/O, mid/O	mid

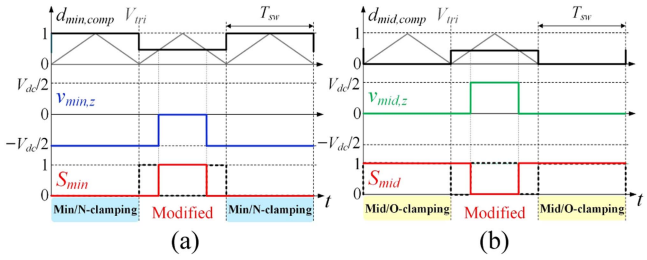

Fig. 12. Modification of switching pattern to avoid additional switching losses. (a) Min phase. (b) Mid phase ($d_{\mathrm{mid,ref,DCSS}} \geq 0$).

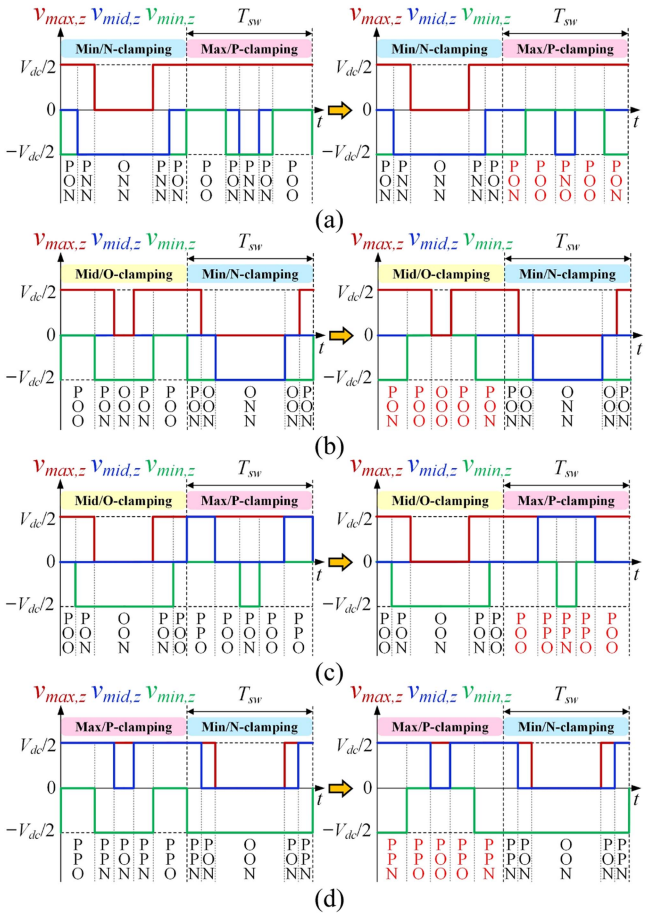

Fig. 13. Illustration of pole voltage of three phases when the switching patterns are modified (outside the standard hexagon). (a) Zone A. (b) Zone B. (c) Zone C. (d) Zone D in Sector I.

Since the duty ratios of all phases must be kept identical, it can be seen that (14) should also be modified in conjunction with (15). Fig. 13 shows the MSP designed to prevent additional switching losses in all zones in the exterior of the standard hexagon. As the switching pattern is modified, it can be observed that no additional switching transitions occur in any of the zones. However, although the duty ratio applied to each phase remains unchanged after the switching pattern is modified, the applied voltage vector may vary. If the modified phase coincides with the clamped phase, the voltage vector remains the same; otherwise, it changes. For example, in zones A and D of Fig. 13(a) and (d),

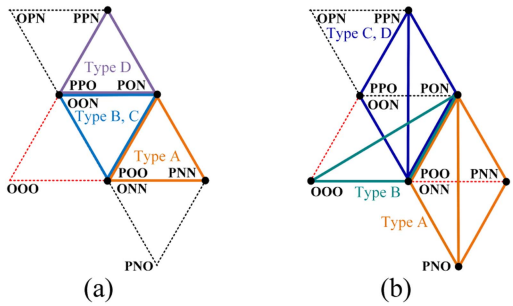

Fig. 14. Applied voltage vector types after modifying switching pattern in Sector I (outside the standard hexagon). (a) $v_{neu,m} > 0$. (b) $v_{neu,m} < 0$.

the voltage vector changes during max/P-clamping as the *min* phase is modified. Similarly, in zone B of Fig. 13(b), the voltage vector changes during mid/O-clamping due to modification of the *min* phase, and in zone C of Fig. 13(c), the voltage vector changes during max/P-clamping due to modification of the *mid* phase. It can be observed that those clamping states in which the voltage vector changes are selected when $v_{neu,m} < 0$. Fig. 14 illustrates the changes in the selected vector types in respective zones (A–D) on the space vector diagram for the exterior of the standard hexagon, resulting from the modification of the switching pattern presented in Fig. 13. After the pattern is modified, the selected vector types A–D form equilateral triangle shapes when $v_{neu,m} > 0$, whereas they form isosceles triangle shapes when $v_{neu,m} < 0$. This change alters the levels of phase voltages and increases switching ripples in the phase current. Moreover, due to this asymmetry between zones A and D, and between zones B and C, the phase current becomes asymmetric between the positive and negative half-cycles within a single fundamental period. These factors consequently lead to a significant increase in the input current THD. To address this asymmetry issue caused by the switching pattern modification, an additional adjustment of the switching pattern can be considered. It can be noted that in each zone, the phase that is not clamped continues to switch, and thus, modifying the switching pattern of that phase does not result in additional switching losses. Therefore, additional modifications of the *min* phase in zone C and the *mid* phase in zone D can be considered. The resulting pole voltages of the three phases with the additional modification are shown in Fig. 15. When the switching pattern of the nonclamped phase is modified, it can be observed that the applied voltage vectors during mid/O-clamping in zone C and min/N-clamping in zone D remain the same as those in the conventional case without any modification, except for a change in the sequence. As a result, the applied voltage vector types in zones C and D become identical to the conventional ones when $v_{neu,m} < 0$, while they are modified when $v_{neu,m} > 0$. The selected vector types with additional modification are illustrated in Fig. 16. Under the NP voltage balancing operation of the DCSS, the clamping states are alternately selected between the cases of $v_{neu,m} > 0$ and $v_{neu,m} < 0$ in steady state where v_{neu} remains within a small deviation around zero. In other words, for each zone, the vectors shown in Fig. 16(a) and (b) are alternately applied. Consequently, as the shapes of the selected vector types

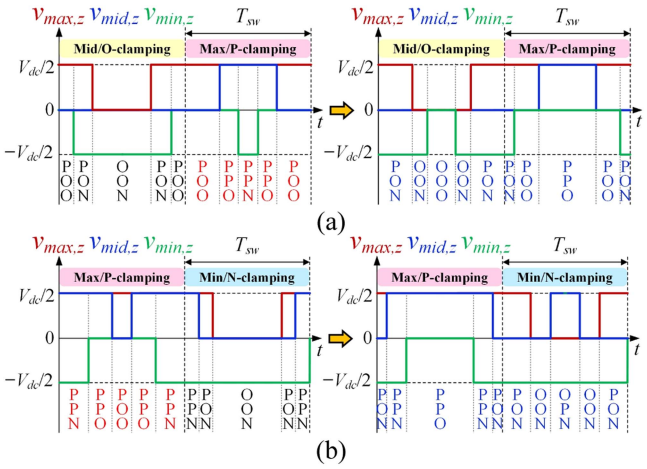

Fig. 15. Pole voltages in Sector I with additional modification (outside the standard hexagon). (a) Zone C. (b) Zone D.

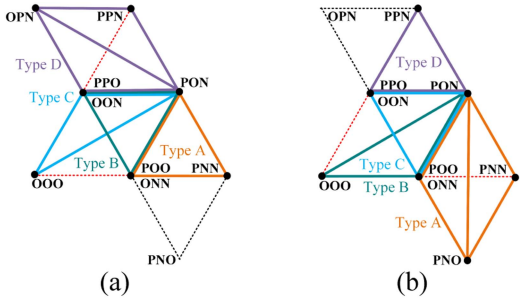

Fig. 16. Applied voltage vector types after applying additional modifications to switching pattern in Sector I (outside the standard hexagon). (a) $v_{neu,m} > 0$. (b) $v_{neu,m} < 0$.

are symmetric between zones A and D, and between zones B and C, the phase current is symmetric. As a result, additional switching losses can be prevented while minimizing the increase in input current THD by applying the proposed MSP. The modified signals of $d_{x,\mathrm{comp}}$ ($d_{x,\mathrm{comp,MSP}}$) and S_x ($S_{x,\mathrm{MSP}}$) with the proposed MSP are defined as

$$\begin{aligned} d_{\mathrm{max,comp,MSP}} &= -d_{\mathrm{max,ref,DCSS}} + 1 \\ d_{\mathrm{mid,comp,MSP}} &= -d_{\mathrm{mid,ref,DCSS}} + 1 \\ d_{\mathrm{min,comp,MSP}} &= -d_{\mathrm{min,ref,DCSS}} \end{aligned} \tag{16}$$

$$\begin{aligned} S_{\mathrm{max,MSP}} &= \begin{cases} 0, & (V_{tri} \geq d_{\mathrm{max,comp,MSP}}) \\ 1, & (V_{tri} < d_{\mathrm{max,comp,MSP}}) \end{cases} \\ S_{\mathrm{mid,MSP}} &= \begin{cases} 0, & (V_{tri} \geq d_{\mathrm{mid,comp,MSP}}) \\ 1, & (V_{tri} < d_{\mathrm{mid,comp,MSP}}) \end{cases} \\ S_{\mathrm{min,MSP}} &= \begin{cases} 1, & (V_{tri} \geq d_{\mathrm{min,comp,MSP}}) \\ 0, & (V_{tri} < d_{\mathrm{min,comp,MSP}}) \end{cases}. \end{aligned} \tag{17}$$

Likewise, in the interior of the standard hexagon, the phase requiring application of MSP can be determined using the same approach as that for the case of the exterior of the standard hexagon. Finally, the implementation of the proposed MSP is summarized in Table III.

TABLE III
SUMMARY OF IMPLEMENTATION OF THE PROPOSED MSP

Case	Zone	Signal compared with V_{tri}	Switching pattern
Exterior of standard hexagon	A	$d_{\mathrm{max,comp}}$, $d_{\mathrm{mid,comp}}$, $d_{\mathrm{min,comp,MSP}}$	S_{max}, S_{mid}, $S_{\mathrm{min,MSP}}$
	B	$d_{\mathrm{max,comp}}$, $d_{\mathrm{mid,comp}}$, $d_{\mathrm{min,comp,MSP}}$	S_{max}, S_{mid}, $S_{\mathrm{min,MSP}}$
	C	$d_{\mathrm{max,comp}}$, $d_{\mathrm{mid,comp,MSP}}$, $d_{\mathrm{min,comp,MSP}}$	S_{max}, $S_{\mathrm{mid,MSP}}$, $S_{\mathrm{min,MSP}}$
	D	$d_{\mathrm{max,comp}}$, $d_{\mathrm{mid,comp,MSP}}$, $d_{\mathrm{min,comp,MSP}}$	S_{max}, $S_{\mathrm{mid,MSP}}$, $S_{\mathrm{min,MSP}}$
Interior of standard hexagon	B	$d_{\mathrm{max,comp,MSP}}$, $d_{\mathrm{mid,comp}}$, $d_{\mathrm{min,comp,MSP}}$	$S_{\mathrm{max,MSP}}$, S_{mid}, $S_{\mathrm{min,MSP}}$
	C	$d_{\mathrm{max,comp}}$, $d_{\mathrm{mid,comp,MSP}}$, $d_{\mathrm{min,comp}}$	S_{max}, $S_{\mathrm{mid,MSP}}$, S_{min}

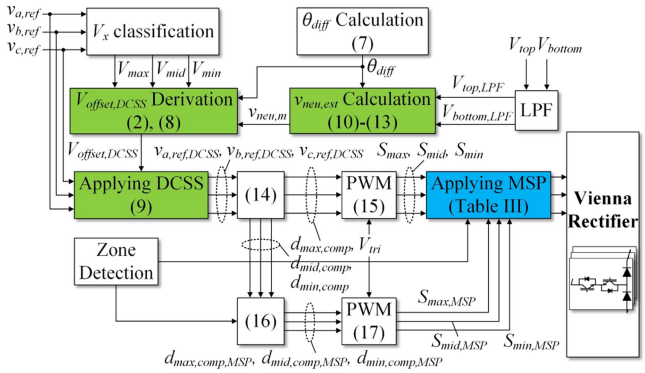

Fig. 17. Block diagram of the proposed DPWM method with DCSS and MSP.

D. Implementation of the Proposed Method

The implementation of the proposed DPWM method with DCSS and MSP is illustrated in the block diagram of Fig. 17.

The three-phase reference voltages $v_{x,ref}$ ($x = a$, b, and c), generated from the current controller, are classified into *max*, *mid*, and *min* phases according to their magnitudes. The sensed V_{top} and V_{bottom} signals are passed through an LPF with a sufficiently low f_c to extract their dc components $V_{\mathrm{top,LPF}}$ and $V_{\mathrm{bottom,LPF}}$. Using these values and θ_{diff} calculated from (7), $v_{neu,est}$ is obtained via (10)–(13). The polarity of $v_{neu,m}$, detected from $v_{neu,est}$, and θ_{diff} are used to compute $V_{\mathrm{offset,DCSS}}$ from (2) and (8), which is then applied to $v_{x,\mathrm{ref}}$ according to (9). The conventional reference duty ($d_{x,\mathrm{comp}}$) and the reference duty for MSP ($d_{x,\mathrm{comp,MSP}}$) are calculated using (14) and (16), respectively. The switching signals S_x and $S_{x,\mathrm{MSP}}$ are generated by comparing $d_{x,comp}$ and $d_{x,\mathrm{comp,MSP}}$ with V_{tri} using (15) and (17), respectively. Finally, the switching signals of the Vienna rectifier are determined based on the detected zone and Table III.

IV. EXPERIMENTAL RESULTS

The parameters and experimental setup are presented in Table IV and Fig. 18. The power semiconductors used in the Vienna rectifier are SiC MOSFETs (GP2T020A120H, SemiQ) and SiC Schottky barrier diodes (GP3D040A120U, SemiQ). The DSP embedded in the control board is TMS320F28377D.

TABLE IV
PARAMETERS OF EXPERIMENT

Parameter	Value
DC-link voltage (V_{dc})	400 V
Grid voltage / frequency (e_x)	130 V_{rms} / 60 Hz
Load power (P_{load})	5.1 kW
Switching frequency (f_{sw})	80 kHz
Control period (T_s)	100 μs
DC-link capacitance (C_{dc})	2040 μF
Input filter inductance (L_f)	100 μH

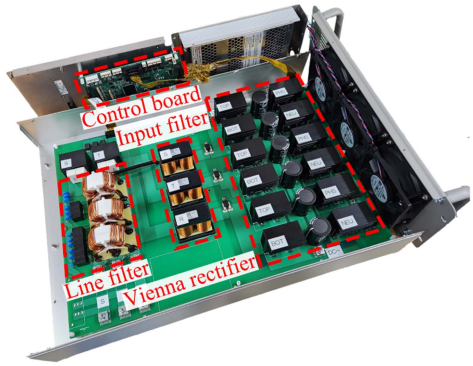

Fig. 18. Experimental setup.

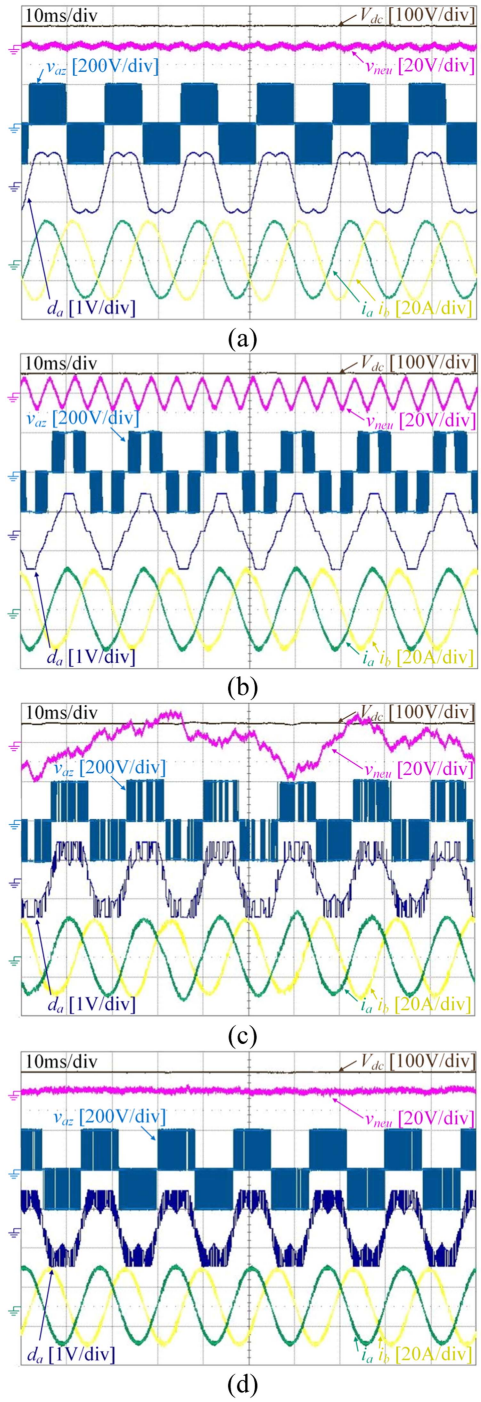

Fig. 19. v_{neu} depending on the methods. (a) SVCPWM. (b) DPWMA. (c) Proposed method with $v_{neu,sen}$. (d) Proposed method.

Fig. 19 shows the waveform of v_{neu} depending on the applied method, where d_a denotes the a-phase reference voltage (commonly referred regardless of the method). For the space vector continuous PWM (SVCPWM) method [12] in Fig. 19(a), v_{neu} contains a small third-harmonic ripple component due to the continuous switching. In contrast, as previously mentioned, the DPWMA method results in a ripple with a peak-to-peak value approaching 20 V, as shown in Fig. 19(b). Fig. 19(c) shows the case where $v_{neu,sen}$ is used for polarity detection of v_{neu} in the implementation of the proposed method. As explained in Section III-B and illustrated in Fig. 9, inaccurate polarity detection causes significantly large fluctuations, although v_{neu} is regulated around zero—worse than those observed in the conventional DPWMA. In the proposed method, the clamping state that reduces v_{neu} toward zero is selected in each switching cycle based on the accurately detected polarity of v_{neu} by $v_{neu,est}$. As shown in Fig. 19(d), v_{neu} is maintained very close to zero with minimal fluctuation, and the third-harmonic ripple component is almost eliminated. Fig. 20 presents the fast Fourier transform (FFT) results of i_a for the same methods. In Fig. 20(a), the SVCPWM method exhibits the lowest harmonic components within the switching frequency bandwidth. Fig. 20(b) shows that the DPWMA method results in the largest low-order harmonics, which is attributed to the third-harmonic ripple in v_{neu} that distorts v_{an}, as shown in Fig. 19(b), thereby causing pole voltage errors. In Fig. 20(c) and (d), the ripple components within the switching frequency bandwidth are reduced compared to those in the DPWMA method, owing to the more frequent transitions of the clamping states. Moreover, the low-order harmonics are significantly mitigated, which appears even smaller than those observed in the SVCPWM method. However, in Fig. 20(c), unlike (d), a substantial amount of low-order harmonic components—previously not observed in the SVCPWM and DPWMA methods—is observed in i_a.

Fig. 21 shows the transient response when $V_{\rm dc}$ is ramped up by stages to 350, 400, and 450 V. It can be observed from the waveform of v_{neu} that NP voltage balancing is properly

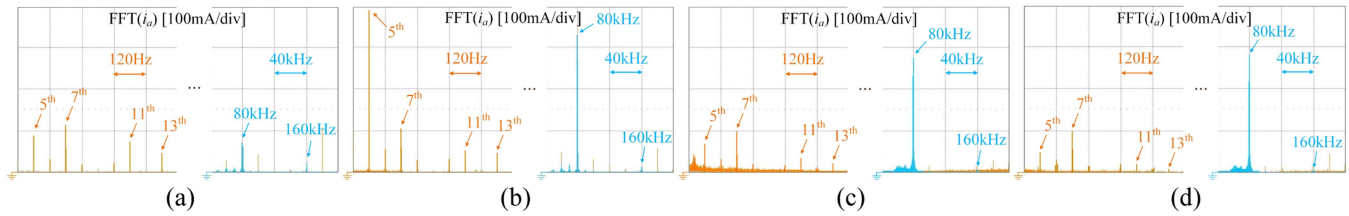

Fig. 20. Comparison of FFT(i_a). (a) SVCPWM. (b) DPWMA. (c) Proposed method with $v_{neu,sen}$. (d) Proposed method.

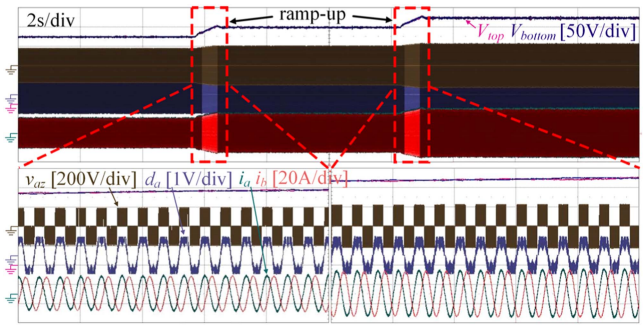

Fig. 21. $V_{\rm dc}$ ramp-up transient response of the proposed method.

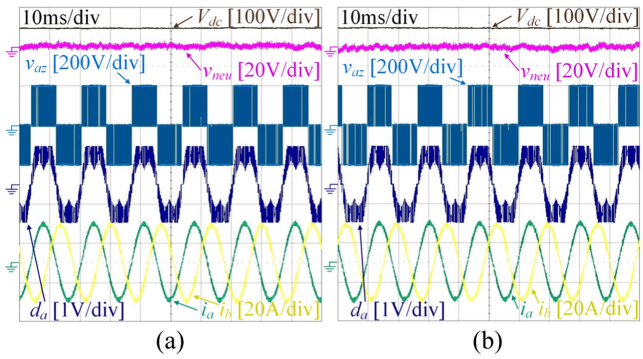

Fig. 22. NP voltage balancing performance of the proposed method under parameter mismatch in $v_{neu,est}$ calculation. (a) $C_{\rm dc}-20\%$ (2448 μF). (b) $C_{\rm dc}$ + 20% (1632 μF).

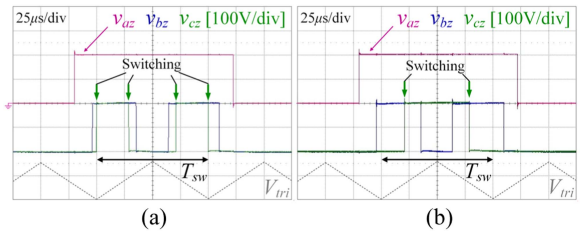

Fig. 23. Pole voltages of three phases when applying DCSS method ($f_{\rm sw}$=10 kHz). (a) Without MSP. (b) With MSP (proposed).

maintained even under transient conditions. Fig. 22(a) and (b) validates the NP voltage balancing performance of the proposed method when applying $v_{neu,est}$, which is derived intentionally using -20% and +20% deviations from the actual $C_{\rm dc}$ value,

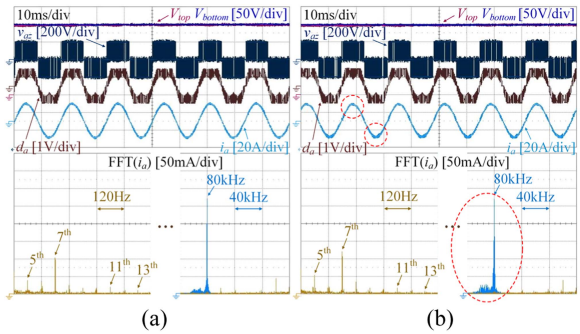

Fig. 24. Waveform of i_a and its FFT. (a) After applying additional modifications to switching patterns (proposed). (b) Before applying additional modifications, as depicted in Fig. 13.

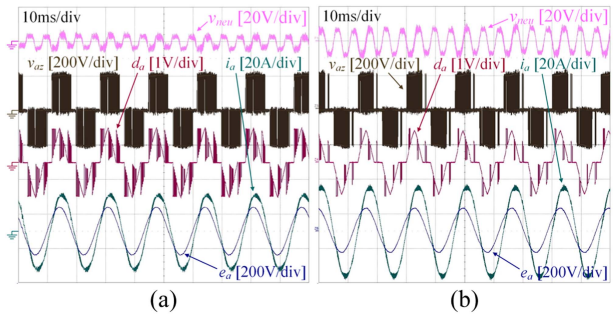

Fig. 25. Waveforms in the proposed method under nonunity power factor. (a) $pf = 0.941$, MI $= 0.6$. (b) $pf = 0.861$, MI $= 0.55$.

respectively, to reflect parameter variations under practical conditions. Despite this mismatch, the proposed method maintains excellent NP voltage balancing performance in both cases. This is because the value deviation in $C_{\rm dc}$ affects only the amplitude of $v_{neu,est,AC}$, making it slightly larger or smaller than the actual value, but it does not impact polarity detection as long as the dc component of v_{neu} is regulated to zero.

Fig. 23(a) and (b) shows the pole voltages of the three phases when the switching frequency ($f_{\rm sw}$) is 10 kHz, for the cases without and with MSP applied in the implementation of the DCSS method, respectively. In Fig. 23(a), where MSP is not applied, additional switching events in the *c*-phase (*min* phase) occur at the zero points of $V_{\rm tri}$ (arbitrarily illustrated) within a switching cycle, as observed in v_{cn}. In contrast, Fig. 23(b) demonstrates that the additional switching events are prevented by modifying the switching pattern of the *c*-phase using MSP.

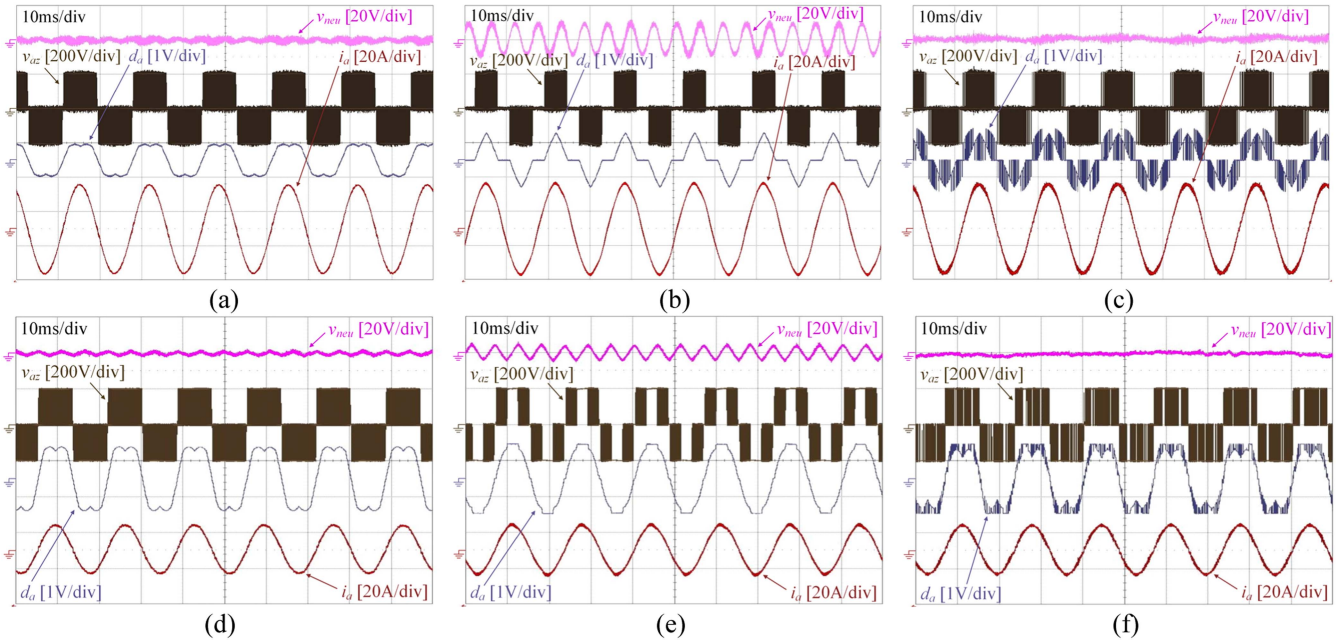

Fig. 26. Waveforms depending on applied modulation methods under different MI conditions. (a) SVCPWM, MI = 0.48. (b) DPWMA, MI = 0.48. (c) Proposed method, MI = 0.48. (d) SVCPWM, MI = 0.92. (e) DPWMA, MI = 0.92. (f) Proposed, MI = 0.92.

Fig. 24(a) shows the waveform of i_a and its FFT when the proposed MSP is applied, including the additional switching pattern modification, as depicted in Fig. 15. In contrast, Fig. 24(b) shows the corresponding results for the case without the additional modification, as illustrated in Fig. 13. As shown in Fig. 24(a), when the proposed MSP is applied, i_a exhibits symmetry between the positive and negative half-cycles. However, as shown in Fig. 24(b), when the additional modification is not applied, i_a becomes asymmetric between the positive and negative half-cycles due to the selection of applied vectors, as illustrated in Fig. 14. Furthermore, as observed in FFT(i_a), a larger number of harmonic components is generated in this case.

Fig. 25 shows the waveforms obtained when the proposed method is applied under different *pf* conditions. It can be seen that the proposed method can be properly implemented even under nonunity *pf* conditions without occurrence of ZCD, by maintaining the O-clamping state during the corresponding interval of θ_{diff}. However, as *pf* decreases, the interval in which O-clamping must be maintained is extended, thereby reducing the region available for NP voltage regulation. In addition, since O-clamping must be applied within the linear modulation range, the feasible *pf* range is limited by the MI [12]. Note that these limitations are not confined to the proposed method but are commonly applicable to all methods for the Vienna rectifier.

Fig. 26 shows the waveforms for different modulation methods under two MI conditions, 0.48 and 0.92, obtained by adjusting the magnitude of E_{mag} under the same conditions as in Table IV. Similar to the trends observed in Fig. 19, the third-harmonic ripple in v_{neu} is most significantly reduced in the proposed method for both MI conditions. In the proposed method, the ripple components within the switching frequency bandwidth are more pronounced in i_a compared to SVCPWM,

TABLE V
MAGNITUDE OF NP VOLTAGE FLUCTUATION FOR DIFFERENT MI DEPENDING ON MODULATION METHODS

MI	0.48	0.6	0.8	0.92
SVCPWM	4.6 V	4.4 V	5.04 V	3.61 V
DPWMA	19.23 V	24.09 V	16.57 V	10.02 V
Proposed	4.92 V	5.04 V	4.31 V	3.44 V

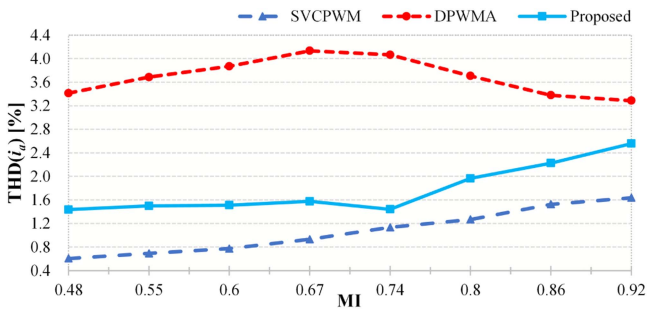

Fig. 27. Comparison of THD(i_a) for different MI values.

whereas the low-order harmonic components are lower than those observed in both SVCPWM and DPWMA. The differences among these modulation methods can be observed in the table and graph that present the magnitude of v_{neu} fluctuation and the THD of *a*-phase current according to MI, as given in Table V and Fig. 27, respectively. In the DPWMA method, the low-order harmonic components have a dominant effect, resulting in the highest THD(i_a) across all MI conditions. The THD(i_a) reaches its peak value of 4.133% at MI = 0.67, and then gradually decreases as MI increases due to the reduction in

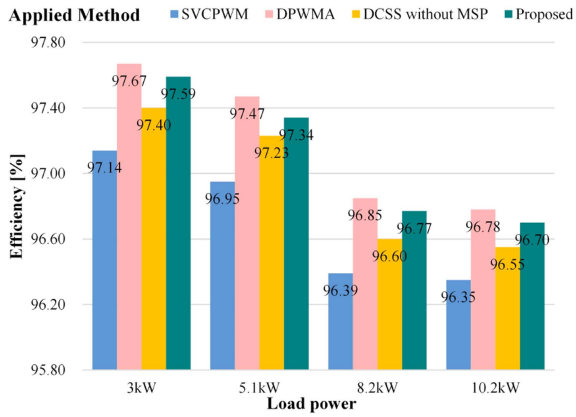

Fig. 28. Comparison of efficiency for different load powers.

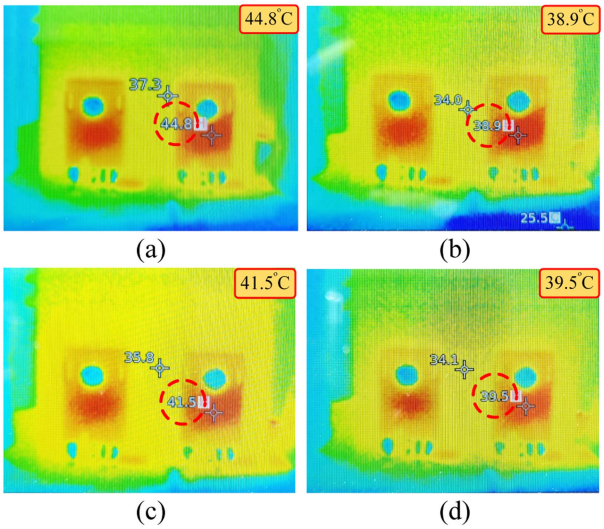

Fig. 29. Measured device temperature of SiC MOSFETs in a-phase at $P_{\mathrm{load}} = 10.2$ kW. (a) SVCPWM. (b) DPWMA. (c) DCSS without MSP. (d) Proposed method.

the magnitude of v_{neu}. In contrast, for both the SVCPWM and proposed methods, the harmonics in the switching frequency bandwidth have a dominant influence on the THD(i_a). As a result, the THD(i_a) increases with increasing MI.

Fig. 28 presents a comparison of efficiencies among different modulation methods as a function of the load power (P_{load}). All methods exhibit higher efficiency at lower P_{load} levels. The DPWMA method achieves the highest efficiency throughout all load conditions, as it performs clamping over the entire fundamental period and clamps the phase near its peak current. In contrast, the SVCPWM method shows the lowest efficiency due to continuous switching across the entire fundamental period. The DCSS method without MSP performs better than the SVCPWM method but suffers from noticeable efficiency degradation compared to the DPWMA method, owing to additional switching losses. On the other hand, the proposed method with MSP significantly improves efficiency by effectively preventing such additional losses. However, compared to the DPWMA method, the proposed method inevitably incurs higher switching losses due to the fact that clamping is selected for NP voltage balancing, which does not always guarantee clamping at the peak current of each phase. This trend is also confirmed by the measured temperatures of the SiC MOSFETs, as shown in Fig. 29. The temperature measurements were conducted under identical conditions ($P_{\mathrm{load}} = 10.2$ kW) and the same operating duration. Consistent with the efficiency comparison in Fig. 28, SVCPWM results in the highest temperature of 44.8 °C, while DPWMA yields the lowest temperature of 38.9 °C. The temperatures for the DCSS without MSP and the proposed method are measured as 41.5 °C and 39.5 °C, respectively, indicating that the proposed method achieves the second-lowest device temperature. Consequently, as previously analyzed, the proposed method achieves NP voltage balancing and substantially reduces the phase current THD compared to the DPWMA method, while maintaining efficiency within only a 0.1% difference from it.

V. Conclusion

In this article, the CB-DPWM method with DCSS to mitigate the NP voltage fluctuation was proposed. The proposed method selects a clamping state that can reduce the magnitude of NP voltage ripple and applies it in each switching cycle based on the polarity of the NP voltage monitored in real time. To address the inaccuracies in the sensed NP voltage signal in practical implementation, the proposed method employs an estimated NP voltage for monitoring, thereby preventing performance degradation in NP voltage balancing. In addition, to avoid additional switching losses caused by the DCSS operation, the MSP is introduced. As a result, the proposed method maintains NP voltage balancing while achieving efficiency comparable to that of the conventional DPWMA method. Furthermore, the phase current THD can be reduced to 0.35–0.78× that of the DPWMA method, depending on MI. The effectiveness of the proposed method was verified through experimental results.

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