AC-Side Stability Analysis of On-Board Bidirectional AC–DC Converters in G2V/V2L Modes

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***Abstract*—This article investigates the alternating current (ac) side stability characteristics of a bidirectional ac direct current (ac–dc) converter with an *LC* filter under six different operating conditions, including forward operation (stiff, medium-strength, and weak grids) and reverse operation (resistive, inductive, and capacitive loads). For each operating condition, the instability boundaries of two voltage–current dual-loop control schemes are analyzed: one without voltage feedforward (VF) and the other with VF. The results indicate that under medium-strength grid conditions, both methods tend to lose stability, while under inductive load conditions, the method without VF is more prone to instability. To address these issues, an improved VF control strategy is proposed, which effectively enhances the stability performance of the converter across all operating conditions. Finally, the validity of the theoretical analysis is confirmed through experimental results obtained from a 3 kW bidirectional ac–dc prototype.**

***Index Terms*—Bidirectional alternating current direct current (ac–dc) converter, grid-to-vehicle (G2V), *LC* filter, stability analysis, vehicle-to-load (V2L).**

I. Introduction

With the development of commercial vehicles, electronic devices have gradually become the core of vehicle configurations. The increasing vehicle electrification has led to a continuous rise in the total power consumption of on-board electrical equipment [1]. In small passenger cars, direct current (dc) powered devices such as lighting and lamps are required, whereas in large commercial vehicles, in addition to dc devices, alternating current (ac) powered equipment such as air conditioners and microwaves is also necessary [2]. The integration of a large number of ac and dc devices has exceeded the power supply capacity of the vehicle chassis power system. To enhance the reliability of the electrical supply, energy storage batteries have been introduced, resulting in a more stable on-board electrical system [3].

The typical power supply architecture of commercial vehicles is shown in Fig. 1. A bidirectional ac–dc converter is a key component for connecting the ac grid, ac loads, and energy storage batteries [4]. It primarily operates in two modes: the first is the grid-to-vehicle (G2V) mode, in which the grid charges the energy storage battery through the bidirectional ac–dc converter; the second is the vehicle-to-load (V2L) mode, in which the battery supplies power to the ac load via the same converter. Additionally, there is the vehicle-to-grid (V2G) mode, in which the vehicle provides energy to the grid through the bidirectional ac–dc converter. However, in commercial vehicles, the practical value of the V2G mode is limited due to the typically low voltage (12–48 V) and relatively low capacity of the energy storage batteries [5].

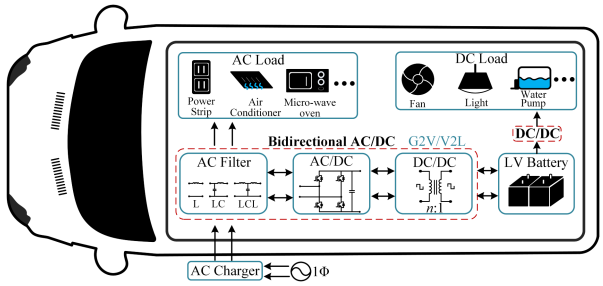

Fig. 1. Commercial vehicle power supply architecture.

In Fig. 1, the bidirectional ac–dc converter primarily adopts a two-stage topology, consisting of a front-end ac–dc converter and a back-end dc–dc converter. The front-end ac–dc converter operates in the G2V mode as a power factor correction (PFC) circuit and in the V2L mode as an inverter (INV). To mitigate high-frequency harmonics on the ac-side, employing a filter is an effective solution, with common types including inductor (*L*), inductor-capacitor (*LC*), and inductor-capacitor-inductor (*LCL*) filters [6]. The *L* filter, characterized by its simple structure, is widely employed in PFC mode [7], [8]. However, when dual-mode PFC/INV operation is required, a higher inductance is necessary for the *L* filter to enhance the sinusoidal waveform quality in INV mode. This results in challenges regarding size and cost. To resolve the issues associated with the *L* filter, it can be modified into either an *LC* or *LCL* filter. The choice of filter significantly influences the selection of front-end control strategies, which can be broadly classified into two categories: linear control methods, such as proportional-integral (PI) and proportional-resonant (PR) controllers [9], [10], [11], [12], [13], [14], and nonlinear control methods, including model predictive current control (MPCC) [15] and deadbeat predictive current

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control (DPCC) [16], [17]. From the perspective of cost-effective implementation, combining an *LC* filter with either linear control or DPCC provides a good balance between performance and simplicity. In contrast, the *LCL* filter introduces high-order resonance peaks, necessitating active damping in linear control schemes or the use of MPCC with high-performance controllers to address modeling complexity and reduce prediction errors. Therefore, for dual-mode PFC/INV applications, the *LC* filter remains the preferred choice.

With the increasing popularity of commercial vehicles, their operating conditions have become more complex. In PFC mode, the grid may be stiff, medium-strength, or weak, whereas in INV mode, the load may be resistive, inductive, or capacitive. Additionally, the electromagnetic compatibility (EMC) circuit significantly affects the configuration of the ac-side filter, thereby altering the *LC* filter structure and further impacting controller stability. These structural variations also compromise the prediction accuracy of DPCC when applied with *LC* filter. Consequently, recent research has primarily focused on *LC* filter combined with linear control strategies. Li et al. [18] investigated the effect of the EMC circuit on ac-side current harmonics in PFC mode without considering the grid inductor L_g, while Wang et al. [19] considered L_g but neglects the EMC circuit, resulting in a single-inductor structure. Both L_g and the EMC circuit are taken into account in [20] and [21], which focus on low-frequency instability induced by negative resistance but lack high-frequency analysis. Notably, these studies are confined to PFC mode. In contrast, Geng et al. [22] and Fernández-Abraldes et al. [23] addressed INV-mode stability under resistive loads only, and [9], [10], [11], [12], [13], [14] emphasize functional design in dual-mode PFC/INV systems without systematic stability analysis. Furthermore, all the aforementioned studies adopt PI or PR controllers, with some introducing voltage feedforward (VF) as an additional enhancement. In PFC mode, VF mainly suppress ac-side harmonics [18] and enhance dynamic response [20], whereas in INV mode, it serves as active damping to suppress *LC* resonance peaks [22], [23]. A comprehensive discussion of VF is available in grid-connected systems with *LCL* filters. Chen et al. [24] pointed out that VF includes two approaches, namely capacitor-voltage feedforward [25], [26], [27], [28] and PCC-voltage feedforward [29], [30]. Since PCC voltage is difficult to measure in practice, capacitor-voltage feedforward is commonly adopted. Lu et al. [25] showed that, after applying VF, the *LCL* filter achieves a stable operating range for resonance frequencies within (0-f_s/3). Liu et al. [26] indicated that delay is an important factor affecting VF stability, and it mitigates this issue by configuring the switching frequency and *LCL* filter parameters to reduce the delay. Faiz et al. [27] employed several pole-zero cancellation methods to suppress *LCL* oscillations. However, the methods in [25], [26], and [27] remain dependent on filter parameters, making them difficult to apply to an *LC* filter. In contrast, Li et al. [28] proposed a strategy that fully compensates for VF-induced sampling delays by modifying the sampling and loading approach, which is independent of the filter parameters, however, this approach demands a more expensive controller. in addition, whether the conclusions for grid-connected *LCL* systems extend to dual-mode PFC/INV operation remains unclear.

In conclusion, from the current research status of PFC/INV stability, most studies on PFC mode focus on ideal conditions; some consider weak grid with *L* filter, but few address the effects of wide variations in L_g. Studies on INV mode mainly address resistive loads, other types of loads are not discussed. Meanwhile, there is little research exploring the connection and differences between the stability characteristics of the two modes. This leaves a significant gap in the understanding of the stability of the bidirectional mode. To address this issue, this article investigates two mainstream PFC/INV control strategies reported in the literature: voltage-current dual-loop control schemes, with and without VF. Based on these methods, the stability boundaries across various grid and load conditions are analyzed in detail.

Table I summarizes the current PFC/INV control schemes. This article classifies the ac-side stability analysis of bidirectional ac–dc converters into two categories. The first involves issues determined by circuit factors, including filter type and EMC circuit configuration. The second addresses issues resulting from external operating conditions, namely grid impedance characteristics and ac load types.

The contributions of this work can be summarized as follows.

1) The stability variations of the dual-mode PFC/INV system under six operating conditions are comprehensively discussed. It is revealed that under medium-strength grid and inductive load conditions, the controller tends to encounter instability.
2) From a common perspective, the instability of both *LC*-based methods is due to the uncontrollable ac-side inductance. From a differentiating perspective, instability without VF results from a second crossing of $-180°$ at the resonance peak, whereas instability with VF is caused by excessively large virtual positive resistance or negative resistance.
3) An improved voltage feedforward (IVF) control strategy is proposed, which achieves a limited positive resistance across the entire frequency range, thereby enhancing stability and enabling implementation on low-cost controllers.

The rest of this article is organized as follows. In Section II, the stability analysis of the ideal operating conditions in the bidirectional mode is discussed. In Section III, the stability analysis of the nonideal operating conditions in the bidirectional mode is presented. In Section IV, the improved voltage feedforward control strategy is proposed. In Section V, the theoretical analysis is validated through experimental results. Finally, Section VI concludes this article.

II. Stability Analysis of the Ideal Operating Conditions in Bidirectional Mode

This section focuses on the PFC mode under an ideal grid and the INV mode with a resistive load, discussing their stability variation characteristics to lay the theoretical foundation for the subsequent sections.

TABLE I
SUMMARY AND COMPARISON OF PFC/INV CONTROL STRATEGIES

PFC control scheme	INV control scheme	Ref	Operating modes	Filter	Consider EMC Circuit	Grid adaptability discussion	Load adaptability discussion
PI+PI	---	[19]	---	*L*	No	Stiff, Weak	---
PI+PR+VF	---	[20],[21]	---	*L*	Yes	Stiff, Weak	---
PI+PR+VF	---	[9]	V2G, G2V	*L*	Yes	Stiff	---
PI+PR	PI+PR	[10]	V2G, G2V, V2L	*LCL*	Yes	Stiff	Resisitive
PI+PI	---	[11],[12]	V2G, G2V	*L*	Yes	Stiff	---
PI+PI	---	[13]	V2G, G2V	*LCL*	No	Stiff	----
PI+PI	PI+PI	[14]	V2G, G2V, V2L	*LCL*	No	Stiff	Resisitive
---	PR+VF	[23]	V2L	*LC*	No	---	Resisitive
The proposed: PI (PR)+ PI + VF		---	G2V、V2L	*LC*	Yes	Stiff, Medium-strength, Weak	Resisitive, Inductive, Capacitive

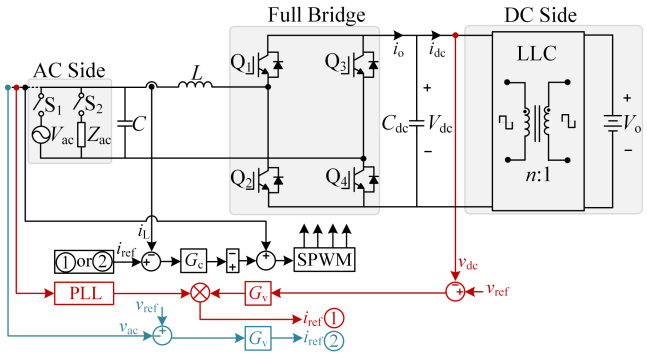

Fig. 2. Topology and control scheme of bidirectional AC–DC converter.

TABLE II
CIRCUIT PARAMETERS OF PFC/INV CONVERTER

Symbol	Description	Value
L	Inductor	1 mH
C	AC filter capacitor	6.8 μF
C_{dc}	DC filter capacitor	2040 μF
R_{ac}	Equivalent ac resistive load	$220^2/P_o$
R_{dc}	Equivalent dc resistive load	$400^2/P_o$
V_{ac}	AC voltage	220 V
V_{dc}	DC Voltage	400 V
ω_{ac}	AC angular frequency	314 rad/s
f_{ac}	AC frequency	50 Hz
f_s	Switching frequency	20 kHz
P_o	Output active power	3 kW

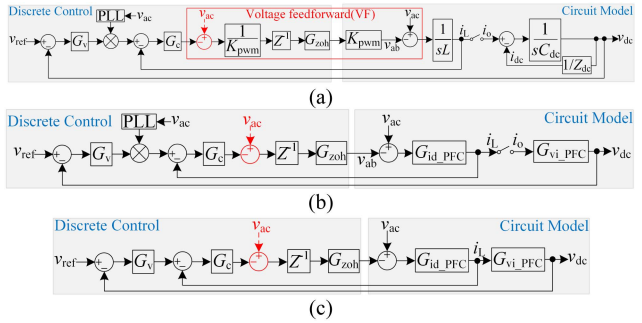

Fig. 3. PFC mode equivalent block diagram. (a) Without simplification. (b) With simplification. (c) Simplification based on three assumptions.

A. System Description

The topology and control scheme of the bidirectional ac–dc converter are depicted in Fig. 2. The converter consists of the ac-side, the ac filter inductor L and capacitor C, switches Q_1–Q_4, dc-side filter C_{dc}, and the bidirectional *LLC* converter [12]. The ESR parameters of L, C, and C_{dc} are neglected to consider the worst-case scenario under undamped conditions [24].

The operating mode of the ac-side is determined by the configuration of switches S1 and S2 in conjunction with the *LLC* converter. ① When S_1 is closed, S_2 is open, and the *LLC* converter operates in charging state, the full-bridge converter operates in PFC mode; ② When S_1 is open, S_2 is closed, and the *LLC* converter operates in discharging state, the converter operates in INV mode.

For the purpose of analysis, the following definitions are made: the ac-side voltage is v_{ac}; the dc-side voltage is v_{dc}; the inductor current is i_L; the currents before and after the C_{dc} are i_o and i_{dc}; PLL is the phase-locked loop; G_c is the current loop controller; G_v is the voltage loop controller. The circuit parameters of the converter are defined in Table II.

B. Equivalent Block Diagram of Bidirectional Mode

Based on Fig. 2, the equivalent block diagrams for the bidirectional mode are derived, as shown in Figs. 3 and 4. In these diagrams, Z^{-1} represents the computational delay, G_{zoh} denotes the zero-order hold, and K_{pwm} corresponds to the converter gain, which equals $1/V_{dc}$. In addition, the red dashed lines in the block diagrams indicate whether VF is implemented.

The equivalent block diagram of the PFC mode is shown in Fig. 3(a), and its equivalent transformation is illustrated in Fig. 3(b). In Fig. 3(c), based on Fig. 3(b), three assumptions are made to simplify the analysis of the voltage control loop: ① the 100 Hz ripple in v_{dc} is neglected; ② the PLL is set to its peak value of 1; ③ the inductor current i_L is approximated as equal to the output current i_o.

Fig. 4(a) illustrates the equivalent block diagram of the INV mode, while Fig. 4(b) shows its transformed equivalent representation.

The open-loop transfer functions of the current and voltage control loops for the two modes, as illustrated in Figs. 3(c) and

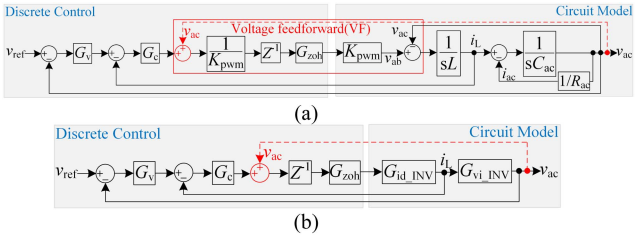

Fig. 4. INV mode equivalent block diagram. (a) Without simplification. (b) With simplification.

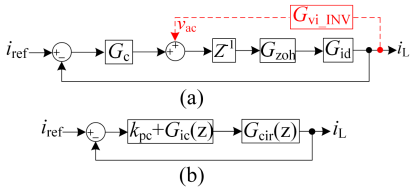

Fig. 5. Unified control block diagram of the current loop. (a) Without simplification. (b) With simplification.

4(b), are given as follows:

$$G_{\text{id\_PFC}} = \frac{1}{sL} \tag{1}$$

$$G_{\text{id\_INV}} = \frac{1 + sR_{\text{ac}}C}{s^2R_{\text{ac}}LC + sL + R_{\text{ac}}} \tag{2}$$

$$G_{\text{vi\_PFC}} = \frac{R_{\text{dc}}}{sR_{\text{dc}}C_{\text{dc}} + 1} \tag{3}$$

$$G_{\text{vi\_INV}} = \frac{R_{\text{ac}}}{sR_{\text{ac}}C + 1}. \tag{4}$$

In bidirectional modes, the current loop is regulated by a PI controller. The voltage loop utilizes a PI controller in the PFC mode, whereas a PR controller is adopted in the INV mode

$$G_{\text{c}} = k_{\text{pc}} + \frac{k_{\text{ic}}}{s} = k_{\text{pc}} + G_{\text{ic}}(s) \tag{5}$$

$$G_{\text{v\_PFC}} = k_{\text{pv}} + \frac{k_{\text{iv}}}{s} = k_{\text{pv}} + G_{\text{iv}}(s) \tag{6}$$

$$G_{\text{v\_INV}} = k_{\text{pv}} + \frac{2k_{\text{iv}}\omega_c s}{s^2 + 2\omega_c s + {\omega_0}^2} = k_{\text{pv}} + G_{\text{iv}}(s). \tag{7}$$

C. Dual-Loop Stability Analysis Method

To facilitate the unified analysis of block diagrams for the two modes in the following sections, G_{id} in (1) and (2) is distinguished by the subscripts PFC and INV. During the block diagram simplification, they are uniformly denoted as G_{id} to represent both modes, as shown in Fig. 5(a).

As shown in Figs. 3(c) and 4(b), VF in bidirectional modes effectively cancels the disturbance caused by the circuit input voltage v_{ac}. However, in the PFC mode, since VF is treated as an external input, it has no impact on the stability of the current loop. In contrast, in the INV mode, i_{L} is directly influenced by v_{ac} through the relationship established by VF, which in turn affects the stability of the current loop.

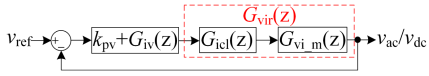

Fig. 6. Unified control block diagram of the voltage loop.

To analyze the combined effect of the current loop and VF the equivalent block diagram of the current loop is extracted and unified, as illustrated in Fig. 5(a). Its corresponding simplified representation is depicted in Fig. 5(b). The unified control block diagram of the voltage loop is presented in Fig. 6.

The closed-loop transfer functions corresponding to Figs. 5(b) and 6 are given as follows:

$$G_{\text{icl}}(\text{z}) = \frac{(k_{\text{pc}} + G_{\text{ic}}(z))G_{\text{cir}}(z)}{1 + (k_{\text{pc}} + G_{\text{ic}}(z))G_{\text{cir}}(z)} \tag{8}$$

$$G_{\text{vcl}}(\text{z}) = \frac{(k_{\text{pv}} + G_{\text{iv}}(z))G_{\text{vir}}(z)}{1 + (k_{\text{pv}} + G_{\text{iv}}(z))G_{\text{vir}}(z)} \tag{9}$$

where $G_{\text{cir}}(\text{z})$ and $G_{\text{vir}}(\text{z})$ in the two modes are defined as follows:

$$G_{\text{cir\_PFC}}(\text{z}) = z^{-1}Z_{\text{ZOH}}(G_{\text{id\_PFC}}) \tag{10}$$

$$G_{\text{cir\_INV}}(\text{z}) = \frac{z^{-1}Z_{\text{ZOH}}(G_{\text{id\_INV}})}{1 - z^{-1}Z_{\text{ZOH}}(G_{\text{id}}G_{\text{vi\_INV}})} \tag{11}$$

$$G_{\text{vir}}(\text{z}) = G_{\text{icl}}(\text{z})G_{\text{vi}}(z). \tag{12}$$

When the denominators of (8) and (9) are equal to zero, the transfer functions for k_{pc} and k_{pv} are derived as follows:

$$1 + k_{\text{pc}}\frac{G_{\text{cir}}(z)}{1 + G_{\text{ic}}(z)G_{\text{cir}}(z)} = 0 \tag{13}$$

$$1 + k_{\text{pv}}\frac{G_{\text{vir}}(z)}{1 + G_{\text{iv}}(z)G_{\text{vir}}(z)} = 0. \tag{14}$$

D. Stability Analysis of Current Loop

Based on (13), the root locus curves of the current loop in bidirectional mode are plotted, as shown in Fig. 7(a)–(c). It can be observed that the stability boundary of the PFC mode remains consistent across the full load range and is independent of VF. In the INV mode, the stability boundary under full load is higher than that under no load, as the increased load attenuates the *LC* resonance peak. The inclusion of VF further enhances the stability boundary. Fig. 7(d) demonstrates that k_{pc} exhibits integral coefficient k_{ic} independence within a certain range.

E. Stability Analysis of Voltage Loop

Based on (14), the root locus curves of the voltage loop in bidirectional mode are plotted, as shown in Fig. 8(a)–(c). The voltage loop k_{pv} in bidirectional mode decreases as the current loop k_{pc} increases, indicating that an increase in k_{pc} leads to a reduction in the crossover frequency of the voltage loop, thereby affecting the dynamic response.

Moreover, under the same k_{pc} value, the k_{pv} in PFC mode is significantly larger than that in INV mode. This is because C_{dc} is much greater than C, causing the pole in $G_{\text{vi\_PFC}}$ to be located

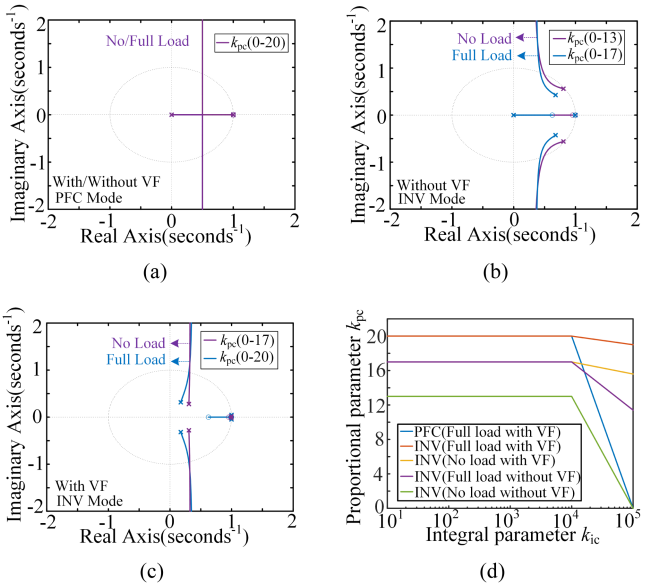

Fig. 7. Stability boundaries of the current loop in bidirectional mode. (a) PFC mode. (b) INV mode without VF. (c) INV mode with VF. (d) Impact of k_{ic}.

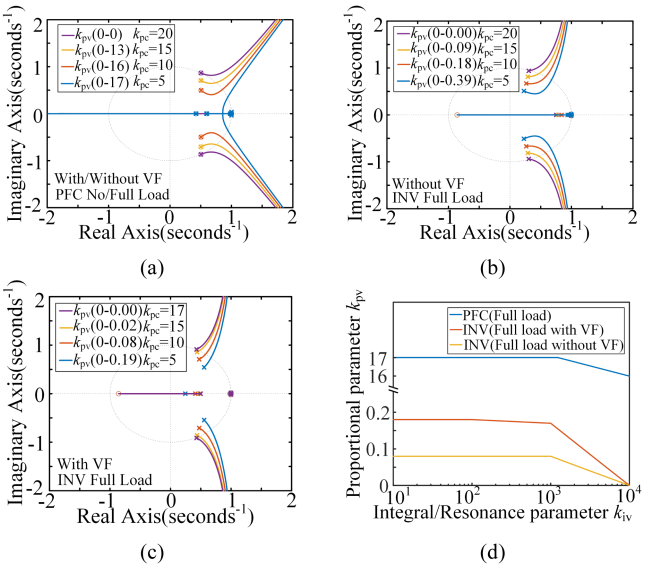

Fig. 8. Stability boundaries of the voltage loop in bidirectional mode. (a) PFC mode. (b) INV mode without VF. (c) INV mode with VF. (d) Impact of k_{iv}.

farther from the unit circle boundary. However, in practice, the k_{pv} in PFC mode cannot reach the values shown in Fig. 8(a), and the specific reason is discussed in Section III–D. Fig. 8(d) demonstrates that k_{pv} exhibits independence from the integral coefficient k_{iv} within a certain range.

F. Summary

Under PFC mode with an ideal grid and INV mode with a resistive load, both modes exhibit stable stability boundaries, regardless of whether VF is considered. This explains why both control methods are commonly adopted in the related literature [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23].

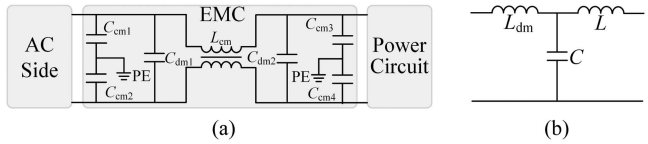

Fig. 9. Consider EMC circuits. (a) Topology. (b) Equivalent model.

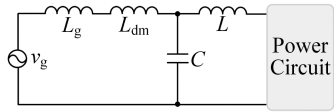

Fig. 10. Equivalent circuit of a nonideal grid.

III. Stability Analysis of the Nonideal Operating Conditions in Bidirectional Mode

Due to complexity of the actual conditions on the ac-side, even if the controller parameters fall within the range specified in Section II, high-frequency oscillations in the inductor current may still occur. This section discusses the causes of this phenomenon.

A. Nonideal Operating Conditions

1) EMC Circuit: The EMC circuit is located between the ac-side and the power circuit, as shown in Fig. 9(a). The EMC circuit typically consists of common-mode inductors L_{cm}, common-mode capacitors C_{cm}, and differential-mode capacitors C_{dm}. Due to the existence of the differential-mode component L_{dm} within the common-mode inductor, L_{dm}, C_{dm}, and L collectively form an *LCL* resonant circuit.

L_{dm} can be tested using an *LCR* digital bridge, with the following range:

$$L_{dm} \approx 10\text{–}30\ \mu\text{H}. \tag{15}$$

2) Nonideal Grid: When operating in PFC mode, the nonideal grid introduces an equivalent inductor L_g on the ac-side, as shown in Fig. 10. The value of L_g is defined by the short circuit ratio (SCR), as described in [19]. The corresponding expression is given as follows:

$$L_g = \frac{{V_{ac}}^2}{P_o \omega_{ac} \text{SCR}}. \tag{16}$$

Based on (16), when the grid is classified as stiff, medium-strength, or weak grid, the different values of L_g result in varying resonant frequencies among L_g, C, and L, thereby affecting the stability of the controller.

3) Inductive and Capacitive Load: When operating in INV mode, in addition to the resistive load discussed in Section II, the loads may also be inductive or capacitive, as shown in Fig. 11. The differences between these loads and the resistive load affect the configuration of the *LC* filter. The inductive load is denoted

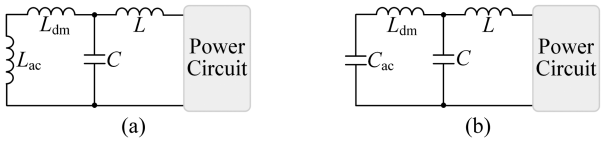

Fig. 11. Equivalent circuit of INV under different loads. (a) Inductive load. (b) Capacitive load.

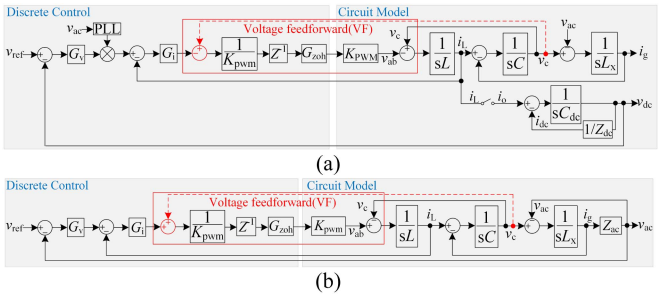

Fig. 12. Nonideal circuit and control block diagram of the bidirectional mode. (a) PFC mode. (b) INV mode.

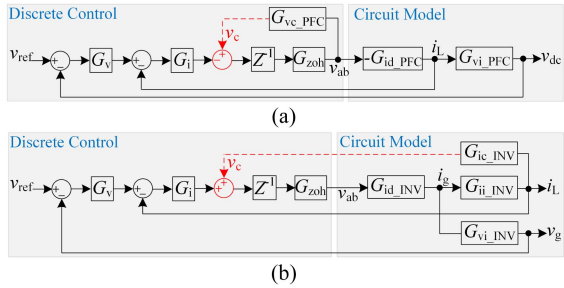

Fig. 13. Simplified nonideal block diagram (a) PFC mode. (b) INV mode.

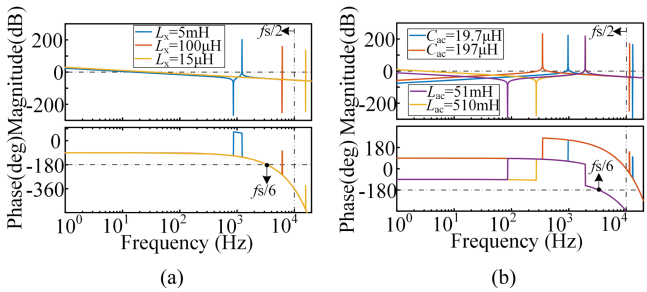

Fig. 14. Bode plot of the current loop under nonideal conditions. (a) PFC mode. (b) INV mode.

as L_{ac}, and the capacitive load as C_{ac}. Based on the parameters in Table II, the values of L_{ac} and C_{ac} from 10% load to 100% load are as follows:

$$L_{ac} = \frac{{V_{ac}}^2}{\omega_{ac} Q} = \frac{220^2}{314 \times (300 \sim 3000)} \approx 510 \sim 51 \text{ mH} \quad (17)$$

$$C_{ac} = \frac{Q}{\omega_{ac} {V_{ac}}^2} = \frac{(300 \sim 3000)}{314 \times 220^2} \approx 19.7 \sim 197\ \mu\text{F}. \quad (18)$$

B. Nonideal Bidirectional Mode Equivalent Block Diagram

In PFC mode, L_x is defined as the sum of L_g and L_{dm}; in INV mode, Z_{ac} represents either a resistive R_{ac}, an inductive load L_{ac}, or a capacitive load C_{ac}. The nonideal block diagram for the bidirectional mode is shown in Fig. 12. The key difference from the ideal equivalent block diagram in Section II–B is that L_x and Z_{ac} modify the transfer function of the current inner loop. Additionally, in PFC mode, VF is no longer treated as an independent voltage source but is introduced into the circuit model as a feedback quantity. As a result, VF in both modes influences the stability of the current inner loop.

The equivalent transformation of the block diagram is shown in Fig. 13, with its components represented by

$$G_{id\_PFC} = \frac{L_x C s^2 + 1}{L L_x C s^3 + (L + L_x)\, s} \quad (19)$$

$$G_{vc\_PFC} = L_x / (L L_x C s^2 + L + L_x) \quad (20)$$

$$G_{id\_INV} = 1/(L L_x C s^3 + (L C Z_{ac}) s^2 + (L + L_x)\, s + Z_{ac}) \quad (21)$$

$$G_{ic\_INV} = (s L_x + Z_{ac})/(L_x C s^2 + C Z_{ac} s + 1) \quad (22)$$

$$G_{ii\_INV} = L_x C s^2 + C Z_{ac} s + 1 \quad (23)$$

$$G_{vi\_INV} = Z_{ac}. \quad (24)$$

Based on (8), (19) and (21)–(23), the bode plots of the current loop are shown in Fig. 14. The resonance frequency of the *LCL* filter is defined as f_r, the expression is as follows:

$$f_r = \sqrt{(L + L_x)/(L + L_x + C)}. \quad (25)$$

When operating in PFC mode, compared to the ideal conditions, the current loop exhibits a resonance peak, and the position of the resonance peak changes with different values of L_x. When $L_x = 15\ \mu$H, f_r is higher than $f_s/2$. As L_x increases, when $L_x = 100\ \mu$H, f_r.is between $f_s/6$ and $f_s/2$. As L_x increases further, when $L_x = 5$ mH, f_r is lower than $f_s/6$. When operating in INV mode, due to the larger value of L_{ac} and C_{ac}, f_r. is either lower than $f_s/6$ or higher than $f_s/2$. From the resonance peak positions in bidirectional modes, it can be observed that in the range of $f_s/6$ to $f_s/2$, the resonance peak is likely to cause a second crossover, leading to instability.

C. Stability Analysis of Current Loop

Based on Fig. 5(b), the circuit transfer functions under nonideal bidirectional mode are given by (26) and (27). By setting G_{vc_PFC} or G_{ic_INV} to zero and substituting the result into (13), the root locus curves with and without VF can be obtained

$$G_{cir\_PFC}(z) = \frac{z^{-1} Z_{ZOH}(G_{id\_PFC})}{1 - z^{-1} Z_{ZOH}(G_{vc\_PFC})} \quad (26)$$

$$G_{cir\_INV}(z) = \frac{z^{-1} Z_{ZOH}(G_{id\_INV} G_{ii\_INV})}{1 - z^{-1} Z_{ZOH}(G_{id\_INV} G_{ii\_INV} G_{ic\_INV})}. \quad (27)$$

1) PFC Mode: The current loop stability boundaries, accounting for the L_{dm}, are shown in Fig. 15(a)–(b). Under both

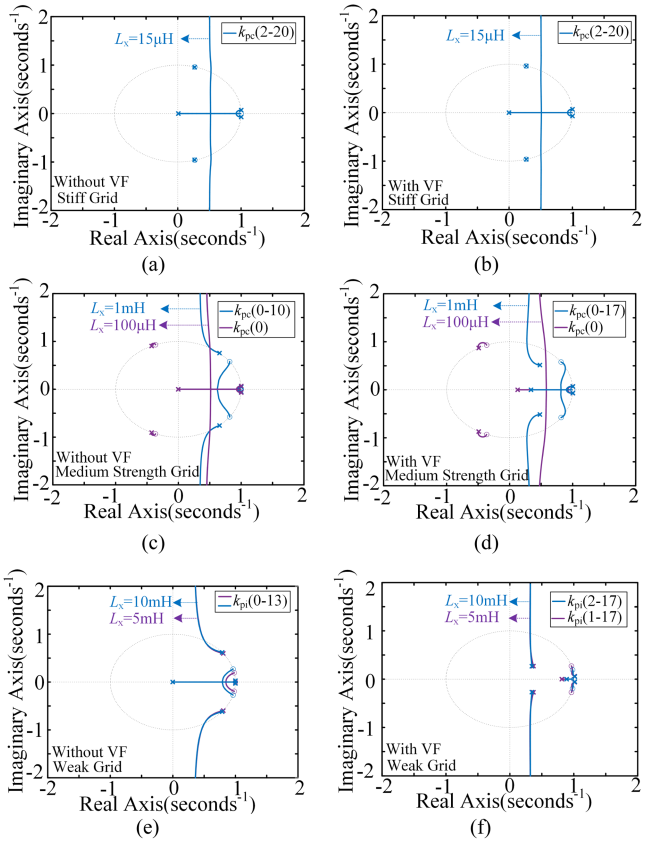

Fig. 15. Stability boundaries of the current loop in PFC mode. (a) Stiff grid without VF. (b) Stiff grid with VF. (c) Medium-strength grid without VF. (d) Medium-strength grid with VF. (e) Weak grid without VF. (f) Weak grid with VF.

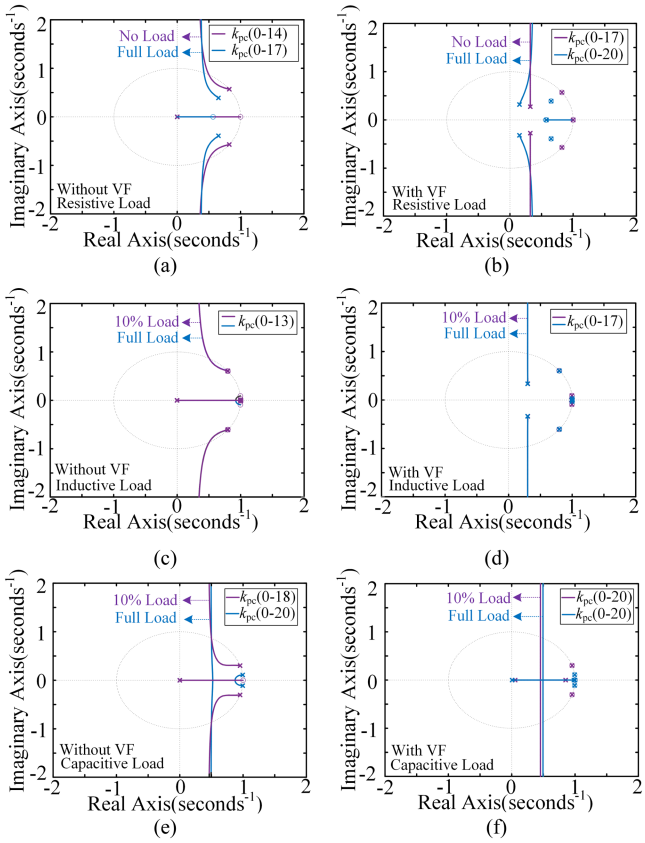

Fig. 16. Stability boundaries of the current loop in INV mode. (a) $Z_{ac} = R_{ac}$ without VF. (b) $Z_{ac} = R_{ac}$ with VF. (c) $Z_{ac} = L_{ac}$ without VF. (d) $Z_{ac} = L_{ac}$ with VF. (e) $Z_{ac} = C_{ac}$ without VF. (f) $Z_{ac} = C_{ac}$ with VF.

conditions (with and without VF), compared to the ideal case, an additional pair of conjugate poles appears near the unit circle. However, these poles remain within the unit circle and do not compromise system stability.

The current loop stability boundaries, considering the grid-side inductor L_g, are shown in Fig. 15(c)–(f). When $L_x = 100\ \mu$H, the conjugate poles lie outside the unit circle regardless of the presence of VF, resulting in current loop instability. When $L_x = 1$ mH, the system exhibits a stability boundary; however, this boundary is extremely close to the unit circle, making practical parameter selection difficult. After the introduction of VF control, the stability boundary is improved and moves further away from the unit circle. When $L_x = 5$ mH and 10 mH the system remains stable with or without VF, and the presence of VF further enlarges the stability boundary.

2) INV Mode: When operating with a resistive load, as shown in Fig. 16(a) and (b), the stability boundary aligns with the ideal case, indicating that L_{dm} does not affect system stability. For an inductive load, as shown in Fig. 16(c) and (d), the boundary without VF lies close to the unit circle, while the inclusion of VF improves stability. For a capacitive load, as shown in Fig. 16(e) and (f), a wide stability region exists regardless of whether VF is applied.

D. Stability Analysis of Voltage Loop

1) PFC Mode: When $k_{pc} = 10$, the root locus curves of the voltage loop for different values of L_x are plotted, illustrating the variation in the voltage loop stability boundary k_{pv}. It can be observed that the stability trend of the voltage loop with respect to changes in L_x is consistent with that of the current loop.

According to [20], the crossover frequency of the voltage loop in PFC mode should be set below 20 Hz, as an excessively high crossover frequency may allow the 100 Hz ripple to interfere with normal circuit operation. Taking stiff grid PFC as an example, the open-loop bode plot of the voltage loop is shown in Fig. 17. It can be seen that only by simultaneously reducing both k_{iv} can the crossover frequency be lowered to 10–20 Hz, which is significantly lower than the stability boundary values shown in Fig. 18. Therefore, under these conditions, the impact of the three simplifying assumptions made for the voltage loop in Section II can be considered negligible. To further increase k_{pv}, it is necessary to eliminate the influence of the 100 Hz ripple. This issue has been discussed in [26], and remains a valuable research topic.

2) INV Mode: As shown in Fig. 19, when $Z_{ac} = R_{ac}$, the voltage loop stability boundary without VF is close to the unit circle, whereas including VF enhances the stability boundary. Additionally, the 100% load condition exhibits a larger stability

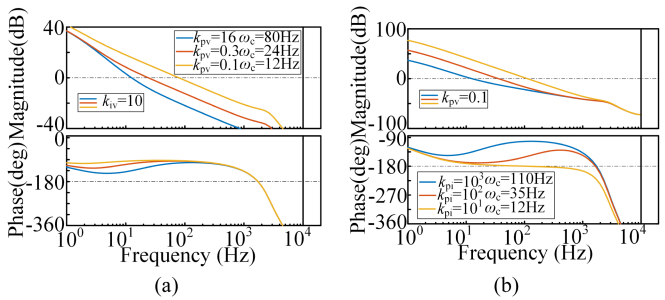

Fig. 17. Voltage open-loop bode plots in PFC mode. (a) Impact of the k_{pv}. (b) Impact of the k_{pi}.

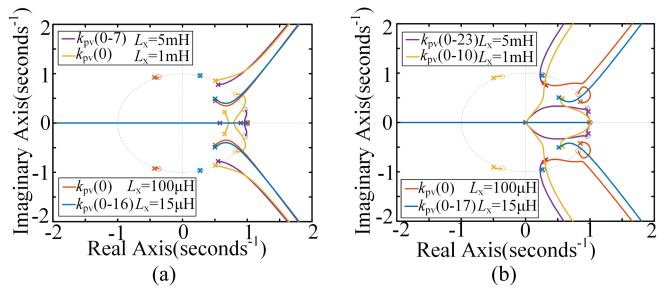

Fig. 18. Stability boundaries of the voltage loop in PFC mode. (a) Without VF. (b) With VF.

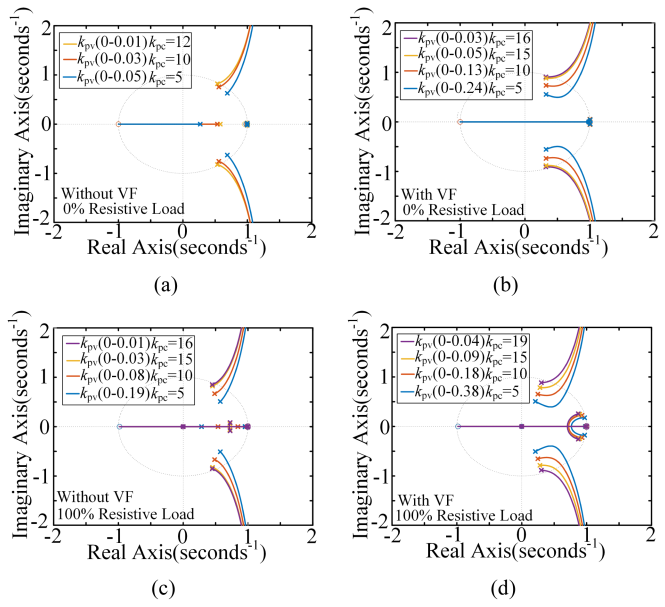

Fig. 19. Stability boundaries of the voltage loop in INV mode with resistive load. (a), (b) 0% resistive load. (c), (d) 100% resistive load.

region compared to the 0% load condition, as the 100% resistive load provides stronger damping of the resonance peak.

As shown in Fig. 20, when $Z_{\mathrm{ac}} = L_{\mathrm{ac}}$, the stability boundary from 10% to 100% load remains relatively low without VF, resembling that of the 0% resistive load case. Therefore, under inductive load conditions, the system may encounter stability

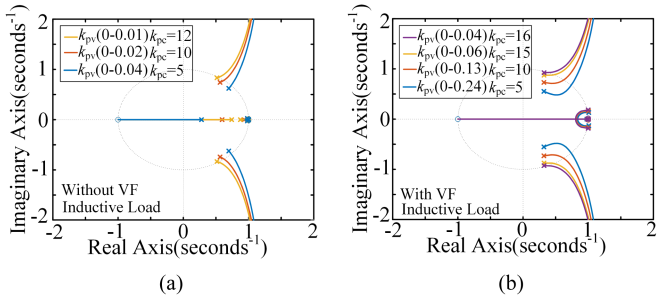

Fig. 20. Stability boundaries of the voltage loop in INV mode with inductive load. (a) Without VF. (b) With VF.

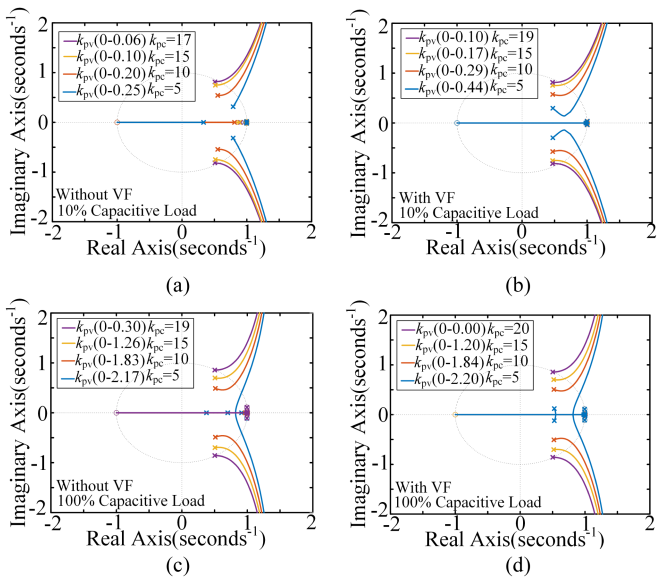

Fig. 21. Stability boundaries of the voltage loop in INV mode with capacitive load. (a), (b) 10% capacitive load. (c), (d) 100% capacitive load.

issues in the absence of VF. When VF is included, the stability boundary improves significantly.

As shown in Fig. 21, when $Z_{\mathrm{ac}} = C_{\mathrm{ac}}$, the capacitive load exhibits a wide stability boundary regardless of whether VF is applied. This is because C_{ac} lowers the resonance frequency of the *LC* filter and increases the phase margin (PM), which is consistent with the analysis in Fig. 14(b).

E. Effect of the Integral Parameters K_{ic} and K_{iv}

Sections II-C and II-D clarify that k_{ic} and k_{iv} have no impact on the stability boundary under ideal conditions. Under nonideal conditions, the influences of k_{ic} and k_{iv} are illustrated in Fig. 22. It can be observed that under several nonideal conditions, the current loop integral parameter k_{ic} and the voltage loop integral parameter k_{iv} also exhibit integral-independence within a certain range.

Based on (8), the bode plots of the closed-loop transfer function for the current loop in PFC mode are illustrated in Fig. 23. Without VF, increasing k_{ic} enhances the tracking performance

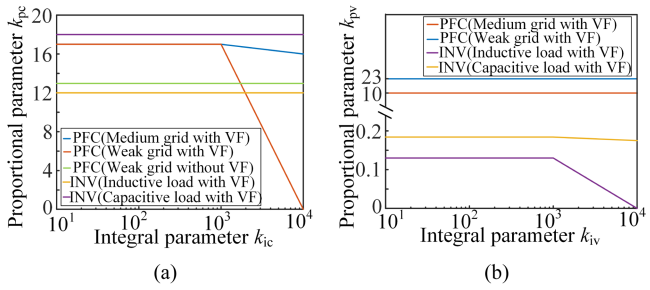

Fig. 22. (a) Impact of k_{ic}. (b) Impact of k_{iv}.

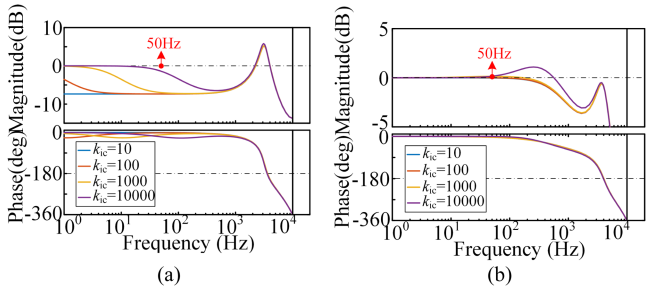

Fig. 23. Bode plots of current close-loop in PFC mode. (a) Without VF. (b) With VF.

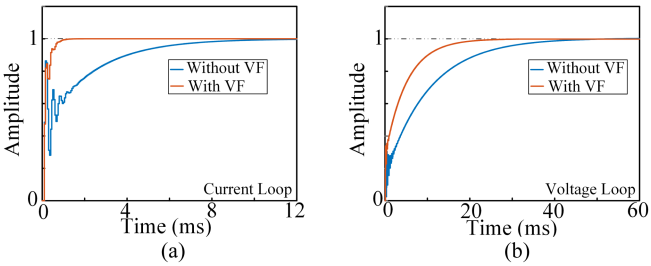

Fig. 24. Unit step response in INV mode. (a) Current loop. (b) Voltage loop.

at 50 Hz; therefore, the turning point at which the stability boundary becomes independent of k_{ic} can be used to select its optimal value. In contrast, with VF, the impact of k_{ic} on tracking performance is minimal, as VF dominates the output duty cycle. Hence, k_{ic} should be minimized to avoid excessively large values that may cause interference between the current loop and VF control.

F. Dynamic Response

Once the stability boundaries of the voltage and current loops are determined, their dynamic performance should also be evaluated. As an example, Fig. 24 shows the unit step responses of the current and voltage loops in INV mode with a 100% resistive load, derived from (8) and (9). With $k_{pc} = 10$ and $k_{pv} = 0.03$, the system incorporating VF exhibits a faster step response, indicating improved dynamic performance.

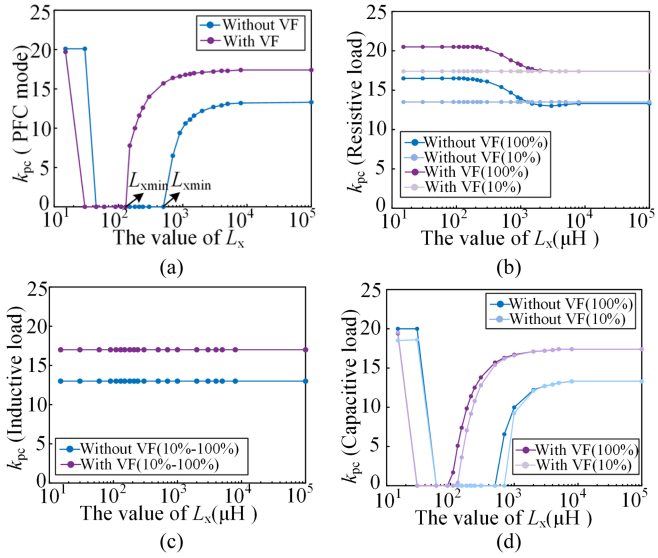

Fig. 25. Influence of L_x on the stability boundary of the PFC/INV mode. (a) PFC mode. (b) INV mode with resistive load. (c) INV mode with inductive load. (d) INV mode with capacitive load.

IV. Proposed Improved Voltage Feedforward Control Strategy

A. Controllable AC-Side Inductance

According to the analysis in Section III, L_x in PFC mode varies from 15 μH to 10 mH. Previous discussions only considered several typical values, which do not fully reflect the influence of L_x on system stability. Therefore, Fig. 25(a) shows the stability boundary as L_x varies within this range. An unstable region appears regardless of the presence of VF. Setting the minimum L_x above the instability threshold can effectively avoid instability, providing a practical hardware-based solution.

The impact of this approach in INV mode is also evaluated. Fig. 25(c) and (d) shows the current innerloop stability boundaries for three load types as L_x changes. When $Z_{ac} = R_{ac}$, the stability boundary first decreases and then stabilizes with increasing L_x. When $Z_{ac} = L_{ac}$, the boundary remains unchanged since increasing L_x is equivalent to a larger inductive load. When $Z_{ac} = C_{ac}$, the trend is similar to that in PFC mode, as the capacitive load resembles a stable voltage source.

B. Improved Voltage Feedforward Control Strategy

Although increasing the L_x can improve stability, it also raises the volume, cost, and losses. Therefore, this section proposes an improved VF method to enhance stability without additional hardware.

1) Stability Analysis of VF Control: As analyzed in Section III, even with the inclusion of VF, regions of instability still exist, and the root locus method is unable to identify the underlying causes of instability. Therefore, the first step is to discuss the reasons why VF improves the stability boundary. For ease of analysis, the discrete-domain equivalent block diagram

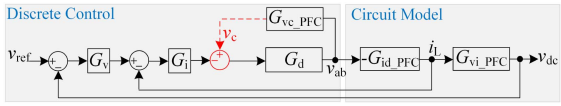

Fig. 26. PFC continuous-domain equivalent block diagram.

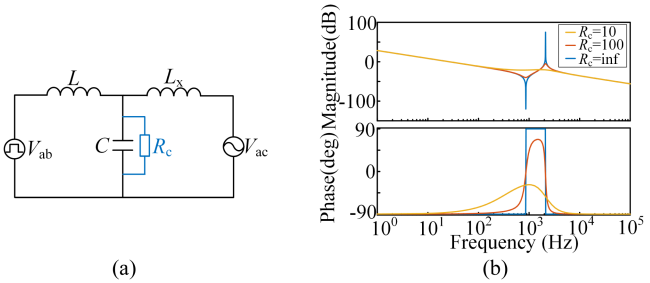

Fig. 27. (a) Circuit model of capacitor in parallel with resistor R_c. (b) Influence of R_c on the resonance peak of the *LCL* filter.

in Fig. 13(a) is modified into a continuous-domain equivalent block diagram, as shown in Fig. 26.

In Fig. 26, G_d is used to replace Z^{-1} and G_{zoh}, and its expression is given by

$$G_d = e^{-1.5sT_s}. \tag{28}$$

The current open-loop transfer function in Fig. 26 is

$$G_{cir\_PFC}(s) = \frac{L_x C s^2 + 1}{LL_x C s^3 - G_d L_x s + (L + L_x)\, s}. \tag{29}$$

When passive damping is implemented using a capacitor connected in parallel with a resistor R_c, the equivalent circuit is shown in Fig. 27(a), and its open-loop transfer function is given as follows:

$$G_{LCL} = \frac{L_x C s^2 + (L_x/R_c)s + 1}{LL_x C s^3 + LL_x s^2/R_c + (L + L_x)s}. \tag{30}$$

Based on (30), the bode plot is shown in Fig. 27(b). It can be observed that as R_c decreases, the resonance peak is attenuated and the stability margin increases.

By comparing the denominators of (29) and (30), it can be derived that

$$R_c = -sLe^{1.5sT_s}. \tag{31}$$

Let $s = j\omega$, and substitute into (31), then R_c expressed as

$$R_c(j\omega) = \omega L(\sin(1.5\omega T_s) - j\cos(1.5\omega T_s)) = R_{eq}//X_{eq}. \tag{32}$$

The real part R_{eq} and the imaginary part X_{eq} of the virtual impedance R_c can be expressed as

$$\begin{aligned} R_{eq} &= \omega L/\sin(1.5\omega T_s) \\ X_{eq} &= -j\omega L/\cos(1.5\omega T_s). \end{aligned} \tag{33}$$

Therefore, the VF control can be constructed in the form of a capacitive parallel virtual impedance, as shown in Fig. 28(a). By combining C and X_{eq}, the total imaginary part X_{eq1} can be obtained.

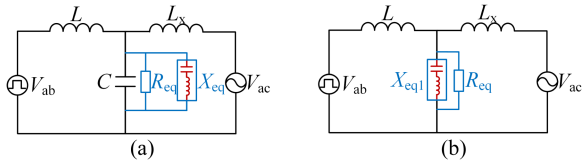

Fig. 28. Equivalent circuit of virtual impedance. (a) Virtual impedance in parallel with C. (b) Combination of the imaginary part of the virtual impedance with C.

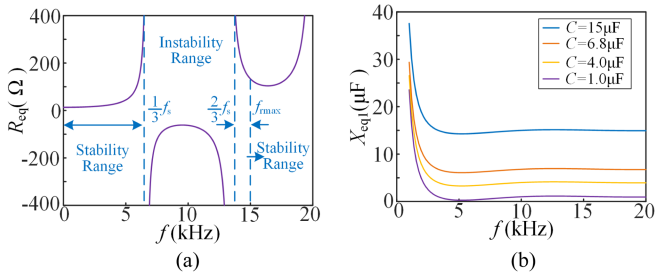

Fig. 29. Relationship between virtual impedance and frequency. (a) R_{eq}. (b) X_{eq1}.

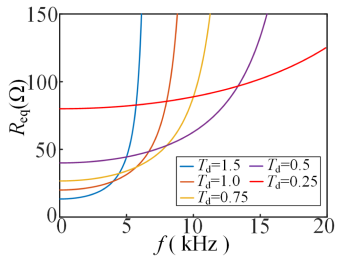

Fig. 30. Impact of control delay T_d on virtual resistance R_{eq}.

The X_{eq} in (32) can be modified as

$$X_{eq1} = C//(-j\omega L/\cos(1.5\omega T_s)). \tag{34}$$

Based on (33) and (34), the curves of R_{eq} and X_{eq1} are plotted as shown in Fig. 29. The range of the horizontal axis is determined based on (25). When $L_x = 15\ \mu$H, the f_{rmax} is approximately 15 kHz. Therefore, setting the horizontal axis range to 0–20 kHz allows for a comprehensive observation of the impact of L_x variation on the virtual impedance.

As shown in Fig. 29(a), R_{eq} exhibits positive resistance in the ranges of 0 to $f_s/3$ and $2f_s/3$ to f_{rmax} while negative resistance is observed between $f_s/3$ and $2f_s/3$. As depicted in Fig. 29(b), X_{eq1} exhibits capacitive reactance between 0 and f_{rmax}, and it can only transform into inductive reactance when C is small. Therefore, the imaginary part X_{eq1} does not affect stability. The characteristics of R_{eq} between $f_s/3$ and $2f_s/3$ are the main cause of controller instability.

2) Implementation of the IVF Method: In order to prevent R_{eq} approaching infinity at $f_s/3$ and exhibiting negative resistance between $f_s/3$ and $2f_s/3$, the influence of the delay in (33) needs to be reduced. By defining the 1.5 times delay in (33) as T_d, the variation curves of R_{eq} for different values of T_d can be plotted, as shown in Fig. 30. It can be observed that as the T_d decreases, R_{eq} exhibits finite positive resistance across a broader

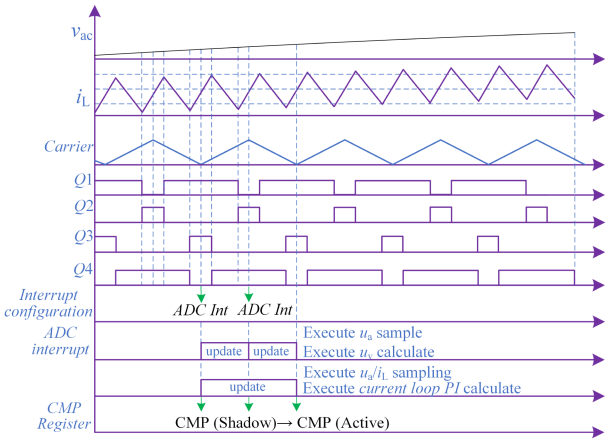

Fig. 31. Dual sampling and dual loading configuration.

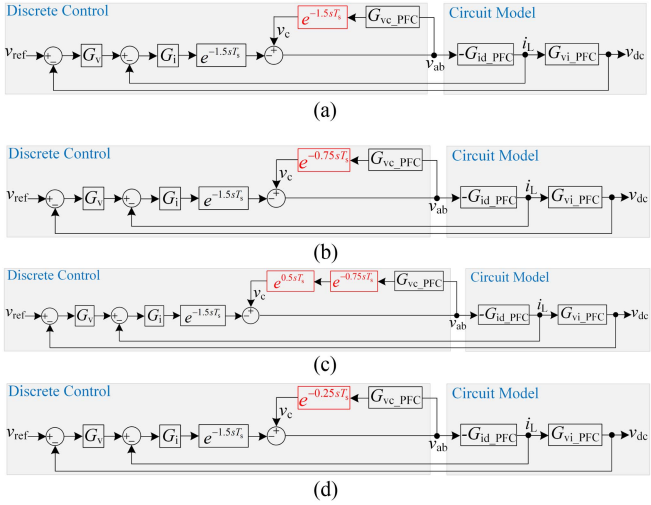

Fig. 32. Block diagram transformation process for delay reduction. (a) Feedforward delay-compensation stage before improvement. (b) Delay reduction using the method shown in Fig. 31. (c) Insertion of a lead-compensation stage. (d) Improved feedforward delay-compensation stage.

frequency range. When the T_d is reduced to below $0.5T_s$, R_{eq} shows finite positive resistance throughout the f_s range.

To achieve a sampling delay within $0.5T_s$, it is necessary to modify the sampling method. As shown in Fig. 31, the method of one sample and one load per switching cycle is modified to two samples and two loads per switching cycle. In this case, the delay of the VF is reduced from the initial 1.5 sampling periods to $0.75T_s$, as seen in the transition from Fig. 32(a) to (b). Subsequently, a lead element of $0.5T_s$ is introduced [27], as shown in Fig. 32(c), which further reduces the overall delay to $0.25T_s$, as shown in Fig. 32(d).

The lead-control part in Fig. 32(c) can be expanded using the Taylor series as follows:

$$e^{sT_s/2} = 1 + s\frac{T_s}{2} + \frac{1}{2}\left(s\frac{T_s}{2}\right)^2 + \cdots. \tag{35}$$

The first three terms are retained and discretized using the backward difference method. This equation serves as the key

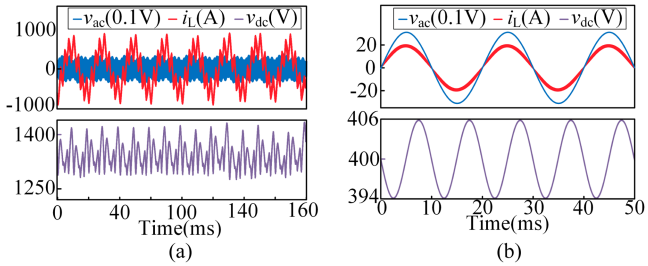

Fig. 33. Simulation verification under different delay conditions. (a) $T_d = 1.5T_s$. (b) $T_d = 0.25T_s$.

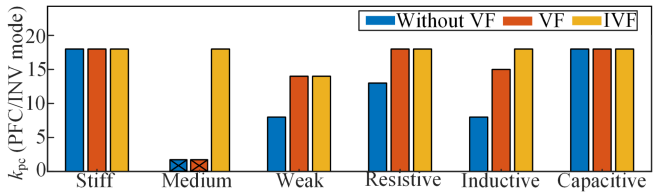

Fig. 34. Impact of *LC* tolerance on stability boundary.

equation for implementation in the DSP controller

$$e^{sT_s/2} = \left(2.5 - 2z^{-0.5} + 0.5z^{-1}\right). \tag{36}$$

3) Simulation Verification of the INF Method: After delay compensation, due to the presence of two discrete sampling times (T_s and $0.25T_s$) in the system, the discrete-domain root locus cannot be plotted. Therefore, this section employs PLECS simulations to verify the improvement in the stability of the PFC mode between $f_s/3$ and $2f_s/3$.

Fig. 33 shows the simulation waveforms for $L_x = 100\ \mu$H under conditions without and with delay compensation, respectively. It can be observed that the system remains unstable for all values of k_{pc} without compensation, whereas stability is achieved when k_{pc} is extended to $k_{pc} = 19$ with IVF, thereby confirming the accuracy of the theoretical analysis.

C. Impact of Parameters

1) LC Parameter Tolerance: This section considers the impact of a 10% parameter tolerance on the stability boundary. In an extreme case where both L and C are reduced by 10%, the variation in stability boundaries under different operating conditions is plotted, as shown in Fig. 34. Compared to the case without parameter tolerance, the proposed IVF method exhibits some degradation in stability margins. However, it still maintains a relatively wide stable region across all operating conditions.

2) Switching Frequency f_s: Under constant *LC* parameters, the influence of varying f_s on R_{eq} is illustrated in Fig. 35. As shown in Fig. 35(a), when $T_d = 1.5T_s$, various values of f_s demonstrate stable positive resistance intervals within the range of 0 to $f_s/3$. At lower switching frequencies, multiple positive and negative resistance intervals occur within the range of 0 to f_{rmax}. When $T_d = 0.25T_s$, as illustrated in Fig. 35(b), limited intervals of positive resistance are observed for f_s in the range from 10 kHz to 20 kHz. However, when f_s is further reduced,

TABLE III
STABILITY BOUNDARY OF THE PFC MODE

Mode	PFC under no/full load					
Conditions	$L_{dm}=0$	$L_{dm}=15$uH	$L_{dm}=100$uH	$L_{dm}=1$mH	$L_{dm}=5$mH	$L_{dm}=10$mH
k_{pc}(without VF)	(0–20)	(0–20)	Unstable	Unstable	(0–13)	(0–13)
k_{pc}(with VF)	(0–20)	(0–20)	Unstable	(0–17)	(0–17)	(0–17)
k_{pc}(Improved IVF)	(0–20)	(0–20)	(0–20)	(0–17)	(0–17)	(0–19)
(100 Hz Ripple Limit)	---					

TABLE IV
STABILITY BOUNDARY OF THE INV MODE

Mode		INV under 0% load		INV under 10% load		INV under 100% load			
Conditions		$L_{dm}=0$ $Z_{ac}=R_{ac}$	$L_{dm}=15$uH $Z_{ac}=R_{ac}$	$L_{dm}=15$uH $Z_{ac}=L_{ac}$	$L_{dm}=15$uH $Z_{ac}=C_{ac}$	$L_{dm}=0$ $Z_{ac}=R_{ac}$	$L_{dm}=15$uH $Z_{ac}=R_{ac}$	$L_{dm}=15$uH $Z_{ac}=L_{ac}$	$L_{dm}=15$uH $Z_{ac}=C_{ac}$
k_{pc}(without VF)		(0–14)	(0–14)	(0–13)	(0–18)	(0–17)	(0–17)	(0–13)	(0–20)
k_{pc}(with VF)		(0–18)	(0–18)	(0–17)	(0–20)	(0–20)	(0–20)	(0–17)	(0–20)
k_{pc}(Improved IVF)		(0–20)	(0–20)	(0–20)	(0–20)	(0–20)	(0–20)	(0–20)	(0–20)
k_{pc}= 10	k_{pv}(without VF)	0.03	0.03	0.02	0.2	0.08	0.08	0.02	0.2
	k_{pv}(with VF)	0.13	0.13	0.13	1.8	0.18	0.18	0.13	1.8
	k_{pv}(Improved IVF)	0.10	0.10	0.10	1.8	0.14	0.14	0.10	1.8
k_{pc}= boundary-1	k_{pv}(with VF)	0.03	0.03	0.04	0.1	0.04	0.04	0.04	0.3

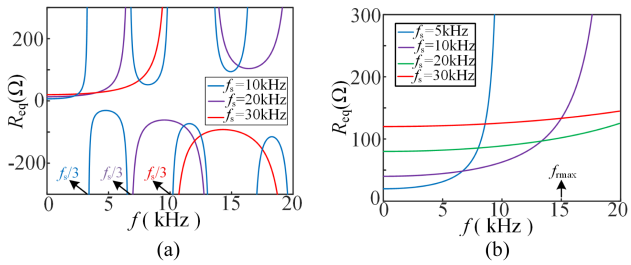

Fig. 35. Relationship between stability boundary k_{pc} and switching frequency f_s. (a) $T_d = 1.5T_s$. (b) $T_d = 0.25T_s$.

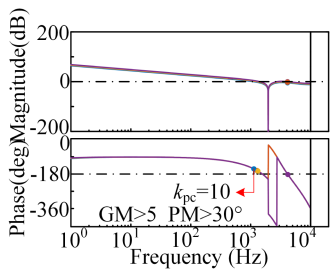

Fig. 36. Bode plots of current open-loop in PFC mode.

intervals of negative resistance also appear within the range of 0 to f_{rmax}. By setting the denominator of R_{eq} in (33) equal to zero, the critical minimum f_s required to maintain limited positive resistance can be determined as 7.5 kHz.

D. Voltage and Current Dual-Loop Parameter Design Method

Tables III and IV summarize the changes in the stability boundaries of the traditional and improved control methods in bidirectional mode, clearly demonstrating the improvement in stability boundaries with the IVF method. These tables can serve as a reference for the design of voltage and current loop parameters.

Step 1 (Design LC filter): The *LC* filter parameters are designed considering the constraints on the inductor current ripple and the reactive power handled by the filter capacitor

$$0.81\ \text{mH} = \frac{V_{ac}}{4\Delta I_{max} 2 f_s} \le L \le \frac{5\% V_{ac}}{\omega_{ac}(P_o/V_{ac})} = 2.56\ \text{mH} \tag{37}$$

$$1.87\ \mu\text{F} = \frac{1}{(2\pi f_n)^2 L} \le C \le \frac{5\% I_L}{\omega_{ac} V_{ac}} = 9.87\ \mu\text{F} \tag{38}$$

where f_n is the cutoff frequency, I_L is the rms value of the inductor current.

Step 2 (Determination of the Current Loop Boundary k_{pc}): As indicated in Tables III and IV, the medium-strength grid condition in bidirectional mode represents the worst-case scenario. Therefore, based on (13), the root locus under this condition is plotted in Fig. 15(d), from which the boundary value of the current loop gain is determined as $k_{pc} = 17$.

Step 3 (Determination of k_{ic} All Operating Conditions): Based on the analysis in Section III–E, a smaller value of k_{ic} is selected under VF control. In this article, $k_{ic} = 10$ is adopted.

Step 4 (Determination of k_{pc} for All Operating Conditions): Based on the denominator of (25), open-loop bode plots are generated for various values of k_{pc} by gradually decreasing its value, as shown in Fig. 36. A suitable k_{pc} is selected such that the gain margin exceeds 5 dB and the PM exceeds 30°.In this article, $k_{pc} = 10$ is adopted.

Step 5 (Determine k_{pv} and k_{iv} in PFC Mode): In PFC mode, the voltage loop bandwidth is significantly limited by the 100 Hz ripple. Therefore, the voltage loop parameters k_{pv} and k_{iv} are calculated according to a target bandwidth of 10–20 Hz to ensure stability [24]. In this article, the selected parameters are $k_{pv} = 0.213$ and $k_{iv} = 7.55$.

Step 6 (Determine k_{pv} and k_{iv} in INV Mode): The key difference between the voltage loop in INV mode and that in PFC mode is the absence of the 100 Hz ripple limitation. Therefore,

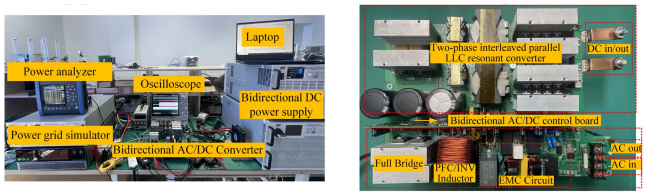

Fig. 37. (a) Experimental test platform. (b) Prototype of PFC/INV converter.

TABLE V
PARAMETERS OF THE DOUBLE-LOOP CONTROLLER IN THE EXPERIMENT

Mode	k_{pc}	k_{ic}	k_{pv}	k_{iv}
PFC	10	10(With VF/IVF) 10000(Without VF)	0.213	7.55
INV			0.06(With VF/IVF) 0.02(Without VF)	100

by repeating Steps 2 and 4, the voltage loop gain k_{pv} for INV mode is determined to be 0.06. Since k_{iv} is related to the 50 Hz tracking performance, it is adjusted experimentally based on Fig. 23(b). In this article, $k_{iv} = 100$ is selected.

Step 7 (DSP Sampling and Computation Configuration): The sampling and loading configurations in the DSP are set according to Fig. 31.

Step 8 (IVF Discretization): The computation of IVF in the DSP controller is implemented based on (36).

V. EXPERIMENTAL VERIFICATIONS

To verify the correctness of the theoretical analysis, an experimental platform for a bidirectional ac–dc converter is established, as shown in Fig. 37. The controller used is the TMS320F28035 with a main clock frequency of 60 MHz. Table V summarizes the parameters designed in Section IV–D for experimental validation. It should be noted that the current loop parameters listed in the table must be divided by the gain K_{pwm} when applied in the DSP to match the circuit implementation.

A. PFC Experimental Waveforms

Fig. 38 shows the experimental waveforms of the PFC mode under stiff grid conditions. Fig. 38(a) verifies the accuracy of the stability boundary. Fig. 38(b)–(d) indicates that stable steady-state waveforms are achieved with all three methods under the parameters listed in Table V. Among these, the method without VF exhibits phase deviation, which is caused by the grid voltage v_{ac}.

Fig. 39 shows the experimental waveforms of the PFC mode under medium-strength grid, the method with VF becomes unstable and triggers protection immediately after the completion of soft start. In contrast, the IVF method remains stable from startup to 100% load, thereby verifying the instability region of the VF method shown in Fig. 25(a).

Fig. 40 shows the experimental waveforms of the PFC mode under weak grid conditions. Fig. 40(a) verifies the accuracy

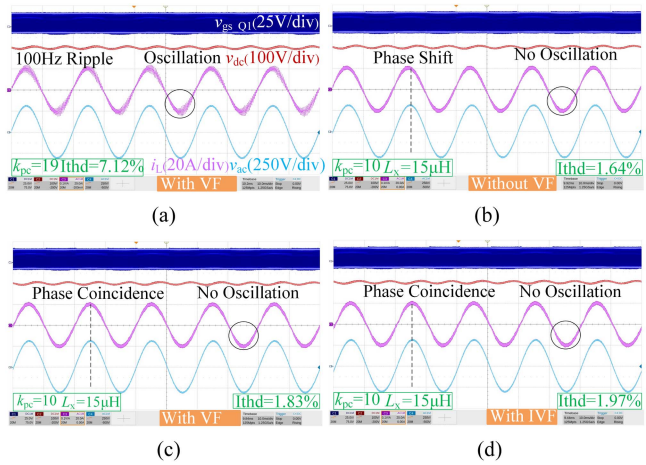

Fig. 38. PFC experimental results under stiff grid conditions. (a) Stability boundary verification. (b) Without VF. (c) With VF. (d) With IVF.

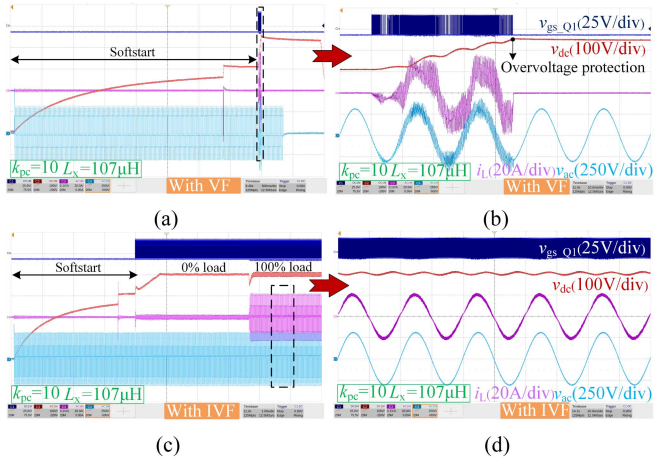

Fig. 39. PFC experimental results under medium-strength grid conditions. (a), (b) With VF. (c), (d) With IVF.

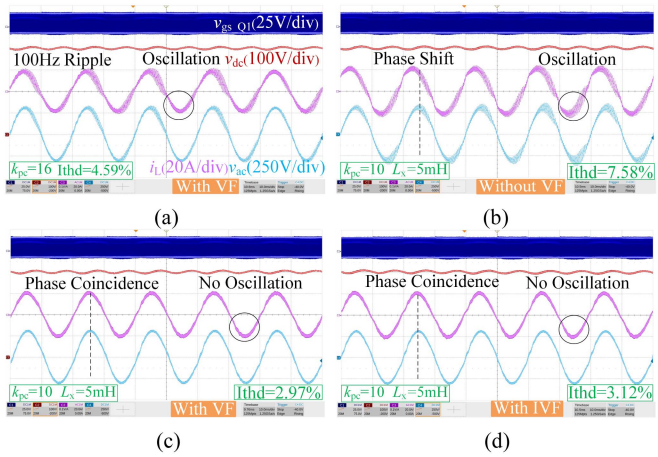

Fig. 40. PFC experimental results under weak grid conditions. (a) Stability boundary verification. (b) Without VF. (c) With VF. (d) With IVF.

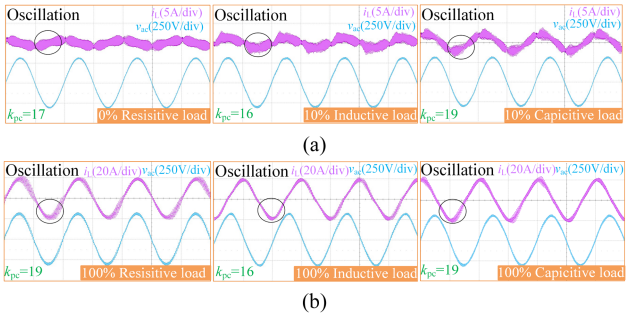

Fig. 41. INV stability boundary verification. (a) Light load. (b) 100% load.

of the stability boundary. Fig. 40(b)–(d) indicates that, under the parameters given in Table V, the method without VF loses stability, whereas both VF and IVF maintain stable steady-state waveforms.

B. INV Experimental Waveforms

To validate the stability boundary of the INV mode, the case with VF is analyzed. Based on Table IV, the parameters are selected as k_{pc} = boundary value -1 and $k_{\mathrm{pv}} = 0.02$ (corresponding to the 0% resistive load). As shown in Fig. 41, under all three load conditions, the inductor current waveforms exhibit critical oscillations, confirming the accuracy of the stability boundary.

Fig. 42 shows the experimental waveforms under resistive, inductive, and capacitive load conditions, respectively. Based on the parameters in Table V, all three methods demonstrate stable experimental waveforms. Fig. 43 presents the steady-state waveforms considering a 10% tolerance in the *LC* parameters. It can be observed that, under the parameter settings in Table V, the method without VF becomes unstable under inductive load conditions, whereas both VF and IVF still maintain stable operating regions.

C. Discussion on the Proposed IVF in Reducing THD

After completing all experimental analyses, it can be observed from Figs. 38–42 that the THD of IVF is higher than that of VF. This also validates the analysis presented in Fig. 30, where reducing the delay improves stability across the entire frequency range but comes at the cost of reducing the virtual resistance R_{eq} in the low-frequency region, thereby weakening the suppression capability of resonance peaks over the full frequency spectrum.

D. Dynamic Response Experimental Validation

Fig. 44 shows the transient waveforms of the two modes from 0% load to 100% load. As observed in Fig. 44(a), the voltage loop bandwidth in PFC mode is limited by the 100 Hz ripple, resulting in similar voltage loop dynamic response times for both methods. In terms of the current loop, IVF exhibits a faster dynamic response compared to the method without VF. Moreover, due to interference from the grid voltage, the 0% load loss is higher in the case without VF than with IVF.

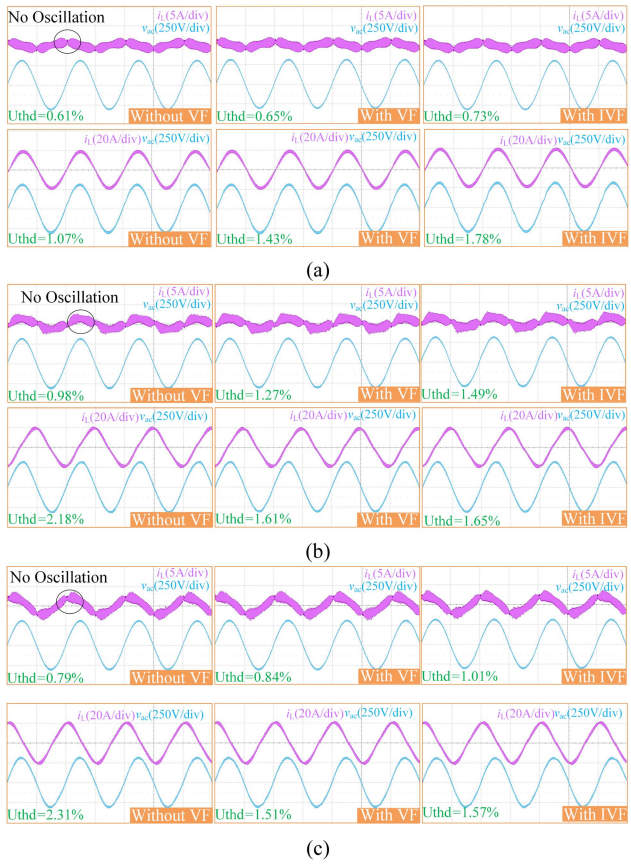

Fig. 42. INV mode experimental results under three load conditions. (a) Resistive load. (b) Inductive load. (c) Capacitive load.

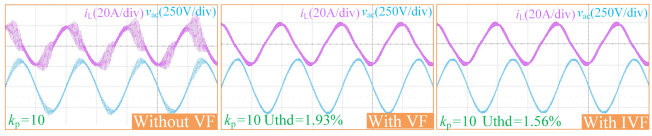

Fig. 43. Impact of 10% parameter tolerance on the three methods in INV mode.

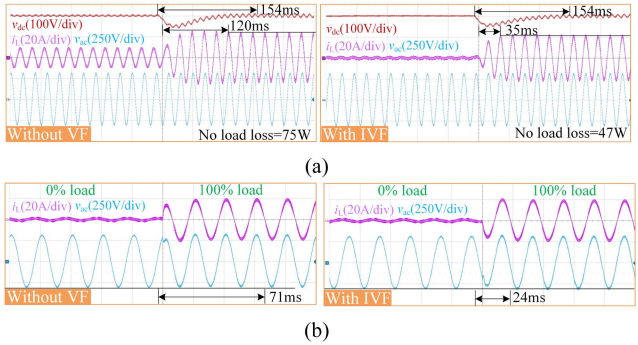

Fig. 44. Dynamic response experimental validation. (a) PFC mode with stiff grid. (b) INV mode with resistive load.

TABLE VI
COMPARISONS OF DIFFERENT VF METHODS

Ref.	Model	Method	Stability region	Dependence of resonant parameters	Controller requirements
[25]	VF	Preset resonance parameters	(0-f_s/3)	No	Low
[26]	IVF	Preset resonance parameters	non-fixed	No	Low
[27]	IVF	resonance peak cancellation	(0-f_s)	No	Low
[28]	IVF	full delay compensation	(0-f_s)	Yes	High
Proposed	IVF	partial delay compensation	(0-f_s)	Yes	Low

In INV mode, since the voltage loop is not affected by the 100 Hz ripple, both methods exhibit significantly improved dynamic responses. Nevertheless, the IVF method still outperforms the method without VF in terms of response speed.

E. Comparison of VF Methods

Table VI compares the proposed IVF method with other IVF approaches. The proposed IVF method offers the advantages of resonance-parameter independence and suitability for implementation on low-cost controllers, in comparison with existing approaches.

VI. CONCLUSION

Based on two conventional control methods (without VF and with VF), this article comprehensively summarizes the stability variations on the ac-side of a bidirectional ac–dc converter under six operating conditions. The results show that both methods lose stability under medium-strength grid conditions, and the method without VF may also lose stability under inductive load conditions. An improved VF control strategy is proposed, which enables the converter to achieve superior stability and dynamic performance across all bidirectional operating conditions. Moreover, compared to the VF method, although the IVF method enhances stability, it results in a higher THD, which is a drawback of this approach.

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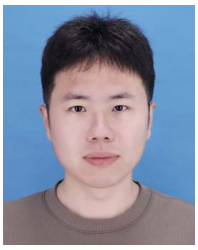

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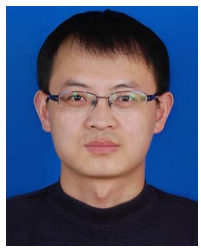

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