Utilizing Silicone Gel Encapsulation in Power Semiconductor Module to Improve Manufacturability While Reducing Common-Mode Noise

Sihoon Choi, *Member, IEEE*, Jiyoon Choi, *Student Member, IEEE*, Thiyu Warnakulasooriya, *Student Member, IEEE*, Jong-Won Shin, *Senior Member, IEEE*, Jun Imaoka, *Member, IEEE*, and Masayoshi Yamamoto, *Member, IEEE*

***Abstract*—The novel power module introduced in this article features an etched section of the bottom copper layer of a direct-bonded copper substrate, encapsulated in silicone gel. The proposed design improves manufacturability and reduces common-mode (CM) electromagnetic interference, while it does not sacrifice size, thermal performance, and manufacturing process. The measured CM noise in prototype hardware was decreased by maximum 5 dBμV in steady-state operation. Thermal cycling tests with a total of 1000 cycles confirmed the proposed power module does not compromise mechanical stability.**

***Index Terms*—Common-mode (CM) noise, encapsulation, manufacturability, power module packaging, reliability, silicone gel.**

I. Introduction

VARIOUS approaches to reduce conducted common-mode (CM) noise were introduced to compensate high *dv/dt* and *di/dt* during the switching transition of power semiconductor devices. Various filters and circuits have been introduced to attenuate CM noise. Passive and/or active filters are widely employed to reduce the CM noise [1]. Adopting symmetric circuit topologies effectively attenuates CM noise by generating antiphase CM current [2], [3]. Impedance balancing techniques design the CM equivalent circuit into a Wheatstone bridge and remove the CM noise without configuring symmetric topology [4], [5].

Various power module designs have been proposed to reduce the CM noise. Additional direct-bonded copper substrate (DBC hereafter) was placed under the main DBC, working as a CM noise screening layer [7]. Designing the screening middle layer pattern further improved the noise attenuation [8]. Four power modules with different screening architectures were fabricated and compared in [6]. However, Screening CM noise with an extra substrate may degrade thermal performance, complicate manufacturing, and decrease cost effectiveness.

Other approaches attenuated CM noise by modifying capacitive coupling of power module. A top copper layer was redesigned to reduce the area of pulsating nodes and the capacitance between the midpoint of half-bridge circuit and a baseplate [9]. Additional printed circuit board (PCB) on the DBC places the pulsating nodes without close contact with the grounded baseplate, resulting in low CM capacitance [10], [11]. Adjusting capacitances between each power module terminal and the grounded baseplate effectively canceled out the CM current [12], [13]. Comprehensive analysis was conducted to clarify the influence of the parasitic capacitances in power modules [14]. Nevertheless, the approach may complicate manufacturing and decrease reliability.

Suppressing capacitive coupling of power modules was realized by etching away a portion of the bottom copper layer. The work in [15] and [16] replace the etched area with air which has the lowest relative permittivity, i.e., 1. This approach does not compromise the size and layout of the power module, while its mechanical reliability remains uncertain. Low-permittivity epoxies were used instead of air to improve the mechanical reliability and realized effective CM noise reduction [17], [18]. However, injecting and curing the epoxies requires longer manufacturing time. Selection of epoxy materials and their packaging conductions also need to be carefully determined.

Received 3 February 2025; revised 17 April 2025 and 23 June 2025; accepted 30 September 2025. Date of publication 3 October 2025; date of current version 23 December 2025. This work was supported in part by Green Innovation Fund Projects for Development of Next Generation Motor under Grant JPNP21026 commissioned by the New Energy and Industrial Technology Development Organization (NEDO) and in part by the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT under Grant RS-2023-00217270 and Grant 2022R1C1C1010027. Recommended for publication by Associate Editor N. Zargari. *(Corresponding author: Jong-Won Shin.)*

Sihoon Choi, Jun Imaoka, and Masayoshi Yamamoto are with the Institute of Materials and Systems for Sustainability, Nagoya University, Nagoya 464-8601, Japan (e-mail: choi.sihoon.w4@f.mail.nagoya-u.ac.jp; imaoka.jun.n9@f.mail.nagoya-u.ac.jp; yamamoto.masayoshi.n5@f.mail.nagoya-u.ac.jp).

Jiyoon Choi and Thiyu Warnakulasooriya are with the Department of Electrical Engineering, Nagoya University, Nagoya 464-8601, Japan (e-mail: choi.jiyoon.t3@s.mail.nagoya-u.ac.jp; warnakulasooriya.thiyu.sansika.w8@s.mail.nagoya-u.ac.jp).

Jong-Won Shin is with the Department of Electrical and Computer Engineering and with Electric Power Research Institute, Seoul National University, Seoul 08826, South Korea (e-mail: jongwonshin@snu.ac.kr).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3617463.

Digital Object Identifier 10.1109/TPEL.2025.3617463

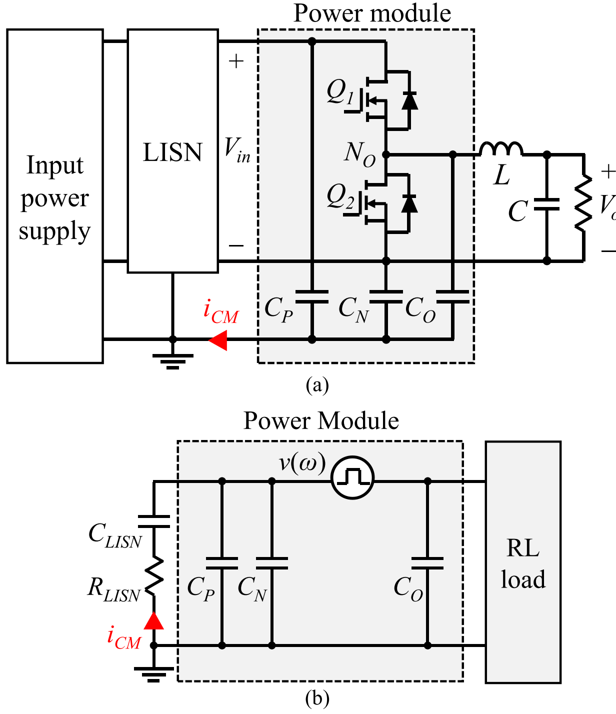

Fig. 1. (a) Half-bridge power module and its parasitic capacitances. (b) High-frequency equivalent circuit of Fig. 1(a).

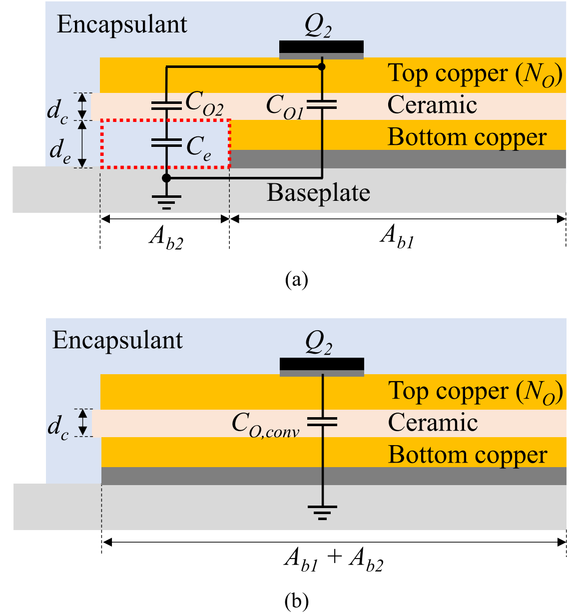

Fig. 2. (a) Cross section of the proposed power module near N_O. In red-dotted box, a part of the bottom copper is replaced by the encapsulant material. (b) Cross-section of the conventional power module near N_O.

This article improves manufacturability and reduces the CM noise of the power module. The proposed power module replaces etched area between the bottom copper layer and the baseplate by silicone gel instead of air [16] or epoxies [17]. The proposed design does not require extra material and manufacturing process because: the gel is the encapsulation material typically used in power modules; the injection of this gel is fulfilled by conventional encapsulation process; the gel has high surface tackiness and low viscosity so that the mechanical reliability is not sacrificed. The proposed design merely degrades CM noise, module size, and thermal performance. The prototype power module was tested in a 1-kW 50-kHz buck converter to measure the CM noise. The prototype module is visually inspected before and after 1000-cycle thermal cycling test (TCT) to verify the enhanced reliability compared to the modules in [17].

The rest of the article is organized as follows: Section II explains the configuration of the proposed power module to reduce CM capacitance. The CM capacitance is estimated and compared with various power modules. Thermal performance, thermomechanical stress, and manufacturability are introduced. Section III validates the manufacturability and reliability of the proposed power module. The CM noise and thermal resistance are experimentally measured and verified its effectiveness in Section IV. The results of TCTs show the good reliability of the proposed method. Finally, Section V concludes the article.

II. Proposed Power Module Design

Fig. 1(a) illustrates a power module including the high-side bare die Q_1, and the low-side bare die Q_2. The module is connected to the input power supply through line impedance stabilization networks (LISNs). The module, inductor L, and capacitor C build a buck converter of which input and output voltages are V_{in} and V_{out}, respectively. The CM capacitance C_P (C_N) is connected between the positive (negative) dc terminal and the ground. Another CM capacitance between the node N_O and ground is denoted as C_O. Fig. 1(b) presents the high-frequency equivalent circuit of Fig. 1(a). Capacitances C_P and C_N are in parallel due to the low-impedance of the large input capacitor at the high frequency. The impedance of LISN is represented by R_{LISN} and C_{LISN}. The pulsating voltage at N_O or the drain-source voltage of Q_2 is expressed by $v(\omega)$. The CM current i_{CM} is calculated as in (1). Fig. 1(b) presents the high-frequency equivalent circuit of Fig. 1(a). Capacitances C_P and C_N are in parallel due to the low-impedance of the large input capacitor at the high frequency. The impedance of LISN is represented by R_{LISN} and C_{LISN}. The pulsating voltage at N_O or the drain-source voltage of Q_2 is expressed by $v(\omega)$. The CM current i_{CM} is calculated as

$$i_{\text{CM}} = \frac{j\omega C_O C_{\text{LISN}} v(\omega)}{C_A + C_{\text{LISN}} + j\omega C_A C_{\text{LISN}} R_{\text{LISN}}} \tag{1}$$

where C_A is defined as (2).

$$C_A = C_P + C_N + C_O. \tag{2}$$

From (1)–(2), i_{CM} increases as C_O increases as also introduced in [22] and [23].

A. Estimation of CO

Fig. 2(a) shows a cross section view of the proposed power module. Top copper [corresponds to N_O shown in Fig. 1(a)],

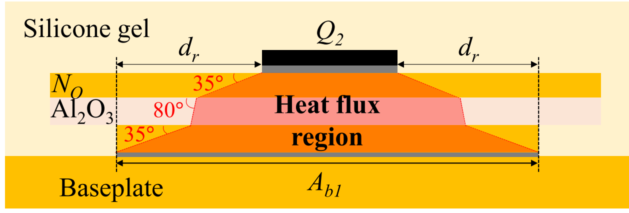

Fig. 3. Estimation of A_{b1} based on the heat spreading angle and heat flux region.

ceramic (Al_2O_3 in this article), and bottom copper layers configure DBC. Device Q_2 is on the top copper layer and a baseplate is attached beneath the bottom copper layer, which is a typical lay-up structure of power modules. A specific portion of the bottom copper layer, indicated by red-dotted box in Fig. 2(a), is etched away and replaced by silicone gel, the encapsulant material. The thickness of the ceramic layer is d_c, and the distance between the bottom surface of the ceramic layer and the top surface of the baseplate is d_e. The capacitance C_O in Fig. 2(a) is obtained as

$$C_O = C_{O1} + \frac{C_{O2}C_e}{C_{O2} + \mathrm{C_e}} \tag{3}$$

where C_{O1}, C_{O2}, and C_e are expressed as

$$\mathrm{C}_{O1} = \varepsilon_0\varepsilon_c\frac{A_{b1}}{d_c} \tag{4}$$

$$C_{O2} = \varepsilon_0\varepsilon_c\frac{A_{b2}}{d_c} \tag{5}$$

$$C_e = \varepsilon_0\varepsilon_e\frac{A_{b2}}{d_e}. \tag{6}$$

In (4)–(6), ε_o is the permittivity of free space or 8.85×10^{-12} $\mathrm{F{\cdot}m^{-1}}$; ε_c is the relative permittivity of the ceramic material; ε_e is the relative permittivity of the encapsulant. Literals A_{b1} and A_{b2} represent the area of the remaining and etched-away bottom copper, respectively, as illustrated in Fig. 2(a).

If the bottom copper in the red-dotted portion in Fig. 2(a) is not etched out, the design will become the conventional power module in Fig. 2(b). The CM capacitance between N_O and the baseplate or $C_{O,conv}$ is as in (7).

$$C_{O,\mathrm{conv}} = \varepsilon_0\varepsilon_c\frac{A_{b1} + A_{b2}}{d_c}. \tag{7}$$

Numerically, $C_O < C_{O,\mathrm{conv}}$ and thus CM EMI is lower in Fig. 2(a) than in Fig. 2(b). The calculated capacitances from (3)–(7) can be slightly lower than actual values since this article neglects fringing effect to simplify the estimation [19].

The bottom copper layer is etched considering heat flux not to increase the thermal resistance. Fig. 3 shows major heat flux region among layers. The head spreading angles are 35° for the copper layers and 80° for the Al_2O_3 ceramic layer [21]. The area except the remaining bottom copper area A_{b1} beneath N_O is etched out. The horizontal distance from Q_2 is d_r which is

TABLE I
COMPARISON OF DIMENSIONS AND ESTIMATED CAPACITANCES OF POWER MODULES

Module name	full-copper	epoxy15	epoxy32	proposed
d_c	0.38 mm			
d_e	0.45 mm assuming 0.15-mm thickness of solder layer			
Bottom copper design	Fig. 4(c)	Fig. 4(b)		
A_{b1}	50 mm²			
A_{b2}	106.4 mm²			
C_{O1}	Not applicable	11.39 pF		
C_{O2}		24.26 pF		
ε_e		3.8	3.5	3
C_e		7.95	7.32 pF	6.28 pF
$C_{O,conv}$ or C_O	**35.71 pF**	**17.38 pF**	**17.01 pF**	**16.38 pF**

obtained as

$$d_r = d_t/\tan(35^\circ) + d_c/\tan(80^\circ) + d_b/\tan(35^\circ). \tag{8}$$

In (8), d_t and d_b are the thickness of top and bottom copper layers, respectively.

Fig. 4 presents the 25 × 19.2 $\mathrm{mm^2}$ DBC to build prototype power modules. Fig. 4(a) shows the layout of the top copper layer with the location of Q_1 and Q_2. Fig. 4(b) presents the bottom copper layer with the etched region A_{b2}.

In this article, A_{b2} was filled by three different materials: epoxy of which coefficient of thermal expansion (CTE) is 15 ppm/K (the module using this epoxy is referred as epoxy15 module hereafter); another epoxy of which CTE is 32 ppm/K (epoxy32 module hereafter); and encapsulant (proposed module). In contrast to epoxy15 or epoxy32 modules which require additional manufacturing process to inject and cure epoxies, the proposed module features simpler manufacturing–the encapsulant is extended into A_{b2} during the encapsulation process and does not need any extra development.

The bottom copper in the orange region, A_{b1} in Fig. 4(b), was not etched out in order to maintain the same thermal performance between modules. The estimated d_r was 0.92 mm based on the thicknesses of the copper and Al_2O_3 layers. The DBC was designed and prototyped with 1-mm d_r to secure enough margin. Fig. 4(c) shows the etch-free bottom copper layer of the conventional module (full-copper module hereafter).

Table I compares the estimated CM capacitances of the four prototype modules: full-copper, epoxy15, epoxy32, and proposed modules based on (3)–(7). The estimated C_O was 16.38 pF, implying 54.1% reduction compared to $C_{O,\mathrm{conv}}$.

B. Thermal Performance

A steady-state thermal simulation of the three modules was performed by Ansys 2023 R2 Icepak. The coolant temperature and flow rate were 65°C and 8 liter per min, respectively, which are typical in automotive power module cooling. A thermal load of 10 W was assigned to the top surface of each die. The thermal conductivity of silicone gel (encapsulant) was set to only 0.18 W/m·K.

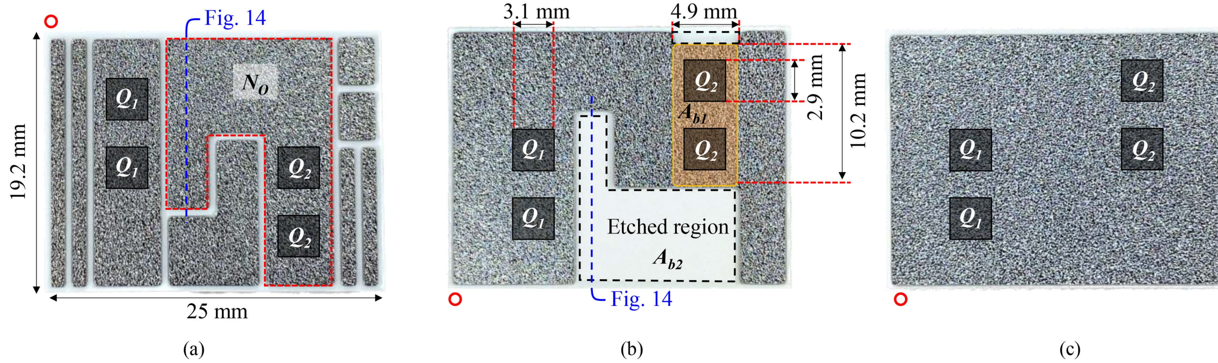

Fig. 4. Photographs of the DBC used in this article. (a) Top copper. (b) Etched bottom copper layer for epoxy32, epoxy15, and the proposed modules. (c) Etch-free bottom copper for the conventional module.

Fig. 5 shows the simulation results of the full-copper and the proposed modules. The average maximum temperature of the two Q_2 bare dies are 92.3°C in the full-copper module [see Fig. 5(a)] and 92.6°C in the proposed module [see Fig. 5(b)]. Fig. 5(c) presents the temperature of Q_2 as d_r varies. It shows that a 1-mm d_r is at an acceptable level with only 0.3°C difference, while $d_r < 1$ mm cause a significant increase in Q_2 temperature. The structure function of each module was also experimentally measured, and the same thermal performance was also observed in Section IV-C.

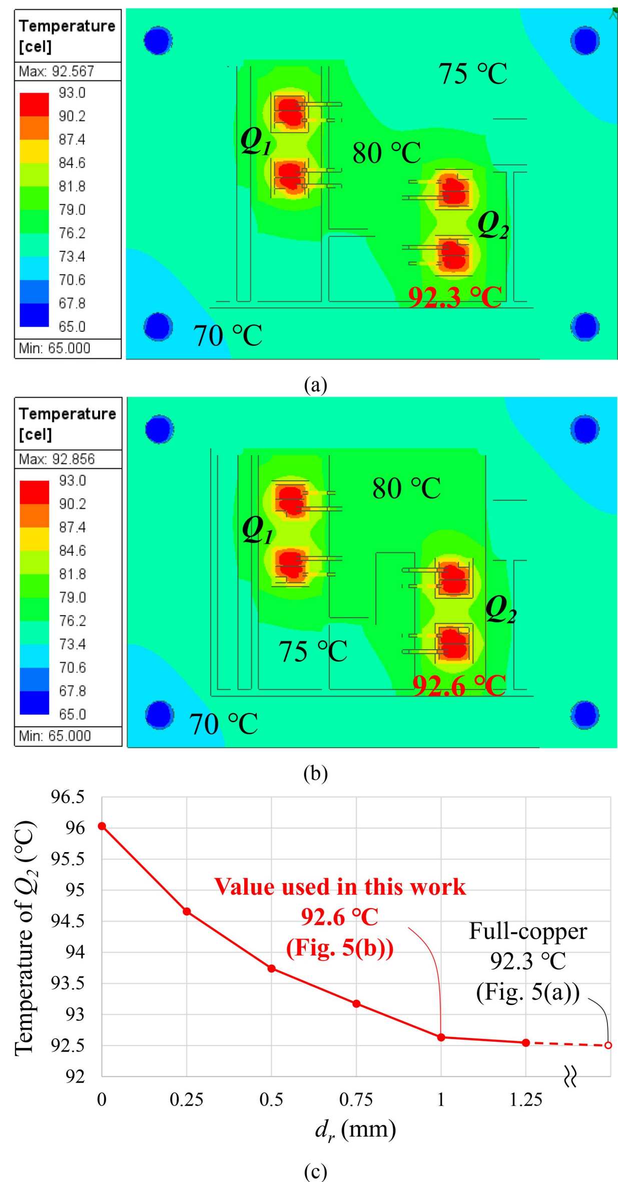

Fig. 5. Steady state thermal simulation results. (a) Full-copper module. (b) Silicone gel module ($d_r = 1$). (c) The average maximum temperature of two Q_2 bare dies as d_r varies.

C. Thermomechanical Stress

Static structural analysis was performed by Ansys 2023 R2 Mechanical to assess the reliability of the proposed power module assuming 9.8-m/s^2 gravity. A thermal load of 10 W was applied to the top surface of each die. Film coefficient of 4 kW/m^2·K was assigned to the baseplate of the power module with 65°C ambient temperature. The side and bottom surfaces of the baseplate and screw holes of the busbars were fixed in position as a boundary condition.

All power modules regardless of the bottom copper configuration tend to experience high thermal stress at the edges of the baseplate solder layer. Delamination typically initiates from these edge regions. This behavior leads to a common stress distribution pattern: higher stress at the periphery and lower stress toward the center. Fig. 6 presents the simulated von-Mises stress of the baseplate solder for epoxy32 module [see Fig. 6(a)] and silicone gel module [see Fig. 6(b)]. The simulation results also show localized high thermal stress near the solder edge. However, the proposed modification does not introduce additional thermal stress near the etched region. The maximum thermal stress at the innermost area was approximately 40 MPa, which is below the ultimate tensile strength of SAC305 solder. Actual stress is expected to be even lower in practical configurations, since the solder fillets which are not reflected in the simulation will relieve the stress. Delamination is more likely to occur in the outermost regions as with conventional modules, which is further confirmed in Fig. 16. Mechanical reliability is additionally supported by the experimental results presented in Section IV-B.

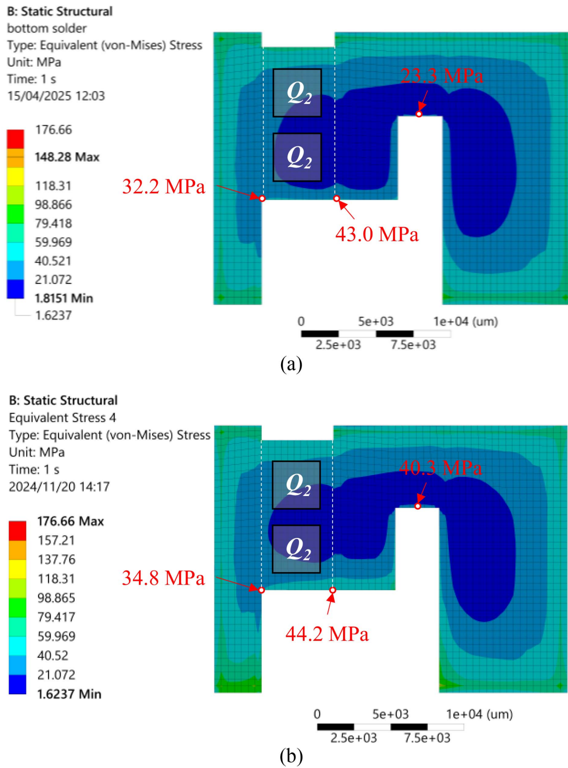

Fig. 6. Simulated von-Mises stress of the baseplate solder (a) in epoxy32 module and (b) in silicone gel module.

The results indicate that the epoxy32 module shown in Fig. 6(a) presents slightly lower thermal stress in the baseplate solder layer than the silicone gel module, assuming the epoxy completely fills the etched region without voids or delamination. In practice, however, epoxies often introduce voids and delamination which causes long-term reliability issues. Moreover, the proposed silicone gel module simplifies the manufacturing process while still achieving comparable mechanical reliability.

D. Manufacturability

The manufacturing process of the power modules is explained as follows to validate the feasibility of the proposed method for mass production: the first stage is to place all components including bare dies, the DBC, a thermistor, busbars, and a baseplate within a jig. The position of the DBC is laser-marked on the baseplate. A tip of bonding wire is attached at each corner of the baseplate to secure the same solder thickness as shown in Fig. 7(a). This provides the same d_e to all modules for fair comparison. Fig. 7(b) and (c) show the position of baseplate-attach solder (SAC305) and die-attach solder (Pb95Sn5), respectively. Bare dies Q_1 and Q_2 were placed on the die-attach solder as shown in Fig. 7(d). After the components placement, single vacuum reflow with formic acid is conducted.

The epoxy15 and epoxy32 modules need additional manufacturing process to inject and cure the epoxy material after the reflow, which is not necessary for the proposed power module.

TABLE II
SPECIFICATIONS OF PROPOSED POWER MODULE

Components		Description
SiC die		S4503/750 V/56 A/26 mΩ by Rohm
Die-attach solder		Pb95Sn5, 48.1 W/m·K
DBC		19.2 mm × 25 mm × 0.98 mm
	Top Cu	0.3-mm thickness
	Ceramic	Al_2O_3/0.38-mm thickness
	Bottom Cu	0.3-mm thickness
Baseplate		C1020/2-mm thickness
Baseplate-attach solder		SAC305, 58 W/m·K
Epoxy15		ε_e = 3.8, CTE = 15 ppm/K, viscosity = 50 Pa·s, T_g = 145°C, curing condition = 130°C for 5 minutes + 160°C for 10 minutes
Epoxy32		ε_e = 3.5, CTE = 32 ppm/K, viscosity = 40 Pa·s, T_g = 137°C, curing condition = 150°C for 1 hour
Aluminum wire		(source connections) 400-μm diameter (gate connections) 125-μm diameter
Thermistor		HM104J1A by Littelfuse
Silicone gel		(Two types of gel, A and B, were combined by 1:1 ratio) viscosity of A: 0.95 Pa·s, viscosity of B: 0.5 Pa·s, ε_e of A and B = 3, curing condition = 80°C for 1 h

A syringe with 0.3-mm diameter was used to inject epoxy into 0.45-mm gap between the Al_2O_3 layer and the baseplate which is d_e defined in Fig. 2(a) and Table I. The injection was carried out on an 80-°C hotplate to lower the viscosity of the epoxy, since low viscosity is preferred to avoid potential voids in the epoxy [17]. Epoxy32 was cured in a temperature chamber at 150°C for an hour. The epoxy15 module was cured at 130°C for 5 min, and again at 160°C for 10 min as recommended in its datasheet. Fig. 8(a) shows the conceptual cross section image of epoxy15 and epoxy32 modules.

The etched area of the silicone gel module is filled during the conventional encapsulation process without additional processes. In the proposed module presented in Fig. 8(b), the encapsulant extends beneath the ceramic layer of DBC in the etched region. The gel was cured at a temperature of 80°C for 1 hour based on the recommended curing condition.

Fig. 8(c) shows the prototype power modules. Aluminum wires are bonded to bare dies for interconnections. Power lines used in the power modules are 400-μm diameter wires, while signal lines utilize 125-μm diameter wires. All three modules appear identical when observed from above. Table II summarizes characteristics of the components used in the prototype modules.

III. VALIDATION OF MANUFACTURABILITY AND RELIABILITY

The prototype modules in Section II-D were scanned to validate their manufacturability. Fig. 9 shows constant-depth mode scanning acoustic microscopy (C-SAM) images of epoxy32 [see Fig. 9(a)] and epoxy15 modules [see Fig. 9(b)]. The depth was adjusted to capture the bottom copper layer. White and gray areas are the etched region or A_{b2} in Fig. 4(b). The color difference at the etched region implies a defect in epoxy32 and epoxy15 modules.

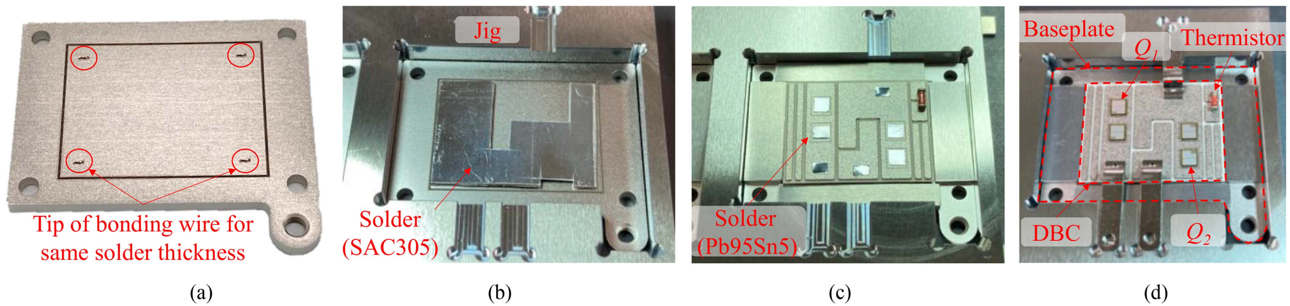

Fig. 7. (a) Baseplate with laser-marking and tip of bonding wires. (b) Baseplate-attach solder (SAC305) is placed on the baseplate. (c) DBC and die-attach solder (Pb95Sn5) is positioned. (d) All components are set in the jig.

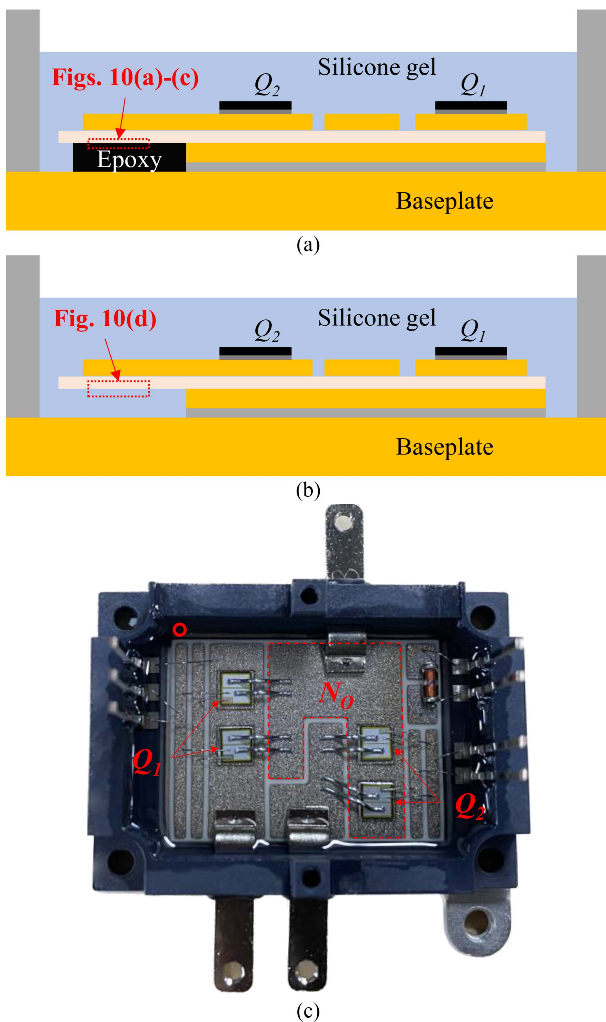

Fig. 8. Cross section view of (a) epoxy15 and epoxy32 modules and (b) the proposed power module using silicone gel (encapsulant). (c) Photograph of the prototype power module.

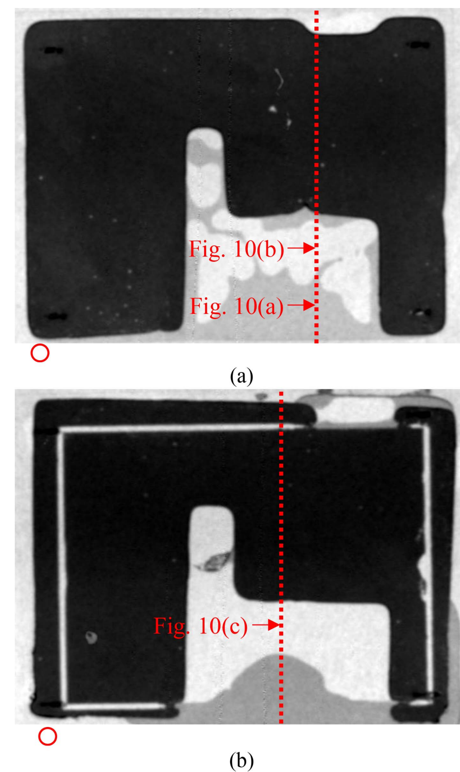

Fig. 9. C-SAM images of (a) epoxy32 and (b) epoxy15 modules. The depth was adjusted to scan the bottom copper layer.

Epoxy32 and epoxy15 modules were cut along the red broken lines in Fig. 9(a) and (b) to observe the cross-sections. The interfaces between the ceramic and epoxy layers were captured using a scanning electron microscope (SEM) as shown in Fig. 10. Fig. 10(a) shows the gray area of epoxy32 module and Fig. 10(b) and (c) describe the white area of epoxy32 and epoxy15 modules, respectively. Epoxy32, of which the CTE is higher than copper, resulted in cracks at ceramic layer as shown in Fig. 10(b). The high temperature of curing conditions may cause damage to the ceramic layer due to the high mismatch of CTE. Epoxy15 with similar CTE with copper, in contrast, exhibited no ceramic crack as shown in Fig. 10(c). However, delamination or low adhesion was observed at the interface. Due to difficulties in fabricating the epoxy15 module in an acceptable condition, it was excluded from the experimental verification. These observations suggest that the material properties and packaging conditions of the epoxy such as its adhesion strength, CTE, and viscosity must be carefully considered in a design stage.

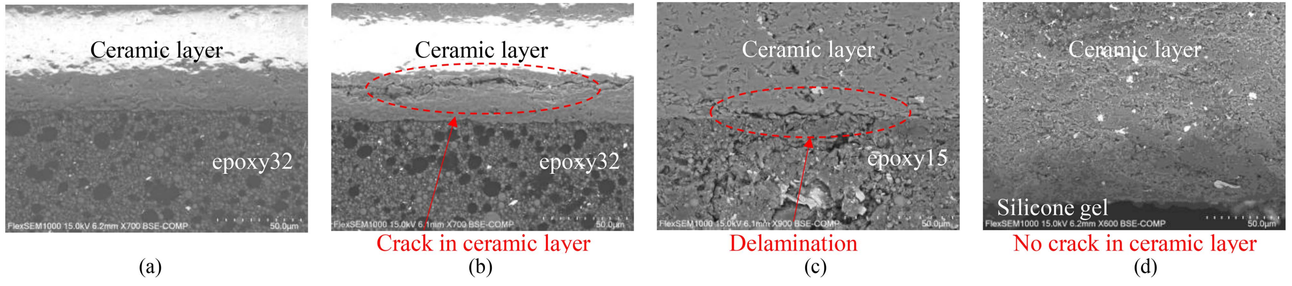

Fig. 10. Cross-section images captured by SEM. The location of each cross-section is indicated by red dashed squares in Fig. 8 or red broken lines in Fig. 9. (a) Gray area of epoxy32 module shown in Fig. 9(a). (b) White area of epoxy32 module shown in Fig. 9(a). (c) White area of epoxy15 module shown in Fig. 9(b). (d) Proposed power module encapsulated by silicone gel.

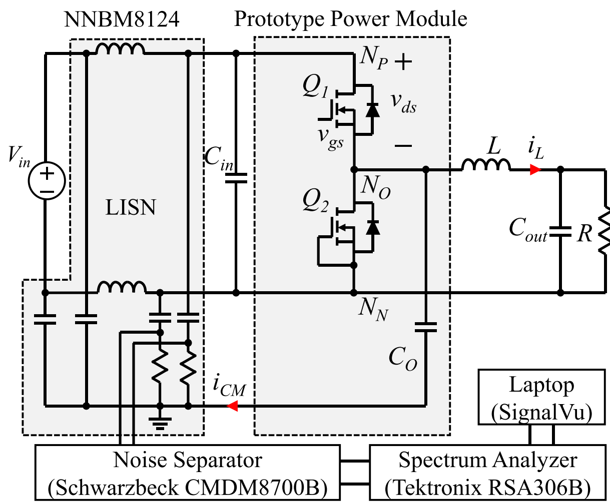

Fig. 11. Experimental setup to measure CM noise.

Fig. 10(d) presents the cross-section of the proposed power module encapsulated by silicone gel as shown in Fig. 6(b). The silicone gel is softer and tackier than epoxies and it hardly made voids and delamination. The curing temperature of the gel is lower than that of epoxy resins, scarcely damaging the ceramic layer. No cracks and delamination were detected in the proposed module.

TABLE III
SPECIFICATIONS OF THE CIRCUIT TO MEASURE CM NOISE

V_{in}	400 V
V_O	200 V
Switching frequency	50 kHz
L	7 mH
Output power	1 kW
C	401.8 μF
LISN	NNBM8124
Spectrum Analyzer	RSA306B

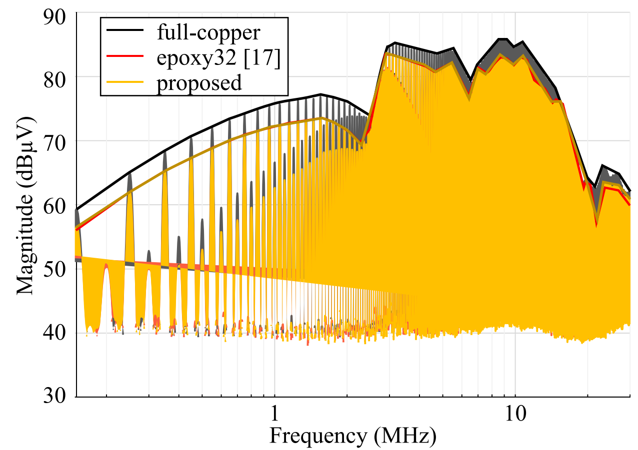

Fig. 12. Measured CM noise spectra of full-copper (black), epoxy32 (red), and proposed modules using silicone gel (yellow).

IV. Experimental Verification

A. CM Noise Measurement

The experimental setup using the prototype modules is shown in Fig. 11. Two LISNs NNBM8124 and noise separator CMDM8700B were used to measure CM noise. Spectrum analyzer RSA306B with a 9-kHz resolution bandwidth processed the noise with SignalVu. The parameters of the circuit are given in Table III.

Fig. 12 shows the measured CM noise spectra of the full-copper (black), epoxy32 (red), and proposed module using silicone gel (yellow). The epoxy32 and proposed power modules reduced CM noise by approximately 5 dBμV compared to the full-copper module. It is noted that the proposed module achieves nearly identical performance to the epoxy32 module despite the simpler manufacturing process explained in Section II-D.

B. Thermal Cycling Test

The proposed power module modifies the vertical structure through the etched region, focusing on the structural stability of the entire module. TCTs were conducted in this article because the tests are more relevant for evaluating package-level reliability [20]. Power cycling tests of which aim is chip-level interconnections such as die attachment and wire bonding were not conducted in this article. TCTs with 1000 cycles were performed

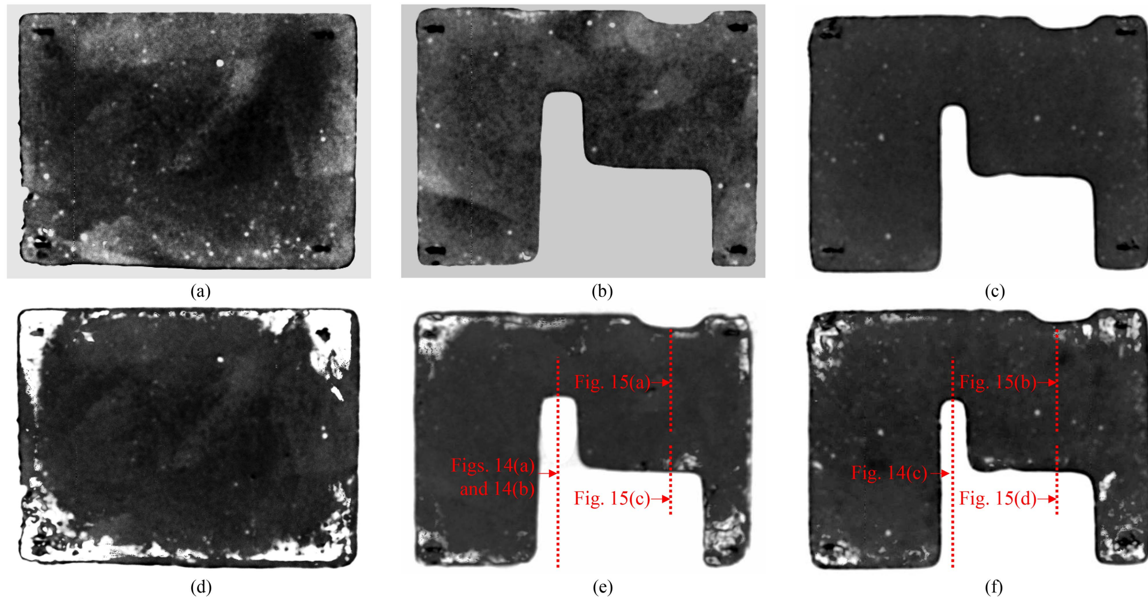

Fig. 13. C-SAM images of the baseplate solder layer of (a) full-copper module before TCTs, (b) epoxy32 module before TCTs, (c) silicone gel module before TCTs, (d) full-copper module after TCTs, (e) epoxy32 module after TCTs, and (f) silicone gel module after TCTs.

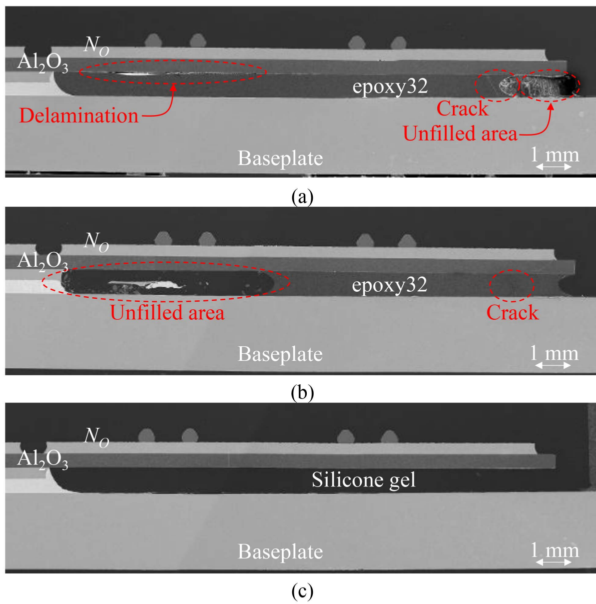

Fig. 14. SEM images of the cross-sections indicated in Fig. 4. (a) and (b) Captured from epoxy32 modules, while (c) is from the proposed module encapsulated by silicone gel.

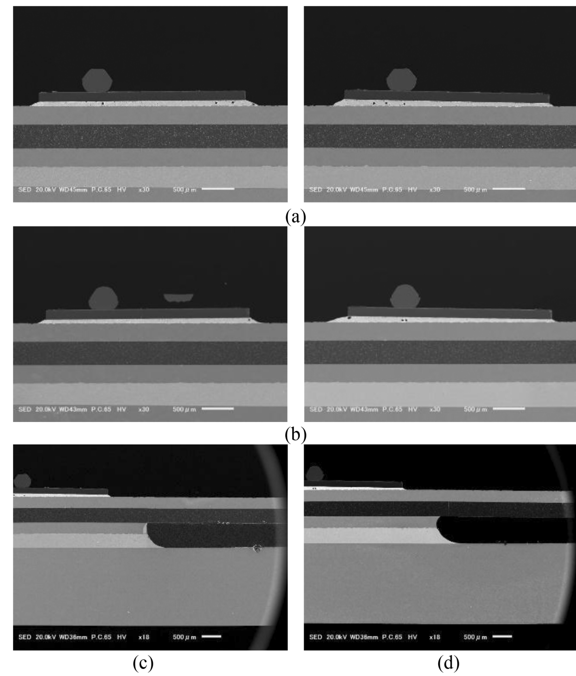

Fig. 15. SEM images after the thermal cycling test. Die attachment of Q_2 in (a) the epoxy32 module and (b) the silicone gel module. Baseplate attach solder near Q_2 in (c) the epoxy32 module and (d) the silicone gel module.

by a thermal shock chamber TSA-73ES to validate the reliability of the proposed module. In a cycle, the temperatures were –40 °C and 125 °C, and each temperature was maintained for 30 minutes. The test conditions were determined based on AQG324 standards [20]. Among the fabricated samples, epoxy32 modules in the best achievable condition were selected and conducted TCTs alongside the proposed silicone gel modules.

Fig. 13(a)–(c) shows C-SAM images of the baseplate solder layer for the full-copper, epoxy32, and silicone gel power modules before TCTs, and Fig. 13(d)–(f) presents the corresponding images after TCTs. Delamination was observed at the edge regions due to high thermal stress. In contrast, the etched region hardly showed delamination, as predicted in Section II-C, indicating that the proposed modification does not induce additional thermal stress.

Fig. 14(a) and (b) shows the cross sections of two different epoxy32 modules captured by SEM after the TCT. The location of the cross section is indicated in Fig. 4. The results imply

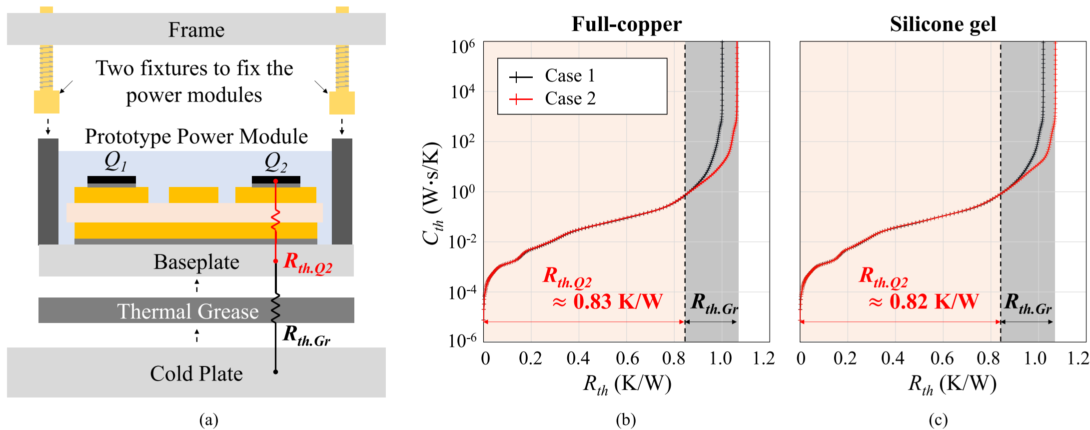

Fig. 16. (a) Setup for measuring structure function. Measured structure functions of (b) the full-copper (conventional) and (c) silicone gel (proposed) modules. Case 1 and case 2 are with adequate and minimal amount of thermal grease, respectively, to distinguish $R_{\mathrm{th}.Q2}$ and the thermal resistance of thermal grease $R_{th.Gr}$.

that the epoxy may delaminate from the ceramic layer and leave several areas in the etched region unfilled. This reminds the importance of careful selection of epoxy material and packaging conditions mentioned in Section III. Fig. 14(c) presents the cross section of the proposed module. The silicone gel used in the proposed module features low viscosity, high surface tackiness, and inherent softness, making it less prone to delamination and damage during the manufacturing process or operation. These characteristics contribute to complete filling of the etched region and improving manufacturability while maintaining CM noise reduction. There were also no solder cracks at the baseplate attachment, while cracks were observed without silicone gel filling [16].

Fig. 15(a) and (b) shows SEM images of the die attach for Q_2 of epoxy32 and the silicone gel module, respectively, after the thermal cycle test. Fig. 15(c) and (d) present the baseplate attach solder near Q_2 for epoxy32 and the silicone gel module, respectively. The location of the cross sections is indicated in Fig. 13(e) and (f). No delamination and cracks were observed as expected in Section II-C and Fig. 6. This verifies that the proposed power module with the etched bottom copper hardly degrades the overall reliability and does not damage adjacent components.

The proposed power module was not subjected to an H3TRB (High-humidity, high-temperature reverse bias) test [20], since this test is typically intended to evaluate insulation degradation and passivation layer failure at the chip level due to moisture ingress under high humidity and high temperature conditions. The proposed scheme does not modify chip-level configuration, hence H3TRB may not be suitable for validating the specific structural aspects of the proposed power module. Nevertheless, the silicone gel, a widely adopted encapsulant in power modules, provides a high level of moisture protection: it effectively shields encapsulated devices from moisture, chemicals, and contamination. Silicone gel also slightly absorbs moisture. However, it dissolves moisture gradually, acting as a moisture buffer that delays rapid humidity transmission to the semiconductor surface. Therefore, it prevents localized condensation by distributing absorbed water uniformly, reducing the risk of moisture-induced failure.

C. Thermal Resistance

The structure functions were evaluated using a Power Tester 1500A from Mentor Graphics (currently Siemens EDA) to ensure that the proposed module maintains thermal performance Fig. 16(a) illustrates the setup used to measure the thermal resistance from Q_2 to the baseplate, denoted as $R_{th.Q2}$. The power modules were mounted on a cold plate using fixtures on the top frame with a torque of 0.5 N·m. Each structure function was obtained after the body diode of Q_2 conducted a 13-A current for 30 seconds. The measurements were performed twice; first with an adequate amount of thermal grease (case 1) and then with a minimal amount of the grease (case 2) to distinguish between $R_{\mathrm{th}.Q2}$ and the thermal resistance of the thermal grease, $R_{\mathrm{th}.Gr}$.

Fig. 16(b) and (c) presents the measured structure functions of the full-copper and silicone gel modules, with C_{th} representing their thermal capacitance. The red and black traces correspond to cases 1 and 2, respectively. The measured $R_{\mathrm{th}.Q2}$ of the proposed power module was even slightly lower than that of the full-copper module, although the difference may be within the range of measurement error. These findings confirm that the selective etching of the bottom copper described in Section II-A does not degrade the overall thermal performance.

V. Conclusion

This article proposed a low-CM-noise power module which does not require additional materials or manufacturing processes. A portion of the bottom copper layer was etched and filled with silicone gel during the conventional encapsulation process, resulting in 54.1% reduction in CM capacitance and 5-dBμV reduction in CM noise. Due to the softness, low viscosity, and high surface tackiness of the silicone gel, defects such as cracks, delamination, and unfilled area were not observed in the cross-sections of the proposed module. TCTs comprising a total of 1000 cycles were conducted, and cross-sectional images confirmed that the proposed power module maintains mechanical stability, exhibiting no cracks in the solder layers.

The thermal performance was also verified by simulation and measured structure functions.

REFERENCES

[1] J. Biela, A. Wirthmueller, R. Waespe, M. L. Heldwein, K. Raggl, and J. W. Kolar, "Passive and active hybrid integrated EMI filters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1340–1349, May 2009.

[2] M. Shoyama, G. Li, and T. Ninomiya, "Balanced switching converter to reduce common-mode conducted noise," *IEEE Trans. Ind. Electron.*, vol. 50, no. 6, pp. 1095–1099, Dec. 2003.

[3] S. Wang, P. Kong, and F. C. Lee, "Common mode noise reduction for boost converters using general balance technique," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1410–1416, Jul. 2007.

[4] S. Wang, F. C. Lee, and Q. Li, "Improved balance technique for common-mode noise suppression of PCB-based PFC," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4174–4182, Apr. 2022.

[5] S. Choi, Y. Yin, J. Shin, J. Imaoka, and M. Yamamoto, "Common-mode noise reduction for bridgeless flyback PFC rectifier with balance technique," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2024, pp. 1478–1483.

[6] T. Moaz, N. Rajagopal, C. DiMarino, and M. Fish, "EMI mitigation for SiC MOSFET power modules using integrated common-mode screen," *IEEE Open J. Power Electron.*, vol. 4, pp. 873–886, 2023.

[7] A. Emon, M. Hassan, A. B. Mirza, Z. Yuan, and F. Luo, "EMI propagation path modeling of 3-level T-type NPC power module with stacked DBC enabled EMI shielding," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 5233–5239.

[8] X. Li. et al., "EMI mitigation with stacking DBC substrate for high voltage power module," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–7.

[9] A. Jørgensen et al., "Reduction of parasitic capacitance in 10 kV SiC MOSFET power modules using 3D FEM," in *Proc. IEEE Eur. Conf. Power Electron. Appl.*, 2017, pp. 1–8.

[10] Y. Xie, Z. Huang, C. Chen, and Y. Kang, "An EMI performance improved stacked substrate packaging structure with ultra-low parasitics for SiC half-bridge power module," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, 2019, pp. 1–6.

[11] Y. Zhang et al., "Comprehensive analysis and optimization of parasitic capacitance on conducted EMI and switching losses in hybrid-packaged SiC power modules," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 13988–14003, Nov. 2023.

[12] A. Brovont, A. Lemmon, C. New, B. Nelson, and B. DeBoi, "Analysis and cancellation of leakage current through power module baseplate capacitance," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4678–4688, May 2020.

[13] N. Rajagopal, C. DiMarino, B. DeBoi, A. Lemmon, and A. Brovont, "EMI evaluation of a SiC MOSFET module with organic DBC substrate," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 2338–2344.

[14] Q. Yang, L. Wang, Z. Qi, X. Lu, Z. Ma, and F. Yang, "Analysis and optimization of high-frequency switching oscillation conducted CM current considering parasitic parameters based on a half-bridge power module," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12659–12674, Oct. 2023.

[15] J. Shin, C. Wang, and E. Dede, "Power semiconductor module with low-permittivity material to reduce common-mode electromagnetic interference," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10027–10031, Dec. 2018.

[16] S. Choi, J. Choi, T. Warnakulasooriya, J. Shin, J. Imaoka, and M. Yamamoto, "Power module with low common-mode noise and high reliability," *IEEE Access*, vol. 12, pp. 90929–90939, 2024.

[17] S. Choi, J. Choi, T. Warnakulasooriya, J. Shin, J. Imaoka, and M. Yamamoto, "Improved packaging of power module with low-permittivity material for low common-mode noise and high reliability," *IEEE Trans. Power Electron.*, vol. 39, no. 11, pp. 14261–14270, Nov. 2024.

[18] S. Choi, J. Choi, J. Shin, Y. Yonezawa, J. Imaoka, and M. Yamamoto, "SiC power module design with a low-permittivity material to reduce common-mode noise," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2024, pp. 1472–1477.

[19] X. Li, Y. Chen, H. Chen, R. Paul, X. Song, and H. A. Mantooth, "A 10kV SiC MOSFET power module with optimized system interface and electric field distribution," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 9540–9553, Aug. 2024.

[20] European Center for Power Electronics (ECPE) Guideline AQG324, "Qualification of Power Modules for Use in Power Electronics Converter Units in Motor Vehicles," *Release no. 04.1/2025*, pp. 38 41, Mar. 2025. [Online] Available: https://www.ecpe.org/research/workinggroups/automotive-aqg-324/

[21] Y. Xu and D. C. Hopkins, "Misconception of thermal spreading angle and misapplication to IGBT power modules," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, pp. 545–551, 2014.

[22] D. Dalal et al., "Impact of power module parasitic capacitances on medium-voltage SiC MOSFETs switching transients," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 298–310, Mar. 2020.

[23] N. Jia, L. Xue, and H. Cui, "Mitigating EMI noise in propagation paths: Review of parasitic and coupling effects in power electronic packages, filters, and systems," *IEEE Open J. Power Electron.*, vol. 5, pp. 352–368, 2024.

Sihoon Choi (Member, IEEE) received the B.S. degree in energy systems engineering from Chung-Ang University, Seoul, South Korea, in 2019, and the M.S. and Ph.D. degrees in electrical engineering from Nagoya University, Nagoya, Japan, in 2022 and 2025, respectively.

He was an Associate Research Engineer with Automotive Power Development Team, LG Innotek, Seoul, South Korea, from 2019 to 2020. Since 2025, he has been a Designated Assistant Professor with Institute of Materials and Systems for Sustainability, Nagoya University. His research interests include power module packaging, passive components, and electromagnetic interference.

Jiyoon Choi (Student Member, IEEE) received the B.S. degree in electrical engineering, electronics, and information engineering in 2023 from Nagoya University, Nagoya, Japan,, where she is currently working toward the M.S. degree in electrical engineering.

Her research interest includes SiC power module packaging.

Thiyu Warnakulasooriya (Student Member, IEEE) received the B.Eng. degree in electrical engineering, electronics, and information engineering, and the M.Eng. degree in electrical engineering in 2022, and 2024, respectively, from the Nagoya University, Nagoya, Japan, where he is currently working toward the doctorate degree in electrical engineering.

His research interests include SiC power module design and packaging and EMI.

Jong-Won Shin (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 2006 and 2013, respectively.

From 2013 to 2015, he was a Postdoctoral Researcher with Virginia Tech, Blacksburg, VA, USA. From 2015 to 2018, he was a Senior Scientist with the Electronics Research Department, Toyota Research Institute of North America, Ann Arbor, MI, USA. He was an Assistant Professor with Chung-Ang University, Seoul, Korea, from 2018 to 2022 and as an Associate Professor from 2022 to 2024. In 2024, he was with Seoul National University, Seoul, Korea, where he is currently an Assistant Professor with the Department of Electrical and Computer Engineering, a Member of Seoul National University Electric Power Research Institute, and a Member of Seoul National University Energy Initiative. He was a Visiting Associate Professor with Nagoya University, Nagoya, Japan, from 2021 to 2024. His research interests include power conversion, energy management, and power semiconductor packaging.

Jun Imaoka (Member, IEEE) received the M.S. and Ph.D. degrees in electronic function and system engineering from Shimane University, Matsue, Japan, in 2013 and 2015, respectively.

From 2015 to 2018, he was with Kyushu University, Fukuoka, Japan, as an Assistant Professor. From 2018 to 2021, he was an Assistant Professor with Nagoya University, Nagoya, Japan. He is currently an Associate Professor with the Institute of Materials and Systems for Sustainability, Nagoya University. His research interests include the design of integrated magnetic components, modeling for high-power-density power converters, thermal management for power converters, magnetic material application, and EMI of switching power supply.

Masayoshi Yamamoto (Member, IEEE) received the M.S. and Ph.D. degree in science and engineering from Yamaguchi University, Yamaguchi, Japan, in 2000 and 2004 respectively.

From 2004 to 2005, he was with Sanken Electric Company Ltd., Saitama, Japan. From 2006 to 2017, he was with the Interdisciplinary Faculty of Science and Engineering with Shimane University, Matsue, Japan, as an Associate Professor. He is currently a Professor with the Institute of Materials and Systems for Sustainability, Nagoya University, Nagoya Japan. His research interests include automotive power electronics, power module packaging, EMI of switching power supply, and wireless power transfer.