Unified Fault Ride-Through Capability-Based Resilience-Aware Metrics for Grid-Forming Inverter-Based Systems

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***Abstract*—Various fault ride-through (FRT) strategies have been proposed to constrain the maximum current during faults to levels below predefined thresholds for grid-forming (GFM) inverters, as current limiting is the primarily required FRT capability due to its direct impact on the security of inverter semiconductors and the resilience of power systems. In addition, the latest IEEE standards and grid codes also mandate other FRT capabilities in terms of voltages, currents, and powers to further enhance the safety, stability, and resilience of power systems. However, few existing studies have comprehensively summarized these FRT capabilities and proposed effective quantification metrics to assess them. To address these gaps, this article presents a thorough summary of the FRT capabilities of GFM inverters and introduces a set of quantification metrics to completely evaluate these capabilities, which can also indirectly quantify the FRT capabilities' impacts on power system resilience. These metrics not only enable real-time tracking but also provide a quantitative basis for comparing distinct FRT capabilities across various FRT control strategies. Furthermore, this article also proposes a comprehensive metric that integrates the weighted contributions of all proposed quantification measures to guide the selection of the most appropriate FRT strategy. Finally, experiments in a single GFM inverter system and simulations in large-scale power systems involving four FRT strategies demonstrate the effectiveness of the proposed quantification metrics in assessing the FRT capabilities and identifying the most suitable FRT strategy of GFM inverters under grid fault conditions.**

***Index Terms*—Fault ride-through (FRT), grid-forming (GFM) inverters, quantification metric, resilience.**

I. Introduction

THE resilience of a power grid can be interpreted as its ability to withstand and rapidly recover from disruptive events, whether high-probability, low-impact occurrences, such as component failures, or low-probability, high-impact incidents, such as natural disasters or coordinated cyberattacks [1].

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To enhance grid resilience and combat global warming, distributed energy resources (DERs), such as wind turbines and solar photovoltaics, are widely integrated into modern power systems through voltage source converters (VSCs) [2]. These VSCs are primarily controlled as grid-following (GFL) inverters, which behave as current sources and synchronize with grids via phase-locked loops (PLLs). However, due to the adverse effects of PLLs caused by high grid impedance, GFL inverters often face stability issues in weak grids [3]. In contrast, grid-forming (GFM) inverters, another way the VSCs can be controlled as, operate stably against weak grids since they are controlled as voltage sources and independently regulate their output voltages and frequencies [4]. Strengthening the resilience of power grids is another major benefit of GFM inverters since their voltage and frequency support capabilities allow them to serve as power sources in standalone mode when the utility grid is disrupted. Moreover, GFM inverters can be configured as virtual synchronous generators (SGs) to enhance system inertia. Consequently, these advantages render GFM inverters highly preferable and widely incorporated into modern power grids to improve the security and resilience of power systems [5], [6].

Unfortunately, GFM inverters are not without their own limitations, particularly their high susceptibility to overcurrent damage, caused by grid faults [7]. Unlike conventional generation devices, such as SGs that can tolerate 5–10 times the rated current, GFM inverters are limited by the thermal inertia of their semiconductors and can only withstand 1–1.5 times their rated current [1], [4], [8]. Traditionally, tripping these inverters during grid faults could be an effective solution to ensure the safety and stability of power systems. Yet, in today's network where inverter-based DERs constitute an increasing share of generation, forcing these devices offline can trigger or accelerate cascading failures, significantly deteriorating overall grid resilience. To this end, modern grid codes require inverters to stay online during faults, a capability known as fault ride-through (FRT), to prevent cascaded disturbances and potential blackouts [5], [6], [9], [10]. In response, numerous adaptive FRT strategies have been proposed for GFM inverters to improve system performance during faults [4], [7]. However, a systematic framework for evaluating how these strategies affect grid resilience is still lacking. Prior work largely develops resilience metrics for permanent failures (e.g., device outages [11]) and on the sustained impacts of cyberinduced physical

disruptions [12], [13], or proposes resilient control strategies for such failures [14], [15]. Our contribution in this article is a systematic way to assess how FRT capabilities affect resilience during transient faults.

Presently, the primary objective of FRT strategies for GFM inverters is to constrain inverter output currents within the maximum allowable current magnitude (MACM), as this current limiting capability directly impacts the thermal safety of inverter semiconductors. Consequently, various FRT strategies, known as current-reference-limiting controls (CRLCs), have been developed to enhance this capability by directly regulating current references during faults [16], [17]. However, existing studies typically evaluate current-limiting capability based on the peak values of output currents exceeding the MACM during faults, which neglects the temporal behavior of overcurrent peaks and fails to effectively account for multiple overcurrent peaks [16], [18]. Furthermore, by limiting current references at the MACM, CRLCs enable GFM inverters to effectively utilize the current support (overcurrent) capability [19], [20], thereby enhancing fault detection [8], [9], [19], [20], [21]. Nevertheless, this capability has yet to be assessed by existing research.

In addition, recent grid codes require GFM inverters to achieve the voltage support capability, which entails maintaining normal voltage levels during faults [8], [22], [23]. This requirement aims to enhance power system stability by preventing device disconnections and mitigating cascading failures caused by undervoltage conditions. However, CRLCs may compromise voltage support capability, as they typically emulate resistive virtual impedance (VI) during grid faults [23]. In contrast, voltage-reference-limiting controls regulate voltage references to indirectly limit output currents while maintaining voltage source characteristics, thus improving voltage support capability [8], [23]. Despite the importance of this function, few studies have proposed effective quantification metrics to evaluate voltage support performance during fault conditions.

In addition to the voltage support capability, voltage limiting capability also plays a crucial role in ensuring the safety of metering equipment and customer loads by constraining maximum voltage magnitudes during faults. Furthermore, this capability ensures controlled and stable recovery after faults, helping to prevent secondary issues (e.g., overvoltage collapses) that could initiate cascading failures. Besides, IEEE Standard 2800-2022 and various grid codes specify the voltage magnitude limits for inverters during grid faults, aiming to enhance security and resilience of power systems [9], [10], [24]. However, existing quantification metrics have yet to comprehensively evaluate this capability in boosting the resilience.

Moreover, the latest IEEE Standard 2800-2022 mandates that inverter-based DERs should operate in either active or reactive power priority mode, as determined by system operators [24]. Insufficient active or reactive power support can also lead to cascading failures. Reactive power support contributes to voltage recovery and prevents cascading undervoltage [8], [23], whereas active power support mitigates frequency dips and enhances the active power–power angle relationship [7], [24]. Nonetheless, these two capabilities are rarely incorporated into the assessment of existing FRT strategies, and corresponding quantification metrics remain underdeveloped.

In summary, to ensure inverter safety and maintain power system stability, FRT strategies are expected to fulfill the above-mentioned multiple essential capabilities for GFM inverters [5], [6]. These capabilities directly impact the thermal safety of inverters and stability of power systems, and thus be regarded as indicators of overall power system resilience. However, to the best of our knowledge, few existing studies have systematically summarized these capabilities or developed comprehensive quantification metrics to assess them. To address these gaps, this article introduces a unified set of quantification metrics to assess the key FRT capabilities of GFM inverters. These metrics serve as resilience assessment tools by quantifying the inverter's capability to remain online and to reduce the potential risk of cascading failures. Specifically, the voltage limiting quantification metric assesses voltage limiting capability by calculating overvoltage areas that exceed the continuous voltage ride-through threshold after fault occurrence and the nominal voltage magnitude after fault clearance. The voltage support quantification metric evaluates voltage support capability through positive- and negative-sequence voltage magnitudes. Similarly, the current limiting quantification metric measures current limiting capability by identifying overcurrent areas that exceed MACM after fault occurrence and the nominal current magnitude after fault clearance. The current support metric measures the maximum current magnitude during faults, reflecting inverters' current support capability. Finally, the power support quantification metrics calculate the average active and reactive powers during faults to assess active and reactive power support capabilities. The contributions of the proposed unified set of resilience-aware quantification metrics are summarized as follows.

1) This article is the *first* to propose a unified set of resilience-aware quantification metrics to assess various FRT capabilities of GFM inverters for different control strategies, aligning with the latest grid code requirements. The practical limits for each metric are also calculated based on grid codes to enhance their practicality. Moreover, a weighted comprehensive metric is proposed to identify the most appropriate FRT strategy, thereby laying the groundwork for assessing overall power system resilience.
2) The proposed metrics can be calculated in real-time, enabling dynamic monitoring of a system's FRT performance. In addition, they highlight the strengths of different FRT strategies, providing practical insights for enhancing existing strategies based on specific metrics.
3) The proposed metrics can be applicable to various FRT strategies under various grid fault scenarios and system parameters. Their effectiveness is experimentally validated across multiple fault severities. Furthermore, the metrics are applied to both experimental tests in a single GFM inverter system and simulations in a large-scale power system, demonstrating their generality and practicality for both metric evaluation and strategy selection.

II. Limitation of Conventional FRT Capability Evaluation

To examine the limitations of conventional FRT capability evaluation, this article takes adaptive virtual impedance (AVI)

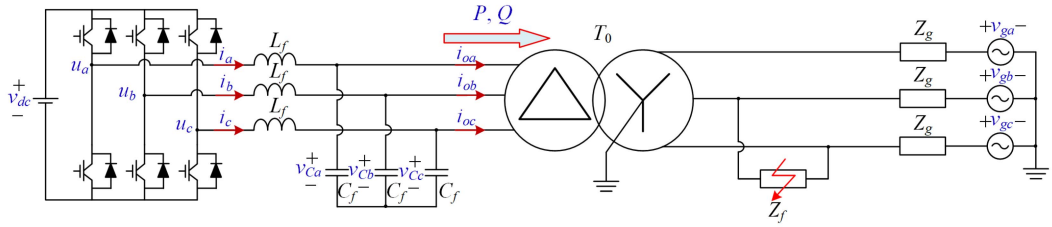

Fig. 1. Circuit diagram of a three-phase grid-connected GFM inverter under an LL fault.

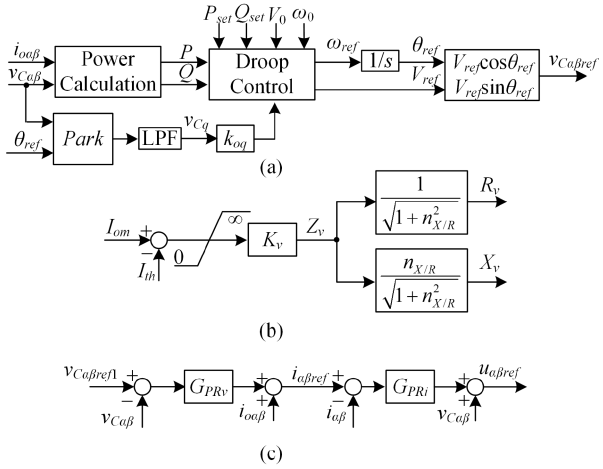

Fig. 2. Block diagrams of AVI. (a) Outer-loop control. (b) Implementation of AVI. (c) Inner-loop control.

as an example, as it is widely utilized as an FRT strategy for GFM inverters [25]. Fig. 1 depicts the circuit diagram of a grid-connected GFM inverter under a line-to-line (LL) fault, where Z_f denotes the fault impedance, L_f denotes the inverter-side filter inductance, and C_f denotes the filter capacitance. In addition, T_0 denotes the delta-wye transformer; Z_f and Z_g denote the fault impedance and grid impedance, respectively; v_{dc}, u_{abc}, v_{Cabc}, and v_{gabc} denote the dc-link voltage, the inverter terminal voltage, the capacitor voltage, and the grid voltage, respectively; i_{abc} and i_{oabc} denote the filter and output currents, respectively; P and Q denote the active and reactive powers, respectively.

Fig. 2 illustrates the control block diagrams of AVI. As shown in Fig. 2(a), $v_{C\alpha\beta}$ and $i_{o\alpha\beta}$ respectively denote the capacitor voltage and output current in the stationary reference frame (STRF). These variables are derived from the natural reference frame (NRF) through a Park transformation. Also, a typical droop control, as described in [7] and [18], is used to generate voltage and frequency references

$$\begin{cases} \omega_{\text{ref}} - \omega_0 = K_P\left(P_{\text{set}} - P\right) + k_{oq} v_{cq} \\ V_{\text{ref}} - V_0 = K_Q\left(Q_{\text{set}} - Q\right) \end{cases} \tag{1}$$

where V_{ref} and ω_{ref} denote voltage magnitude reference and angular frequency reference, respectively; V_0 and ω_0 denote the nominal voltage magnitude and angular frequency, respectively; P_{set} and Q_{set} denote the setting active power and reactive power, respectively; and K_P and K_Q denote P–f droop gain and Q–V droop gains, respectively. Furthermore, the transient stability enhancement term $k_{oq}v_{Cq}$ is adopted to ensure the system's transient stability during faults, where k_{oq} is a proportional gain and v_{Cq} is the q-axis capacitor voltage. The design process of k_{oq} has been elaborated in [26] and verified in [7]; thus, it is not introduced in this article. Besides, θ_{ref} denotes the phase angle reference of the voltage reference, and the voltage reference can be expressed as $v_{C\alpha\text{ref}} = V_{\text{ref}}\cos(\theta_{\text{ref}})$ and $v_{C\beta\text{ref}} = V_{\text{ref}}\sin(\theta_{\text{ref}})$.

Fig. 2(b) shows the implementation of AVI, where I_{om} denotes the maximum phase current magnitude; I_{th} denotes the current threshold, beyond which AVI is activated; K_v denotes a proportional gain to generate AVI, Z_v, which are generally designed under symmetrical grid faults [25]; R_v and X_v denote the virtual resistance and reactance, respectively; and $n_{X/R}$ denotes the ratio between the reactance and resistance. Using AVI, the final voltage references can be deduced as

$$\begin{cases} v_{C\alpha\text{ref1}} = v_{C\alpha\text{ref}} - R_v i_{o\alpha} + X_v i_{o\beta} \\ v_{C\beta\text{ref1}} = v_{C\beta\text{ref}} - R_v i_{o\beta} - X_v i_{o\alpha}. \end{cases} \tag{2}$$

As shown in Fig. 2(c), the dual-loop voltage and current vector control is adopted as the inner control to achieve voltage reference tracking, where $G_{\text{PR}v}$ and $G_{\text{PR}i}$ denote the proportional-resonant (PR) voltage and current controllers, respectively. For a more detailed elaboration of this control strategy, readers are referred to [27].

A. Limitation of Conventional Magnitude-Based Metrics in Evaluating Overvoltage and Overcurrent Issues

An LL fault is taken as an example to examine FRT capabilities of AVI, as shown in Fig. 1, where the fault is activated at $t = 2$ s and deactivated at $t = 3$ s. Besides, the system and control parameters are listed in Table I.

The voltage limiting capability of GFM inverters during the fault can be specifically indicated by the overvoltage issues. Fig. 3 shows the simulation waveforms of capacitor voltages, where V_{hth} denotes the high voltage ride-through threshold, defined in IEEE Standard 2800-2022 [24]. As shown in Fig. 3(a), there are two transient overvoltage peaks of 1.21 and −1.3 p.u. around the fault occurrence, which are higher than V_{hth}. These voltage peaks demonstrate that AVI may cause overvoltage issues during grid faults. To optimize AVI or compare different FRT strategies in the voltage limiting capability, it is essential to establish quantification metrics that can fairly and intuitively evaluate the severity of overvoltage issues. Conventionally,

TABLE I
SYSTEM AND CONTROL PARAMETERS

Symbol	Description	Value
S_n	Rated power	500 VA
V_{dc}/V_g	Dc voltage/Grid voltage (LL, rms)	200/104 V
L_f/C_f	Filter inductance/capacitance	3 mH/30 μF
Z_g	Grid impedance	5 mH/1 Ω
R_f	Fault resistance	3.9 Ω
P_{set}/Q_{set}	Setting active/reactive power value	1/0 p.u.
ω_0	Nominal angular frequency	314 rad/s
V_0	Nominal voltage magnitude	85.85 V
I_{th}	Current threshold of adaptive VI	1.0 p.u.
I_M	MACM	1.5 p.u.
ω_c	Cutoff angular frequency	$2\pi 20$ rad/s
K_P/K_Q	P-f/Q-V droop gains	0.01/0.05 p.u.
K_{pv}/K_{rv}	PR gains of voltage control	0.1/80 S
K_{pi}/K_{ri}	PR gains of current control	15/500 Ω
K_{oq}	Proportional gain for transient stability	0.4 rad · V^{-1}
K_v	Proportional gain of adaptive VI	7 Ω · A^{-1}
T_s	Sampling period	100 μs

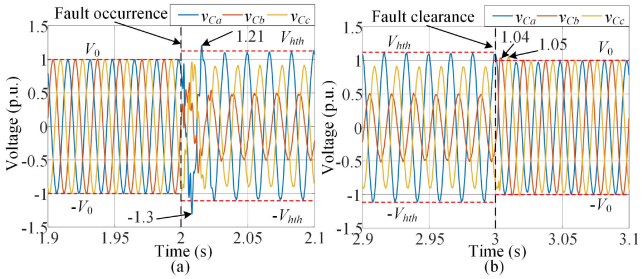

Fig. 3. Simulation waveforms of capacitor voltages under an LL fault. (a) Around fault occurrence. (b) Around fault clearance.

magnitude-based metrics are employed to assess the overvoltage severity for GFM inverters during faults [28]. However, for dynamic overvoltage peaks, which may vary significantly in magnitudes and distribution time, as shown in Fig. 3, the magnitude-based metrics are insufficient to thoroughly evaluate the voltage limiting capability. Likewise, such magnitudes fail to capture the temporal behavior of these overvoltage peaks. Unfortunately, to the best of our knowledge, few comprehensive or effective quantification metrics currently exist for evaluating voltage limiting capability in this context.

Moreover, as shown in Fig. 3(b), two peaks of 1.04 and 1.05 p.u. occur around the fault clearance, which both exceed the nominal voltage magnitude V_0 and approach V_{hth}. These voltage peaks are expected to quickly recover to nominal values to ensure the safety of devices and the stability of power systems [6], [16]. However, few quantification metrics have yet been developed to assess the behavior of these voltage peaks during fault clearance. Besides, similar to the overvoltage peaks around fault occurrence, magnitude-based metrics alone are insufficient for a comprehensive evaluation of the voltage limiting capability after fault clearance.

Similarly, the current limiting capability of GFM inverters during faults can be specifically indicated by the overcurrent issues. Fig. 4(a) shows the simulation waveforms of inverter output currents around the fault occurrence. Three overcurrent peaks of 1.74, 1.64, and −1.56 p.u. are observed, exceeding

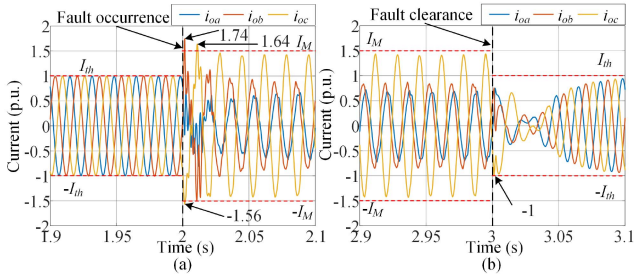

Fig. 4. Simulation waveforms of inverter output currents under an LL fault. (a) Around fault occurrence. (b) Around fault clearance.

MACM I_M. This phenomenon confirms that AVI may cause transient overcurrent issues around fault occurrence. However, the varying magnitudes and complex distribution of these peaks around the fault occurrence make it challenging to evaluate them through magnitude-based metrics.

Furthermore, Fig. 4(b) shows the simulation waveforms of the inverter output currents around the fault clearance. A current peak of −1 p.u. is observed, which is close to the nominal current magnitude (I_{th}, current threshold). This phenomenon indicates that AVI performs well in current recovery without causing overcurrent issues. However, for other FRT strategies, high current peaks that exceed I_{th} may be observed around fault clearance. Therefore, it is also crucial to establish a quantification metric to evaluate the current limiting capability around fault clearance.

In summary, magnitude-based metrics are insufficient to evaluate voltage and current limiting capabilities around fault occurrence and clearance. Consequently, advanced quantification metrics should be established to address these challenges.

B. Neglecting Evaluation of Voltage, Current, and Power Support Capabilities

In addition to evaluating the voltage limiting capability during faults, the voltage support capability of GFM inverters should also be evaluated, as it is essential for ensuring the stability and resilience of power systems [6], [24]. In addition, as shown in Fig. 4, the steady-state maximum current magnitude during faults is 1.44 p.u., which is lower than I_M, indicating that the current support capability of GFM inverters is not fully optimized for AVI. Furthermore, IEEE Standard 2800-2022 has defined either active or reactive power support capability for inverter-based resource units, in response to the needs of system operators. Nevertheless, to the best of authors' knowledge, few effective quantification metrics have yet been developed to systematically assess these FRT capabilities that affect resilience.

Consequently, comprehensive quantification metrics must be established to thoroughly evaluate the voltage, current, and power support capabilities. In the next section, these capabilities will be fully elaborated, and the corresponding quantification metrics will be introduced.

III. FRT CAPABILITY-BASED RESILIENCE METRICS

The capabilities related to regulating voltages, currents, and powers across various FRT strategies have a direct impact

on the security and stability of GFM inverters and affect the resilience of power systems. To quantify how various FRT strategies impact the grid's resilience, it is critical to define a set of metrics capable of capturing their performance during different phases following a fault. This section first introduces two types of voltage-based metrics: voltage-limiting capability-based and voltage-support capability-based metrics. The voltage-limiting capability-based metric is designed to quantify how long overvoltage conditions can be sustained, and voltage-support capability-based metric is employed to assess the inverter's ability to maintain prefault voltage levels. Subsequently, current-based metrics, including current-limit capability-based and current-support capability-based metrics, are developed. The current-limiting metric serves as an indicator of thermal stress on system components, preventing overheating and potential tripping. The current-support metric indicates the overcurrent capability of inverters during faults. Furthermore, active and reactive power-based metrics are introduced to evaluate how effectively FRT capabilities manage power injection. These metrics will provide a structured and quantitative means to assess key FRT capabilities that contribute to resilience.

A. *Voltage-Based Metrics*

Overvoltage issues can result in overheating and insulation damage in DERs [29]. In addition, they can also threaten metering equipment and customer loads, thereby reducing the resilience of power systems [30]. Given this, voltage limiting during grid faults is a crucial FRT capability for the safety and resilience of power systems. To evaluate voltage limiting capability as well as overvoltage severity for GFM inverters during grid faults, a corresponding resilience-aware quantification metric should be established.

IEEE Standard 2800-2022 mandates the upper voltage threshold, V_{hth} (1.1 p.u.), for DERs, which operate in continuous operation mode during faults [24]. In addition, the severity of overheating and insulation damage is related to both the magnitude and duration of overvoltage peaks. Hence, as shown in Fig. 5(a), the overvoltage areas S_{VFO} are utilized to indicate the voltage limiting capability after fault occurrence. Moreover, voltages are expected to quickly recover after fault clearance to the nominal voltage V_0 to ensure the safety of devices and the stability of power systems [6], [16]. Finally, as shown in Fig. 5(b), the overvoltage areas S_{VFC} are used to reflect the voltage limiting capability after fault clearance. Accordingly, the voltage limiting capability-based resilience-aware metrics after fault occurrence and clearance are respectively defined as

$$S_{\text{VFO}} = \begin{cases} \displaystyle\int_{t_0}^{t_1} \frac{|v_{Cabc}| - V_{\text{hth}}}{V_0}\, dt, & |v_{Cabc}| \geq V_{\text{hth}} \\ 0, & |v_{Cabc}| < V_{\text{hth}} \end{cases}$$

$$[1.2em] S_{\text{VFC}} = \begin{cases} \displaystyle\int_{t_1}^{t_2} \frac{|v_{Cabc}| - V_0}{V_0}\, dt, & |v_{Cabc}| \geq V_0 \\ 0, & |v_{Cabc}| < V_0 \end{cases} \tag{3}$$

where S_{VFO} and S_{VFC} denote the voltage limiting quantification metrics after fault occurrence and clearance, respectively. t_0, t_1, and t_2 denote the fault occurrence instant, fault clearance instant, and the next fault occurrence instant, respectively. Specially, smaller values of S_{VFO} and S_{VFC} indicate less severe overvoltage issues and better voltage limiting capability. This reflects a stronger ability to mitigate the risk of cascading failures caused by inverter tripping due to overvoltage, thereby enhancing grid resilience.

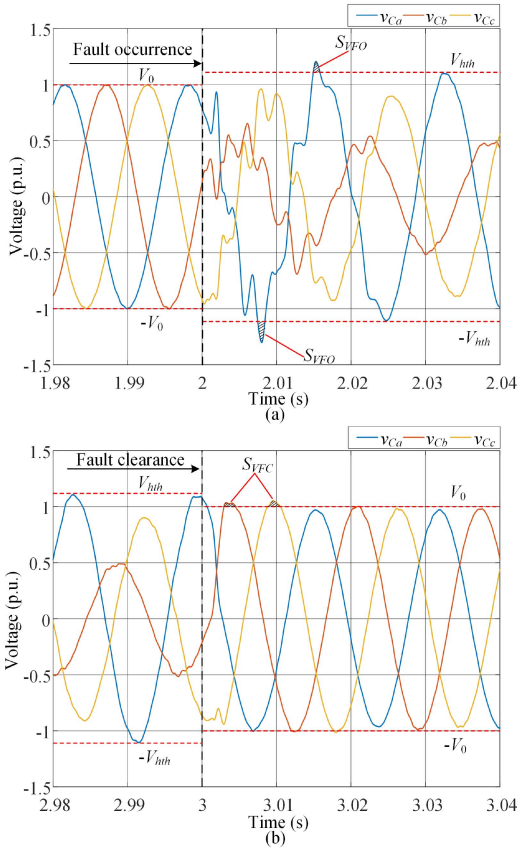

Fig. 5. Illustration of voltage limiting quantification metric for capacitor voltages under an LL fault. (a) Around fault occurrence. (b) Around fault clearance.

In addition, according IEEE Standard 2800 [24], DERs may trip if the voltage exceeds the voltage ride-through threshold V_{hth} and lasts for 10 s. The maximum voltage ride-through voltage is 1.2 p.u., as defined in IEEE Standard 2800. Therefore, the upper bound of the voltage-limiting metric (S_{VFOmax}), is calculated accordingly as 3.71. Although IEEE Standard 2800 does not specify a strict time limit for voltage recovery, it requires that active power must recover within 1 s following a disturbance. This 1 s interval can be reasonably used as the upper limit for voltage recovery time. Combined with the maximum ride-through voltage of 1.2 p.u., the upper bound of the voltage-limiting metric (S_{VFCmax}) is determined as 0.34.

To enable real-time evaluation of the voltage-limiting quantification metric, its discrete calculation process is shown in Algorithm 1. FaultEN denotes a fault detection signal, which becomes 1 after fault occurrence and 0 after fault clearance. This fault detection can be simply implemented through measuring the minimum capacitor voltage magnitude. In addition, A_{VFO}

Algorithm 1: Voltage Limiting Metric Calculation.

Input: $v_{Ca}, v_{Cb}, v_{Cc}, V_{hth}, V_0, T_s$, FaultEN
Initialize persistent variables:
  A_{VFO}, A_{VFC}
if A_{VFO} *is empty* **then**
  $A_{VFO} \leftarrow 0$
end
% Initialize other persistent variables similarly if empty
if FaultEN $== 0$
  $\Delta V_{CA} = |v_{Ca}| - V_0$, **if** $\Delta V_{CA} < 0, \Delta V_{CA} = 0$ **end**
  $\Delta V_{CB} = |v_{Cb}| - V_0$, **if** $\Delta V_{CB} < 0, \Delta V_{CB} = 0$ **end**
  $\Delta V_{CC} = |v_{Cc}| - V_0$, **if** $\Delta V_{CC} < 0, \Delta V_{CC} = 0$ **end**
  $A_{VFO} = 0$
  $A_{VFC} = A_{VFC} + (\Delta V_{CA} + \Delta V_{CB} + \Delta V_{CC}) T_s$
  $S_{VFO} = A_{VFO}/V_{hth}, S_{VFC} = A_{VFC}/V_0$
else
  $\Delta V_{CA} = |v_{Ca}| - V_{hth}$, **if** $\Delta V_{CA} < 0, \Delta V_{CA} = 0$ **end**
  $\Delta V_{CB} = |v_{Cb}| - V_{hth}$, **if** $\Delta V_{CB} < 0, \Delta V_{CB} = 0$ **end**
  $\Delta V_{CC} = |v_{Cc}| - V_{hth}$, **if** $\Delta V_{CC} < 0, \Delta V_{CC} = 0$ **end**
  $A_{VFC} = 0$
  $A_{VFO} = A_{VFO} + (\Delta V_{CA} + \Delta V_{CB} + \Delta V_{CC}) T_s$
  $S_{VFO} = A_{VFO}/V_{hth}, S_{VFC} = A_{VFC}/V_0$
end
Output: S_{VFO}, S_{VFC}

and A_{VFC} denote the overvoltage areas after fault occurrence and clearance, respectively. This algorithm can be executed in each control period, allowing the voltage limiting quantification metrics S_{VFO} and S_{VFC} to be calculated in real time.

Similarly, voltage support is another crucial FRT capability, as it is beneficial in maintaining voltage stability during faults and enhancing grid voltage recovery after fault clearance, thereby improving the resilience of power systems [31], [32]. To enhance voltage support capability, for symmetrical grid faults, the voltage magnitude should be maximized, while for asymmetrical grid faults, the positive-sequence voltage magnitude should be maximized, and the negative-sequence voltage magnitudes should be minimized [33]. To quantify voltage support capability under both symmetrical and asymmetrical grid faults, a voltage support capability-based resilience-aware quantification metric that considers positive- and negative-voltage magnitudes is proposed as

$$V_{\mathrm{VS}} = \frac{V_{Cp} - V_{Cn}}{V_0} \tag{4}$$

where V_{Cp} and V_{Cn} denote the positive- and negative-sequence voltage magnitudes, respectively. The larger this voltage support metric is, the stronger the voltage support capability. According to the U.K. grid code modification GC0137 [22], the voltage during faults is expected to maintain the prefault level. Consequently, the maximum value of the voltage support metric (V_{VSmax}) is set to 1.0.

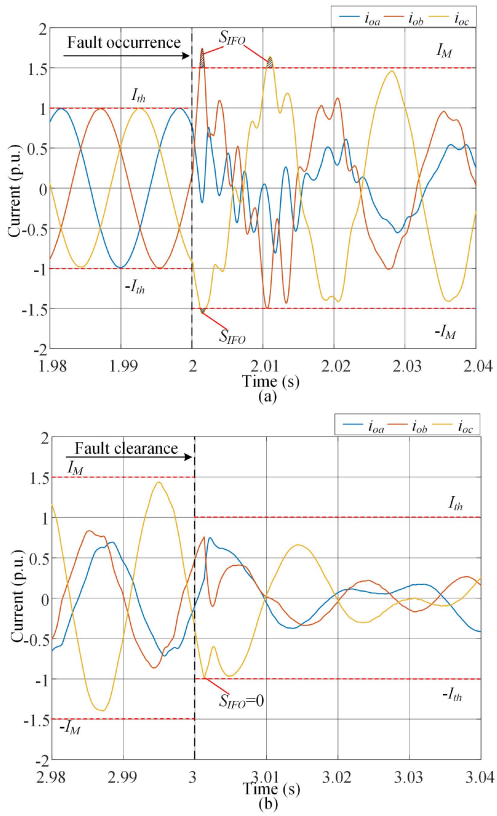

Fig. 6. Illustration of current limiting quantification metric for inverter output currents under an LL fault. (a) Around fault occurrence. (b) Around fault clearance.

B. Current-Based Metrics

Due to the limited thermal inertia of semiconductors, GFM inverters cannot withstand high currents. To prevent overcurrent damage during faults, the dynamic overcurrent peaks after fault occurrence must be constrained below I_M (1.5 p.u. of the rated current), as required in existing studies and grid codes [16], [20], [23]. Furthermore, dynamic overcurrent peaks after fault clearance must be controlled to quickly converge to nominal currents. Otherwise, these dynamic overcurrent peaks will threaten the safety of GFM inverters, thereby reducing the resilience of power systems. As such, current limiting is a critical FRT capability for safety and resilience of power systems. Therefore, to evaluate current limiting capability as well as overcurrent severity for GFM inverters during grid faults, relevant resilience-aware overcurrent quantification metrics should be established.

Similar to overvoltage issues, overcurrent issues are also influenced by the magnitudes of overcurrent peaks and their duration. Hence, the overcurrent areas are employed to reflect the severity of these overcurrent issues. As shown in Fig. 6(a), the overcurrent areas S_{IFO} are utilized to indicate the severity of overcurrent after fault occurrence. In addition, currents are expected to quickly recover after fault clearance to the nominal current I_{th} to ensure the safety of devices [16]. Similarly, as shown in Fig. 6(b), the overcurrent areas S_{IFO} are used to reflect the severity of overcurrent after fault clearance, where $S_{\mathrm{IFO}} = 0$ indicates no overcurrent issue after fault clearance for AVI.

Consequently, the current limiting quantification metrics after fault occurrence and clearance are respectively defined as

$$S_{\text{IFO}} = \begin{cases} \int_{t_0}^{t_1} \dfrac{|i_{oabc}| - I_M}{I_{\text{th}}}\, dt, & |i_{oabc}| \geq I_M \\ 0, & |i_{oabc}| < I_M \end{cases}$$

$$[1.2em] S_{\text{IFC}} = \begin{cases} \int_{t_1}^{t_2} \dfrac{|i_{oabc}| - I_{\text{th}}}{I_{\text{th}}}\, dt, & |i_{oabc}| \geq I_{\text{th}} \\ 0, & |i_{oabc}| < I_{\text{th}} \end{cases} \tag{5}$$

where S_{IFO} and S_{IFC} denote the current limiting quantification metrics after fault occurrence and clearance, respectively, t_0, t_1, and t_2 denote the fault occurrence instant, fault clearance instant, and the next fault occurrence instant, respectively. Particularly, smaller values of S_{IFO} and S_{IFC} imply less severe overcurrent issues and better current limiting capability, which reduces thermal stress on components, thus preventing overheating and eventual tripping.

The allowable overcurrent duration is mainly determined by the thermal inertia of semiconductor devices. According to literature [34], the typical duration ranges from several tens to a few hundred milliseconds. In addition, as noted in [9], short-circuit current contributions from GFM inverters are typically limited to 4–6 p.u. for short durations (< 10 cycles). For longer durations, grid codes and literature (e.g., [20], [23]) suggest a current magnitude of 1.5 p.u. as acceptable. Therefore, the maximum value of the current-limiting metric (S_{IFOmax}) is 0.43. Postfault, no explicit overcurrent duration limit is specified in the standards. Referring again to the 1-s active power recovery requirement in IEEE 2800, the overcurrent duration is set to 1 s, and the maximum current magnitude remains at 1.5 p.u. Accordingly, the maximum value of the current-limiting metric (S_{IFCmax}) is 0.4

To enable real-time assessment of the discrete current limiting quantification metric, its calculation is shown in Algorithm 2, in which FaultEN is the same signal as in Algorithm 1. As per Algorithm 2, A_{IFO} and A_{IFC} denote the overcurrent areas after fault occurrence and clearance, respectively. A_{IFF} denotes the areas where inrush currents exceed MACM at the instant of fault occurrence, prior to fault detection. Similar to Algorithm 1, the current limiting quantification metrics S_{IFO} and S_{IFC} also offer the real-time characteristic.

Moreover, grid codes require GFM inverters to maximize their overcurrent capacity during faults to enhance voltage support capability [8], [19], [20], [21]. In addition, high fault currents are also required by grid codes for fault detection [9], [21]. As such, the current support capability (overcurrent capacity) is considered as an important factor influencing the resilience of power systems. To indicate the current support capability, a resilience-aware current support quantification metric is proposed as

$$I_{\text{CS}} = \frac{I_{om}}{I_{\text{th}}} \tag{6}$$

where a higher I_{CS} indicates a stronger current support capability, with the caveat that I_{CS} should not exceed I_M/I_{th} in case of overcurrent issues. Grid codes require GFM inverters to fully utilize their overcurrent capacity during grid faults to support voltage stability [21]. Therefore, the maximum value of the current support metric (I_{CSmax}) is set to 1.5.

Algorithm 2: Current Limiting Metric Calculation.

Input: $i_{oa}, i_{ob}, i_{oc}, I_{th}, I_M, T_s$, FaultEN
Initialize persistent variables:
  $A_{IFO}, A_{IFC}, A_{IFF}$
if A_{IFO} *is empty* **then**
  $A_{IFO} \leftarrow 0$
end
% Initialize other persistent variables similarly if empty
if FaultEN $== 0$
  $\Delta I_{OA} = |i_{oa}| - I_{th}$, **if** $\Delta I_{OA} < 0, \Delta I_{OA} = 0$ **end**
  $\Delta I_{OB} = |i_{ob}| - I_{th}$, **if** $\Delta I_{OB} < 0, \Delta I_{OB} = 0$ **end**
  $\Delta I_{OC} = |i_{oc}| - I_{th}$, **if** $\Delta I_{OC} < 0, \Delta I_{OC} = 0$ **end**
  $\Delta I_{FA} = |i_{oa}| - I_M$, **if** $\Delta I_{FA} < 0, \Delta I_{FA} = 0$ **end**
  $\Delta I_{FB} = |i_{ob}| - I_M$, **if** $\Delta I_{FB} < 0, \Delta I_{FB} = 0$ **end**
  $\Delta I_{FC} = |i_{oc}| - I_M$, **if** $\Delta I_{FC} < 0, \Delta I_{FC} = 0$ **end**
  $A_{IFO} = 0$
  $A_{IFC} = A_{IFC} + (\Delta I_{OA} + \Delta I_{OB} + \Delta I_{OC}) T_s$
  $A_{IFF} = A_{IFF} + (\Delta I_{FA} + \Delta I_{FB} + \Delta I_{FC}) T_s$
  $S_{IFO} = A_{IFO}/I_M, S_{IFC} = A_{IFC}/I_{th}$
else
  $\Delta I_{OA} = |i_{oa}| - I_M$, **if** $\Delta I_{OA} < 0, \Delta I_{OA} = 0$ **end**
  $\Delta I_{OB} = |i_{ob}| - I_M$, **if** $\Delta I_{OB} < 0, \Delta I_{OB} = 0$ **end**
  $\Delta I_{OC} = |i_{oc}| - I_M$, **if** $\Delta I_{OC} < 0, \Delta I_{OC} = 0$ **end**
  $A_{IFC} = 0$
  $A_{IFO} = A_{IFO} + (\Delta I_{OA} + \Delta I_{OB} + \Delta I_{OC}) T_s$
  $S_{IFO} = (A_{IFO} + A_{IFF})/I_M, S_{IFC} = A_{IFC}/I_{th}$
end
Output: S_{IFO}, S_{IFC}

C. Power-Based Metrics

In most scenarios, reactive power is preferred and should be provided by DERs to ensure voltage support during grid faults [8], [21], [23], [33]. Nevertheless, the latest IEEE Standard 2800-2022 specifies that inverter-based resource units should operate in either active or reactive current priority mode, depending on the needs of system operators [7], [24]. In addition, active power can enhance the P-δ relationship of the GFM inverters that synchronize with power grids via active power control [7]. Therefore, both active and reactive powers are crucial for the resilience of power systems, with their priority and importance determined by system operators. As a consequence, the power support quantification metrics for active and reactive power support capabilities are respectively defined as

$$P_F = \frac{\bar{P}}{S_n}, Q_F = \frac{\bar{Q}}{S_n} \tag{7}$$

where $\bar{P}$ and $\bar{Q}$ denote the average active and reactive powers during grid faults, respectively. And larger values of P_F and Q_F indicate stronger active and reactive power support capabilities. The active and reactive power injection from DERs is inherently limited by the rated apparent power of the inverter. Hence, the

TABLE II
FRT CAPABILITIES AND THEIR CORRESPONDING METRICS, PRIORITY RATINGS, AND WEIGHTING FACTORS

FRT capability	Metric	Value preference	Priority rating	Weighting factor
Current-limiting	S_{IFO} , S_{IFC}	Smaller value preferred	⋆⋆⋆⋆	W_4
Voltage-limiting	S_{VFO} , S_{VFC}	Smaller value preferred	⋆⋆⋆	W_3
Voltage-support	V_{VS}	Larger value preferred	⋆⋆	W_2
Reactive power-support	Q_F	Larger value preferred	⋆⋆	W_2
Current-support	I_{CS}	Larger value preferred	⋆	W_1
Active power-support	P_F	Larger value preferred	⋆	W_1

upper bounds of the active power support metric ($P_{F\text{max}}$) and reactive power support metric ($Q_{F\text{max}}$) are both set to 1.0.

D. Comprehensive Metric

Although the voltage-based, current-based, and power-based metrics can individually provide intuitive insights into various aspects of FRT performance, it remains challenging to directly identify the most suitable FRT strategy from these separate indicators. To address this issue, a unified comprehensive metric is proposed, which consolidates all the individual metrics by assigning appropriate weighting factors according to their relative significance for system safety, stability, and resilience. Table II summarizes the detailed classification of FRT capabilities, the corresponding evaluation metrics, the preferred direction of each metric based on their definition (i.e., whether a larger or smaller value represents better performance), their priority levels, and the associated weighting factors.

Among these capabilities, the current-limiting function is regarded as the most critical. This is because it directly safeguards inverter hardware integrity by restricting output currents within the permissible ratings of semiconductor devices [20], [23]. The second priority is assigned to voltage-limiting capability, which ensures that voltage magnitudes remain within acceptable thresholds, thereby preventing overstress of metering devices and protecting end-user equipment [29], [30]. Although overvoltage incidents are relatively less frequent compared to overcurrent conditions, their impact on equipment safety remains significant.

The third level of importance is attributed to voltage support capability, typically realized through reactive power injection. This functionality contributes to maintaining system voltage stability during fault events and facilitates postfault voltage recovery, thereby strengthening the overall resilience of the grid [31], [32]. Furthermore, current support capability, which enhances the inverter's fault current contribution, is recognized as a supplementary function. While it indirectly benefits voltage support and assists in fault detection, its direct impact on inverter or system safety is comparatively limited, and thus it is assigned a lower priority. Finally, active power support during faults, although potentially beneficial for frequency stability in some scenarios, has relatively lower application probability under existing grid codes [24]. Therefore, both active power support and current support are given the lowest priority rating.

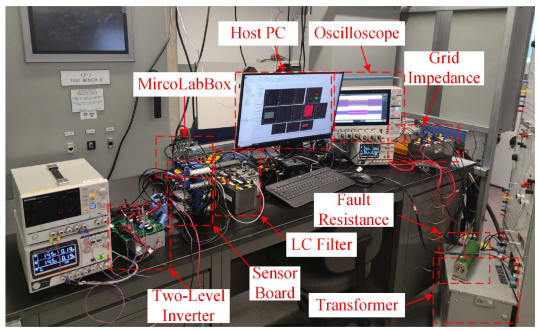

Fig. 7. Experiment setup of the grid-connected GFM inverter.

Based on these priority assignments, weighting factors are systematically allocated. Nevertheless, these values can be adapted to comply with specific grid code requirements in different regions or operational contexts. Using the defined weighting factors, the comprehensive metric S is formulated as (8) shown at the bottom of this page, where W_4 corresponds to the weighting factors for S_{IFO} and S_{IFC}, W_3 for S_{VFO} and S_{VFC}, W_2 for V_{VS} and Q_F, and W_1 for I_{CS} and P_F. A larger value of S signifies stronger overall FRT capability. Consequently, by comparing the comprehensive metric values, the most appropriate FRT strategy can be directly identified in a quantitative and systematic manner

IV. EXPERIMENT-BASED CASE STUDY OF A GFM INVERTER SYSTEM

This section demonstrates the effectiveness of the proposed resilience-aware metrics by applying them to evaluate four different FRT strategies. The experiment setup is shown in Fig. 7, and the experimental system parameters are identical to those used in the simulations, as listed in Table I. The grid is simulated using an MX30 power supply, while a Keysight power supply provides the dc voltage. The dSPACE MicroLabBox DS1202 serves as the digital controller, and a fault resistance of 3.9 Ω is integrated into or removed from the circuit via a solid-state relay (SSR3-D48100ZK). Finally, an LL fault lasting approximately 2 s is applied to the four strategies to examine the proposed resilience-aware quantification metrics.

A. FRT Strategy Example

As the first representative FRT strategy selected for evaluation, AVI was thoroughly analyzed in Section II. The other

$$S = -W_4\frac{S_{\text{IFO}}}{S_{\text{IFOmax}}} - W_4\frac{S_{\text{IFC}}}{S_{\text{IFCmax}}} - W_3\frac{S_{\text{VFO}}}{S_{\text{VFOmax}}} - W_3\frac{S_{\text{VFC}}}{S_{\text{VFCmax}}} + W_2\frac{V_{\text{VS}}}{V_{\text{VSmax}}} + W_2\frac{Q_F}{Q_{F\text{max}}} + W_1\frac{I_{\text{CS}}}{I_{\text{CSmax}}} + W_1\frac{P_F}{P_{F\text{max}}}. \quad (8)$$

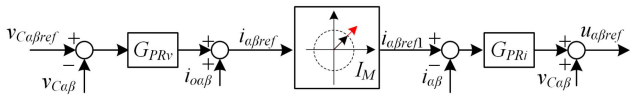

Fig. 8. Block diagram of the CLF.

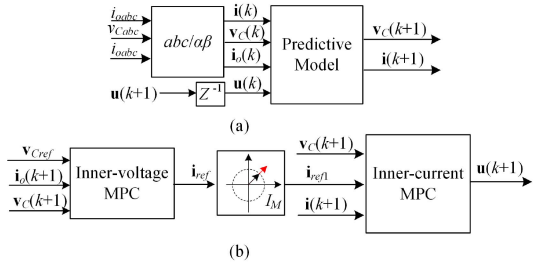

Fig. 9. Block diagram of the MPDCL. (a) Predictive control. (b) Inner voltage and current controls.

three FRT strategies are the current-limiting factor (CLF) [17], the model-predictive dual-control loop (MPDCL) [16], and the active power enhancement control strategy (APECS) [7]. Each strategy has its respective advantages and will be introduced in this section. For a fair comparison, all four strategies utilize the same outer-loop control to generate the voltage and frequency references.

Fig. 8 shows the block diagram of CLF, where the maximum magnitude of filter current references $i_{\alpha\beta\text{ref}}$ is scaled down to I_M in case of overcurrent. Thus, the new filter current references can be calculated as

$$i_{\alpha\beta\text{ref1}} = i_{\alpha\beta\text{ref}} \cdot \min\left\{1, \frac{I_M}{\max\{I_{a\text{ref}}, I_{b\text{ref}}, I_{c\text{ref}}\}}\right\} \quad (9)$$

where $I_{a\text{ref}}$, $I_{b\text{ref}}$, and $I_{c\text{ref}}$ denote the magnitudes of the filter current references in the NRF. Since the CLF directly operates within the current control loop with a high bandwidth, it achieves a significantly fast dynamic response. Furthermore, the maximum magnitude of the filter current references is limited to I_M, ensuring that the current support (maximum current injection) capability is fulfilled.

Fig. 9 illustrates the block diagram of the MPDCL, where all variables are complex vectors in the STRF, e.g., $\mathbf{i}(k) = i_\alpha + ji_\beta$ and $\mathbf{v}_C(k) = v_{C\alpha} + jv_{C\beta}$. Here, k denotes the current time instant, and $k+1$ refers to the next time instant. As shown in Fig. 9(b), the inner-voltage model-predictive control (MPC) realizes accurate voltage reference tracking, while the inner-current MPC achieves precise current reference tracking. Due to the advantages of MPC, both inner-voltage and inner-current loops exhibit high bandwidths. In addition, the CLF is also integrated into the MPDCL to effectively limit overcurrent. As a result, the MPDCL demonstrates outstanding performance in fast current limiting and voltage recovery during faults. For a more detailed explanation of this strategy, refer to [16].

Fig. 10 presents the block diagram of the APECS [7]. On the one hand, as shown in Fig. 10(a), i_{ondq} and $v_{Cndq\text{ref}}$ denote the negative-sequence inverter output currents and capacitor voltage references in the synchronous reference frame. $v_{Cn\alpha\beta\text{ref}}$

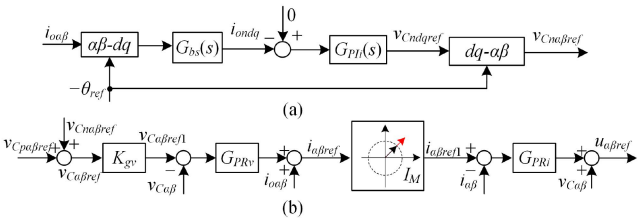

Fig. 10. Block diagram of the APECS. (a) Negative-sequence voltage compensation. (b) Inner voltage and current controls.

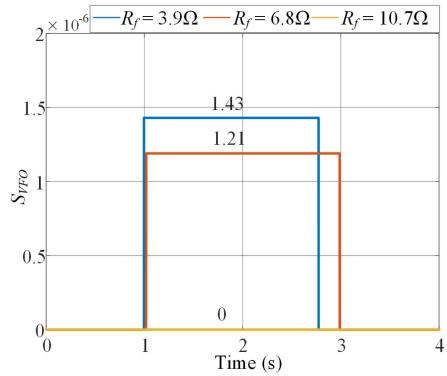

Fig. 11. Voltage limiting metric S_{VFO} during different severities of grid faults.

denotes the negative-sequence capacitor voltage reference in the STRF. $G_{bs}(s)$ denotes the transfer function of a band-stop filter designed to eliminate signals at the second harmonic frequency signal. Finally, $G_{\text{PIi}}(s)$ denotes a proportional–integral controller. The objective of the negative-sequence voltage compensation is to eliminate negative-sequence output currents by injecting negative-sequence capacitor voltages into the inner voltage and current controls. On the other hand, as shown in Fig. 10(b), $v_{Cp\alpha\beta\text{ref}}$ denotes the positive-sequence capacitor voltage references from the outer control loop shown in Fig. 2(a). The proportional gain K_{gv} is used to proportionally scale down capacitor voltages to prevent overvoltage, and its expression of K_{gv} is shown as

$$K_{gv} = \min\left\{1, \frac{V_{\text{hth}}}{\max\{V_{Ca\text{ref}}, V_{Cb\text{ref}}, V_{Cc\text{ref}}\}}\right\} \quad (10)$$

where $V_{Ca\text{ref}}$, $V_{Cb\text{ref}}$, and $V_{Cc\text{ref}}$ denote the magnitudes of capacitor voltage references in the NRF. Consequently, the APECS can enhance the active power output and limit overvoltage of GFM inverters under asymmetrical grids. For more detailed theoretical and experimental verification, please refer to [7].

B. Effectiveness of Proposed Metrics Across Distinct Severities of Grid Faults

To evaluate the sensitivity and effectiveness of the proposed metrics under various fault severities, experimental tests are conducted using three fault resistances (3.9, 6.8, and 10.7 Ω), representing different levels of fault severity. The AVI strategy is adopted as a representative control method.

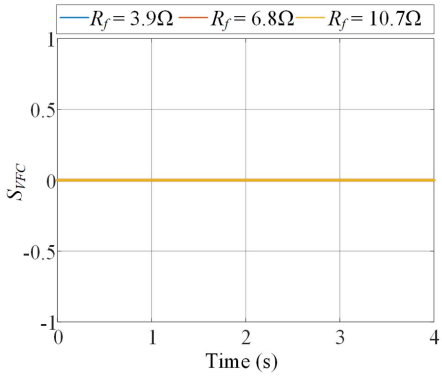

Fig. 12. Voltage limiting metric S_{VFC} after fault clearance under different fault severities.

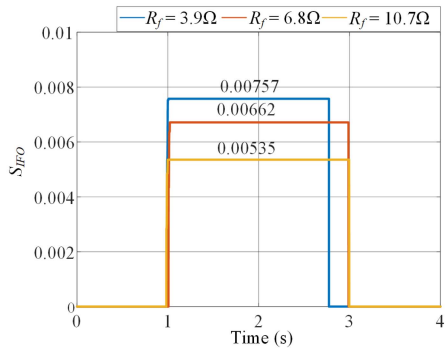

Fig. 13. Current limiting metric S_{IFO} during different severities of grid faults.

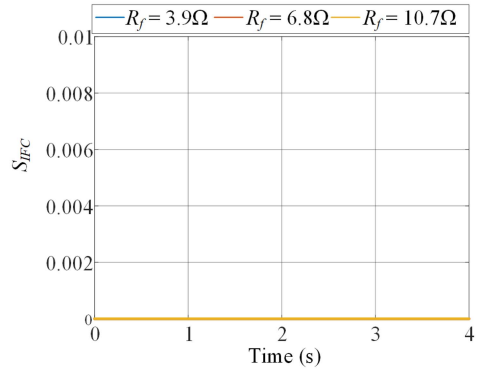

Fig. 14. Current limiting metric S_{IFC} after fault clearance under different fault severities.

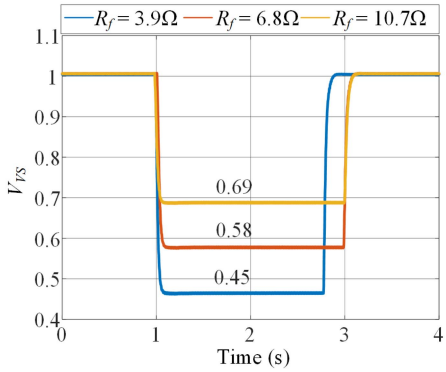

Fig. 15. Voltage support metric V_{VS} under different fault severities.

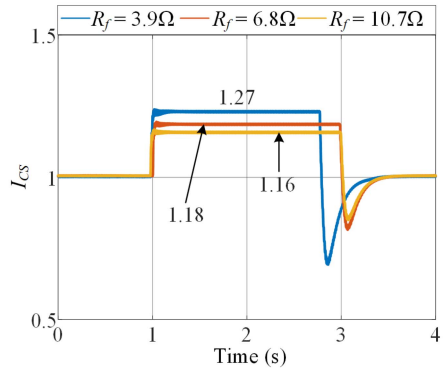

Fig. 16. Current support metric I_{CS} under different fault severities.

Fig. 11 presents the voltage-limiting metric S_{VFO}, which captures the overvoltage area during the fault period. As expected, S_{VFO} increases with decreasing fault resistance, confirming that the metric effectively reflects the severity of overvoltage conditions.

Fig. 12 shows S_{VFC}, which measures overvoltage area after fault clearance. The results indicate that S_{VFC} remains zero across all tested fault severities, verifying the absence of postfault overvoltage and the robustness of the AVI strategy in this aspect.

Similarly, Fig. 13 illustrates the current-limiting metric S_{IFO}, which quantifies the overcurrent area during faults. The results show that S_{IFO} increases with fault severity, validating the metric's effectiveness in capturing current-limiting performance.

Fig. 14 shows S_{IFC}, which assesses overcurrent issues after fault clearance. Across all severities, S_{IFC} remains zero, indicating that the AVI strategy successfully prevents postfault overcurrent, and that this metric effectively captures such performance.

Fig. 15 displays the voltage support metric V_{VS}, which measures the capability of the GFM inverter to preserve the prefault voltage level under various fault severities. As expected, a less severe fault (i.e., higher fault resistance) leads to a higher retained voltage, and the proposed metric accurately reflects this trend.

Fig. 16 illustrates the current support metric I_{CS}, which quantifies the inverter's current injection capability during faults. the maximum current magnitude of currents during distinct fault severities. Under more severe faults, a larger VI must be generated to avoid overcurrent, resulting in a higher current setpoint I_{om}, as dictated by the AVI strategy. The metric effectively captures this dynamic across different fault scenarios.

Figs. 17 and 18 depict the active power support metric P_F and reactive power support metric Q_F, respectively. Under a less severe fault severity, both active and reactive power support capabilities will be higher. As shown in these two figures, the proposed metrics effectively and consistently reflect the active and reactive power support capabilities.

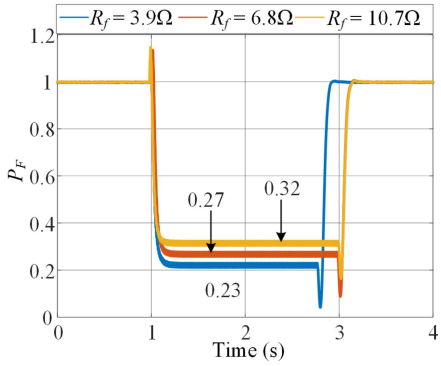

Fig. 17. Active power support metric P_F under different fault severities.

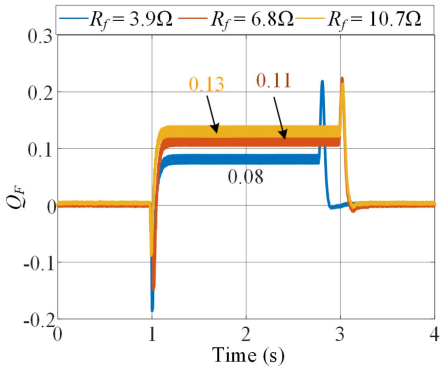

Fig. 18. Reactive power support metric Q_F under different fault severities.

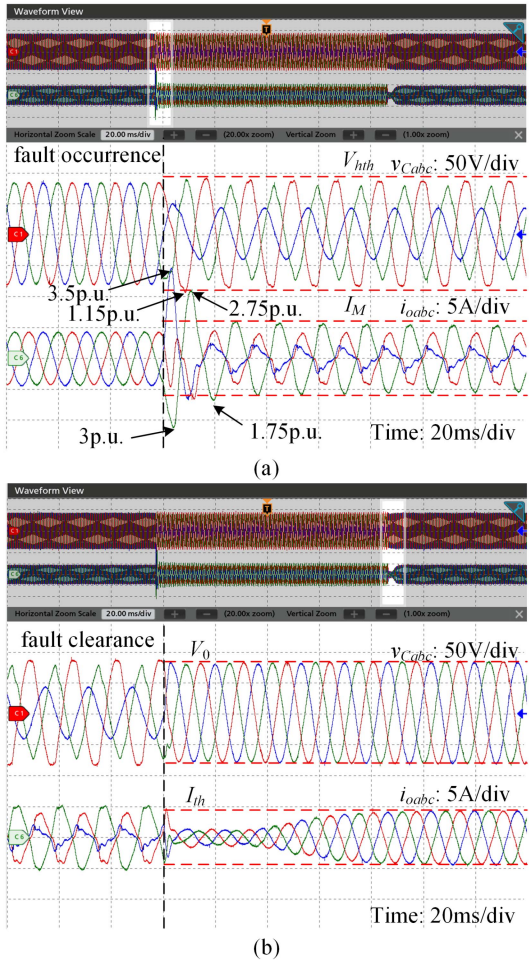

Fig. 19. Experimental waveforms of capacitor voltages and inverter output currents for AVI under an LL fault. (a) Around fault occurrence. (b) Around fault clearance.

In summary, these experimental results confirm that the proposed set of metrics are highly effective in characterizing various FRT capabilities, including voltage limiting, current limiting, voltage support, current support, and power injection, across a broad range of grid fault severities.

C. Limitation of Comparison by Conventional FRT Capability Evaluation

Figs. 19–22 show the experimental waveforms of capacitor voltages and inverter output currents for the four control strategies under an LL fault. Among them, only the AVI leads to a small overvoltage peak of 1.15 p.u., as shown in Fig. 19(a). In contrast, the other three strategies effectively prevent overvoltage after the fault occurrence, as illustrated in Figs. 20(a), 21(a), and 22(a). In addition, the AVI exhibits the most severe overcurrent issue after the fault occurrence, as its dynamic response is the slowest among the four strategies. Moreover, as shown in Fig. 19(a), the AVI produces four overcurrent peaks of 3.5, 2.75, 1.75, and 1.15 p.u., which are significantly higher than the overcurrent peaks observed with the other strategies. Although slight overcurrent peaks are also present after the fault occurrence with the other three strategies, as shown in Figs. 20(a), 21(a), and 22(a), it is difficult to intuitively compare the severity of overcurrent issues with the four strategies in a quantitative manner.

Moreover, Figs. 20(b) and 22(b) illustrate overvoltage peaks after the fault clearance with the CLF and APECS. However, directly comparing their severity is challenging due to the differences in the number and magnitudes of the overvoltage peaks: five overvoltage peaks of 1.03 p.u. versus two overvoltage peaks of 1.02 p.u. and three overvoltage peaks of 1.05 p.u. Similarly, both figures also show overcurrent peaks after fault clearance for CLF and APECS, with the APECS demonstrating both higher magnitudes and a greater number of overcurrent peaks. However, despite such large values and multiple peaks, determining the severity of the overcurrent issue intuitively remains difficult.

Ultimately, Table III summarizes the overvoltage and overcurrent peaks after fault occurrence and clearance for the four strategies. Nevertheless, this table cannot clearly and intuitively indicate which strategy performs best in voltage and current limiting during grid faults. Furthermore, comparing any two strategies is complicated by such numerous peak magnitudes. Consequently, a more intuitive quantification set of metric to effectively evaluate the FRT capabilities of different control strategies is presented in Section IV-D.

TABLE III
BASIC FRT PERFORMANCE EVALUATION OF FOUR CONTROL STRATEGIES

Description	AVI	CLF	MPDCL	APECS
Magnitudes of overvoltage peaks around fault occurrence	1.15 p.u.	No	No	No
Magnitudes of overcurrent peaks around fault occurrence	3.5, 3, 2.75, 1.75 p.u.	1.88, 1.75, 1.63, 1.63 p.u.	1.6, 1.51 p.u.	1.88, 1.75, 1.6, 1.63 p.u.
Magnitudes of overvoltage peaks around fault clearance	No	1.03 p.u. (five peaks)	No	1.05 p.u. (three peaks), 1.02 p.u. (two peaks)
Magnitudes of overcurrent peaks around fault clearance	No	1.45 p.u. (four peaks)	No	1.75 p.u. (three peaks), 1.5 p.u. (two peaks)

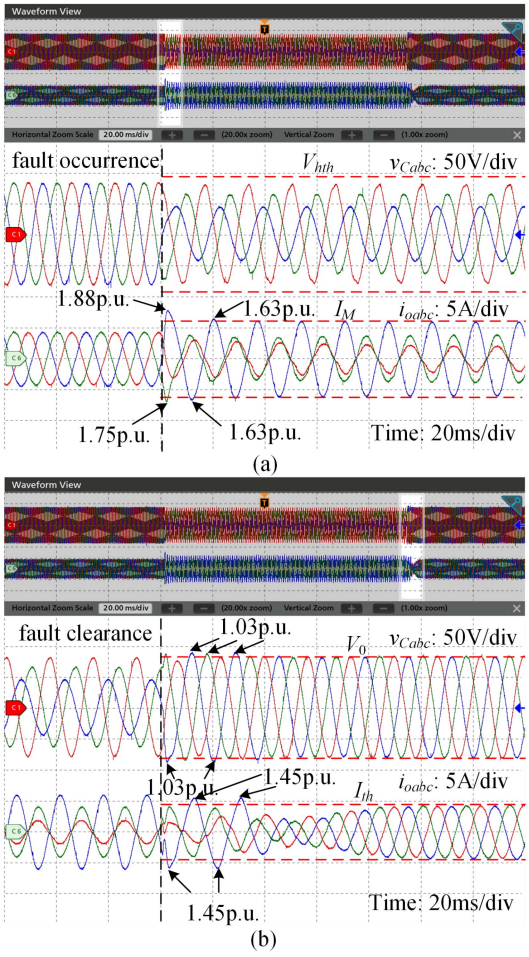

Fig. 20. Experimental waveforms of capacitor voltages and inverter output currents for CLF under an LL fault. (a) Around fault occurrence. (b) Around fault clearance.

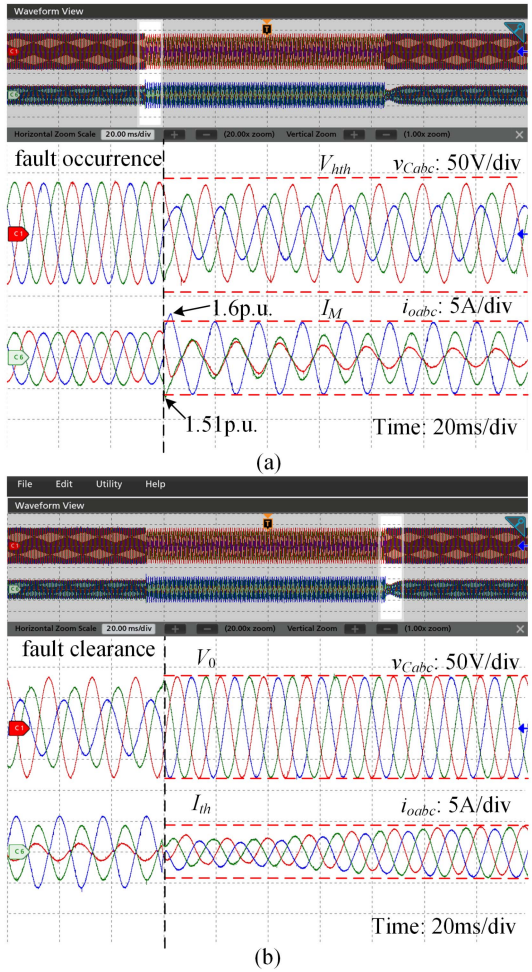

Fig. 21. Experimental waveforms of capacitor voltages and inverter output currents for MPDCL under an LL fault. (a) Around fault occurrence. (b) Around fault clearance.

D. Comparison by Proposed Resilience-Aware Quantification Metrics

Although the faulty durations for the four control strategies differ slightly, the proposed metrics remain unaffected since the solid state relay detects the voltage zero-crossing point to connect or disconnect the fault resistance. Consequently, the dynamic response of different control strategies is not influenced by the fault duration. Furthermore, the primary objective of this article is to propose and examine a set of quantification metrics for evaluating FRT capabilities of different control strategies based on the obtained experimental results, rather than designing new control strategies. Therefore, the slight variations in fault durations do not impact the validity of the proposed metrics.

Fig. 23 illustrates the voltage limiting quantification metric for the four control strategies around fault occurrence and clearance. As shown in Fig. 23(a), the voltage limiting metric S_{VFO} for the AVI rises to 0.14×10^{-5} at the fault occurrence, while the metric S_{VFO} for the other three strategies remains 0 around the fault occurrence. This indicates that only the AVI will cause overvoltage issues after the fault occurrence. Nevertheless, the metric S_{VFO} for the AVI is 47 times smaller than the voltage limiting metric S_{VFC} for the CLF and APECS, indicating that the

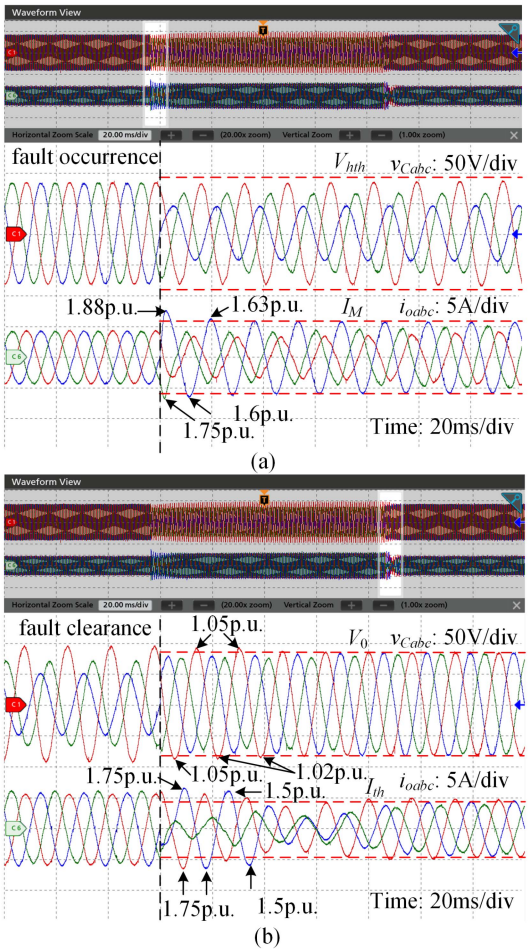

Fig. 22. Experimental waveforms of capacitor voltages and inverter output currents for APECS under an LL fault. (a) Around fault occurrence. (b) Around fault clearance.

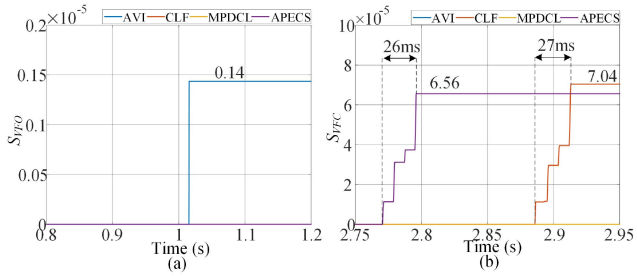

Fig. 23. Voltage limiting quantification metrics for the four control strategies under an LL fault. (a) Around fault occurrence. (b) Around fault clearance.

overvoltage issue around the fault occurrence is negligible. On the other hand, as shown in Fig. 23(b), the voltage limiting quantification metrics S_{VFC} of the CLF and APECS respectively rise to 7.04×10^{-5} and 6.56×10^{-5} after the fault clearance, indicating a more severe overvoltage issue in the CLF case. In contrast, the metrics for the AVI and MPDCL remain at 0 around fault clearance, demonstrating that these two strategies do not lead to overvoltage issues. In addition, it respectively takes 27 and 26 ms for the overvoltage peaks of the CLF and

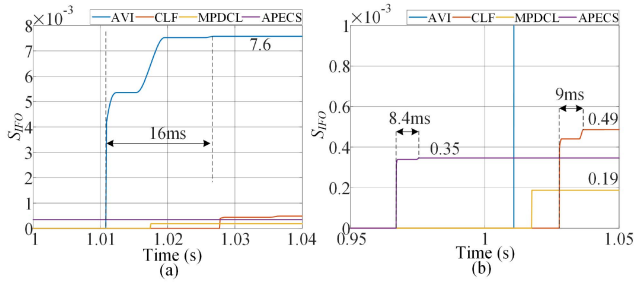

Fig. 24. Current limiting quantification metrics for the four control strategies around an LL fault occurrence. (a) Current limiting metric diagram. (b) Zoom-in current limiting metric diagram.

APECS to converge below the nominal voltage magnitude V_0, indicating that the voltage recovery around fault clearance is faster with the APECS. In summary, the established voltage limiting metrics provide an intuitive and real-time quantitative evaluation of the voltage-limiting capability for the four control strategies. Besides, the proposed metrics align consistently with the experimental waveforms.

Fig. 24 illustrates the current limiting quantification metrics for the four control strategies around an LL fault occurrence. The current limiting metric S_{IFO} for the AVI is significantly higher than that of the other three strategies. In addition, as shown in Fig. 24(a), the AVI has the longest dynamic response time among the four strategies. Therefore, the current limiting metric can intuitively and clearly indicate that the AVI experiences the most severe overcurrent issue after fault occurrence. On the other hand, Fig. 24(b) shows that the metric S_{IFO} for the MPDCL exhibits the lowest increases, rising only to 0.19×10^{-3} at the fault instant due to inrush currents, and then remains steady as the overcurrent peaks quickly dwindle. Consequently, the metric S_{IFO} for the MPDCL can validate that the MPDCL performs best in mitigating transient overcurrent after fault occurrence. Besides, this metric aligns well with the experimental waveform shown in Fig. 21(a). Finally, the metric S_{IFO} for the CLF is 0.49×10^{-3}, which is higher than the 0.35×10^{-3} for the APECES, indicating that the CLF results in more severe overcurrent issues than the APECS. In summary, the metrics S_{IFO} can clearly and intuitively reflect the current-limiting capability of the four strategies after fault occurrence.

Fig. 25 illustrates the overcurrent quantification metric S_{IFC} for the four strategies around an LL fault clearance. The metric S_{IFC} for the APECS is approximately four times higher than that of the CLF. Meanwhile, the metrics S_{IFC} for the other two strategies remain zero, indicating that they do not cause overcurrent issues. Furthermore, APECS requires over four times duration of CLF to mitigate overcurrent after fault clearance, highlighting the performance differences between the two strategies in managing transient overcurrent. In summary, the proposed metric S_{IFC} provides a clear and intuitive assessment of the current-limiting capability of the four strategies around fault clearance.

Fig. 26(a) and (b) respectively illustrates the voltage and current support quantification metrics for the four strategies during an LL fault. As shown in Fig. 26(a), the voltage support

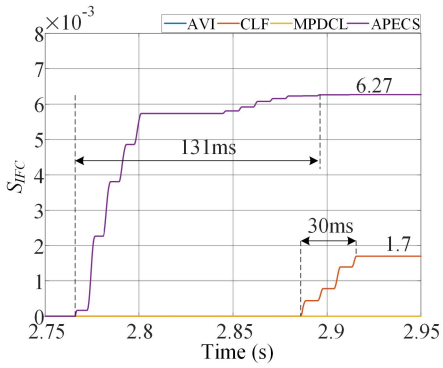

Fig. 25. Current limiting quantification metrics for the four strategies around an LL fault clearance.

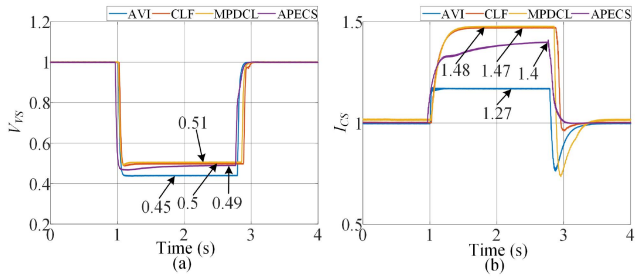

Fig. 26. Voltage and current support quantification metrics. (a) Voltage support quantification metric. (b) Current support quantification metric.

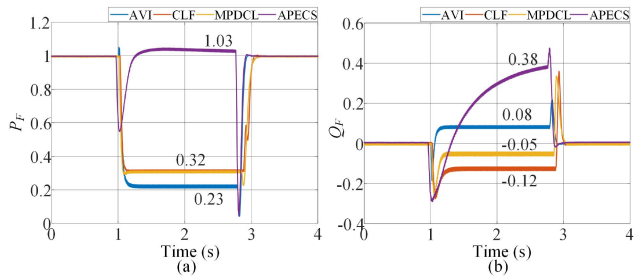

Fig. 27. Power support quantification metrics for the four strategies under an LL fault. (a) Active power support quantification metric. (b) Reactive power support quantification metric.

metric for the MPDCL is the highest during the fault, indicating its strongest voltage support capability. This observation aligns well with Fig. 26(b), which shows that the MPDCL achieves the maximum current support (current injection) capability. Moreover, the CLF exhibits a similar voltage support capability to the MPDCL, as shown in Fig. 26(a), due to its comparable current support capability, as demonstrated in Fig. 26(b). In contrast, the AVI has the lowest voltage support capability, as shown in Fig. 26(a), because its current support capability is the weakest, as observed in Fig. 26(b). This limitation arises from the fact that the AVI typically designs its VI based on symmetrical grid faults, significantly compromising its current support capability during asymmetrical grid faults.

Fig. 27 illustrates the power support quantification metrics for the four strategies under an LL fault. As shown in Fig. 27(a), the active power support metric P_F for the APECS is the highest, as its primary purpose is to enhance active power output [7]. In contrast, the metric P_F for the AVI is the lowest because inductive VI is emulated during faults [23]. Moreover, due to the symmetrical current injection during faults depicted in Fig. 22, the reactive power support Q_F for the APECS is the highest, as shown in Fig. 27(b). Alternatively, the metric Q_F for the AVI is higher than that of the CLF and MPDCL, as the inductive VI enhances reactive power support during faults. Finally, the metrics P_F and Q_F for the CLF and MPDCL are similar, as both strategies employ the same CLF.

Ultimately, all resilience-aware quantification metrics for the four strategies under an LL fault are summarized in Table IV. The performance preference for each metric indicates whether a "higher" or "lower" value represents superior performance. The proposed metrics provide a straightforward and intuitive method for evaluating FRT capabilities by comparing their values. The results indicate that the MPDCL excels in voltage and current limiting as well as voltage and current support capabilities, while the APECS exhibits the best performance in both active and reactive power support capabilities. Metrics based on the evaluated FRT capabilities effectively indicate the ability of GFM-based inverters to remain online, thus preventing disconnection and mitigating the risk of cascading failures, which would otherwise reduce system resilience.

E. Comprehensive Metric in Determining the Most Suitable FRT Strategy

In Table III, experimental results of different metrics for four FRT strategies have been summarized. While it is easy to select the best strategy in any specific FRT capability, determining the most appropriate FRT control strategy based on all metrics is still tough. To address this, a comprehensive metric, as defined in (8), is employed to integrate the performance across all individual metrics. By assigning representative weighting factors (e.g., $W_4 = 0.4$, $W_3 = 0.3$, $W_2 = 0.2$, and $W_1 = 0.1$) as example, the comprehensive metric values for the four FRT strategies are computed and summarized in Table V.

As shown in Table V, APECS achieves the highest comprehensive score due to its superior active and reactive power support, which can also be verified by the significantly high values of the P_F and Q_F metrics in Table IV. Consequently, APECS is identified as the most effective FRT control strategy. MPDCL ranks second, driven by strong current and voltage support capabilities. AVI and CLF score lower, as they respectively exhibit weaker current and reactive power support. These results demonstrate the usefulness of the proposed metric for holistic evaluation and strategy selection.

V. Simulation-Based Case Study of a Modified Kundur Two-Area System

The previous section experimentally validated the effectiveness of the proposed metrics in revealing distinct FRT capabilities and identifying the most suitable FRT strategy in a single

TABLE IV
RESILIENCE-AWARE QUANTIFICATION METRICS FOR THE FOUR STRATEGIES UNDER AN LL FAULT IN EXPERIMENTAL TESTS

Metric	AVI	CLF	MPDCL	APECS	Performance preference	Best strategy
S_{VFO}	0.14×10^{-5}	0	0	0	Lower	CLF/MPDCL/APECS
S_{VFC}	0	7.04×10^{-5}	0	6.56×10^{-5}	Lower	AVI/MPDCL
S_{IFO}	7.6×10^{-3}	0.49×10^{-3}	0.19×10^{-3}	0.35×10^{-3}	Lower	MPDCL
S_{IFC}	0	1.7×10^{-3}	0	1.7×10^{-3}	Lower	AVI/MPDCL
V_{VS}	0.45	0.5	0.51	0.49	Higher	MPDCL
I_{CS}	1.27	1.47	1.48	1.4	Higher	MPDCL
P_F	0.23	0.32	0.32	1.03	Higher	APECS
Q_F	0.08	–0.12	–0.05	0.38	Higher	APECS

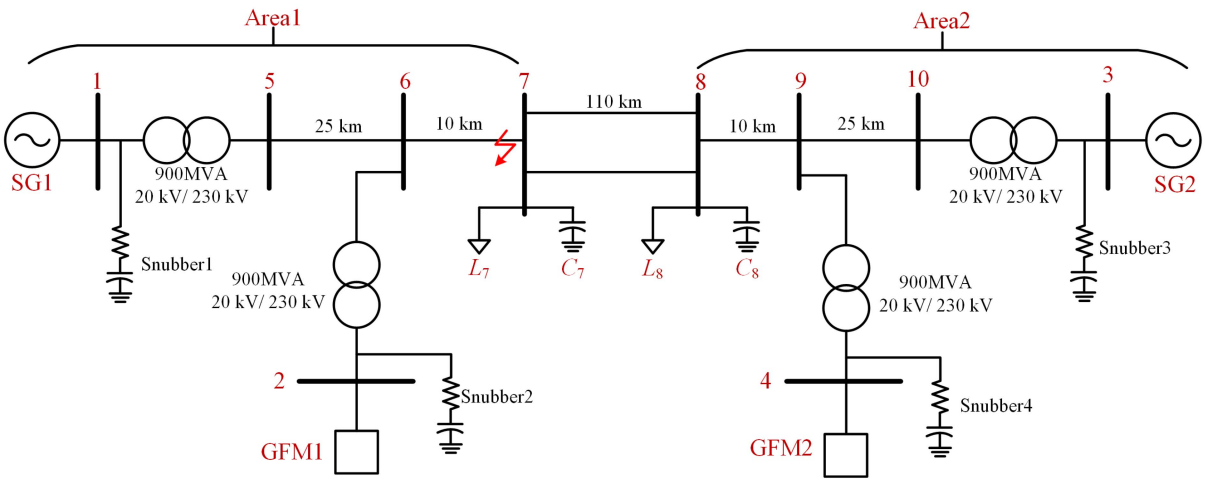

Fig. 28. Illustration of the modified Kunder two-area system.

TABLE V
COMPREHENSIVE METRICS FOR THE FOUR FRT STRATEGIES

FRT strategy	Comprehensive metric (S)
AVI	0.207
CLF	0.204
MPDCL	0.232
APECS	0.368

TABLE VI
SIMULATION PARAMETERS OF THE MODIFIED KUNDER TWO-AREA SYSTEM

Symbol	Description	Value
S_B	Rated power	900 MVA
V_B	Base voltage	400 V
P_{ref}	Reference active power for SG/GFM	0.291 p.u.
Q_{ref}	Reference reactive power for SG/GFM	0 p.u.
r	Line resistance per km	$1 \cdot 10^{-4}$
x_L	Line inductance per km	$1 \cdot 10^{-3}$
b_C	Line capacitance per km	$1.75 \cdot 10^{-3}$
P_{L7}	Active load at bus 7	0 MW
Q_{L7}	Inductive reactive load at bus 7	100 MVAr
Q_{C7}	Capacitive reactive load at bus 7	200 MVAr
P_{L8}	Active load at bus 8	1767 MW
Q_{L8}	Inductive reactive load at bus 8	100 MVAr
Q_{C8}	Capacitive reactive load at bus 8	350 MVAr
P_{Sn}	Snubber active power	1 MW
Q_{Sn}	Snubber capacitive reactive power	10 MVAr

GFM inverter system. To further validate the applicability of the metrics in more complex scenarios, this section presents a simulation-based case study of a modified Kundur two-area system, as illustrated in Fig. 28 [35], [36], [37], [38]. The system comprises two SGs and two GFM inverters. Key system parameters are listed in Table VI, while detailed parameters of the SGs can be found in [35].

A. Simulation Results for Different FRT Strategies

In this case study, the two GFM inverters within the Kundur two-area system both respectively implement the four FRT strategies introduced in Section IV-A in each simulation test: AVI, CLF, MPDCL, and APECS. All control parameters are adopted from the experimental setup with the same per-unit values, except for the reference active power values. An LL fault with the same per-unit fault resistance as in experiments is applied at bus 7 from 30 to 32 s.

The resulting capacitor voltages and output currents of GFM1 under the four strategies are shown in Fig. 29. As the dynamic behavior of GFM2 is similar to that of GFM1, its waveforms are omitted for brevity.

Compared to the experimental results presented in Figs. 19–22, the dynamic responses of GFM inverters in the large-scale Kundur system are noticeably extended both during the fault and after fault clearance. For instance, as shown in Fig. 29(a) and (d), under the AVI and APECS strategies, the capacitor voltages of GFM1 exceed the overvoltage threshold

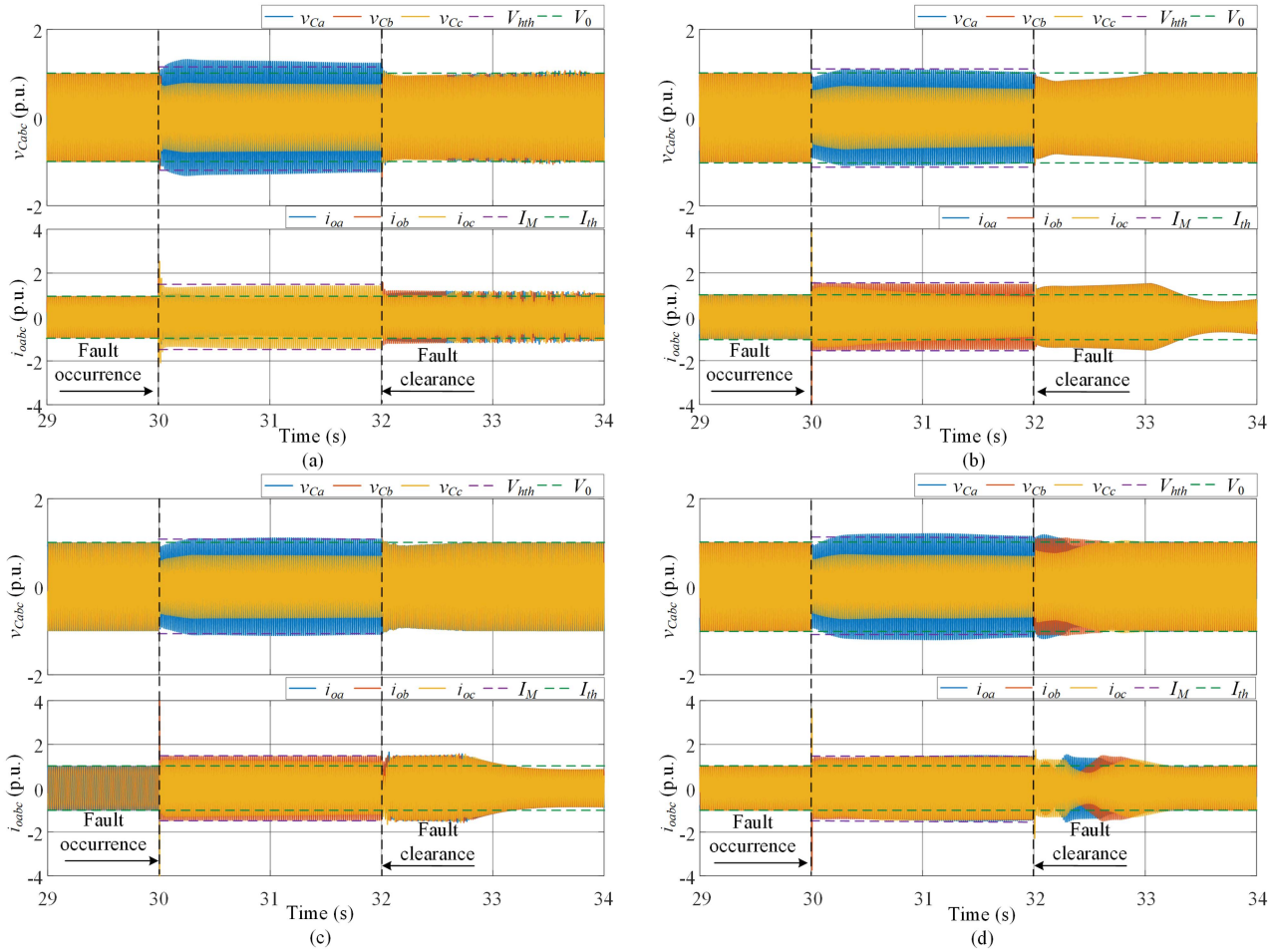

Fig. 29. Simulation results of capacitor voltages and output currents of the GFM1 inverter system for the four FRT strategies. (a) AVI. (b) CLF. (c) MPDCL. (d) APECS.

Vhth throughout the fault duration. Postfault recovery of capacitor voltage takes approximately 2 s, and significant voltage overshoots occur near fault clearance with APECS, as observed in Fig. 29(d).

While all four strategies effectively limit inverter current below the MACM ($I_M = 1.5$ p.u.) during the fault, the postfault recovery of output current is notably prolonged. Moreover, severe overcurrent phenomena are observed after fault clearance under the CLF, MPDCL, and APECS strategies, as shown in Fig. 29(b)–(d).

These observations highlight that in a complex system with interactions between SGs and GFM inverters, the dynamic performance during and after grid faults becomes significantly more intricate than in isolated GFM systems. In addiiton, both overvoltage and overcurrent risks are amplified. Therefore, selecting the most appropriate FRT strategy by comparing conventional transient performance metrics—particularly peak voltage and current deviations—becomes substantially more challenging.

B. FRT Capability Comparison Through Proposed Metrics

The previous section demonstrated that conventional indicators, such as peak overvoltage and overcurrent values, are insufficient to accurately evaluate the FRT capabilities of GFM inverters under complex grid conditions. In contrast, the results presented in this section confirm that the proposed metrics remain effective for distinguishing different FRT capabilities and for identifying the most appropriate FRT strategy applicable to GFM inverters.

For clarity and conciseness, only the metric calculation results of GFM1 are presented. Fig. 30 illustrates the voltage-limiting metrics of GFM1 during the LL fault. As shown in Fig. 30(a), the S_{VFO} values corresponding to the AVI and APECS strategies continue to increase significantly, which aligns with the observation in Fig. 29(a) and (d) that overvoltage conditions persist throughout the fault duration. As illustrated in Fig. 30(b), the S_{VFC} value corresponding to the APECS strategy is notably higher than those of the other three strategies following fault clearance. This result is consistent with the severe overvoltage behavior observed in Fig. 29(d). Furthermore, the magnitudes of the S_{VFO} and S_{VFC} metrics provide an intuitive and quantitative indication of the voltage-limiting capability of GFM inverters.

Fig. 31 presents the current-limiting metrics of GFM1 during the LL fault. As shown in Fig. 31(a), the S_{IFO} value associated with the AVI strategy is significantly lower than those of the other three strategies throughout the fault period. This

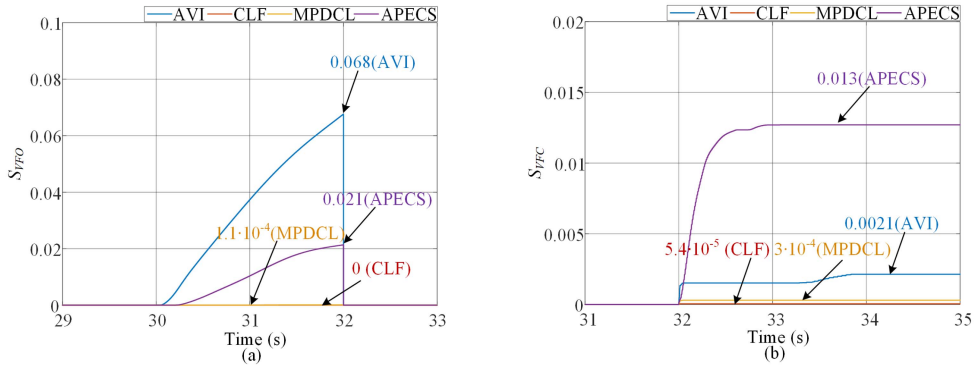

Fig. 30. Voltage-limiting metric results of GFM1 during the LL fault. (a) S_{VFO}. (b) S_{VFC}.

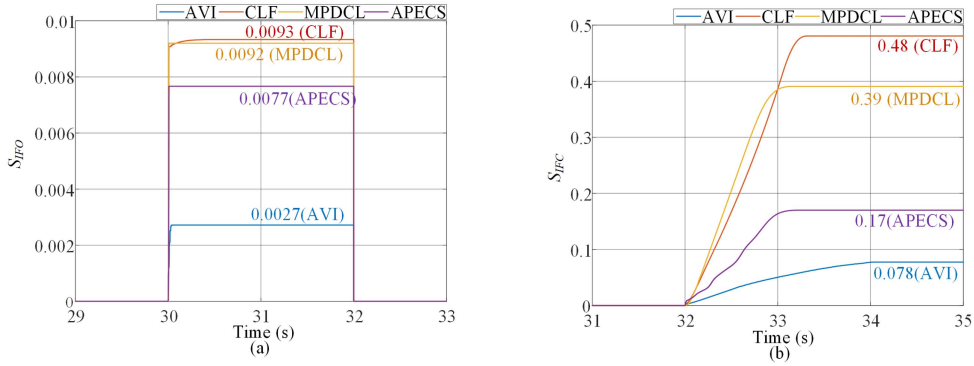

Fig. 31. Current-limiting metric results of GFM1 during the LL fault. (a) S_{IFO}. (b) S_{IFC}.

result corresponds to the relatively smaller overcurrent peaks observed at the onset of the fault, as seen in Fig. 29(a). In addition, Fig. 31(b) shows that the S_{IFC} value under the AVI strategy remains considerably lower than those of the other strategies. This outcome is consistent with the postfault behavior in Fig. 29(a), where the output currents of the AVI-controlled inverter recover to nominal levels, in contrast to the sustained high current levels observed under the other three strategies, as shown in Fig. 29(b)–(d).

The mechanism underlying the persistent postfault overcurrents associated with the CLF, MPDCL, and APECS strategies has been discussed in [39], but is beyond the scope of this article. Nevertheless, the proposed current-limiting metrics effectively capture the relative performance of different FRT strategies during both the fault and recovery stages. Similar to the voltage-limiting metrics, the magnitudes of S_{IFO} and S_{IFC} offer intuitive and quantitative insight into the current-limiting capability of GFM inverters.

Fig. 32 illustrates the voltage-support and current-support metrics of GFM1 during the LL fault, while Fig. 33 presents the active power- and reactive power-support metrics of GFM1 under the same fault condition. Due to the complex interactions between SGs and GFM inverters, the FRT support capabilities exhibit slight variations across the four strategies. Nevertheless, the proposed metrics remain effective in capturing these differences, providing a clear and quantitative assessment of each strategy's performance.

TABLE VII
PROPOSED RESILIENCE-AWARE METRICS FOR THE FOUR FRT STRATEGIES IN THE KUNDUR SYSTEM

Metric	AVI	CLF	MPDCL	APECS	Best strategy
S_{VFO}	0.068	0	$1.1 \cdot 10^{-4}$	0.021	CLF
S_{VFC}	0.0021	$5.4 \cdot 10^{-5}$	$3 \cdot 10^{-4}$	0.013	CLF
S_{IFO}	0.0027	0.0093	0.0092	0.0077	AVI
S_{IFC}	0.0078	0.48	0.39	0.17	AVI
V_{VS}	0.09	0.13	0.17	0.17	MPDCL/APECS
I_{CS}	1.41	1.5	1.49	1.45	CLF
P_F	0.12	–0.01	0.01	0.42	APECS
Q_F	–0.18	–0.13	–0.03	0.055	APECS
S	0.00014	–0.39	–0.271	–0.227	AVI

All metric values corresponding to the four strategies are summarized in Table VII, where the relative performance of each strategy across different FRT capabilities can be clearly identified based on the metric magnitudes. To determine the most appropriate FRT strategy under complex grid conditions, a comprehensive evaluation metric was introduced in Section IV-D. This comprehensive metric is also applied to the large-scale power system in this study (taking the same weighting factor as in experiments).

As shown in Table VII, the comprehensive metric value (S) for the AVI strategy is significantly higher than those of the other

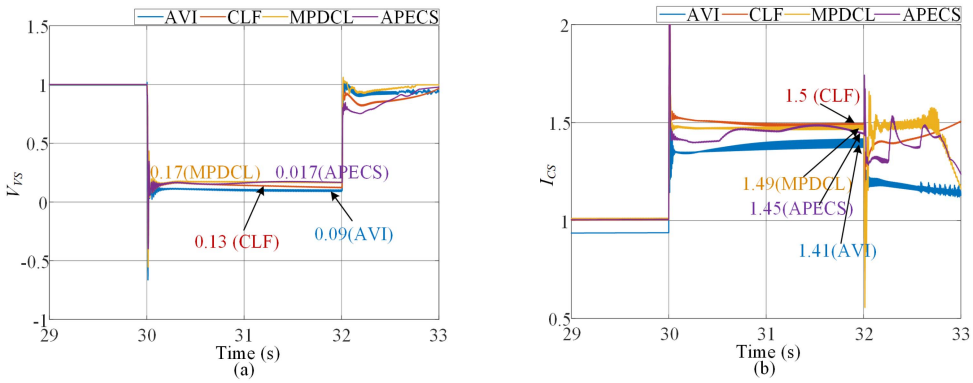

Fig. 32. Voltage and current-support metric results of GFM1 during the LL fault. (a) V_{VS}. (b) I_{CS}.

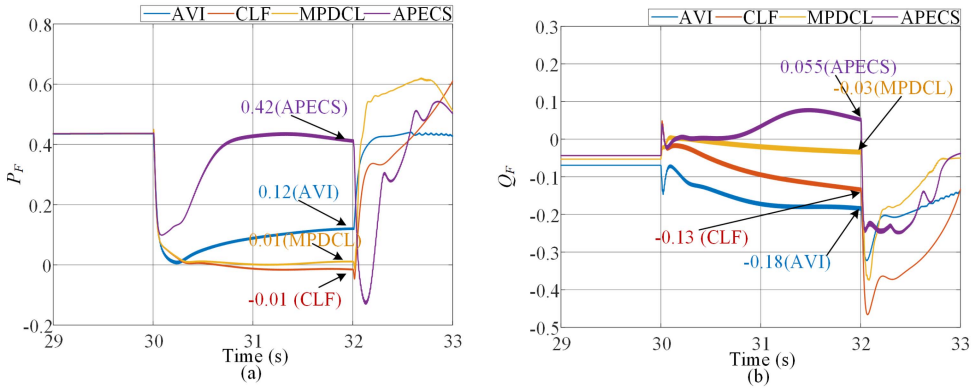

Fig. 33. Active power and reactive power-support metric results of GFM1 during the LL fault. (a) P_F. (b) Q_F.

three strategies. This result indicates that AVI remains the most appropriate FRT strategy in large-scale systems, consistent with its superior current-limiting performance and the minimal post-fault current observed in Fig. 29(a). The APECS strategy ranks second, primarily due to its strong active and reactive power support capabilities, which aligns well with the experimental observations. In contrast, the CLF and MPDCL strategies exhibit relatively poor performance in the large-system case, mainly due to excessive postfault overcurrents, and are therefore not recommended for application under such grid conditions.

In summary, this section has validated the applicability and robustness of the proposed FRT evaluation metrics in a large-scale power system with mixed SG and GFM components. Despite the increased system complexity and the extended dynamic responses caused by SG-GFM interactions, the proposed voltage-limiting, current-limiting, and support-oriented metrics remain effective in characterizing the relative performance of different FRT strategies. The simulation results demonstrate that the AVI strategy provides the most favorable balance among various FRT capabilities, followed by APECS, while CLF and MPDCL are less suitable due to postfault overcurrent issues. These findings further confirm that the proposed metrics not only capture essential FRT behaviors in single-inverter systems but also scale effectively to more realistic and complex multisource power networks.

VI. Conclusion

This article proposes a unified set of resilience-aware quantification metrics to evaluate essential FRT capabilities of four selected strategies for GFM inverters under grid faults. The metrics include overvoltage areas exceeding the continuous FRT voltage threshold after fault occurrence and the nominal voltage threshold after fault clearance, serving as indicators of voltage-limiting capabilities. Similarly, overcurrent areas that exceed the MACM after fault occurrence and the nominal current threshold after fault clearance, quantify current limiting capabilities. Positive- and negative-sequence voltage magnitudes during faults are used to assess voltage support, while maximum current magnitudes during faults measure current support. Finally, average active and reactive powers during faults provide metrics to evaluate active and reactive power support. These metrics comprehensively quantify the FRT capabilities related to voltages, currents, and powers, as required by grid codes.

In addition, the proposed metrics offer several advantages. They are designed to be calculated in real time, allowing for real-time FRT capability evaluation and comparison of different FRT strategies. By reflecting the respective strengths and weaknesses of various strategies, these metrics enable a detailed and intuitive assessment of FRT capabilities. Moreover, the metrics are expressed in per-unit values, ensuring their applicability

across different types of grid faults and system configurations. A comprehensive metric is proposed to combine all proposed individual metrics to determine the most appropriate FRT strategies. Experiments for a single GFM inverter system and simulations for a large-scale power system incorporating four distinct FRT strategies confirm the effectiveness and robustness of the proposed framework. In conclusion, this framework provides a systematic and scalable tool for evaluating and optimizing FRT strategies, offering valuable insights for the development of resilient GFM inverter control schemes. In the near future, we will extend our proposed framework to explicitly model and simulate the effects of cyber-induced disturbances, including attacks on a central controller or on peer-to-peer communication channels. We will also account for time delays introduced by remote terminal units and other communication devices, using probabilistic models and compensation strategies to mitigate those delays and preserve realtime performance.

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