Uncertainty Analysis of the Interface Thermal Resistance Between Power Module and Heatsink

Ziheng Wang, *Student Member, IEEE*, Yi Zhang, *Senior Member, IEEE*, and Huai Wang, *Senior Member, IEEE*

***Abstract*—Thermal resistance of the thermal interface materials (TIMs) between power module and heatsink plays a significant role in thermal stress. This article investigates the variances in thermal resistances of TIMs during thermal cycling test and among different chips of a six-switch power module. An experimental setup to facilitate the emulation of practical power state operation is built for the test. The dual interface method with structure function analysis is applied to characterize the TIMs thermal resistances. The results reveal considerable changes and variances in the thermal resistances during the test and among the six switches of the power module, implying high-level of uncertainty caused application-level thermal modeling. A case study of PV inverter application is presented to demonstrate the impact on thermal stress and reliability modeling.**

***Index Terms*—Lifetime prediction, power module, thermal interface materials (TIMs), thermal resistance, uncertainty analysis.**

I. Introduction

POWER electronic converters are widely used in electric vehicles, photovoltaic power generation, high-speed rail, aerospace, and other power conversion fields, and its reliability has become a research hotspot in academia and industry [1]. Especially, compared with other components in the power converter, power semiconductors/modules are regarded as the most vulnerable components that need future research to improve their reliability in an industry survey [2], [3].

Typically, the dominant failure mechanism of the power modules in power converters is related to the junction temperature [4]. Thermal models serve as the connection between the electrical parameters and thermal parameters, facilitating the mapping of the power losses to the junction temperatures of devices [5]. The thermal modeling typically involves in the models of the power module itself, the thermal interface material (TIM), and the cooling system. According to [6], TIMs typically account for over 50% of the thermal resistance from the junction to the heatsink. As the contribution of the TIM to the overall thermal resistance is significant, the uncertainty of the TIM and its impact on the predicted lifetime of power modules in power converter systems must be evaluated.

However, as far as we can see, comprehensive study on power electronics application-oriented thermal resistance of TIMs analysis in multichip power modules can be rarely found. In existing studies, most of the previous works are focused on the junction-to-case thermal resistance within the internal structure of power module [7]. Furthermore, the thermal coupling phenomenon among neighboring chips has been studied for years in literatures [8], [9], mainly for the accurate estimation of semiconductor junction temperatures in field applications. In [10], thermal coupling has also been identified as the primary cause of thermal imbalance among paralleled chips. Nevertheless, it is worth noting that the external case-to-ambient thermal resistance also plays a critical role in determining overall thermal behavior as well as the phenomenon of thermal coupling and thermal imbalance. Specifically, the ABB's application note points out that the TIM influences the heat-spreading much more than the heat sink [11]. It is, thus, of great importance to investigate the thermal resistance of TIM in power module applications.

Thermal resistance increase associated with TIMs in power modules can be caused by two aspects: impaired interface integrity and material aging. Mismatch in the coefficients of thermal expansion (CTE) among different material interfaces can induce considerable thermomechanical stress, which may compromise the integrity of the contact interface between the baseplate of the power module and cooling metal plate [12], [13], [14], [15]. These stresses can result in physical degradation phenomena, such as delamination, void, and TIM pump-out [16]. Simultaneously, intrinsic aging of the TIMs itself, including hardening, drying, or reduction in thermal conductivity, can occur even in the absence of visible mechanical damage [17], [18], [19]. Whether impaired interface integrity, material aging, or both, the effective area for heat dissipation from the die to the heatsink can be reduced. This reduction can lead to an increase in the overall thermal resistance of the module, or cause variations in thermal resistance among different chips within the same module and thus eventually raises the junction temperature. With the increased junction temperature, the module is more prone to further degradation [20].

Researchers have employed various testing methodologies to study the uncertainty of TIMs, including power cycling, thermal cycling, and mechanical or vibrational stress tests. Zhang et al. [21] evaluated the aging characteristics of the dual power modules under power cycle test, and 27% thermal resistance

Received 8 May 2025; revised 30 July 2025; accepted 7 September 2025. Date of publication 16 September 2025; date of current version 23 December 2025. This work was supported by MSCA-RISE - Marie Skłodowska- Curie Research and Innovation Staff Exchange (RISE) project DORNA - Development of high reliability motor drives for next generation propulsion applications under Grant 872001. Recommended for publication by Associate Editor S. Ji. *(Corresponding author: Ziheng Wang.)*

Ziheng Wang and Huai Wang are with the Department of Energy, Aalborg University, 9220 Aalborg, Denmark (e-mail: ziwa@energy.aau.dk; hwa@energy.aau.dk).

Yi Zhang is with Hong Kong Polytechnic University, Hong Kong 999077 (e-mail: yiz@ieee.org).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3610704.

Digital Object Identifier 10.1109/TPEL.2025.3610704

increase was observed, primarily due to the degradation of TIM, which leads to 30°C temperature increase inside the power module. The degradation of TIM induces temperature jumps, highlighting the substantial impact of TIM aging on the thermal performance of the power module. Heimler et al. [22] explored the effects of various TIMs impact the junction temperature under power cycling conditions, respectively, showing significant variations in thermal resistance and reliability outcomes of discrete Si IGBT, underlining the critical influence of TIMs selection on the thermal and reliability performance of discrete components. Tompkins et al. [23] investigated the degradation of the TIM layer between a commercial AlSiC baseplate and an aluminum heatsink under thermal cycling, both with or without vibrational stress. The results reveal that vibrational stress aggravates the degradation behavior in the thermal resistance of the TIM. In addition, lifetime prediction can be significantly compromised when the thermal resistance of the TIM is assumed to remain constant according to its datasheet-provided thermal conductivity. However, this assumption neglects the dynamic changes of TIMs during actual operation, potentially leading to an underestimation of thermal resistance growth and an overestimation of module reliability. In [24], the impact of the TIM thickness on the estimated lifetime of IGBT modules in an MMC system for offshore wind power applications is investigated, including the starting assembly thickness and the bond-line thickness (BLT) of TIMs. Results show that both the starting thickness and the BLT of the TIM will affect the lifetime of the power devices. The predicted lifetime can shift as large as 50% with different thickness values of the TIMs.

However, the prior-art work focus on material-level behavior or discrete components, without investigating variability in thermal resistance among different chips within TIM layers in the same power module and its subsequent impact on the overall lifetime of power modules. Moreover, the thermal resitance change of the TIM is time-dependent and may be influenced by the mounting position. For instance, vertically mounted TIMs, which are more affected by gravity, may exhibit different trends compared to horizontally mounted ones. In such cases, assuming constant thermal resistance can lead to unrealistic thermal stress analysis and lack of confidence in the lifetime prediction of power modules.

To address the aforementioned challenges, this study employs the accelerated thermal shock test to investigate the uncertainty of the TIM behavior in the power module. A structure function method is utilized to characterize the thermal resistance between different chips within the TIM layer. In the thermal shock test, two types of TIMs are evaluated under two mounting positions: horizontal and vertical. Furthermore, a mission profile-based lifetime evaluation is conducted in the case of PV systems. According to the above discussion, this article has the following twofold contributions.

1) It quantifies the variances in thermal resistance of the TIM layer among different switches along the testing and explores the impact the thermal stress increase and imbalance at power module level.
2) It focuses on power electronics application-oriented testing and analysis, which is distinguished from existing material-level or discrete component-level studies.

TABLE I
TIM PROPERTIES

Property	Dow corning 340	HTSP50T
Thermal conductivity (W/m K)	0.67	3.0
Viscosity (Pa.s)	542	42 to 48
Temperature Range (°C)	−40 to 177	−50 to 200

The rest of this article is organized as follows: Section II introduces the prototype structure and the testing procedure. The structure function is utilized to characterize the thermal resistance among the chips and show the process of extracting the thermal resistance of TIMs. Section III focuses on data analysis of TIMs with thermal shock tests. The results show a significant thermal imbalance in the power module due to the TIM layer. Section IV briefly discusses a PV inverter case study to demonstrate the impact of the TIM layer on thermal stress, thermal unbalance, and reliability among the six switches of the applied power module. Finally, Section V concludes this article.

II. TIMs Testing Under Thermal Shock Test

Fig. 1 shows the entire work pipeline. A prototype was devised to investigate the clarity, which is detailed in Section II-A, and the test procedure is provided in Section II-B. Throughout the thermal shock test (TST), periodic offline measurements of the thermal parameters of the prototype are performed to track its degradation, at a frequency of every 200 cycles. Thermal resistance characterization is conducted by the structure function, which is explained in Section II-D.

A. Test Sample Preparation

To investigate whether the type of TIMs and the placement have a significant difference in the thermal interface layer, this study uses two commercially available thermal greases which shall be referred to as Dow Corning 340 Heat Sink Compound and HTSP50T and the properties related to the individual types of TIM are provided in Table I.

The test fixture is shown in Fig. 1, a prototype consisting of the IGBT module (FS25R12KT3) [25] assemble with PCB, and the TIMs applied to the IGBT module, and finally assemble with the heatsink. The starting thickness of the TIM is controlled by the thickness of the steel stencil 150 μm and screw torque 3 N.m, which is shown in Fig. 1(b). Then, according to the instructions of [26], the applied TIM is shown in Fig. 1(b) as well. The steel stencil pattern assists with providing collapse of the TIM during mounting, by allowing adjacent features to flow together, and thereby reduce the TIM layer thickness. The stencil was laid flat against the baseplate with the TIM applied at the edge and drawn over the stencil pattern to spread the TIM evenly, and with the stencil vertically removed a clear pattern of TIM is visible.

In the experiment, there are four test cases (Dow corning 340 in horizontal position, Dow corning 340 in vertical position, HTSP50T in horizontal position, and HTSP50T in vertical position), named as Case 1, Case 2, Case 3, and Case 4, respectively.

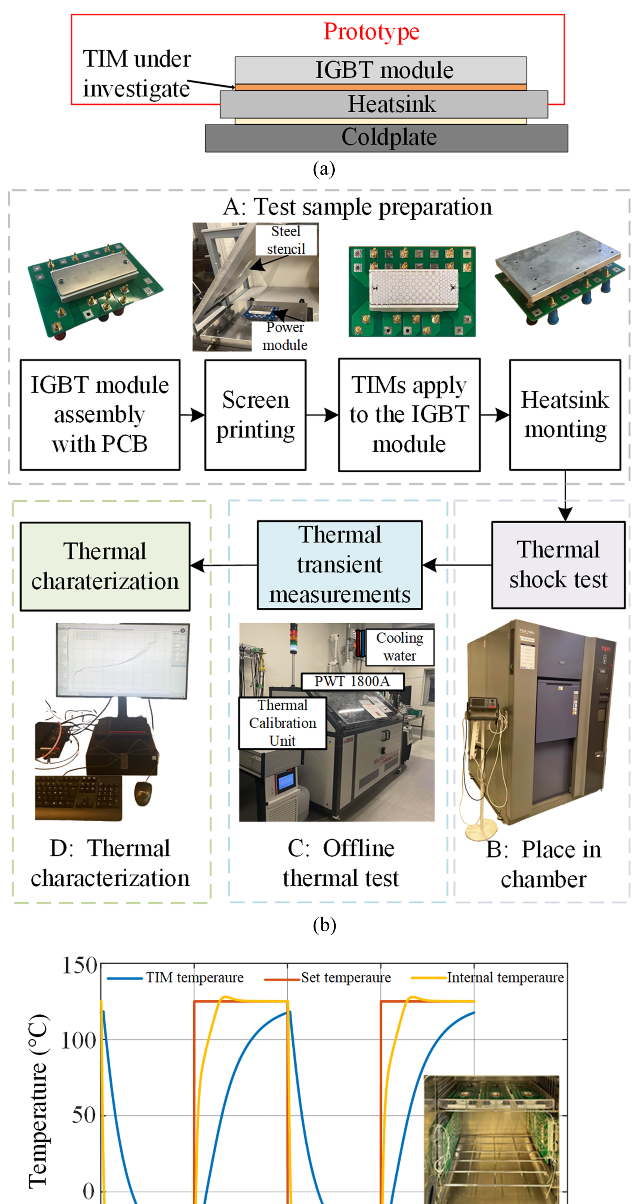


Fig. 1. Thermal shock test. (a) Cross section of the prototype. (b) Flow of the test. (c) Thermal profile.

Each case includes three test samples (module 1–3, module 4–6, module 7–9, and module 10–12).

B. Thermal Shock Test

This study utilizes the accelerate thermal shock test to reduce test time and promote the aging process. According to the JEDEC Thermal Cycling standard of JESD22-A104F [27], the temperature range is −40°C to 125°C, and the soak time of high and low temperatures is 5 min. Dealing with the above requirements, the test is executed a double air heating/cooling chamber. Fig. 1 presents an external view of the chamber and the samples mounted on the thermal shock platform inside the chamber. To ensure soak duration at the temperature prescribed by the JEDEC JESD22-A104F standard, a thermal cycle consisting of 15-min heating and 15-min cooling is selected. Furthermore, the heatsink block is equipped with thermocouples allow for characterization of temperature at the point near the interface of TIMs. The temperature profile is plotted in Fig. 1(c).

C. Transient Thermal Impedance Measurements

To characterize the thermal resistance and its associated degradation in the TIMs layer, the transient thermal impedance measurement is an effective and nondestructive way for the characterization without dismounting prototype, which could be used for TIM evaluation. As shown in Fig. 2, the thermal transient measurement involves following three steps.

1) *Calibration:* put a low sensing current I_{M} on the device under test in a thermostat and calibrate the *static* temperature-sensitive electrical parameters (TSEP).
2) *Cooling curve measurement:* add a high heating current I_{heat} to heat the device up, subsequently switch OFF I_{heat} and measure the *time-resolved* TSEP voltage at I_{M} to obtain a cooling curve.
3) *Post-processing:* convert the cooling curve into the thermal impedance curve as well as the structure function (extract thermal resistance), which can be automated and performed using commercially available software, T3Ster-Master in this study [28]. Details of these conversions should refer to [29] and [30].

The transient thermal impedance measurements are carried out using the commercially available Mentor Graphics Power Tester as shown in Fig. 1(b) [31]. Offline measurements are performed periodically to characterize the thermal resistance of the samples during the test, at a frequency of every 200 cycles by the experiment kit.

The measuring circuit is shown in Fig. 3, where I_{heat} is the load current applied to the IGBT device, mainly used to heat up the device; I_{M} is a small current that is used to measure the junction temperature by utilizing the collector–emitter voltage $V_{\mathrm{CE,sat}}$ as a TSEP; the gate voltage V_{ge} keeps the channel of the IGBT activated. An external temperature control unit keeps the cooling plate at a constant temperature. The exact parameters are listed in Table II. The junction temperature T_{j} has a linear relationship with the collector–emitter voltage under the sense current $V_{\mathrm{CE,sat}}$ of IGBT [32], which can be expressed as

$$T_{\mathrm{j}} = kV_{\mathrm{CE,sat}}(I_{\mathrm{c}}) + b. \tag{1}$$

To estimate T_{j} in real time through (1), the coefficients k and b have to be obtained before the thermal transient measurements [33]. After stabilizing the junction temperature of the device at different temperature points, the sense current I_{M} is applied to measure the collector–emitter voltage $V_{\mathrm{CE,\ sat}}$, correspondingly [20]. The coefficients k and b can be solved by the least squares method. In addition, it is imperative to ensure consistency between the device's gate bias conditions and test

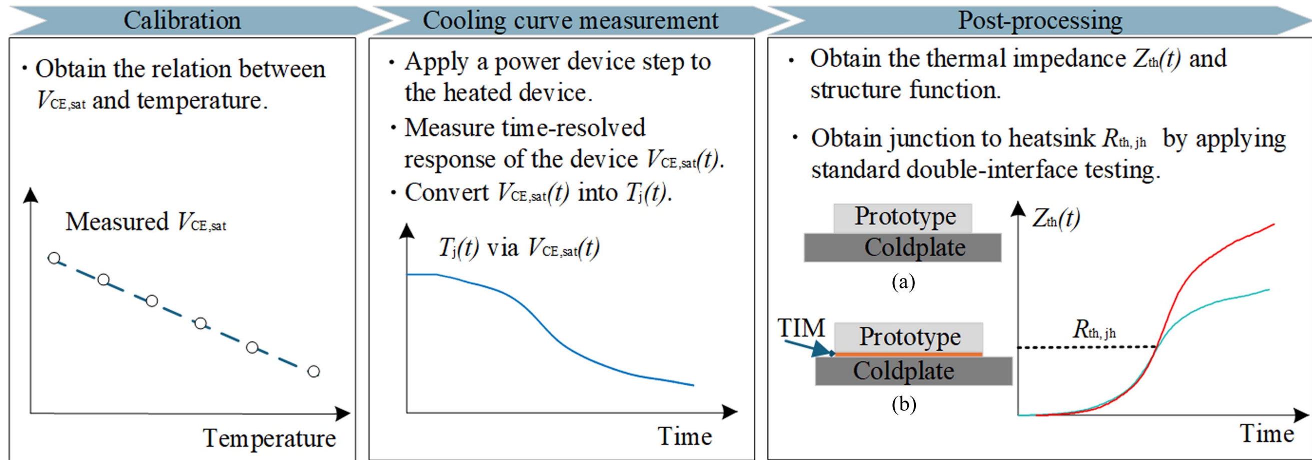


Fig. 2. Procedure of thermal transient measurement.

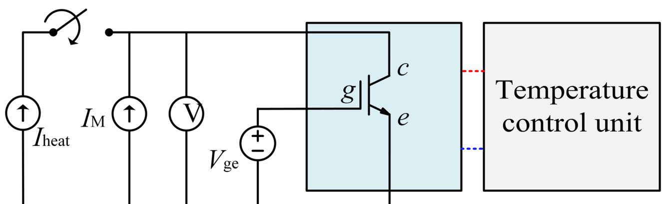


Fig. 3. TSEP method testing circuit.

TABLE II
EXPERIMENTAL PARAMETERS

Parameter	Value
Heating current I_{heat}	25 A
Sensing current I_M	100 mA
Gate voltage V_{ge}	15 V
Heating time	300 s
Cooling time	300 s
Coolant temperature	25°C
Temperature sampling frequency	1 MHz

current with the parameters specified for the thermal transient measurements.

D. Thermal Resistance Characterization

Structure function is provided in the standard JEDEC JESD51-14 to identify the thermal impedance from the junction to the ambient. Fig. 4(a) shows the junction-to-ambient thermal resistance with accumulated temperature cycles of the prototype. Ten structure function curves are measured before and after the thermal shock test. The thermal resistance from the bottom baseplate to the top heatsink, marked as $R_{\text{th-TIMs}}$, is to analyses the thermal resitance of the TIMs. To explore the thermal distribution among the module, each sample measures chips of S_1, S_3, S_6 as shown in Fig. 4(d). In the prototype, based on the thermal model in Fig. 4(b) and (c), thermal resistance increase comes from following two parts.

1) *Module package:* related aging, e.g., die solder and substrate solder aging.
2) *TIMs:* impaired interface integrity and aging.

To characterize the thermal resistance, analysis involves following three primary steps.

1) *Obtain the thermal resistance increase resulting from the prototype:* thanks to the transient dual interface test method [30], it is possible to determine the separation point between the heatsink (bottom prototype surface) and cold plate, as well as to obtain the thermal resistance increase resulting from both the module package and TIMs. The principle of the determination of the junction-to-heatsink thermal resistance of the power devices is shown in Fig. 2. Two Z_{th} curves are required to measure with two different contact interface conditions: with and without TIM, which causes the two Z_{th} curves to separate at one point. Because the heat paths only differ at the bottom surface of the prototype (heatsink surface), those two Z_{th} curves are always consistent from the junction-to-heatsink surface. Therefore, the transient thermal impedance $Z_{\text{th}}(t)$, which is specified at the splitting point, is assumed to be the junction-to-heatsink thermal resistance (R_{thjh}) of the prototype.
2) *Obtain thermal resistance change from module package only:* with high confidence of no degradation at baseplate, by pulling curves together based on high confidence of no degradation at baseplate, the thermal resistance increases from module package can be obtained individually.
3) *Calculate thermal resistance change from TIMs:* after obtaining the thermal resistance from the prototype and the internal module package, based on the thermal model in Fig. 4(b) and the physical structure of the sample in Fig. 4(c), the difference between the two is the thermal resistance increase resulting from TIM only.

To clarify the thermal resistance characterization of the prototype, Module 5 is selected as a representative case study. As shown in Fig. 2, the thermal impedance curves are measured

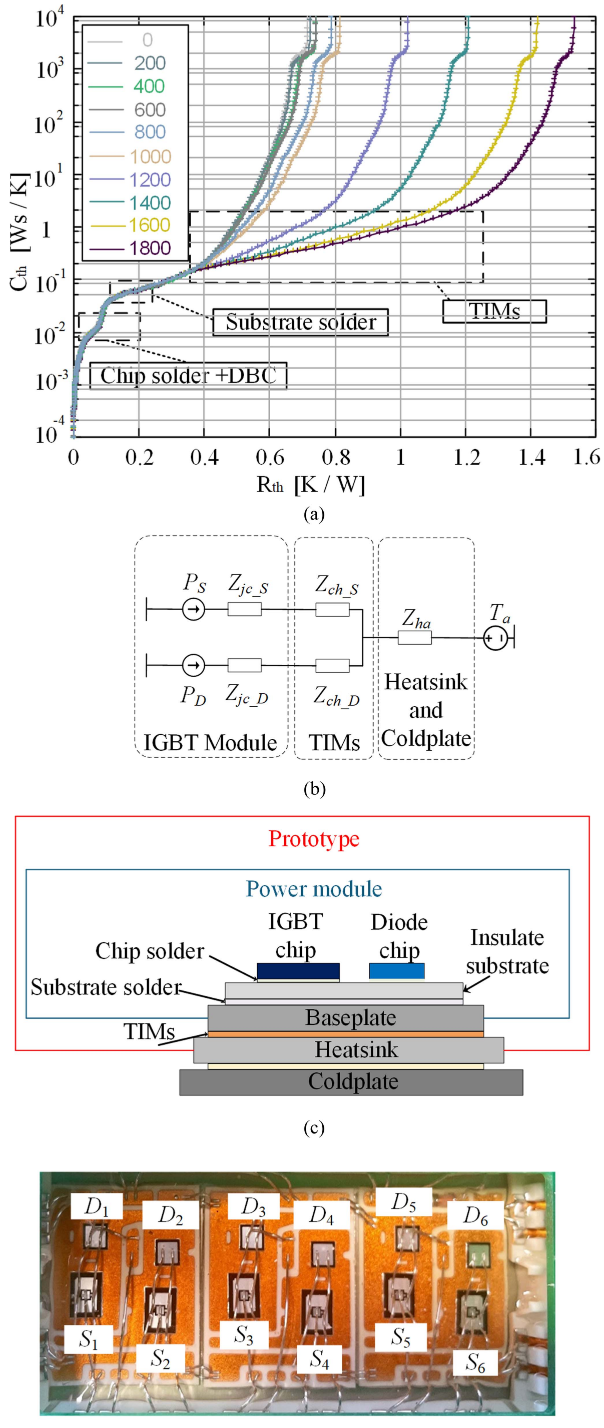


Fig. 4. Thermal resistance characterization analysis. (a) Structure function. (b) Thermal model for IGBT modules with TIMs and heatsinks. (c) Internal physical structure of the sample. (d) Layout of the IGBT module.

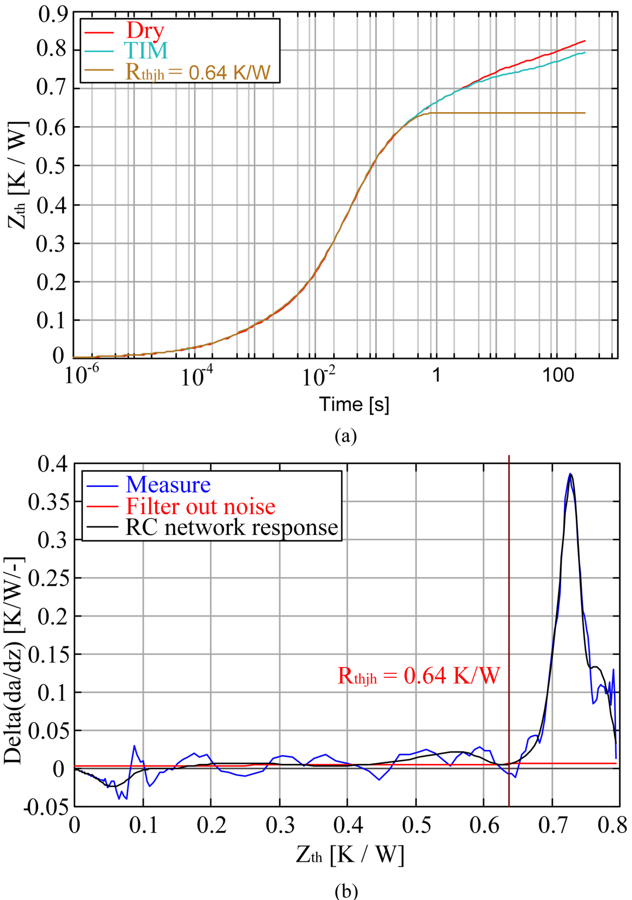
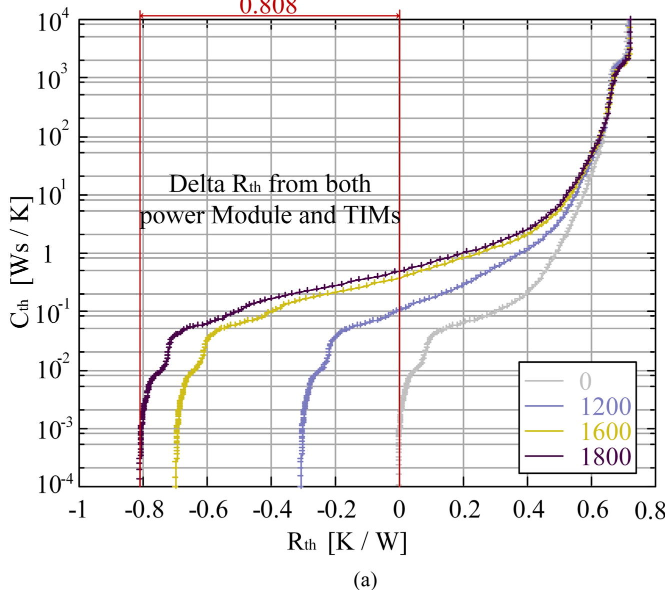


Fig. 5. Determination of the thermal resistance from junction to heatsink. (a) Thermal impedance curves under two different interface conditions(dry and TIMs) (b) Delta(da/dz) curve.

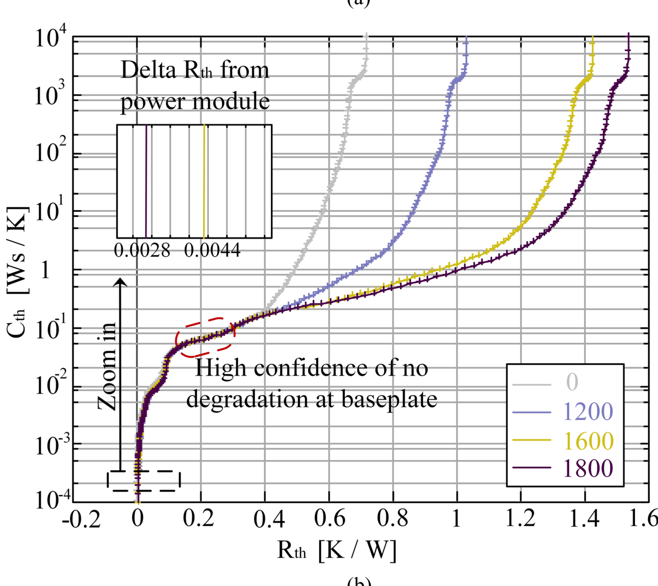
under two different interface conditions: dry and with TIM applied. In Fig. 5(a), the separation point of the two curves helps determine the thermal resistance from the junction to the heatsink(R_{thjh}). Meanwhile, a delta(da/dz) curve (the derivative da/dz is the slope of the Z_{thjh}-curve plotted with a logarithmic timescale) is defined in the standard [30] to justify the separation point between the heatsink and cold plate quantitatively, which is shown in Fig. 5(b). The obtained R_{thjh} is shown in Fig. 5. Each measurement has been repeated three times to avoid possible random effects during the measurement.

Before the thermal shock test, the initial R_{thjh} of the tested prototype is 0.64 K/W. After aligning the curves based on the bottom surface of heatsink, the total increase in thermal resistance including contributions from both the module package and the TIM is 0.808 K/W at the end of the test, as shown in Fig. 6(a). Meanwhile, by pulling curves together based on high confidence of no degradation at baseplate, the thermal resistance increases attributed solely to the module package is −0.0028 K/W, as shown in Fig. 6(b). Consequently, the difference between the two, representing the thermal resistance increase due to TIM layer, is therefore calculated as 0.8108 K/W.

The thermal resistance in power module showed negligible variation throughout the cycling test. In contrast, a large increase in thermal resistance was observed in the TIM layer. The thermal resiatance increase result from Module 5 clearly demonstrates that the dominant contribution to the overall thermal resitance increase originates from the TIM layer rather than the internal module packaging.



(a)



(b)

Fig. 6. Thermal Resistance increase. (a) From both module package and TIMs. (b) From module package.

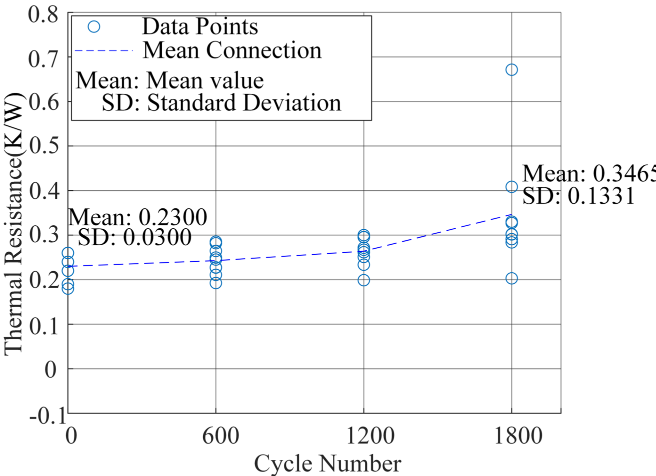


Fig. 7. Probability density curves of thermal resistance of TIMs in Case 1.

TABLE III
MEAN VALUE AND STANDARD DEVIATION OF THERMAL RESISTANCE UNDER DIFFERENT CASES

NO.	Mean	Standard deviations
Case 1 cycle 0	0.23	0.03
Case 1 cycle 1800	0.3465	0.1331
Case 2 cycle 0	0.2256	0.0230
Case 2 cycle 1800	0.3977	0.2234
Case 3 cycle 0	0.2267	0.0245
Case 3 cycle 1800	0.3365	0.1081
Case 4 cycle 0	0.2389	0.0262
Case 4 cycle 1800	0.6444	0.2814

III. UNCERTAINTY ANALYSIS IN THERMAL RESISTANCE AMONG THE CHIPS IN THE MODULE

To investigate the uncertainty of thermal resistance from TIMs, a comprehensive database has been derived from the structure function in Section II.

A. Uncertainties Caused by TIM

TIMs degrade over time due to thermal resistance changes influenced by various operational and environmental conditions. This section delves into the uncertainty analysis of these thermal resistance increases, and the variability on TIMs in Case 1 as shown in Fig. 7, with the corresponding indicators compared with other cases given in Table III. All samples show a general increase in thermal resistance as the number of cycles increases. This could be due to material degradation or accumulated damage over time.

For the same TIMs in different placement directions, the vertically placed TIMs (Case 2, Case 4) shows a larger increase in thermal resistance, which may be due to the influence of gravity or the different internal stress distribution, especially for HTSP50. Given that HTSP50T has a lower viscosity and thus, more affected by gravity, the orientation of its placement plays a significant role compared to Dow corning 340.

For different TIMs with the same placement direction, both show a similar increasing trend in thermal resistance when orientation horizontally. However, the increase in thermal resistance for HTSP50T is more gradual due to its significantly higher thermal conductivity compared to Dow Corning 340.

The above assessments indicate that the degradation of the interface thermal resistance between power module and heatsink precipitates the junction temperature increase of the power module. Different materials and placement exhibit varying trends in thermal resistance even under identical external conditions. Choosing the appropriate material and placement is critical to

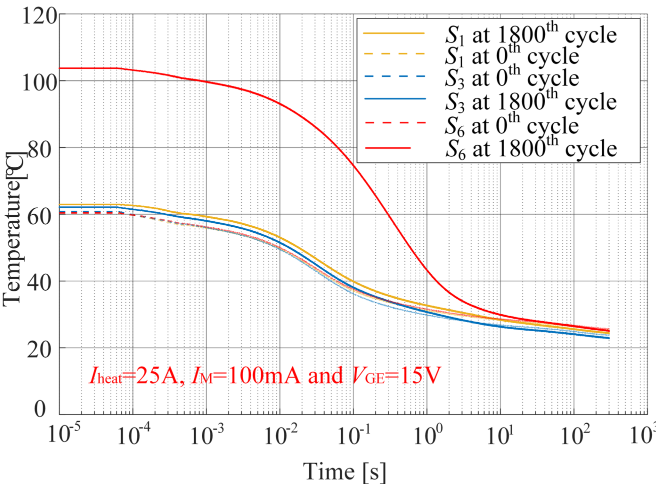


Fig. 8. Comparison of Cooling curves for module 5 between 0 th cycle and 1800 th cycle.

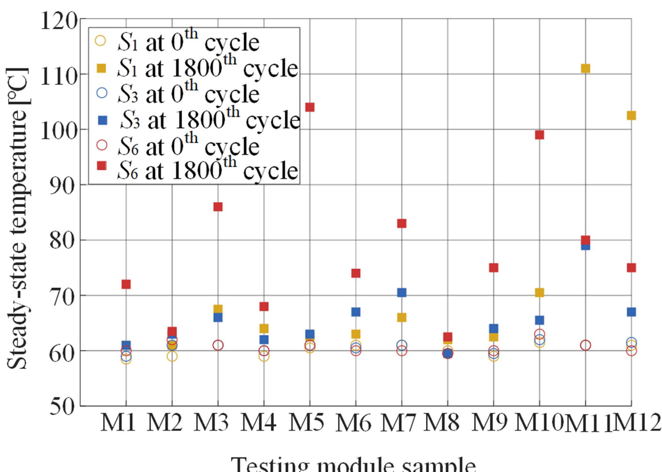


Fig. 9. Comparison of steady state junction temperature for all modules between 0 th cycle and 1800 th cycle.

ensuring that the device maintains optimal performance under expected operating conditions.

B. Uncertainties Caused by Thermal Imbalance Among a Power Module

In this study, a significant thermal imbalance was observed among the chips in module 5 after TST. As depicted in the cooling curves in Fig. 8, clear variations in the temperature responses of different chips under identical conditions are evident, with temperature differences even reaching up to 41.5°C. To provide statistical results, the corresponding steady state junction temperature of all modules are compared before TST and after TST in Fig. 9.

As shown in Fig. 9, the thermal imbalance phenomenon was observed across all 12 modules. As summarized in Table IV, at cycle 0, the thermal imbalance between chips within each module is minimal, the temperature difference generally <3°C, indicating a highly uniform initial temperature distribution.

TABLE IV
DISTRIBUTION OF THE STEADY STATE JUNCTION TEMPERATURE DIFFERENCES AMONG ALL THE MODULES

Cycle NO.	Cycle 0	Cycle 1800
Maximum (°C)	3.0	41.5
Minimum (°C)	0.0	2.5
Mean	1.04	18.79
Standard deviations	0.81	13.58

However, at cycle 1800, the temperature variation increases significantly, with a mean value of 18.79°C and a standard deviation of 13.58°C. The maximum temperature difference within the same module reaches 41.5°C, demonstrating substantial temperature nonuniformity in many modules after TST. These statistical results show that as the number of cycles increases, the thermal imbalance trend is common among modules rather than an isolated case.

To investigate the thermal imbalance phenomenon in the power module, Module 5 is selected as a representative case study. In other words, the thermal imbalance in Module 5 is the junction temperature difference among different chips in Module 5. Therefore, the junction temperature T_j formula is important, which can be expressed as

$$T_j = T_{cool} + P_{loss} \times (R_{th,j_c} + R_{th,c_cool}) \quad (2)$$

where T_{cool} is the coolant temperature, an external temperature control unit keeps the cooling plate at a constant temperature 25°C as listed in Table II, P_{loss} is the power loss of the chips, R_{th,j_c} is the thermal resistance from the junction to the case (bottom baseplate layer as shown in Fig. 4(c), R_{th,c_cool} is the thermal resistance from the case to the coldplate.

For a multichip power module, according to the above formula, thermal imbalance in power modules can arise from multiple factors, including

1) Nonuniform power losses P_{loss} across the chips.
2) Cooling temperature.
3) Thermal coupling effects between neighboring chips inside the module.
4) Variations in thermal resistance, which include both:
    1) internal thermal resistance R_{th,j_c} within the module package (e.g., die attach, substrate solder);
    2) external thermal resistance R_{th,c_cool} due to the TIMs.

In the transient thermal test, all samples under the same testing conditions: T_{cool} is constant because the cooling plate temperature is kept unchanged, P_{loss} is constant because the power applied is controlled. The factor of power loss and cooling temperature can be excluded as potential causes. On the other hand, only one chip was activated and measured at a time, while all other chips remain in the OFF-state. Therefore, the effect of thermal coupling can be excluded.

When a thermal imbalance phenomenon is observed, the cause of the imbalance should be the changes of thermal resistance. Based on previous structure function analysis described

TABLE V
SPECIFICATIONS OF THE THREE-PHASE PV INVERTER

PV array rated power	1500 W
Rated current	4 A
DC-link voltage	700 V
Switching frequency	10 kHz
Output frequency	50 Hz
DC-link capacitance	340 uF
Resistive load	33 Ω

in Section II-D, the thermal resistance in module 5 (including the die attach and substrate layers) showed negligible variation throughout the test. In contrast, a large increase in thermal resistance was observed in the TIM layer. The results indicate that the thermal imbalance in module 5 is primarily caused by the changes in the TIM layer rather than by the internal parts of the power module.

In an ideal case, when all the chips in the power module are heated, the resulted junction temperature should be the same. The uniform temperature among the chips ensures the same temperature-related electrical parameters and thus good current sharing among them, which is a beneficial factor for long-term reliability of the semiconductor power module [34]. The uneven increase in the thermal resistance of TIMs leads to the thermal imbalance in the prototype. Thermal imbalances not only affect the chips performance but may also shorten their lifespan due to the thermal stress and fatigue on the semiconductor materials caused by temperature extremes. Therefore, understanding and addressing this thermal imbalance from TIMs is crucial for optimizing the reliability and efficiency of the overall device.

IV. IMPACT OF TIMS UNCERTAINTY ON THE POWER ELECTRONICS CONVERTER LIFETIME

To investigate the impact of TIMs uncertainty from semiconductor chip level to the converter system level, the experimentally verified the thermal properties in a converter. The change of TIMs plays a dominant role in thermal resistance increase and thermal imbalance, significantly impacting the lifetime assessment of the converter.

A. Experimental Testing Under Dynamic Operating Conditions on a PV Converter

To verify the uncertainty in a converter-level, a three-phase PV inverter is employed. The system specifications are given in Table V, while the physical hardware realization is shown in Fig. 10(b). The test bench uses a PV simulator to emulate the behaviour of a PV array and the dSPACE is used as the controller to implement the closed-loop control. Optic fiber is attached to the center of the chip surface of the power module as shown in Fig. 10(c). The junction temperature from the opened module is measured and recorded using the signal conditioner.

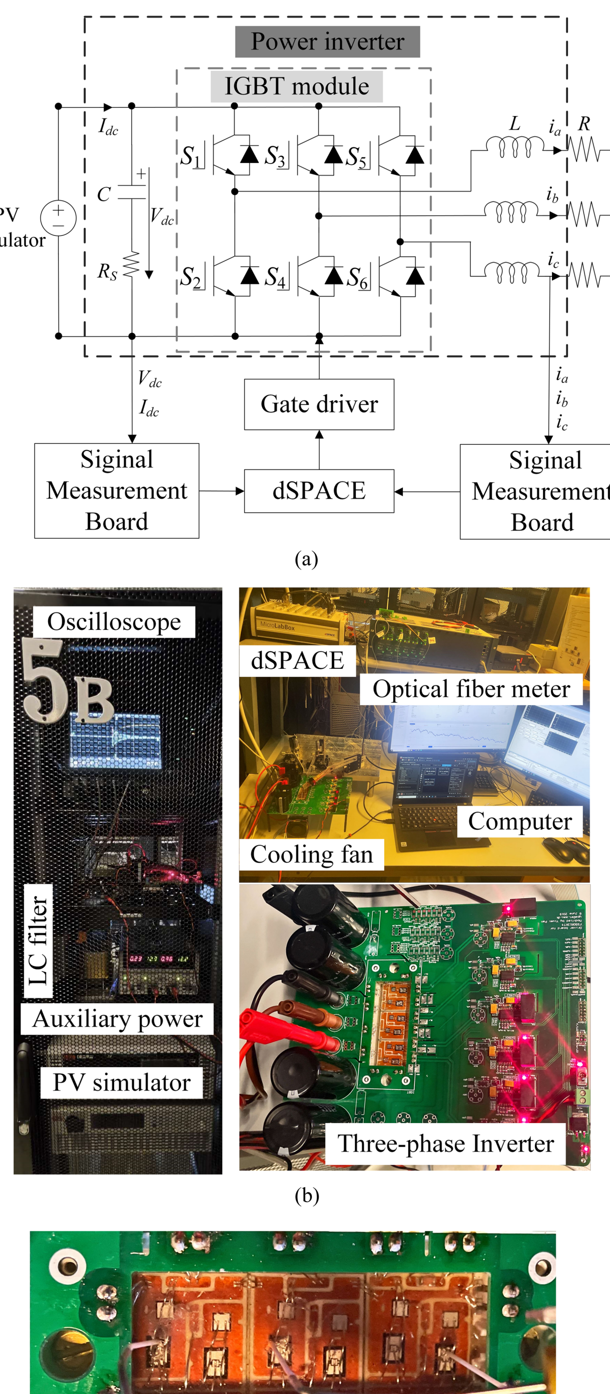


Fig. 10. Three-phase inverter prototype. (a) Inverter topology. (b) Hardware realization. (c) Measurement point of the optical fiber temperature sensor (OTG-F type from OPsens) [35] on the module.

To investigate the impact of TIMs uncertainty from semiconductor chip level to the converter system level, Module 5 is utilized equipped to the PV converter both before and after the thermal shock test. The junction temperature variation is a consequence of the power device loading. In this regard, the

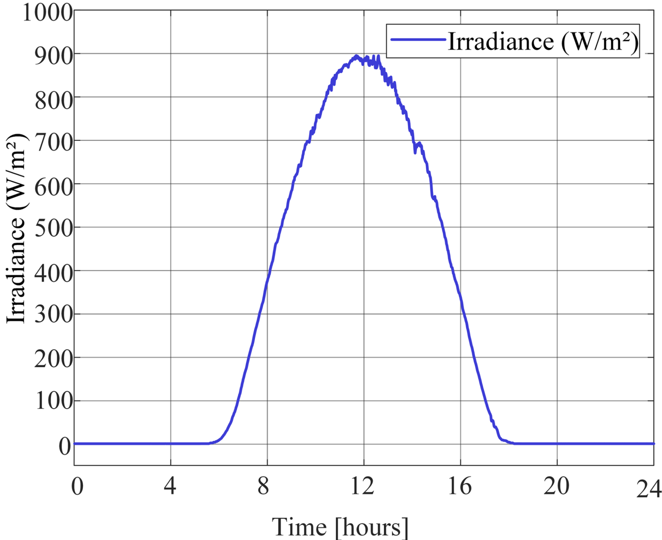


Fig. 11. One-day mission profile (irradiance and ambient temperature with a sampling rate of 1 min per sample) in the PV inverter.

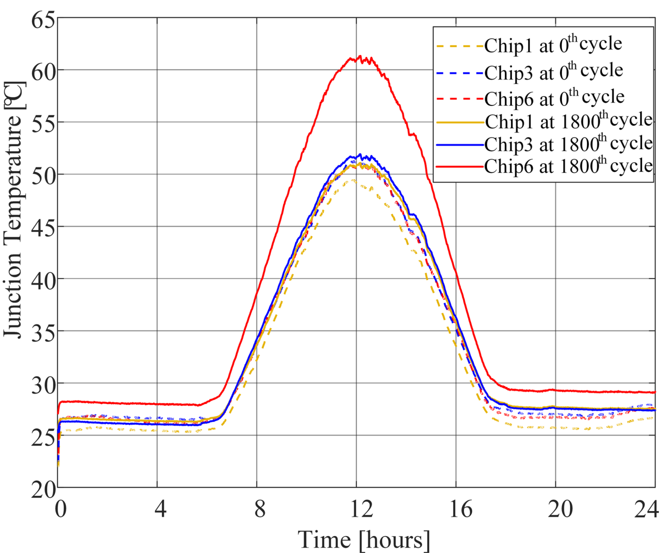


Fig. 12. Comparison of junction temperature with daily mission profiles for Module 5 between 0 th cycle and 1800 th cycle.

impact of TIMs degradations can be observed in the junction temperature variations in the PV inverters.

A mission profile is a representation of the operating condition of the system [36]. The solar irradiance and ambient temperature are considered as mission profiles of the PV systems, since the PV power production is strongly dependent on the two parameters. An example of a one-day mission profile during clear-day conditions is demonstrated in Fig. 11. In the experiments, a PV simulator was programmed to emulate the behavior of the PV array during a day. The corresponding power device junction temperatures can be observed in Fig. 12 for both module 5 before and after the thermal shock test.

Fig. 12 shows the junction temperatures for S_1, S_3, and S_6, observed with the one-day mission profile of the PV inverter with module 5 before and after the thermal shock test. It can be seen from Fig. 12 that the junction temperature in S_3 and S_6 is approximately 2°C higher compared to S_1 before the thermal shock test, and the reason is that the cooling fan is closer to S_1. Notably, after the thermal shock test, the junction temperature of S_6 in the PV inverter is much higher than the other chips, indicating thermal imbalance in the converter. This observation aligns with the results of the transient thermal test conducted on the prototype. According to the above results, the degradation of the TIMs has a strong influence on the long-term device junction temperature and, thus, the PV converter lifetime.

It is therefore important to model the thermal stress conditions of the power devices in the converter during the entire operation in order to apply the lifetime analysis discussed in the following section.

B. Impact on the Module-Level Reliability Analysis

Since the thermal loading profiles in Fig. 12 are random, it is difficult to directly map thermal performance to lifetime. It is required to employ a cycle counting algorithm, and the rain-flow counting algorithm is adopted in this article. For the selected lifetime model in [37], the algorithm is used to obtain the number of cycles, the temperature swing from the junction temperature profile. The overall process of the reliability assessment in the PV inverter is shown in Fig. 13. The lifetime model of the power module is given as

$$N_{\mathrm{f}} = A(\Delta T)^{-n} \tag{3}$$

where N_{f} is the number of cycle to failure. ΔT is the temperature swing. A, n are fitting parameters provided by the manufacturer. Based on [37], $A = 1.42 \times 12$, $n = -7.14$.

With the counted cycles, the accumulated damage can be obtained according to the Palmgren–Miner linear cumulative damage law, and is expressed by [38]

$$D = \sum \frac{n_j}{N_{\mathrm{f}_j}} \tag{4}$$

where n_j is the cycles to a certain stress and $N_{\mathrm{f}j}$ is the cycles to failure under the same stress. D is the damage level of the device, where the device fails when D equals to 1.

The reliability of the power device (e.g., one single component) can be evaluated by considering the cumulative density function (CDF) of the Weibull distribution [39]. This Weibull CDF *F(t)* is normally referred to as the unreliability function, which can be obtained as

$$F(t) = 1 - e^{-(t/\eta)^{\beta}} \tag{5}$$

where t is the operation time, β is the shape parameter and η is the scale parameter. In general, the unreliability function *F(t)* represents the proportion of failure population as a function of time. Then, the B_x lifetime, which represents the time when *x*% of a population is failed, of one power device can be obtained from the unreliability function, and the power device lifetime can be predicted. Here, we assume a Weibull shape parameter of $\beta = 3.5$ to derive the unreliability function.

The unreliability function with S_1 and S_6 both before and after TST is shown in Fig. 14. It can be seen from Fig. 14 that S_6 lifetime differs significantly before TST and after TST. For

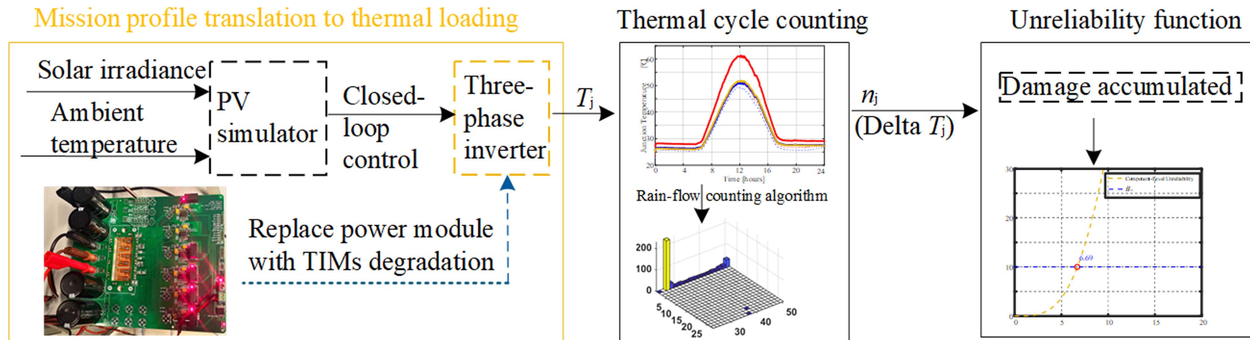


Fig. 13. Overall process of the reliability assessment in the PV inverter.

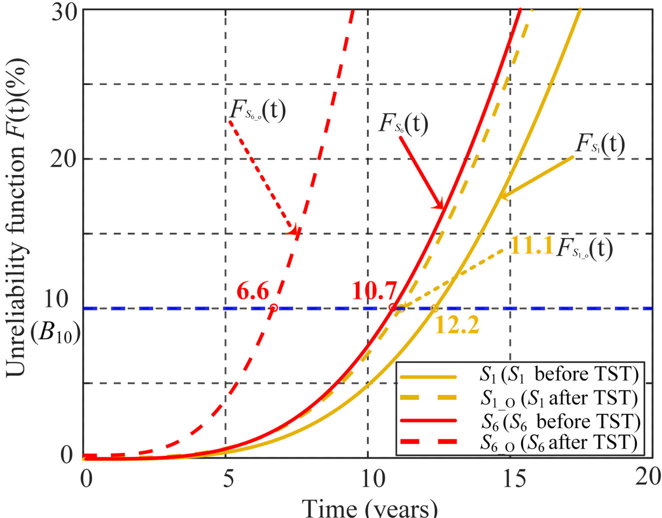


Fig. 14. Unreliability function with S_1 and S_6 both before and after TST.

instance, the B_{10} lifetime of S_6 with and without considering the degradation of TIMs is 6.6 and 10.7 years, respectively. This means that lifetime of the power device in the case is underestimated by 4.1 years if the TIMs degradation is not considered. This will inevitably lead to a significant overestimation in the maintenance costs of converters during the entire operation and, thus, the cost during the design phase. Similar deviations are also observed among different chips before and after TST. Specifically, the B_{10} lifetime of S_6 and S_1 before TST is 10.7 and 12.2 years, respectively. The B_{10} lifetime of S_6 and S_1 after TST is 6.6 and 11.1 years, respectively. This indicates that if the thermal imbalance from TIMs is not taken into account, the lifetime of the converter is underestimated by 4.5 years. Power modules affected by thermal imbalance lead to significant differences in lifetime prediction results. In summary, it is clear from the results that the TIM layer change has a strong impact on the PV inverter lifetime prediction, and thus it should be taken into account when evaluating the PV inverter lifetime.

V. Conclusion

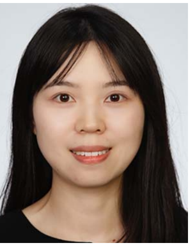
This study systematically investigates the uncertainty of the interfacial thermal resistance of the TIMs between power modules and heat sinks, and its impact on the junction temperature of semiconductor chips and system reliability. In addition, thermal imbalance among chips within the same module was observed, indicating that thermal resistance nonuniformity caused by TIMs will significantly affect chip performance, shortening semiconductor life. Through dynamic experimental verification in photovoltaic converters, it is further demonstrated that TIMs uncertainty plays a dominant role in system life assessment. The key conclusions are summarized as follows.

1) The structure function analysis reveals that the thermal resistance in the power module shows negligible variation throughout the cycling test. In contrast, a large increase in thermal resistance is observed in the TIM layer.
2) For all tested power modules, the thermal resistance of TIMs rises significantly as the thermal cycling progresses. Even with 3 modules 9 chips per case, significant differences in thermal resistance values were observed over time. This indicates that the variability of the TIM interfaces is substantial, and from the practical industrial perspective, a larger sample size would be expected to yield an even broader distribution.
3) For the single module, significant thermal imbalance among chips within the same module is observed. The analysis indicates that the thermal imbalance in the power module is primarily caused by the variations in the TIM layer, rather than the internal module package. Statistical results confirm that thermal imbalance is a common trend between modules, rather than an isolated case.
4) Dynamic experimental in photovoltaic converter reveals that the change of the TIMs layer has a considerable impact on the power module lifetime. In that case, the power module lifetime prediction can be deviated by 4.1 years, if the impact of the change of the TIMs layer is not taken into account. In addition, if the thermal imbalance caused by TIM layer is neglected, the lifetime prediction can deviate by 4.5 years.

References

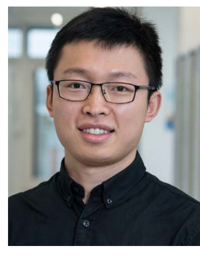
[1] Z. Ni, X. Lyu, O. P. Yadav, B. N. Singh, S. Zheng, and D. Cao, "Overview of real-time lifetime prediction and extension for SiC power converters," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7765–7794, Aug. 2020.

[2] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, “Condition monitoring for device reliability in power electronic converters: A review,” *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2734–2752, Nov. 2010.
[3] H. Oh, B. Han, P. McCluskey, C. Han, and B. D. Youn, “Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review,” *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2413–2426, May 2015.
[4] Y. Zhang, H. Wang, Z. Wang, F. Blaabjerg, and M. Saeedifard, “Mission profile-based system-level reliability prediction method for modular multilevel converters,” *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6916–6930, Jul. 2020.
[5] P. D. Reigosa, H. Wang, Y. Yang, and F. Blaabjerg, “Prediction of bond wire fatigue of IGBTs in a pv inverter under a long-term operation,” *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7171–7182, Oct. 2016.
[6] A. Wintrich, N. Ulrich, T. Werner, and T. Reimann, *Application Manual Power Semiconductors*. Nuremberg, Germany: Semikron Int. GmbH, 2015.
[7] E. Deng, Z. Zhao, P. Zhang, J. Li, and Y. Huang, “Study on the method to measure the junction-to-case thermal resistance of press-pack IGBTs,” *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4352–4361, May 2018.
[8] H. Wang et al., “A thermal network model for multichip power modules enabling to characterize the thermal coupling effects,” *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 6225–6245, May 2024.
[9] A. S. Bahman, K. Ma, and F. Blaabjerg, “A lumped thermal model including thermal coupling and thermal boundary conditions for high-power IGBT modules,” *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2518–2530, Mar. 2018.
[10] H. Li et al., “Thermal coupling analysis in a multichip paralleled IGBT module for a DFIG wind turbine power converter,” *IEEE Trans. Energy Convers.*, vol. 32, no. 1, pp. 80–90, Mar. 2017.
[11] R. Schnell, M. Bayer, and S. Geissmann, “Semiconductor power devices: Physics, characteristics, reliability,” ABB, Appl. Note 5SYA 2093-00, Switzerland, Thermal Des. Temp. Ratings IGBT Modules, 2013.
[12] L. Feller, S. Hartmann, and D. Schneider, “Lifetime analysis of solder joints in high power IGBT modules for increasing the reliability for operation at 150∘,” *Microelectronics Rel.*, vol. 48, no. 8, pp. 1161–1166, 2008, 19th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2008). [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271408001832
[13] N. Patil, J. Celaya, D. Das, K. Goebel, and M. Pecht, “Precursor parameter identification for insulated gate bipolar transistor (IGBT) prognostics,” *IEEE Trans. Rel.*, vol. 58, no. 2, pp. 271–276, Jun. 2009.
[14] D. Katsis and J. vanWyk, “A thermal, mechanical, and electrical study of voiding in the solder die-attach of power MOSFETs,” *IEEE Trans. Compon. Packag. Technol.*, vol. 29, no. 1, pp. 127–136, Mar. 2006.
[15] T. Kim and T. Funaki, “Thermal measurement and analysis of packaged SiC MOSFETs,” *Thermochimica Acta*, vol. 633, pp. 31–36, 2016. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0040603116300260
[16] D. Xiang, L. Ran, P. Tavner, A. Bryant, S. Yang, and P. Mawby, “Monitoring solder fatigue in a power module using case above ambient temperature rise,” *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2578–2591, Nov./Dec. 2011.
[17] C. Choe, C. Chen, S. Nagao, and K. Suganuma, “Real-time acoustic emission monitoring of wear-out failure in SiC power electronic devices during power cycling tests,” *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4420–4428, Apr. 2021.
[18] I. Austrup, C. H. van der Broeck, S. Kalker, T. B. Albert, F. Janoth, and R. W. De Doncker, “Diagnosing thermal-interface aging of power devices using self-sensing,” *IEEE Trans. Power Electron.*, vol. 40, no. 3, pp. 4386–4398, Mar. 2025.
[19] Y. Wu et al., “Unveiling the degradation mechanism of polymer-based thermal interface materials under thermo-oxidative condition,” *IEEE Trans. Device Mater. Rel.*, vol. 24, no. 4, pp. 514–521, Dec. 2024.
[20] X. Ma, J. Wang, Z. Wei, and L. Ding, “Online prediction method for the remaining useful life of power devices based on composite indicator,” *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 10326–10338, Aug. 2024.
[21] Y. Zhang, R. Wu, F. Iannuzzo, and H. Wang, “Aging investigation of the latest standard dual power modules using improved interconnect technologies by power cycling test,” *Microelectronics Rel.*, vol. 138, 2022, Art. no. 114740. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271422002645
[22] P. Heimler, M. Günther, C. Künzel, J. Lutz, and T. Basler, “Influence of thermal interface material using discrete Si-IGBTs and consideration of power cycling conditions,” *Microelectronics Rel.*, vol. 150, 2023, Art. no. 115089. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271423001890
[23] J. Tompkins, A. M. Garcia, D. Huitink, and H. Liao, “Module-level thermal interface material degradation in halt,” *J. Electron. Packag.*, vol. 145, no. 1, 2022, Art. no. 011106, doi: 10.1115/1.4056030.
[24] Y. Zhang, H. Wang, Z. Wang, Y. Yang, and F. Blaabjerg, “Impact of the thermal-interface-material thickness on IGBT module reliability in the modular multilevel converter,” in *Proc. 2018 Int. Power Electron. Conf.*, 2018, pp. 2743–2749.
[25] Infineon, “IGBT module fs25r12kt3,” Infineon Technologies AG, Tech. Rep., 2023, accessed: Feb. 26, 2025. [Online]. [Online]. Available: https://www.infineon.com/cms/en/product/power/igbt/igbt-modules/fs25r12kt3/
[26] Baginski, “Application of screen print templates to paste thermal grease within IGBT modules,” Infineon, Warstein, Application Note AN-2006-02, 2005.
[27] JEDEC Solid State Technology Association, JESD22-A104F Temperature Cycling, JEDEC Solid State Technology Association Std., 2020.
[28] Siemens, “T3Ster Master Thermal Transient Evaluation Tool User and Reference Guide, Siemens AG,” n.d., Accessed: Jul. 28, 2025.
[29] JEDEC, “EIA/JESD 51-1: Integrated Circuits Thermal Measurement Method—Electrical Test Method (Single Semiconductor Device),” JEDEC Solid State Technol. Assoc., Tech. Rep., 1995.
[30] *JESD51-14: Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction-to-Case of Semiconductor Devices With Heat Flow Through a Single Path*, JEDEC Std., 2010.
[31] Mentor Graphics Power Tester Guide, Mentor Graphics Corporation, Wilsonville, OR, USA, 2020, [Online]. [Online]. Available: https://www.mentor.com/products/mechanical/micred/power-tester-1800a/
[32] Y. Avenas, L. Dupont, and Z. Khatir, “Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters—A review,” *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3081–3092, Jun. 2012.
[33] Y. Peng, Q. Wang, H. Wang, and H. Wang, “An on-line calibration method for TSEP-based junction temperature estimation,” *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 13616–13624, Dec. 2022.
[34] X. Li et al., “Thermal imbalance among paralleling chips in power modules and the impact from traction inverter system view,” *IEEE Trans. Ind. Electron.*, vol. 70, no. 3, pp. 2231–2240, Mar. 2023.
[35] Opsens Solutions, “Fiber optic temperature sensor,” Opsens Solutions, Tech. Rep., Sep. 2023, Accessed: Sep. 6, 2023. [Online]. [Online]. Available: https://opsens-solutions.com/products/fiber-optic-temperature-sensors/otg-f/
[36] M. Musallam, C. Yin, C. Bailey, and M. Johnson, “Mission profile-based reliability design and real-time life consumption estimation in power electronics,” *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2601–2613, May 2015.
[37] Y. Zhang, H. Wang, Z. Wang, Y. Yang, and F. Blaabjerg, “Impact of lifetime model selections on the reliability prediction of IGBT modules in modular multilevel converters,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 4202–4207.
[38] H. Huang and P. A. Mawby, “A lifetime estimation technique for voltage source inverters,” *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4113–4119, Aug. 2013.
[39] ZVEI, “How to measure lifetime for robustness validation–step by step,” ZVEI, Berlin, Germany, Tech. Rep., Nov. 2012.



Ziheng Wang (Student Member, IEEE) was born in Hebei Province, China, in 1997. She received the M.S. degree in electrical engineering from North China Electric Power University, Hebei, China, in 2021. She is currently working toward the Ph.D. degree in power electronics with Aalborg University, Aalborg, Denmark.

From December 2019 to June 2020, she was a Visiting Student with Technische Universität Berlin (TU Berlin), Berlin, Germany. Her research interests include reliability testing and thermal management from power electronic components to power converter systems.



Yi Zhang (Senior Member, IEEE) received the B.S. and M.S. degrees from Harbin Institute of Technology, Harbin, China, in 2014 and 2016, respectively, and the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 2020, all in electrical engineering.

He is currently an Assistant Professor with the Hong Kong Polytechnic University, Hong Kong. During 2020–2023, he was affiliated with multiple institutions as a DFF International Postdoctoral Research Fellow, including RWTH Aachen University, Aachen, Germany, Swiss Federal Institute of Technology Lausanne, Lausanne, Switzerland, and Massachusetts Institute of Technology, Cambridge, MA, USA. He was also a Visiting Scholar with the Georgia Institute of Technology, Atlanta, GA, USA, in 2018. His research focuses on advancing the reliability and sustainability of power electronics through design, testing, packaging, and condition monitoring.

Dr. Zhang was a recipient of the First Place Prize Paper Award of the IEEE Transactions on Power Electronics in 2021, and the IEEE Power Electronics Society Ph.D. Thesis Award in 2020. He is the Guest Associate Editor of IEEE TRANSACTIONS ON POWER ELECTRONICS.

Huai Wang (Senior Member, IEEE) received the B.E. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2007, and the Ph.D. degree in power electronics from the City University of Hong Kong, Hong Kong, in 2012.

He is currently a Professor with AAU Energy, Aalborg University, Aalborg, Denmark, where he leads the Group of Reliability of Power Electronic Converters (ReliaPEC) and the mission on Digital Transformation and AI. He was a Visiting Scientist with ETH Zurich, Switzerland, from August to September 2014, and with the Massachusetts Institute of Technology, Cambridge, MA, USA, from September to November 2013. He was with the ABB Corporate Research Center, Switzerland in 2009. His research interests include the fundamental challenges in modeling and validation of power electronic component failure mechanisms and application issues in system level predictability, condition monitoring, circuit architecture, and robustness design.

Dr. Wang was the recipient of the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society, in 2016, and the 1st Prize Paper Award from IEEE TRANSACTIONS ON POWER ELECTRONICS, in 2021. He serves as an Associate Editor for the *Journal of Emerging and Selected Topics in Power Electronics* and IEEE TRANSACTIONS ON POWER ELECTRONICS. He was Elected as a Member of the Danish Academy of Technical Sciences in 2023.