Third Quadrant Characteristic Model of Silicon Carbide MOSFET Considering Channel and Body-Diode Dynamics

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***Abstract*—A third quadrant characteristic (3rd-QC) model is proposed in this article, which accurately predicts the reverse-conduction behaviors of the silicon carbide (SiC) MOSFET. The proposed model considers the floating substrate effect, interface state effect, and temperature sensitive effect in detail, so the *I-V* trajectory from the source to the drain terminal could be efficiently evaluated. A dynamic test platform is designed to extract the 3rd-QC data more comprehensive than that provided in datasheet, thus the proposed model works well in a wide operation range of the SiC MOSFET. The proposed model decouples the currents in the metal–oxide–semiconductor (MOS) path and body-diode path, making the current-sharing ratio clearly observable. In order to verify the accuracy of the proposed model, a dynamic validating platform is implemented, and the complex converter is also simulated with the proposed model. The simulation results agree well with the experimental results, demonstrating the great potential of the proposed model in predicting the 3rd-QC behaviors of the SiC MOSFET.**

***Index Terms*—Device model, reserve conduction, silicon carbide (SiC) MOSFET, third quadrant characteristic (3rd-QC).**

I. Introduction

THE silicon carbide (SiC) MOSFET has lower conduction and switching losses than the silicon insulated-gate bipolar transistor (IGBT), which helps improving the power density and operation efficiency of the converters [1]. It is well known that the SiC MOSFET can operate in the third quadrant with the load current conducting from the source to the drain terminal [2]. In the third quadrant, if positive gate-source voltage v_{gs} is exerted, the metal–oxide–semiconductor (MOS) structure, namely, the channel and the N-drift layer would mainly carry the source-drain current i_{sd}, and i_{sd} is gradually shifting to the body-diode as v_{gs} decreases [3]. Fig. 1 shows the distribution of MOS current i_{mos} and body diode current i_{pn} inside the SiC MOSFET when the device operates in the third quadrant.

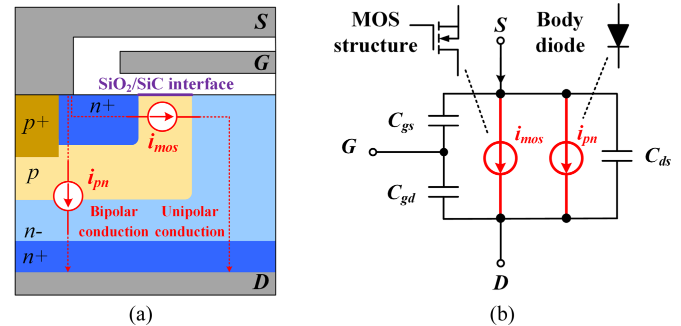

Fig. 1. Current distribution of SiC MOSFET in third-quadrant. (a) Typical planar VDMOSFET structure. (b) Simplified small-signal model.

The MOS structure is different with the body-diode according to the conduction mechanism, where the former belongs to the unipolar conduction while the latter belongs to the bipolar conduction [4]. Due to the inherent characteristics of the SiC MOSFET, the voltage drop of the MOS structure would be significantly lower than that of the body-diode [5]. Therefore, the SiC MOSFET can operate in the synchronous rectification (SR) mode to decrease the reverse-conduction loss of the natural freewheeling (NF) mode, while the Si IGBT can only conduct the reverse current by the external diode [6], [7]. This advantage of the SiC MOSFET has attracted many researchers to investigate the further details of the third quadrant characteristic (3rd-QC), and the full understanding of the 3rd-QC does help to the design of thermal dissipation and dead-time [8], [9], [10]. In [11], the regulation mechanism of v_{gs} on 3rd-QC is analyzed, and it shows the SiC MOSFETs have varied 3rd-QCs according to the different power-ratings and device types. The relationship of the source-drain voltage V_{SD} and junction temperature T_j is studied in [12], and the turn-off voltage is optimized to minimize the reverse-conduction loss under various currents. The current-sharing phenomenon, the body effect and the impact of parasitic NPN transistor are explained in detail with the finite-element simulation in [13].

With the deeper understanding on the 3rd-QC, the device model is tried to establish in some literatures. Since the specific device information is unavailable, the behavior model based on

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the data fitting is more popular than the physical model [14]. The researchers are mainly focused on selecting the appropriate fitting function for high accuracy, such as the quadratic polynomial functions with exponential terms [15], [16], mixed logarithmic-exponential function [17], and hyperbolic tangent function with quadratic terms [18]. However, the behavior models with complex function do not strictly distinguish i_{mos} and i_{pn}, and the i_{mos} behavior in the third quadrant is just supposed same as that in the first quadrant with small corrections to i_{pn}. These simplifications neglect the channel and body-diode dynamics in the 3rd-QC, which is not beneficial for the robust application of the SiC MOSFET. The most important thing is that few literatures have discussed about the data accuracy of the 3rd-QC until now. Almost all the existing models are based on the data extracted from the commercial curve tracer, which is an instrument for static measurement and neglects the dynamics of the SiC MOSFET operating in the converter. Moreover, most of literatures apply the double pulse test (DPT) to verify the models, but the DPT is suitable for validating the first quadrant characteristic (1st-QC) rather than the 3rd-QC [15], [16]. A few literatures use the single pulse test (SPT) for the model validation, but the SPT is also adopted by the commercial curve tracer [18]. Therefore, this self-verifying cycle might be unacceptable.

In this article, a 3rd-QCs model of the SiC MOSFET considering channel and body-diode dynamics is proposed. The innovations of this article are as follows:

1) The dynamic test platform (DTP) is proposed to obtain the 3rd-QC data considering the floating substrate effect (FSE), interface state effect (ISE), and temperature sensitive effect (TSE), which ensures the correction of the raw data in the modeling process.
2) The currents i_{mos} and i_{pn} are independently modeled, and the current-sharing ratio between two reverse-conduction paths could be clearly observed in the proposed model of SiC metal–oxide–semiconductor field-effect transistor (MOSFET).
3) The dynamic validating platform (DVP) emulating the SiC MOSFET behaviors in the converter is implemented to verify the accuracy of the proposed model.

The rest of this article is organized as follows. In Section II, the 3rd-QC behaviors of the SiC MOSFET are studied in detail. In Section III, the 3rd-QC model is established based on the DTP. In Section IV, the simulation and experimental validations are implemented based on the DVP and the single-phase inverter. Finally, Section V concludes this article.

II. Third Quadrant Characteristics

The 3rd-QC of the SiC MOSFET describes the *I-V* behaviors between the source and the drain terminals, and it is commonly obtained from the SPT, as shown in Fig. 2. Fig. 2(a) shows the SPT setup, which records the source-drain current i_{sd} under the static V_{GS} and pulse excitation V_{SD}. The typical 3rd-QC data of the SiC MOSFET (C3M0120065D, 650 V/ 120 mΩ) obtained from the SPT is given in Fig. 2(b) [19]. It is obvious that the 3rd-QC is highly dependent on the gate-source voltage. When V_{GS} is -20 V, the 3rd-QC has typical diode feature with a turn-ON voltage about 3 V. When V_{GS} is 20 V, the 3rd-QC

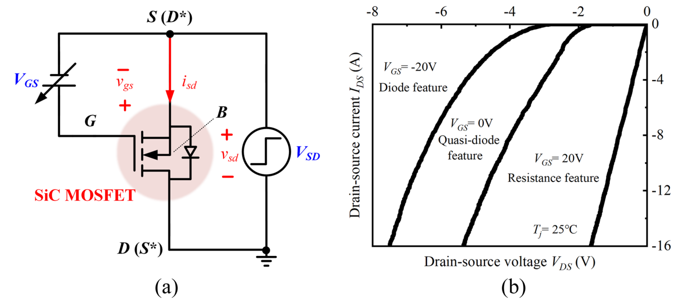
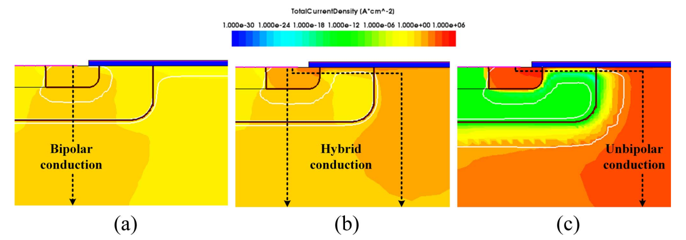


Fig. 2. 3rd-QC of SiC MOSFET. (a) SPT setup. (b) *I-V* data (FSE).



(a) (b) (c)

Fig. 3. Total current distribution with (a) V_{GS} =-20 V, (b) V_{GS} =0 V, and (c) V_{GS} =20 V.

shows resistance feature with linear *I-V* curve. When V_{GS} is zero, the 3rd-QC has the compromise quasi-diode feature, which has a turn-ON voltage about 1.8 V and the conductivity is between those of the diode feature and resistance feature. This phenomenon indicates that the channel is still turned on even if the gate-source voltage is zero, and it can be investigated by the numerical simulation based on the software TCAD.

In order to match the breakdown voltage of C3M0120065D, the thickness of the *N*-drift layer is set at 6 μm and other device parameters of the numerical simulation are same as given in [20]. Fig. 3 shows the simulation results of total current distributions inside the device under different V_{GS}. It is shown that most of carriers are conducted through the body-diode when V_{GS} is -20 V, and the SiC MOSFET operates in the bipolar conduction mode. When V_{GS} is 20 V and strong inversed channel is formed, the device will operate in unipolar conduction mode, where the electrons are moved through the channel and *N*-drift layer. When V_{GS} is zero, the source-drain current is shared by the MOS structure and the body-diode, which is taken as the hybrid conduction mode. It is significant that the current transfers from the body-diode to the MOS structure, and the conductivity of the device increases with the increased V_{GS}. This phenomenon can be explained by the FSE. Different to the 1st-QC test, the electric potentials of substrate terminal (*B*) and the source terminal (*S*) changes with the excitation V_{SD} in the 3rd-QC test as shown in Fig. 2(a). In this case, the drain terminal (*D*) is actually the physical source terminal ($S*$) and the source terminal (*S*) is the physical drain terminal ($D*$) because the inversed electrons move from $D(S*)$ to $S(D*)$ inside the device. So the gate-drain voltage V_{GD}, rather than gate-source voltage V_{GS}, is the gate bias that forming the channel, where V_{GD} has

$$V_{\mathrm{GD}} = V_{\mathrm{GS}} + V_{\mathrm{SD}} \tag{1}$$

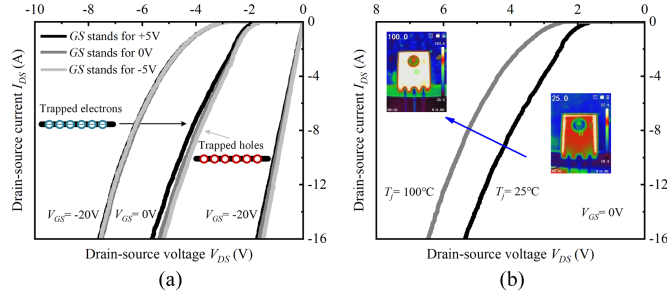


Fig. 4. Effects on 3rd-QC of SiC MOSFET. (a) ISE. (b) TSE.

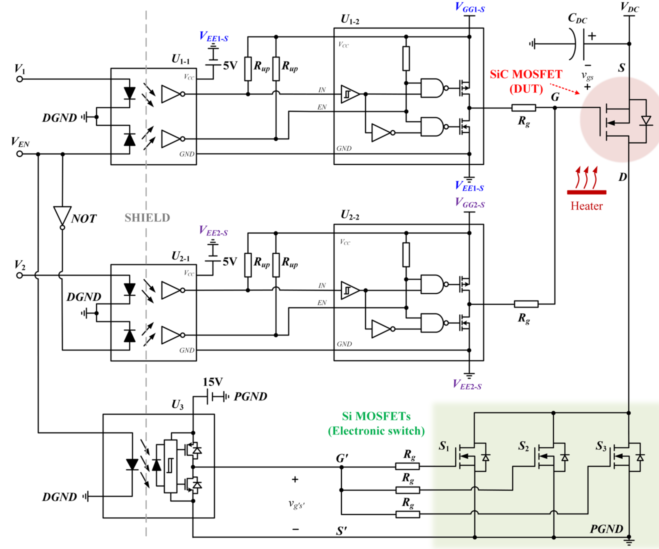


Fig. 5. Schematic of DTP.

Since the substrate-drain voltage V_{BD} (V_{BS*}) is floating, the changing electric potential influences the threshold voltage V_{TH3} of the channel in the 3rd-QC, and it has

$$V_{\mathrm{TH3}} = V_{\mathrm{FB}} + 2\psi_B + \frac{\sqrt{2\varepsilon_s q N_A}}{C_{\mathrm{ox}}}\sqrt{2\psi_B - V_{\mathrm{SD}}} \tag{2}$$

where V_{FB} is the flat-band voltage, ψ_B is the bulk potential, ε_s is the permittivity of SiC material, q is the elementary charge, N_A is the doping concentration, and C_{ox} is the oxide capacitance. Obviously, V_{GD} increases and V_{TH3} decreases with the increasing of V_{SD}. Once V_{GD} is high over V_{TH3}, the channel will be formed and i_{mos} is conducted through the MOS structure. This phenomenon caused by the FSE could be occurred in the case that V_{GS} is 0 V or below zero.

It is well known that the trapped carriers in the SiC/SiO$_2$ interface can influence the device conductivity [21]. So, it is necessary to consider the ISE when studying the 3rd-QC of the SiC MOSFET. Fig. 4 shows the effects on the measured 3rd-QC by different procedures. The gate-source bias V_{GS} statically stands for +5, 0, and -5 V for 1 h before the test by SPT, respectively. It is shown in Fig. 4(a) that the measured V_{DS} is more negative as the gate is positively biased. This is because of the numerous electrons trapped in the interface, which hinders the channel formation and increases the impendence from the source to the drain. The trapped charge Q_{it} has huge impact on the 3rd-QC due to the flat-band voltage V_{FB}, where it has

$$V_{\mathrm{FB}} = \varphi_{\mathrm{MS}} - \frac{Q_f + Q_{\mathrm{it}}}{C_{\mathrm{ox}}} \tag{3}$$

where ϕ_{MS} is the metal-semiconductor work function difference, Q_f is the fixed charge, Q_{it} is the charge trapped in the SiC/SiO$_2$ interface, which is directly influenced by the gate driving voltage v_{gs}. In the power converters, the dynamic voltage v_{gs} is a high frequency pulsewidth modulation (PWM) signal, which is different to the static bias V_{GS}. It is obvious that the conventional SPT can hardly consider the channel dynamics of the SiC MOSFET. Therefore, the 3rd-QC data extracted from the SPT is not accurate due to the ISE.

Fig. 4(b) shows the 3rd-QC of SiC MOSFET under TSE, where the samples are tested under different junction temperature T_j and the conductivity of the reverse-conduction path varies a lot according to T_j. In summary, it can be seen from Figs. 2 and 4 that the 3rd-QC of SiC MOSFET is greatly influenced by V_{GS}, V_{SD}, and T_j at the same time. So the special attentions should be paid to the 3rd-QC test. For commercial reasons, the physical information of the SiC MOSFET is commonly unavailable to the users. In this case, a test platform should be designed to extract the 3rd-QC data by considering the channel and body-diode dynamics. In this article, the device C3M0120065D (CREE, Planar, 650V/20A) is tested as a modeling example, and the modeling technology can be easily applied to other devices by the same testing and modeling procedures.

III. Methodology

A. Dynamic Test Platform

The DTP consists of two high-speed optocouplers $U_{1\text{-}1}$ and $U_{2\text{-}1}$ (TLP2168), an isolated driver U_3 (ACPL-W349), two tri-state gate drivers $U_{1\text{-}2}$ and $U_{2\text{-}2}$ (IXDD609), four pull-up resistance R_{up} (1 kΩ), five gate driving resistance R_g (10 Ω), three Si MOSFETs S_1-S_3 with low on-state resistance (IRFB3206, 2.4 mΩ), the capacitor bank on the dc bus C_{DC} (20 mF), and the device under test (DUT). The power supplies of $U_{1\text{-}2}$ are the positive $V_{GG1\text{-}S}$ and negative $V_{EE1\text{-}S}$, which take the source terminal of the DUT as the reference. Similarly, the power supplies $V_{GG2\text{-}S}$ and $V_{EE2\text{-}S}$ of $U_{2\text{-}2}$ is also based on the source terminal of the DUT. Two 5-V power supplies of $U_{1\text{-}1}$ and $U_{2\text{-}1}$ are based on $V_{EE1\text{-}S}$ and $V_{EE2\text{-}S}$, respectively. A 15-V power supply of U_3 takes PGND as the reference. Three Si MOSFETs S_1-S_3 are connected in parallel to form an electronic switch. The signals V_1, V_{EN}, and V_2 come from the digital signal processor (DSP) and provide the control signals of $U_{1\text{-}1}$, $U_{2\text{-}1}$, and U_3. $U_{1\text{-}2}$ and $U_{2\text{-}2}$ are tri-state gate drivers with high-level, low-level, and high-impedance outputs. If the signal V_{EN} is low-level, $U_{1\text{-}2}$ is enabled and $U_{2\text{-}2}$ is disabled. Then, the gate-source voltage of the DUT will be

$$v_{gs} = \begin{cases} V_{GG1-S} & V_1 = 0 \\ V_{EE1-S} & V_1 = 1 \end{cases} \tag{4}$$

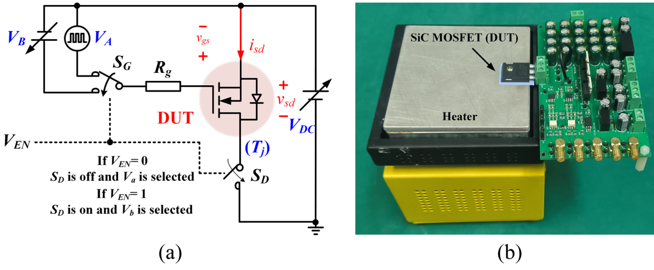


Fig. 6. DTP of SiC MOSFET. (a) Simplified schematic. (b) Prototype.

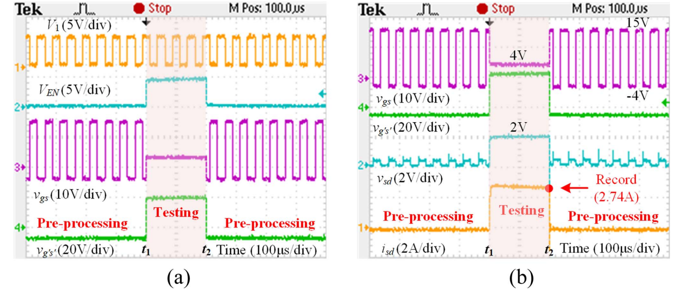


Fig. 7. Operation of DTP. (a) Controlling signals V_1, V_{EN}, $v_{\rm gs}$, and $v_{g's'}$. (b) 3rd-QC trajectories $v_{\rm gs}$, $v_{g's'}$, $v_{\rm sd}$, and $i_{\rm sd}$.

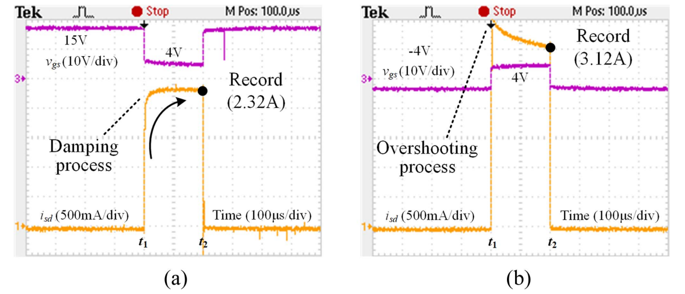


Fig. 8. $v_{\rm gs}$ and $i_{\rm sd}$ trajectories tested by SPT. (a) V_A is 15 V. (b) V_A is -4 V.

If the signal V_{EN} is high-level, $U_{2\text{-}2}$ is enabled and $U_{1\text{-}2}$ is disabled. In this case it has

$$v_{\rm gs} = \begin{cases} V_{GG2-S} & V_2 = 0 \\ V_{EE2-S} & V_2 = 1 \end{cases} \tag{5}$$

The signal V_{EN} also drives the electronic switch by U_3. When the electronic switch is turned ON, the bias $V_{\rm DC}$ is exerted on the source and drain terminal of the DUT. Then, the source-drain current can be measured. It should be noted that S_1-S_3 should be the power devices with low ON-state resistance to avoid large voltage drops on the electronic switch and cause additional measurement errors. Moreover, large capacitance of $C_{\rm DC}$ is favorable to ensure large discharging current without dropping $V_{\rm DC}$ obviously.

The simplified schematic of the DTP is shown in Fig. 6(a), and the dynamic test procedure could be introduced based on it. During the test, V_1 inputs the PWM signal and V_2 inputs the stable high-level or low-level signal. In this case, the driving signal V_A within $V_{GG1\text{-}S}$ and $V_{EE1\text{-}S}$, and the driving signal V_B of $V_{GG2\text{-}S}$ or $V_{EE2\text{-}S}$ are generated. When V_{EN} is 0, the switch S_D is off, and the single-pole double-throw switch S_G links the driving signal V_A to the gate of the DUT. This preprocess imitates the switching operation mode of the SiC MOSFET in the converter, and the channel of the DUT is activated to a dynamic state. When V_{EN} is 1, S_D is on and the testing signal V_B links to the gate of the DUT, then the DUT conducts the current from the source to the drain terminals and this current is recorded. The complete 3rd-QC of the DUT under the specific switching operation mode can be obtained by adjusting the bias voltage $V_{\rm DC}$ and the testing signal V_B. The prototype of the DTP is shown in Fig. 6(b), where the DUT is fixed on the heater (V-1010, Maximum temperature 400°C) by the bolt. The heater is used to set the junction temperature T_j of the DUT during the dynamic test, and the thermal equilibrium should be reached before each test.

Fig. 7 shows the operation of the DTP, where $V_{GG1\text{-}S}$ is 15 V, $V_{EE1\text{-}S}$ is -4 V, $V_{GG2\text{-}S}$ is 4 V, $V_{\rm DC}$ is 2 V, and T_j is 25°C. The frequency f_s and duty cycle D_s of V_A is 20 kHz and 50%, respectively, and V_B is fixed at $V_{GG2\text{-}S}$. It can be seen that $v_{\rm gs}$ of the DUT is a PWM voltage during the preprocessing duration before the moment t_1. In the testing duration from t_1 to t_2, $v_{\rm gs}$ is fixed at $V_{GG2\text{-}S}$ and the S_D is turned ON. Then i_{sd} at the moment t_2 (2.74 A) can be recorded as the current of the 3rd-QC with the bias $V_{\rm SD} = 2$ V and $V_{\rm GS} = 4$ V, After t_2, the DTP enters the preprocess again. It is obvious that v_{gs} and v_{sd} stably keep at 4 V and 2 V during the testing process respectively, which is due to the low ON-state resistance of S_D and large capacitance of $C_{\rm DC}$.

B. Analysis About Channel Dynamics

Different to the conventional SPT shown in Fig. 2, the proposed DTP includes a critical preprocess before the test. During the preprocess, the gate-source terminals of the DUT undertake the continuous switching excitation, which is very close to the situation in the converter. In order to compare the SPT and DTP-based test, Fig. 8(a) and (b) shows the $v_{\rm gs}$ and $i_{\rm sd}$ trajectories under the condition of SPT with $V_B = 4$ V, and V_A is fixed at 15 and -4 V during the preprocess, respectively. This static condition does not consider the channel dynamics of the SiC MOSFET. When the V_A keeps at 15 V before t_1, the recorded $i_{\rm sd}$ at t_2 is 2.32 A, which is lower than that (2.74 A) shown in Fig. 7(b). It is because the static positive $v_{\rm gs}$ attracts and captures numerous electrons into the SiC/SiO_2 interface along the channel, and these electrons hinder the 3rd-QC current. The damping process due to the principle that like charges repel to each other can be seen in the $i_{\rm sd}$ trajectory after t_1. On the contrary, the recorded $i_{\rm sd}$ (3.12 A) is much higher than 2.74 A because a huge number of holes trapped in interface with V_A = -4 V. The overshooting process of the $i_{\rm sd}$ trajectory is attributed to the principle that opposite charges attract each other. Therefore, the data extracted from the SPT is not accurate to model the 3rd-QC of the device due to the ISE.

The proposed DTP well considers the channel dynamics caused by the ISE, because the SiC/SiO_2 interface of the DUT

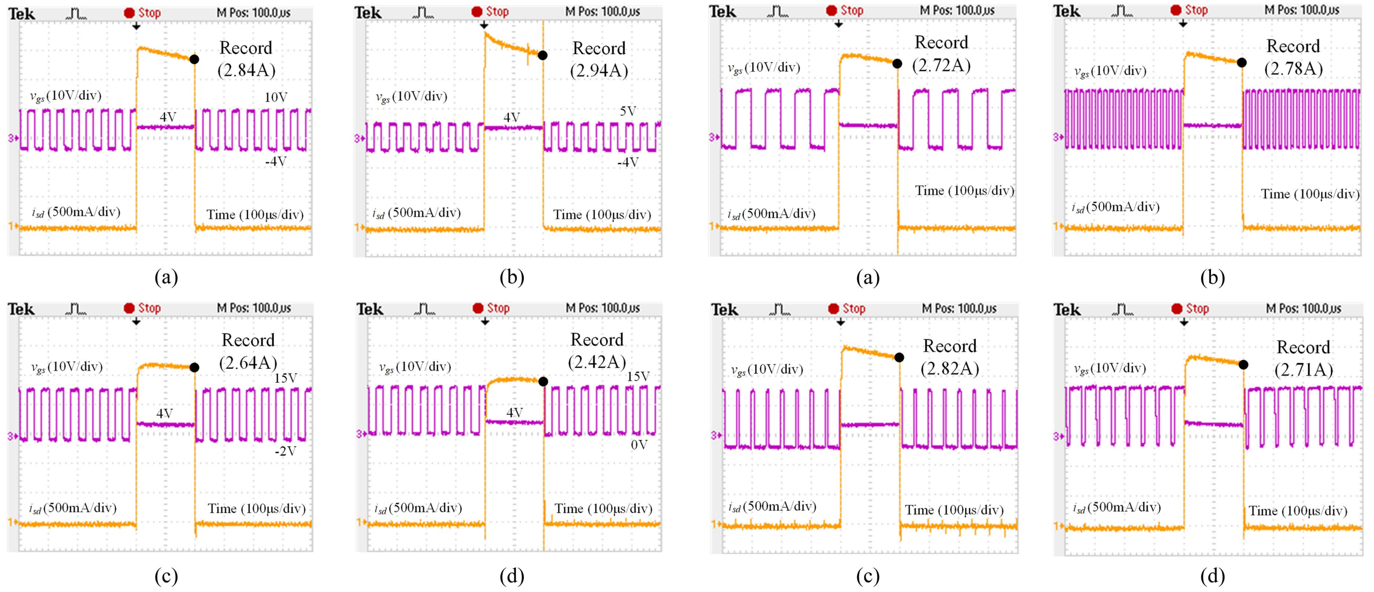


Fig. 9. v_{gs} and i_{sd} trajectories with different amplitudes of driving voltage. (a) $V_{GG1\text{-}S}$ is 10 V and $V_{EE1\text{-}S}$ is -4 V. (b) $V_{GG1\text{-}S}$ is 5 V and $V_{EE1\text{-}S}$ is -4 V. (c) $V_{GG1\text{-}S}$ is 15 V and $V_{EE1\text{-}S}$ is -2 V. (d) $V_{GG1\text{-}S}$ is 15 V and $V_{EE1\text{-}S}$ is 0 V.

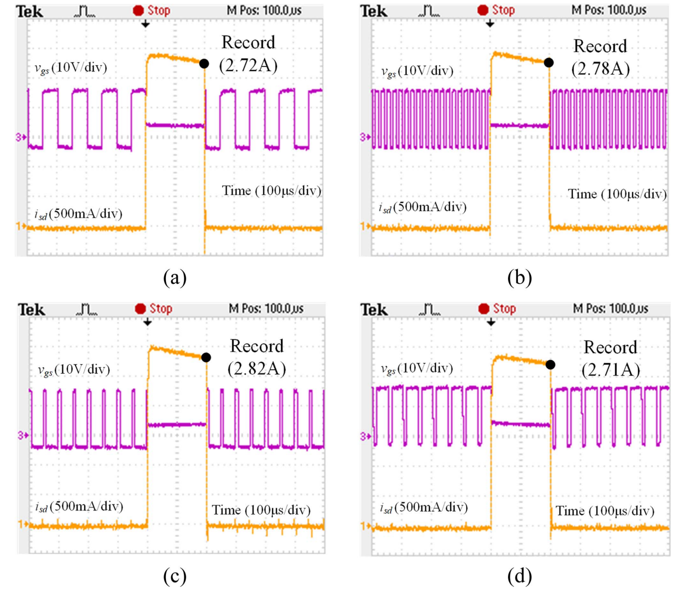


Fig. 10. v_{gs} and i_{sd} trajectories with different frequency f_s and duty cycle D_s. (a) 10 kHz, 50%. (b) 50 kHz, 50%. (c) 20 kHz, 20%. (d) 20 kHz, 80%.

could enter dynamic balance before the test. It should be noted that the operation of the DTP is ought to be similar with those in the converter. Fig. 9 shows the v_{gs} and i_{sd} trajectories of the DUT tested by the DTP under different driving voltages $V_{GG1\text{-}S}$ and $V_{EE1\text{-}S}$. The frequency f_s and duty cycle D_s of V_A are fixed at 20 kHz and 50%, respectively. In Fig. 9(a) and (b), the i_{sd} increases from 2.84 to 2.94 A, when $V_{GG1\text{-}S}$ decreases from 10 to 5 V. Fig. 9(c) and (d) shows that the i_{sd} decreases from 2.64 to 2.42 A when $V_{EE1\text{-}S}$ increases from -2 to 0 V. The lower $V_{GG1\text{-}S}$ has positive influence to the 3rd-QC current i_{sd}, while the higher $V_{EE1\text{-}S}$ has negative influence to the i_{sd}.

Fig. 10 shows the v_{gs} and i_{sd} trajectories of the DUT tested by the DTP under different f_s and D_s, where the driving voltages are fixed at 15 and -4 V. It is shown in Fig. 10 that the deviation is quite small to the i_{sd} when f_s and D_s vary in wide range under the same voltage biases. So, the influences of f_s and D_s on the 3rd-QC could be neglected considering the converter applications.

Obviously, the voltage biases and temperature of DUT can be flexibly set by users, so the FSE and TSE are considered in DTP. Moreover, the SiC/SiO$_2$ interface of DUT reaches dynamic balance before each test, so the ISE are also included in DTP. Therefore, the correction of raw data for the 3rd-QC are ensured. The 3rd-QC of the SiC MOSFET obtained by the proposed DTP is shown in Fig. 11, where T_j is fixed at 25°C. $V_{GG1\text{-}S}$ and $V_{EE1\text{-}S}$ are selected as 15 and -4 V, respectively, which are recommended in the datasheet [19]. f_s and D_s are chosen as 20 kHz and 50%, respectively. These parameters are selected by users, which can be chosen according to the converter application. Fig. 11 shows that the 3rd-QC curves are overlapped as V_{GS} lower than -10 V. This phenomenon means the channel of the SiC MOSFET is completely turned OFF, and the current i_{sd} is conducted through the body-diode. The SiC MOSFET operates

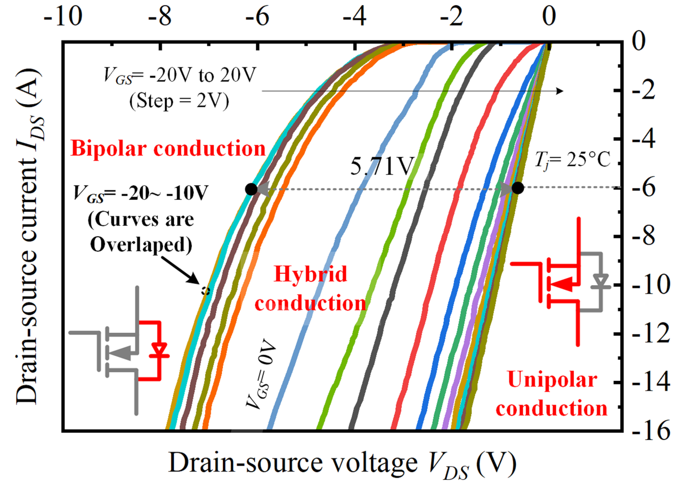


Fig. 11. 3rd-QC of SiC MOSFET at $T_j = 25$°C, $V_{GG1\text{-}S} = 15$ V, $V_{EE1\text{-}S} = -4$ V, $f_s = 20$ kHz, and $D_s = 50$%.

in the bipolar conduction mode, and i_{sd} equals i_{pn}. When V_{GS} is higher than 14 V, the typical straight line of the 3rd-QC is shown. It means the SiC MOSFET has the resistance feature and operates in the unipolar conduction mode. In this case, the current i_{sd} is carried by the MOS structure, and i_{sd} equals i_{mos}. When V_{GS} is about 0 V, the SiC MOSFET operates in the hybrid conduction mode.

C. Temperature Sensitivity

The comprehensive understanding about the TSE of the 3rd-QC is beneficial to the better condition-monitoring and protection of the SiC MOSFET. Until now, the temperature sensitivity about voltage drop of the external diode has been used to sense the junction temperature of the Si IGBT [22]. However, the

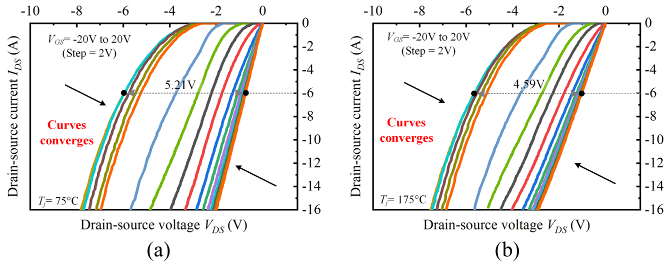


Fig. 12. 3rd-QC of SiC MOSFET with (a) $T_j = 75°C$ and (b) $T_j = 175°C$.

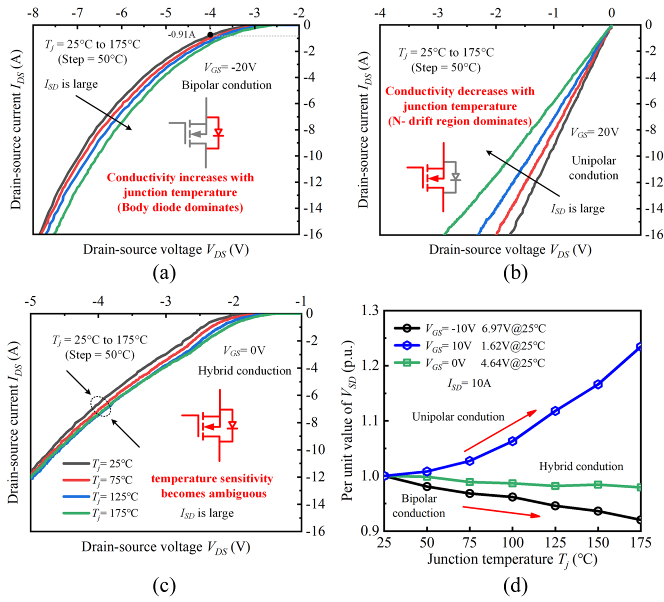


Fig. 13. TSE of 3rd-QC when I_{SD} is large. (a) V_{GS} = -20 V. (b) V_{GS} = 20 V. (c) V_{GS} = 0 V. (d) Relation between V_{SD} and T_j when I_{SD} is 10 A.

case of the SiC MOSFET is more complicated, where both the channel and body-diode dynamics could be appeared in 3rd-QC. Therefore, the TSE of the 3rd-QC should be carefully studied and considered in the proposed model if the users try to apply V_{SD} to predict T_j. Based on the proposed DTP, Fig. 12(a) and (b) shows the 3rd-QC of device when T_j is 75°C and 175°C, respectively. It is obvious that the family of 3rd-QC curves converge towards the center of the figure with the increased T_j. When I_{SD} is selected at 6 A, the V_{SD} difference between the biases V_{GS} = -20 and 20 V is 5.71 V ($T_j = 25°C$), 5.21 V ($T_j = 75°C$) and 4.59 V ($T_j = 175°C$), respectively. It means the device is more possible to operate in the hybrid conduction mode when T_j is increased.

Fig. 13 shows the TSE of the SiC MOSFET when I_{SD} is relatively large (Ampere level) and T_j varies from 25°C to 175°C with step of 50°C. In Fig. 13(a), the bipolar conduction mode is shown as V_{GS} = -20 V, where the conductivity of the reverse-conduction path increases with T_j since i_{pn} dominants i_{sd}. The *I*-*V* characteristic of the body-diode is positively related to T_j because the reverse saturation-current of the PN junction significantly increases with T_j inside the SiC MOSFET. In Fig. 13(b), the unipolar conduction mode is shown as V_{GS} = 20 V, where the conductivity of the reverse-conduction path decreases with T_j since i_{mos} dominants i_{sd}. This is because the

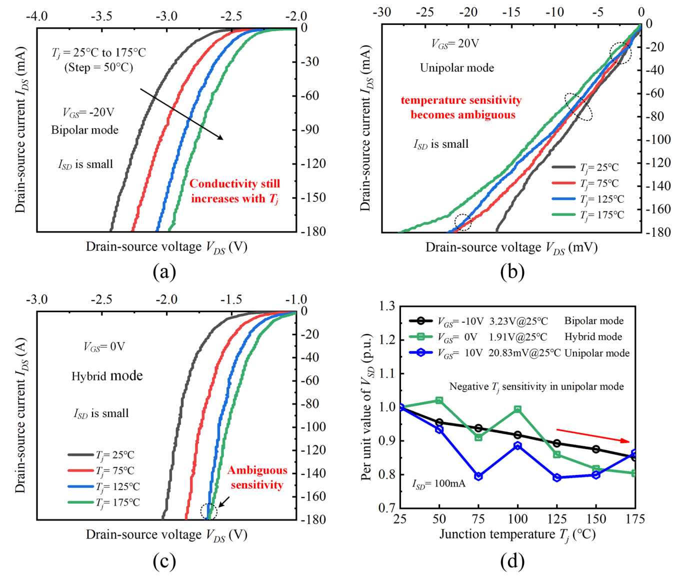


Fig. 14. TSE of 3rd-QC when I_{SD} is small. (a) V_{GS} = -20 V. (b) V_{GS} = 20 V. (c) V_{GS} = 0 V. (d) Relation between V_{SD} and T_j when I_{SD} is 100 mA.

resistance of the *N*-drift region R_{drift} takes a large amount of the MOS resistance when I_{SD} is large, and R_{drift} is positively related to T_j due to the scattering effect [23].

Unlike the bipolar and unipolar conduction mode, the hybrid conduction mode has relatively ambiguous TSE in 3rd-QC. Fig. 13(c) shows the 3rd-QC curves intersect each other when V_{GS} is 0 V. Obviously, the opposing TSE of the 3rd-QC in the bipolar and unipolar conduction mode cancel each other out. Fig. 13(d) shows the normalized V_{SD} (negative of V_{DS}) with varying T_j under different conduction modes when I_{SD} (in reverse direction of I_{DS}) is 10 A. It is clear that V_{SD} is positively related to T_j in the unipolar conduction mode, while V_{SD} is negatively related to T_j in the bipolar conduction mode. It should be noted that V_{SD} is only slightly related to T_j in the hybrid conduction mode, because two opposite TSEs compete each other. Therefore, the 3rd-QC of SiC MOSFET might exhibit weak dependence on T_j when the device operates in the hybrid conduction mode.

Since large-current injection method to sense T_j is relatively complex and the timing calibration is necessary in the converter modulation, some literatures begin to study the small-current injection method by using the additional circuits. However, the TSE of SiC MOSFET would be much different when I_{SD} decreases. Fig. 14 shows the TSE of the device when I_{SD} is relatively small (milliampere level) when T_j varies from 25°C to 175°C. The conductivity of the reverse-conduction path still increases with T_j when the device operates in the bipolar conduction mode, as shown in Fig. 14(a). But the TSE of the 3rd-QC becomes ambiguous in the unipolar conduction mode, as shown in Fig. 14(b), which is different to the result shown in Fig. 13(b). This is because the impact of the channel resistance R_{ch} on the total ON-state resistance becomes comparable to that of R_{drift} when I_{SD} is small. The channel resistance R_{ch} can be expressed as

$$R_{\mathrm{ch}} = \frac{L_{\mathrm{ch}}}{W_{\mathrm{ch}}\mu_{\mathrm{ch}}C_{\mathrm{ox}}(V_{\mathrm{GD}} - V_{\mathrm{TH3}})} \quad (6)$$

where L_{ch} and W_{ch} is the length and width of the channel respectively. μ_{ch} is the electron mobility of the channel, which decreases with T_j due to the scattering effect. The bulk potential ψ_B given in (2) can be expressed as

$$\psi_B = \frac{kT_j}{q} \ln \left[\frac{N_A}{n_i(T_j)} \right] \tag{7}$$

where N_A is the acceptor doping concentration of the channel. It can be found that V_{TH3} decreases with the increase of T_j as negative temperature sensitivity of ψ_B. Obviously, the impact of μ_{ch} competes with that of V_{TH3} on R_{ch} when T_j varies, so the TSE of R_{ch} is hard to be predicted. Therefore, the TSE of the 3rd-QC in the unipolar conduction mode is ambiguous. This conclusion could be supported by the 1st-QC shown in the datasheet [19], where the relation between ON-state resistance R_{on} and T_j is nonmonotonic when R_{ch} dominates R_{on} with the low V_{GS}. Moreover, the similar phenomenon can be found in the experimental result about the TSE of 3rd-QC in the hybrid conduction mode, which is shown in Fig. 14(c). Fig. 14(d) shows the normalized V_{SD} with varying T_j of different conduction modes when I_{SD} is 100 mA. V_{SD} is still negatively related to T_j in the bipolar conduction mode, but no significant relation could be found between V_{SD} and T_j when the SiC MOSFET operates in the unipolar or hybrid conduction mode. Based on the above results, it is important to select the gate-source voltage when applying the TSE of the 3rd-QC to sense the junction temperature of the SiC MOSFET. The negative V_{GS} that ensures the device operates in the bipolar mode is recommended, because the relation between V_{SD} and T_j is clear. At the same time, the impact of ISE on the temperature sensing could be decreased due to the completely turn-OFF of the channel. It should be noted that the temperature sensing under the bipolar conduction mode is better to be conducted in periodic intervals, because the low V_{GS} below the recommended value would induce the additional channel degradation of the SiC MOSFET.

D. Modeling Process

The modeling of the 3rd-QC is aimed to describe the I-V characteristics from the source to the drain terminal of the SiC MOSFET. The total current in the reverse conduction path of the SiC MOSFET could be expressed as

$$I_{\mathrm{SD}} = I_{\mathrm{MOS}} + I_{\mathrm{PN}} \tag{8}$$

where I_{MOS} and I_{PN} is the current conducted through the MOS structure and the body-diode, respectively. As mentioned in Section III-B, the 3rd-QC curves are overlapped when V_{GS} is lower than -10 V. In this case, V_{GS} has trivial impact on the 3rd-QC because the channel is completely turned OFF and the device could be considered as a pure diode. Therefore, the current of MOS structure can be obtained by deducting the current of pure diode from the total current. Fig. 15 shows the three currents I_{PN} (black dots), I_{MOS} (blue dots), and I_{SD} (gray dots) when V_{GS} varies from -4 to 2 V and I_{PN} is the recorded I_{SD} under the condition that V_{GS} is -20 V, which ensures the reverse current is only conducted by the body-diode. As shown in Fig. 15(a), the absolute value of I_{MOS} equals

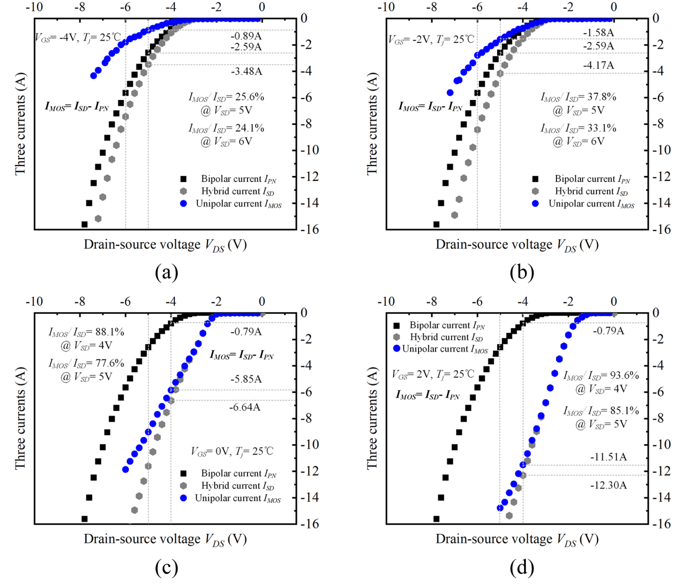


Fig. 15. Decoupling and analysis of I_{MOS} and I_{PN} under condition that T_j is 25°C with (a) V_{GS} = -4 V, (b) V_{GS} = -2 V, (c) V_{GS} = 0 V, and (d) V_{GS} = 2 V.

2.59 A when V_{SD} is 3 V, which is obtained from I_{SD} (3.48 A) deducting I_{PN} (0.89 A). Repeat the calculation, then I_{MOS} under different biases could be obtained. Fig. 15(a)–(d) also shows the current-sharing ratio between two reverse-conduction paths. Obviously, $I_{\mathrm{MOS}}/I_{\mathrm{SD}}$ increases with the enhanced V_{GS} under a fixed V_{SD}. This is because the decreased R_{ch} attracts more current from the body-diode to the MOS structure. Fig. 15(d) shows I_{MOS} accounts for about 93.6% of the total I_{SD} when V_{GS} is 2 V, which means the SiC MOSFET is nearly in a full unipolar conduction mode. This phenomenon indicates that the channel is easier to be turned ON in the third quadrant than the first quadrant, as 2 V is lower than the threshold voltage 2.3 V clarified in the datasheet. Moreover, the group of blue dots shifts in the right direction of the figure with the increased V_{GS}, which means the channel is turned ON under the lower V_{SD} when V_{GS} increases. Combining (1) and (2), it has

$$V_{\mathrm{GS}} = V_{\mathrm{FB}} + 2\psi_B + \frac{\sqrt{2\varepsilon_s q N_A}}{C_{\mathrm{ox}}} \sqrt{2\psi_B - V_{\mathrm{SD}}} - V_{\mathrm{SD}} \tag{9}$$

when V_{GS} is increased, V_{SD} should be decreased to ensure the conservation of (9). Therefore, it can be found that V_{GS} has the significant impact on the turn-ON condition of the channel, which is ultimately due to the FSE. At the same time, the unipolar current curve (group of blue dots) has larger slope with the increased V_{GS}, which is attributed to the decreased R_{ch}. Besides V_{GS}, V_{SD} also influences the current-sharing ratio between the MOS structure and body-diode. For example, $I_{\mathrm{MOS}}/I_{\mathrm{SD}}$ decreases from 88.1% to 77.6% when V_{SD} increases from 4 to 5 V when V_{GS} is fixed at 0 V, as shown in Fig. 15(c). The similar results can also be observed in other subfigures of Fig. 15. This is because the impendence of the body-diode significantly decreases with the increased V_{SD} due to the carrier injection effect, while that of the MOS structure does not change a lot with V_{SD}. Therefore, more current starts to transfer from the

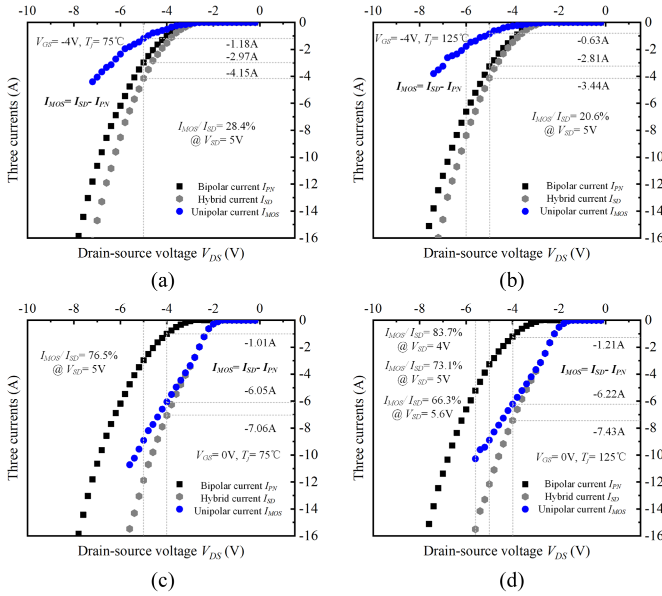


Fig. 16. Decoupling and analysis of $I_{\rm MOS}$ and $I_{\rm PN}$ with (a) $V_{\rm GS}$ is -4 V and T_j is 75°C, (b) $V_{\rm GS}$ is -4 V and T_j is 125°C, (c) $V_{\rm GS}$ is 0 V and T_j is 75°C, and (d) $V_{\rm GS}$ is 0 V and T_j is 125°C.

MOS structure to the body-diode when $V_{\rm SD}$ is increased. It indicates that the value of load current in the converter would cause the fluctuation of the current-sharing ratio between two reverse-conduction paths of the device.

Fig. 16 shows the three currents under different T_j varied from 75°C to 125°C, and $V_{\rm GS}$ are selected as -4 and 0 V. The conclusion that $I_{\rm MOS}/I_{\rm SD}$ increases with $V_{\rm GS}$ can be still held with different T_j. The ratio $I_{\rm MOS}/I_{\rm SD}$ decreases with the increase of T_j under both the conditions that $V_{\rm GS}$ is -4 and 0 V. For example, $I_{\rm MOS}/I_{\rm SD}$ decreases from 28.4% to 20.6% under the condition that $V_{\rm GS}$ is -4 V when T_j increases from 25°C to 125°C. This phenomenon is attributed to the positive temperature sensitivity of $R_{\rm drift}$ in the MOS structure. Fig. 16(d) shows that $I_{\rm MOS}/I_{\rm SD}$ decreases from 83.7% to 66.3% when $V_{\rm SD}$ increases from 4 to 5.6 V under the condition that T_j is 125°C. This phenomenon indicates that the current conducted through the MOS structure and body-diode would tend to be balanced under the extreme operating situations of the SiC MOSFET, such as the over-current and high junction temperature.

Based on the above analysis, the values of $I_{\rm MOS}$ and $I_{\rm PN}$ can be obtained under the different junction temperature and voltage biases. In this article, $V_{\rm GS}$ is fixed at -20 V to establish the body-diode current model because the low $V_{\rm GS}$ could ensure the device operating in the bipolar conduction mode. It is known that $V_{\rm GS}$ below recommended value in datasheet would cause the degradation of channel due to the negative bias temperature instability effect. However, since each testing duration applied -20 V is very short, the proposed modeling process hardly degrades the device. Fig. 17(a) shows the cycling test of the DUT, where the $V_{\rm GS}$ waveform similar with that in Fig. 7 is continuously exerted between the gate-source terminals of DUT. One cycle is set as 2 ms and the testing duration applied -20 V is 200 μs. Fig. 17(b) shows the $V_{\rm SD}$ ($I_{\rm SD}$ is 6 A and $V_{\rm GS}$ is 4

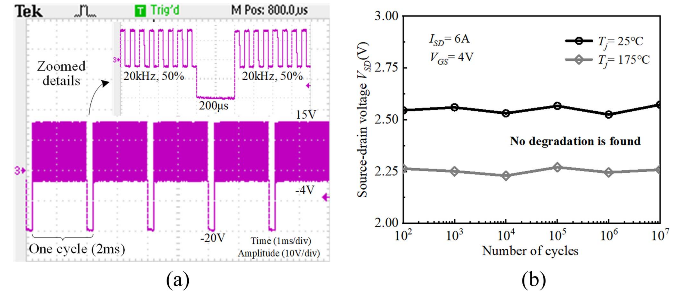


Fig. 17. Cycling test of DUT. (a) $V_{\rm GS}$ waveform as $V_{GG1\text{-}S}$ is 15 V, $V_{EE1\text{-}S}$ is -4 V, $V_{GG2\text{-}S}$ is -20 V, f_s is 20 kHz, and D_s is 50%. (b) $V_{\rm SD}$ after cycling tests as $I_{\rm SD}$ is 6 A and $V_{\rm GS}$ is 4 V.

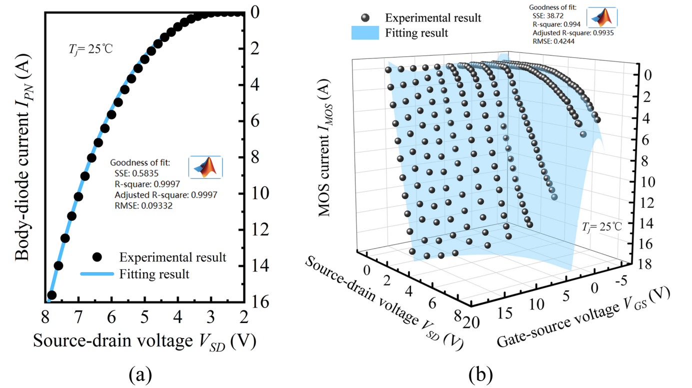


Fig. 18. Fitting results of (a) $i_{\rm pn}$ and (b) $i_{\rm mos}$.

V) after cycling tests with different T_j, and three terminals of DUT are shorted for 10 min before measurement to decrease the influence of threshold voltage hysteresis effect. It is obvious that no degradation is found on the DUT even the number of cycles reaches 10^7, which far exceeds that required in the modeling process of SiC MOSFET. Therefore, the test of body diode is conducted in a safe condition without raising reliability concerns.

A hybrid exponential-polynomial function is adopted to describe the relation between the dynamic body-diode current $i_{\rm pn}$ and source-drain voltage $v_{\rm sd}$ under the specific T_j, and it has

$$i_{\rm pn}(v_{\rm sd})|_{T_j} = a\left(e^{bv_{\rm sd}} - 1\right) + c{v_{\rm sd}}^2 + dv_{\rm sd} \tag{10}$$

where a, b, c, d are the coefficients determined by the data fitting in the MATLAB. The coefficients for different T_j (25°C–175°C) are listed in Table I of the Appendix. Fig. 18(a) shows fitting result of $i_{\rm pn}$ when T_j is 25°C, where the high coefficient of determination R^2 confirms that the relation between $i_{\rm pn}$ and $v_{\rm sd}$ is well fitted. $V_{\rm GS}$ varies from -4 to 16 V with the step of 2 V to establish the MOS current model. A fifth-order bivariate polynomial is applied to describe the relation between the dynamic MOS current $i_{\rm mos}$, gate-source voltage $v_{\rm gs}$ and source-drain voltage $v_{\rm sd}$ under the specific junction temperature T_j, and it has

$$i_{\rm mos}(v_{\rm gs}, v_{\rm sd})|_{T_j} = \sum_{i=0}^{5}\sum_{j=0}^{5} p_{ij}{v_{\rm gs}}^i{v_{\rm sd}}^j \tag{11}$$

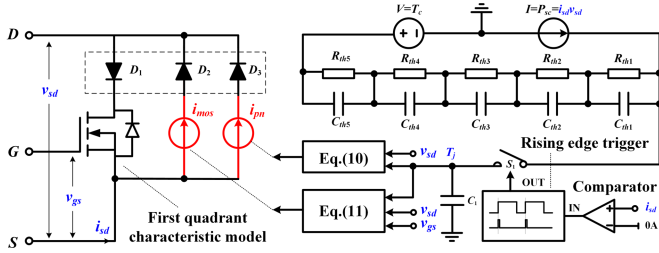


Fig. 19. Application of the proposed model in SPICE software.

where the coefficients p_{ij} for different T_j are listed in Table II of the Appendix. Fig. 18(b) shows the fitting results of $i_{\rm pn}$ at T_j 25°C, where the high R^2 indicates the good data fitting.

The SPICE software is one of the most popular tools for users to observe device dynamics. Fig. 19 illustrates the module embedded the 3rd-QC model into the SPICE software by using graphical language. The SPICE module has three terminals D, G, and S, and the users could observe the trajectories of $v_{\rm sd}$, $v_{\rm gs}$, and $i_{\rm sd}$ in the simulation. The sources $i_{\rm mos}$ and $i_{\rm pn}$ presents the MOS current and body-diode current in the reverse-conduction path of the device respectively. The ideal diodes D_1–D_3 ensures that $i_{\rm mos}$ and $i_{\rm pn}$ are only valid in the reverse direction, and the 1st-QC of the device would not be influenced. The Foster thermal network is adopted to obtain the junction temperature T_j of the device, and the RC parameters of the network are same as those in [24]. In (10) and (11), the coefficients will be changed according to T_j, and then the refreshing and latching unit is used to ensure the model convergence. In Fig. 19, the ideal switch S_1 and the capacitance C_1 (1F) form the refreshing and latching unit, which is enabled by the rising edge trigger. When $i_{\rm sd}$ exceeds 0 A, the SPICE module determines that the device operates in the third quadrant, then T_j is refreshed and latched.

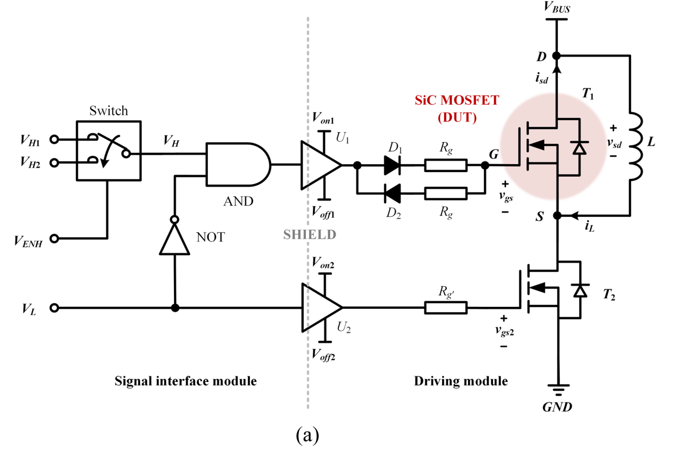
It is obvious that the proposed 3rd-QC model in the SPICE software is compact, easy implementing without complex calculation. Therefore, good convergency and efficient simulation would be realized. In this article, SPICE software Pspice16.6 is applied and the simulation with the proposed model could be carried out.

It should be noted that the proposed model is aimed to accurately describe the reverse-conduction characteristics in the 3rd-QC of SiC MOSFET, and the reverse recovery phenomenon is not included in the proposed model.

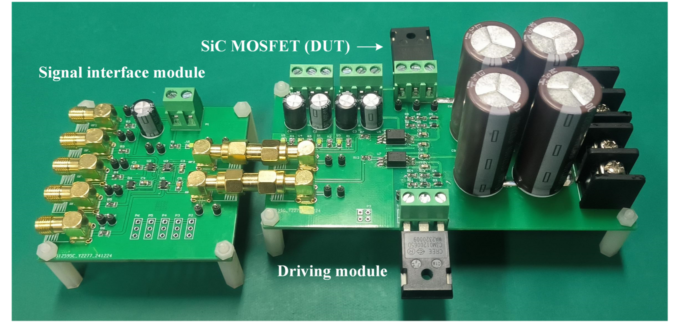
IV. Validations

A. Dynamic Validation Platform (DVP)

It is important to verify the proposed model based on an independent and objective validation platform, which should be close to the industrial application and differ from the test platform. The proposed DVP is shown in Fig. 20, which consists of the driving module (DM) and the signal interface module (SIM). In the DM, T_1 is the DUT and T_2 is the companion device. R_g and $R_{g'}$ are the gate resistance, and U_1 and U_2 are the gate driver of T_1 and T_2, respectively. The positive driving voltage $V_{\rm on1}$ and $V_{\rm on2}$ are 15 V, and the negative $V_{\rm off1}$ and $V_{\rm off2}$ are -4 V.

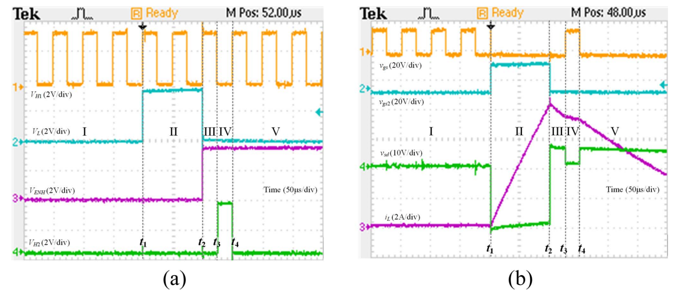


(a)



(b)

Fig. 20. DVP for the proposed model. (a) Schematic. (b) Prototype.



(a) (b)

Fig. 21. Operation principle of DVP. (a) Signals in SIM. (b) Voltage and current trajectories in DM.

The air-core inductance L connected in parallel with T_1 is 220 μH and the voltage $V_{\rm BUS}$ is fixed at 20 V. The SIM includes the analog switch, gate AND, gate NOT, and signals (V_{H1}, V_{H2}, V_{ENH}, V_L) from the DSP. The driving signal V_H of the DUT is V_{H1} or V_{H2} that selected by V_{ENH}. The gate AND and NOT forms the interlock circuit, which ensures T_1 and T_2 are never turned on at the same time.

Fig. 21 shows operation principle of the DVP. V_{H1} is a continuous PWM signal, where the frequency and duty may be adjusted according to the converter requirement. Here, the frequency and duty of V_{H1} is selected as 20 kHz and 50%, respectively, which are consistent with those set in the DTP. Totally five processes are shown in the operation of the DVP and they can be concluded as follows.

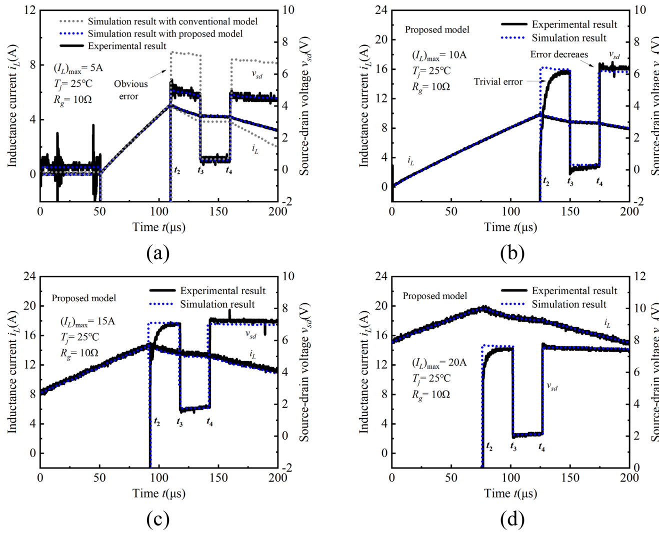


Fig. 22. Experimental results of 3rd-QC trajectories with (a) $I_L = 5$ A, (b) $I_L = 10$ A, (c) $I_L = 15$ A, and (d) $I_L = 20$ A.

Process I, the duration [0 t_1]: V_L, V_{ENH} and V_{H2} are all in low level. T_2 is turned OFF and the gate of T_1 (DUT) undertakes alternative driving voltages of 15 and -4 V. As the result, the SiC/SiO$_2$ interface of T_1 can reach the dynamic balance, which is very close to the case in the converter applications.

Process II, the duration [t_1 t_2]: V_L turns to high level, and then T_2 is turned ON. The inductance L is charging and carries the load current i_L at the moment t_2.

Process III, the duration [t_2 t_3]: V_L turns to low level and V_{ENH} turns to high level. Both T_1 and T_2 are turned OFF because the selected V_{H2} is still at low level. Since L cannot store the energy in the static situation, i_L is forced to the reverse-conduction path of T_1. Therefore, the DUT operates in the NF mode under the condition of $v_{\mathrm{gs}} = $ -4 V.

Process IV, the duration [t_3 t_4]: V_{H2} turns to high level, and then T_1 is turned ON. The DUT operates in the SR mode under the condition of $v_{gs} = 15$ V.

Process V, the duration after t_4: V_{H2} turns to low level and the DUT operates in the NF mode again.

The duration from t_1 to t_2 depends on the charging time of L from zero to the load current. The durations from t_2 to t_3 and from t_3 to t_4 can be set by the users, and these two durations are chosen as the half cycle of V_{H1} in this article. The proposed DVP can emulate the converter operations well and then it may produce the device behaviors in two reverse-conduction modes.

B. Model Validation in DVP

Fig. 22 shows the experimental results of the DVP for the 3rd-QC trajectories of the SiC MOSFET under different I_L, where the comparative simulation results are obtained at Pspice16.6 with Intel Core i5-7th Gen. in the computer. In Fig. 22(a), the conventional model provided by the manufacturer has obvious errors in predicting the 3rd-QC trajectories. The proposed model shows good accuracy in the simulation results, because it considers the channel and body-diode dynamics. Only trivial error is found at the transition of Processes II to III at moment t_2, and this error significantly decreases at the second transition of SR mode to NF mode at moment t_4. This is because the process II induces the transient instability of the SiC/SiO$_2$ interface, and the interface gradually becomes stable with the reverse-conduction, as shown in Fig. 22 after moment t_4. In the converter applications, the SiC MOSFET operates continuously, and the error around the first transition time is neglectable.

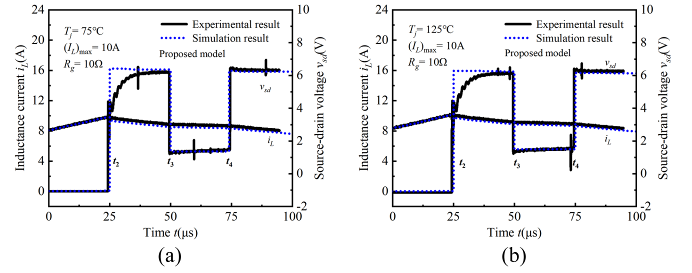


Fig. 23. Comparisons of experimental and simulation results of 3rd-QC trajectories with (a) $T_j = 75$°C and (b) $T_j = 125$°C.

Fig. 23 shows the comparison of experimental and simulation results of the 3rd-QC trajectories with the proposed model under different T_j. When the junction temperature increases from 75°C to 125°C, the proposed model considering the TSE still has high accuracy in predicting the 3rd-QC trajectories of the SiC MOSFET.

It should be noted that the SiC MOSFET is not abruptly switched between the NF mode and the SR mode. The transition processes around the moment t_3 and the moment t_4 are considered in the proposed model for the dynamic current redistribution between the MOS structure and the body-diode. Fig. 24(a) and (b) shows the experimental results of the 3rd-QC trajectories around the moment t_3 and t_4, respectively, where R_g is 10Ω, $\mathrm{I_L}$ is 7.3 A and $\mathrm{T_j}$ is 25°C. In this article, the duration of the v_{sd} varied from 90% to 10% is defined as the turn-ON time t_{on3} of the 3rd-QC, where the SiC MOSFET turns to the SR mode from the NF mode. The duration of the v_{sd} varied from 10% to 90% is defined as the turn-OFF time t_{off3} of the 3rd-QC, where the SiC MOSFET turns to the NF mode from the SR mode. In Fig. 22(a), v_{gs} increases and v_{sd} decreases at the boundary between the Processes III and IV with $t_{\mathrm{on3}} = 19$ ns. Fig. 24(b) shows that t_{off3} is 22 ns where v_{gs} decreases and v_{sd} increases at the boundary between the Processes IV and V. Obviously, the proposed model has high accuracy in predicting the dynamic 3rd-QC trajectories in the transients between the NF mode and the SR mode of the SiC MOSFET, which does help to the deadtime design of the converter. Fig. 24(c) to (f) shows the turn-ON and OFF transients of the 3rd-QC with different R_g. It is evident that t_{on3} and t_{off3} are significantly increased with the increasing of R_g, because the switching time of the channel is related to the slope rate of the v_{gs} trajectory. It can be seen from Fig. 24 that v_{sd} rapidly decreases at the moment that v_{gs} starts to increase from -4 V, rather than the moment v_{gs} reaches the threshold voltage 2.3 V, and 2.3 V is given in the datasheet but not occurred in our experimental results. This is because the FES of the 3rd-QC leads to the easier

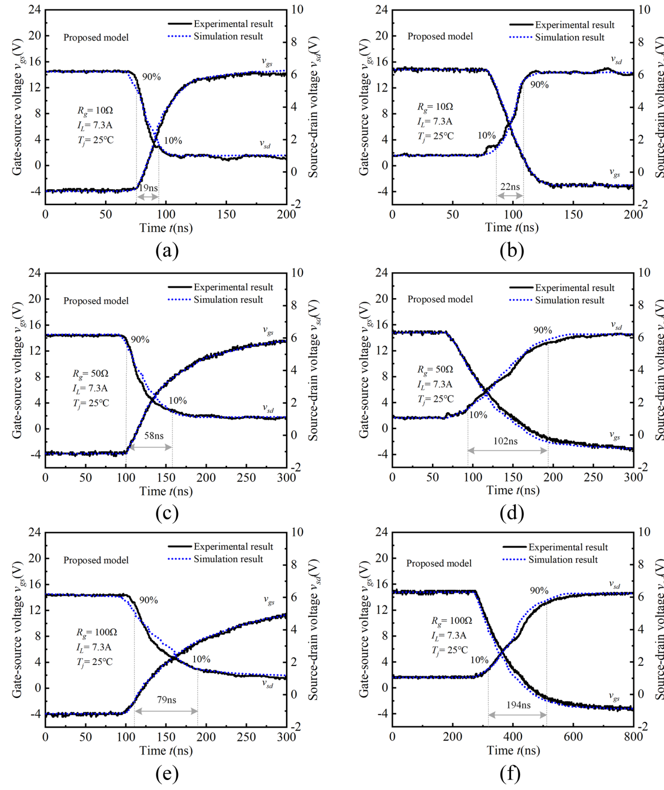


Fig. 24. Comparisons of experimental and simulation results of 3rd-QC trajectories between two reverse-conduction modes. (a) Turn-ON transient with $R_g = 10\ \Omega$. (b) Turn-OFF transient with $R_g = 10\ \Omega$. (c) Turn-ON transient with $R_g = 50\ \Omega$. (d) Turn-OFF transient with $R_g = 50\ \Omega$. (e) Turn-ON transient with $R_g = 100\ \Omega$. (f) Turn-OFF transient with $R_g = 100\ \Omega$.

turn on of the channel in reverse conduction mentioned in the Section II, and the proposed DVP could emulate the operations of the SiC MOSFET. Obviously, all the simulation results with proposed model agree well with the experimental results.

C. Model Validation in Inverter

It is important to validate the convergency and accuracy of the proposed model based on the converter, which is closer to the industrial applications. In this article, a single-phase inverter with four SiC MOSFETs (C3M0120065D, 650V/20A) is fulfilled to verify the proposed model. Fig. 25(a) shows the schematic of the inverter and the simulation blocks with the proposed SPICE module are constructed. Fig. 25(b) shows the prototype of the inverter, and the experimental waveforms of the output current i_{AB} and output voltage v_{AB} are also given. The bus voltage V_{bus} is set at a relatively low value 40 V, aiming to clearly obverse the voltage drop on the reverse-conduction path. Low bus voltage V_{bus} has no negative effect in observing the 3rd-QC of device, because v_{sd} in the reverse-conduction direction has trivial relation with bus voltage.

Fig. 26(a) shows the simulation results of the inverter with the proposed model, where the converter behaviors are well described. The running time and maximum simulation step are 20 ms and 10 ns, respectively. It is shown form Fig. 26(b) that

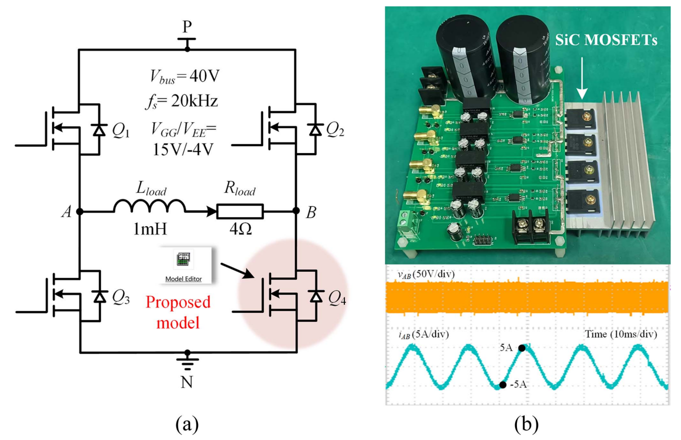


Fig. 25. Single-phase inverter. (a) Schematic and circuit parameters. (b) Prototype and operation waveforms.

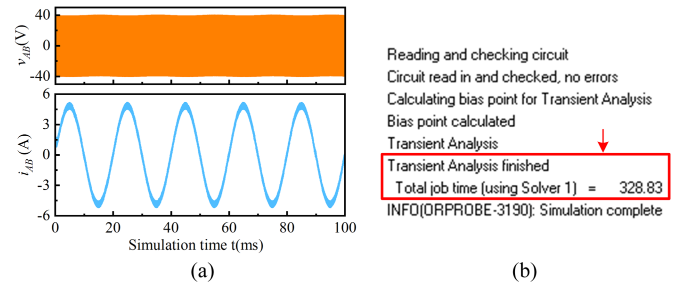


Fig. 26. Simulation results of inverter with proposed model. (a) Voltage and current waveforms. (b) Simulation report in Pspice16.6.

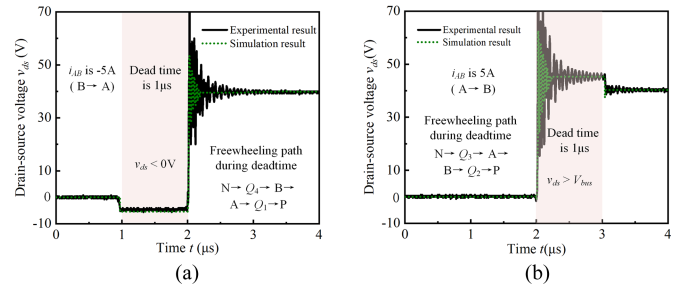


Fig. 27. Simulation result of v_{ds} trajectory of Q_4 with proposed model. (a) i_{AB} is -5 A. (b) i_{AB} is 5 A.

the proposed model well converges in the SPICE software, and no divergency problem is occurred in the simulation.

In both the simulation and experiment, the deadtime of driving signals in the inverter is set at 1 μs. Two SiC MOSFETs in the same bridge are both turned OFF during the deadtime period and operate under the condition with v_{gs} -4 V. When the output current i_{AB} is negative with the current direction from point B to point A, the freewheeling path is "$N\rightarrow Q_4\rightarrow B\rightarrow A\rightarrow Q_1\rightarrow P$" during the deadtime period. In this case, the drain-source voltage v_{ds} of the device Q_4 is below zero. When i_{AB} is positive, the freewheeling path is "$N\rightarrow Q_3\rightarrow A\rightarrow B\rightarrow Q_2\rightarrow P$", and v_{ds} of Q_4 is over V_{bus}. Fig. 27 shows the comparisons of the experimental and simulation results of v_{ds} trajectory of

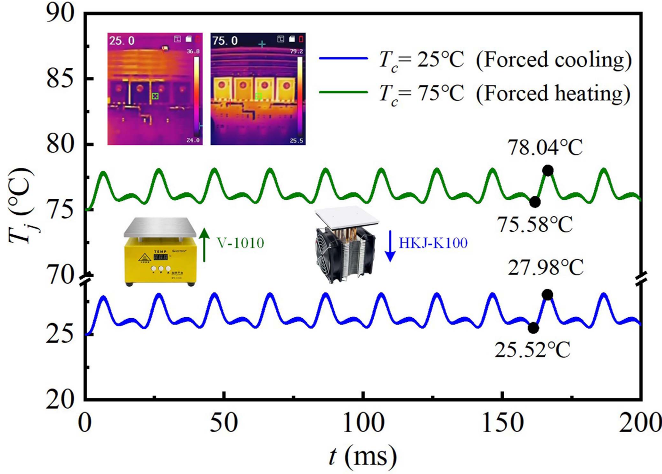


Fig. 28. Junction temperature of Q_4 when T_c is set as 25°C and 75°C.

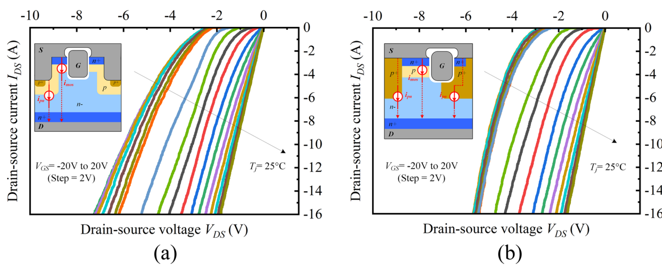


Fig. 29. 3rd-QC data of trench devices based on the proposed DTP as T_j = 25°C. (a) DT device. (b) AT device.

Q_4 with the proposed model. It is obvious that the proposed model accurately reproduced the dip and the bump around zero and V_{bus}, respectively. Therefore, the proposed model can well predict the 3rd-QC behaviors of the SiC MOSFET in the industrial inverter.

It should be noted that the temperature management is necessary in the converter-level validation. Since the bus voltage and load current is set to relatively low values, the self-heating of SiC MOSFET is trivial. Therefore, the junction temperature T_j could be approximately adjusted by controlling the case temperature of the device. Fig. 28 shows T_j of Q_4 in the simulation, where T_c is set as 25°C and 75°C, respectively. It is obvious that T_j only fluctuates in a small range above T_c. So the model validation could be carried out at different T_j by manually setting T_c. In the validation shown in Figs. 26 and 27, the forced cooling and infrared monitoring is adopted in the experiment to ensure the case temperature of the SiC MOSFET keeps at 25°C, which is also set in the Foster thermal network of the simulation.

D. Model Generality

The above validations show the proposed model has high accuracy in predicting the 3rd-QC behaviors of the planar SiC MOSFET. In the industrial applications, the double-trench (DT) device and asymmetric-trench (AT) SiC MOSFETs are also widely adopted in the converter. Fig. 29 shows the 3rd-QC data for

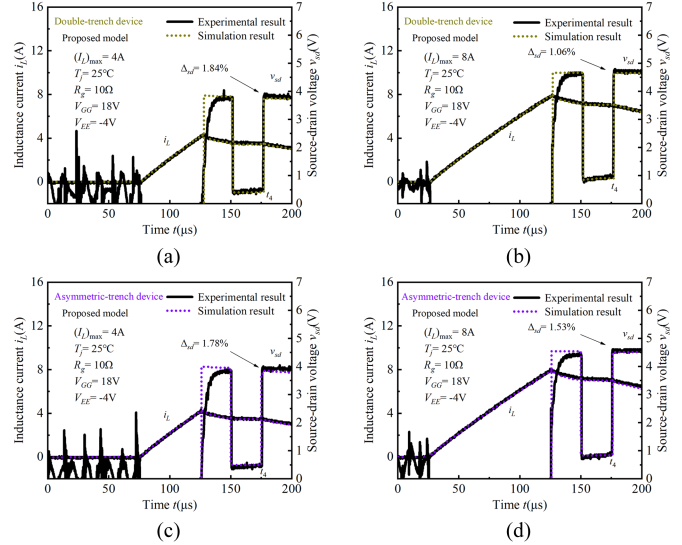


Fig. 30. Experimental results of 3rd-QC trajectories as T_j is 25°C. (a) DT device under $I_L = 4$ A. (b) DT device under $I_L = 8$ A. (c) AT device under $I_L = 4$ A. (d) AT device under $I_L = 8$ A.

two types of trench SiC MOSFETs based on the proposed DTP in this article, where the DT device is SCT3120AL (ROHM, 650V/ 21A) and the AT device is IMW65R107M1H (INFINEON, 650V/ 21A). It shows that the conductivity in the reverse direction varies with the device type, even though the power ratings are similar. However, three conduction modes, namely, the bipolar conduction mode, unipolar conduction mode and hybrid conduction mode, are generally observed in the 3rd-QC of the planar, DT and AT devices. It should be noted that the 3rd-QC curves shown in Figs. 11 and 29 are similar, which means few additional physical differences in 3rd-QC are existed between the trench and planar devices.

Based on the data shown in Fig. 29, the modeling procedure is carried out for the DT device and AT device to verify the model generality. Fig. 30 shows the experimental and simulation results for 3rd-QC trajectories of trench devices as T_j is 25°C and coefficients of the fitting functions are listed in Table III of the Appendix. It is obvious that the proposed model has good accuracy in predicting the 3rd-QC trajectories of the DT device and AT device. The minor relative error $\Delta_{\rm sd}$ of $v_{\rm sd}$ at the moment t_4 shows the modeling procedures could be applied to the different types of SiC MOSFETs.

V. Conclusion

A 3rd-QC model of the SiC MOSFET considering the channel and body-diode dynamics is proposed in this article, which predicts the *I-V* trajectories in the reverse-conduction path in high accuracy and good convergence. The 3rd-QC data including the dynamic effects (FSE, ISE, and TSE) is obtained based on the proposed DTP. The MOS current and PN current are independently modeled by distinguishing the bipolar, unipolar and hybrid conduction modes, and above effects are included in the proposed model. In order to validate the proposed model, the DVP that emulating the NF mode and SR mode is fulfilled to

TABLE I
COEFFICIENTS OF BODY-DIODE CURRENT MODEL FOR PLANAR DEVICE

	a	b	c	d
T_j= 25°C	357.9	0.08914	−1.573	−31.82
T_j= 75°C	10.09	0.2341	−0.2818	−2.488
T_j= 125°C	8.043	0.2463	−0.2238	−2.119
T_j= 175°C	10.49	0.2296	−0.2201	−2.657

TABLE II
COEFFICIENTS OF MOS CURRENT MODEL FOR PLANAR DEVICE

	T_j= 25°C	T_j= 75°C	T_j= 125°C	T_j= 175°C
p_{00}	0.2883	0.4341	0.4522	0.1328
p_{10}	−0.6815	−1.556	−1.684	−1.009
p_{01}	−0.07084	−0.08854	−0.0483	0.01366
p_{20}	−0.3035	0.7233	0.866	0.8139
p_{11}	−0.3945	−0.1722	−0.1556	0.06815
p_{02}	−0.06675	−0.0513	−0.0539	−0.01894
p_{30}	0.4993	0.1343	0.1032	−6.339e-5
p_{21}	0.4524	0.4538	0.466	0.2692
p_{12}	0.1594	0.1574	0.1671	0.1039
p_{03}	0.01759	0.01136	0.009477	6.324e-4
p_{40}	−0.09477	−0.04741	−0.04673	−0.02062
p_{31}	−0.06066	−0.08295	−0.09014	−0.0478
p_{22}	−0.03793	−0.04257	−0.0497	−0.03125
p_{13}	−0.009211	−0.01235	−0.01395	−0.009061
p_{04}	−0.001333	−6.211e-4	−3.591e-4	2.557e-4
p_{50}	0.005128	0.003241	0.00334	0.001426
p_{41}	0.002178	0.004772	0.005304	0.001871
p_{32}	0.003434	0.003909	0.004498	0.002528
p_{23}	3.368e-4	6.593e-4	0.001017	7.264e-4
p_{14}	2.181e-4	3.584e-4	4.049e-4	2.493e-4
p_{05}	3.091e-5	7.125e-06	−1.924e-6	−1.45e-5

verify the model accuracy. The experimental results agree with the simulation results well. Moreover, the model validations are carried out in the single-phase inverter and the different types of SiC MOSFETs. Finally, good convergency and generality are demonstrated in the simulation with the proposed model. The proposed model accurately characterizes the device behaviors in 3rd-QC, which does help to the wide-range application of SiC MOSFETs.

APPENDIX

The coefficients of the fitting function for (10) and (11) under different temperature biases are as follows.

TABLE III
COEFFICIENTS OF PROPOSED MODEL FOR TRENCH DEVICES UNDER 25°C

	DT device	AT device		DT device	AT device
a	1.563	3.162	p_{03}	0.6516	0.2514
b	−0.2119	0.4636	p_{40}	−2.892e-4	−1.786e-4
c	0.4415	−0.4779	p_{31}	−8.352e-4	0.003639
d	−0.7985	−1.638	p_{22}	0.002794	0.02486
p_{00}	−0.1088	−0.2599	p_{13}	−0.03186	0.08129
p_{10}	−0.1361	−0.05631	p_{04}	−0.1061	0.03889
p_{01}	0.9961	0.8649	p_{50}	7.646e-06	6.917e-6
p_{20}	0.01287	0.01562	p_{41}	1.728e-05	−1.35 e-4
p_{11}	−0.0316	−0.0747	p_{32}	−3.766e-4	−1.058e-3
p_{02}	−1.113	−0.9391	p_{23}	−0.001663	−0.00477
p_{30}	0.002537	0.0003422	p_{14}	−2.834 e-4	−0.01325
p_{21}	0.02885	0.005365	p_{05}	0.005067	−9.929e-3
p_{12}	0.2443	−0.0101			

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