Safe-Operation-Area Extended IGBT Module With Enhanced Near-Junction Thermal Capacitance and Advanced Cooling for Transient High-Current Operation

Xiangbo Huang, Zhixin Chen, Weiyu Tang, Kuang Sheng, *Senior Member, IEEE*, and Zan Wu, *Member, IEEE*

***Abstract*—With the growing integration of renewable energy sources, grid-connected converters are expected to provide overcurrent (OC) capability similar to those of synchronous generators. To address this challenge, we propose a power module that incorporates both enhanced near-junction thermal capacitance (NJTC) and exceptional cooling capacity. The module utilizes copper blocks as top-side interconnects, substantially enhancing NJTC and enabling dual thermal paths. Concurrently, it integrates a substrate-embedded manifold microchannel (MMC) heatsink to achieve ultralow thermal resistance. Using the simulation-optimized structural parameters of the NJTC and MMC heat sink, a 1200 V/100 A IGBT half-bridge power module with reliable connections is fabricated through silver sintering technology. Experimental validation demonstrates that the proposed module achieves a 50% higher steady-state current-carrying capacity than the pin-fin module at identical junction temperatures. Under OC conditions, the module operates stably for 3.33 s at 3 p.u. (per unit) with 1000 W heat dissipation per IGBT. At 2.5 p.u., it sustains safe operation over extended periods, outperforming the pin-fin module by a factor of ten. The heat extraction of different mechanisms during OC conditions is quantitatively analyzed through simulation. Double-pulse test results indicate that the proposed module exhibits a parasitic inductance of 25.91 nH, including the parasitics of the test circuit, which is slightly lower than that of typical wire-bonded modules. The demonstrated safe-operation-area extension makes this packaging approach highly promising for future high-reliability, high-performance grid-connected converter systems.**

***Index Terms*—Manifold microchannel (MMC), near-junction thermal capacitance (NJTC), overcurrent operation, power module, safe operation area (SOA), transient thermal management.**

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I. Introduction

The global shift toward carbon neutrality drives rapid adoption of renewable energy systems (RES). However, their inherent intermittency demands advanced power electronics to ensure grid stability. Modern RES relies on IGBT-based converters with limited overcurrent (OC) capability (1.5 p.u.), contrasting sharply with synchronous generators (SGs) (6–8 p.u.) [1]. This gap challenges fault management and postfault voltage recovery in RES-dominated grids. To match SG performance, grid-connected converters are expected to deliver 3.0 p.u. fault current for at least 3 s and sustain 1.5 p.u. current for 30 s [2]. Achieving this requires one to overcome thermal limitations—high heat flux and low thermal inertia in power modules.

Conventional power module packaging primarily uses wire bonding for electrical connections and thermal interface materials (TIM) for heat transfer to cold plates [3]. The multilayer heterogeneous materials along the thermal path and inadequate convective heat transfer efficiency presents substantial challenges in ensuring the safe operating temperature of power module. Advanced thermal management strategies have been developed to address high heat flux by minimizing thermal resistance, thereby providing additional temperature margin during OC events. Techniques including liquid jet impingement [4], microchannel cooling [5], and liquid metals [6] have been used to enhance convective heat transfer. Considering the high pressure drop of jet impingement cooling, its application in power modules requires further analysis and comparison to optimize its overall performance [7]. Structural innovations like integrated liquid cooling [8] and near-junction cooling [9] minimize conductive thermal resistance by reducing the number of layers between heat sources and coolant. However, this also reduces the thermal inertia of the module. Double-sided packaging significantly enhances thermal management and electrical performance by integrating cooling and electrical connections on both sides [10], while also increasing manufacturing complexity, cost, and maintenance.

Integrating passive heat-absorbing materials near the chip effectively enhances OC capability by increasing near-junction thermal capacitance (NJTC), enabling a rapid response to temperature rise [11]. Notably, phase change materials (PCM)

encapsulated in a metal frame beneath the chip have demonstrated remarkable OC tolerance, supporting 3 s operation at 3 p.u. and 30 s at 1.5 p.u. [2]. This advancement provides a critical way for developing power modules with sufficient OC capability for grid applications. However, due to the inherently low thermal conductivity of PCMs, in high-power modules where a single IGBT dissipates over 1 kW during OC events, the large volume of PCM required for effective thermal buffering significantly increases thermal resistance. Simulation results confirm that copper blocks can achieve comparable OC performance at a lower cost [12].

Positioning heat-absorbing materials above the chip can rapidly absorb the excess heat generated by the OC event without compromising thermal resistance [13]. As presented in [14] and [15], PCM is integrated into the molybdenum platelet above the chip to maintain a low thermal resistance and enhance the module's OC capability in press-pack power modules. For planar-packaged modules, employing a metal container integrated with PCM as the top device interconnection significantly increases the thermal capacitance above the chip, offering an effective solution for enhancing the OC capability. Since the top metal interconnection increases the thermal capacitance while also providing an additional heat dissipation path to the bottom heatsink, it is necessary to synergistically consider the impact of the bottom heat dissipation conditions on the top device interconnect. Comparing the OC performance using different materials above the chip and different convective heat transfer coefficients, PCM filling is more effective under a low cooling efficiency, while pure copper interconnections outperform PCM when the convective heat transfer coefficient exceeds 8000 W/(m^2·K) [16]. Meanwhile, considering that voids in PCM may lead to performance degradation after several cycles [17], and that the current water-cooled power modules already exhibit high convective heat transfer efficiency, using pure copper as the top interconnection offers advantages in cost-effectiveness, manufacturing simplicity, and reliability.

Integrating additional active cooling solutions into the module (e.g., placing microchannel cooling [18] or thermoelectric coolers [19] above the chip) dynamically improves OC capability but introduces systematic tradeoffs: added complexity from auxiliary pumps and fluidic networks, coupled with elevated lifecycle costs due to maintenance demands for sustained performance. Furthermore, how to promptly activate these additional cooling systems after an OC event remains a key challenge.

From the summarized literature, achieving high transient OC capability in power modules requires both the enhancement of NJTC and the implementation of advanced thermal management strategies. This article presents a power module with exceptional OC tolerance and ultralow thermal resistance. The module incorporates manifold microchannels within its substrate and replaces wire bonds with copper interconnects, enabling a significant increase in NJTC and providing dual thermal paths. The rest of this article is organized as follows. In Section II, the thermal management bottlenecks of the direct water-cooled pin-fin module are demonstrated. Section III presents the structure of the proposed module and its simulation-based optimization, covering the cost, size, and performance tradeoffs of the NJTC and MMC heat sink, as well as the module's manufacturing process. In Section IV, the proposed module's superior thermal performance under steady-state and OC conditions is experimentally validated, and the critical role of NJTC during OC events is quantitatively analyzed through simulations. Section V validates the electrical performance and practical robustness of the proposed module through double-pulse testing (DPT), experimental condition analysis, and a discussion on reliability considerations, laying the foundation for its future practical application. Finally, Section VI concludes this article.

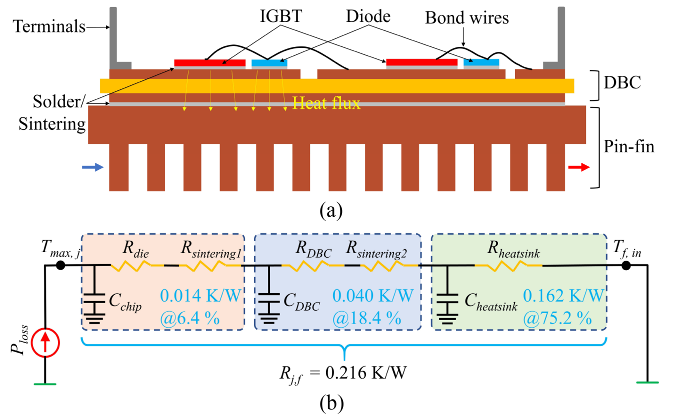

Fig. 1. (a) Structure and (b) thermal network model of the typical pin-fin based direct liquid-cooled module.

II. Thermal Performance Analysis of a Typical Pin-Fin Water-Cooled Power Module

A. Thermal Resistance Bottleneck

Currently, the direct liquid-cooled designs based on pin-fin structures have been widely adopted in commercial power modules [20]. The structure of a typical pin-fin power module, as illustrated in Fig. 1(a), mainly consists of semiconductor chips, a direct bonded copper (DBC) substrate, solder/sintering layers, a pin-fin heat sink, and power terminals [21]. Compared to conventional indirect water-cooled power modules, the elimination of both baseplate and TIM significantly reduces the thermal resistance.

The thermal resistance distribution of the direct liquid-cooled module is shown in Fig. 1(b), where R_{die}, $R_{\text{sintering1}}$, R_{DBC}, $R_{\text{sintering2}}$, and R_{heatsink} represent the thermal resistance of the die, die-attach sintering layer, DBC, sintering layer beneath the DBC, and the pin-fin heatsink, respectively. $R_{j,f}$ represents the thermal resistance from the chip junction to the fluid and is calculated by

$$R_{j,f} = (T_j - T_{f,\text{in}})/P_{\text{loss}} \quad (1)$$

where T_j and $T_{f,\text{in}}$ refers to the maximum temperature on the top surface of the device and coolant inlet temperature, respectively, and P_{loss} represents the power loss dissipated from the device to the coolant.

To further evaluate the overall thermal resistance and the contribution of each layer in the direct liquid-cooled module, finite volume simulations are conducted using ANSYS Fluent.

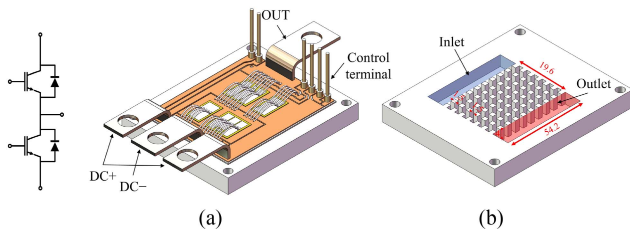

Fig. 2. (a) IGBT half-bridge module with pin-fin heatsink. (b) Schematic diagram of the pin-fin heat sink.

TABLE I
DIMENSIONS AND MATERIAL PROPERTIES OF EACH LAYER IN THE POWER MODULE

Layers	Size (mm)	Material	Thermal Conductivity (W/m·K)	Specific Heat Capacity (J/kg·K)
IGBT	9.6 × 10.26 × 0.16	Si	148	712
Diode	10.2 × 5.6 × 0. 16	Si	148	712
Sintering1	/ × / × 0.07	Nano-Ag	200	350
DBC	34.2 × 44.2 × 0.3	Cu	387	381
	35 × 45 × 0.38	AlN	170	700
	34.2 × 44.2 × 0.3	Cu	387	381
Sintering2	/ × / × 0.07	Nano-Ag	200	350
Heatsink	44.2 × 54.2 × 6	Cu	387	381

As illustrated in Fig. 2(a), the simulated model is a half-bridge IGBT module equipped with integrated direct liquid cooling. The pin-fin heatsink, as shown in Fig. 2(b), has a pin side length and pitch of 1.5 mm and a height of 4 mm. The material properties employed in the simulation are summarized in Table I. Considering the relatively large spacing between the two IGBT chips (>5 mm) and the uniformity of fluid distribution, thermal cross-coupling is limited. To match the experimental conditions, the 15 μm-thick epitaxial layer of a single IGBT chip is modeled as a volumetric heat source, and the maximum temperature within this region is extracted and reported as the junction temperature (T_j).

The thermal resistance distribution at an inlet flow rate of 2 L/min is shown in Fig. 1(b). The heatsink—including both the solid conduction region and the convective cooling interface—accounts for approximately 75.2% of the total junction-to-fluid thermal resistance. This result is consistent with previous studies on direct liquid-cooled modules [22], where the heatsink typically dominates the thermal resistance due to direct contact with the ceramic substrate and the minimized number of intermediate thermal layers.

The cooling challenge at the heat sink level limits further improvement of the module's thermal performance. To enhance the power density of modules, it is essential to develop and integrate thermally optimized heat sinks, particularly those featuring advanced flow field designs or microchannel structures to specifically improve heat dissipation capabilities.

TABLE II
POWER LOSS OF A SINGLE IGBT AT DIFFERENT CURRENTS

Current	Normal (70A)	2 OC (140A)	3 OC (210A)
Power	140 W	567 W	1003 W

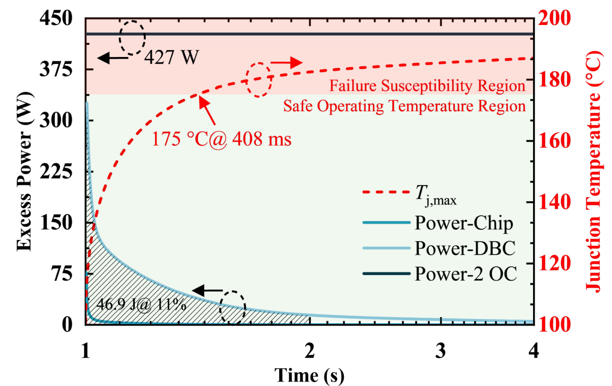

Fig. 3. Excess power absorbed by each layer and the variation of junction temperature over time under 2 p.u. OC condition for the direct liquid-cooled module.

B. Insufficient Transient Thermal Buffering

When an OC event occurs in a power module, the sudden surge in device power disrupts the original thermal equilibrium. During this transient period, the thermal capacitance of each layer buffers the abruptly generated Joule heat, significantly slowing the rise in junction temperature and delaying its approach to the new steady-state value, which would otherwise lead to device failure. This mechanism establishes a critical time window, enabling the protection circuitry to respond effectively. A longer time window enhances the overall system robustness and reliability under fault conditions.

To simulate the power module under OC conditions, the 15 μm-thick epitaxial layer of a single IGBT chip is set up as a variable heat source. Steady-state calculations are performed to establish preovercurrent conditions, followed by transient OC simulations initiating at 1 s. The power loss of the IGBT device used in the simulation at different current conditions is listed in Table II. The listed power loss values correspond to the conduction losses of the IGBT device under conduction state at various dc currents. These data are based on experimental measurements. After experimental validation, the device's power loss parameters used in the simulation are updated with the measured data, and the simulations are rerun to improve accuracy.

Fig. 3 illustrates the excess power absorbed by each layer and the variation of junction temperature over time under 2 p.u. OC condition for the direct liquid-cooled module, where the excess power is calculated as the difference between the OC power and the pre-OC steady-state power. The power absorbed by each layer is calculated as the difference between the heat

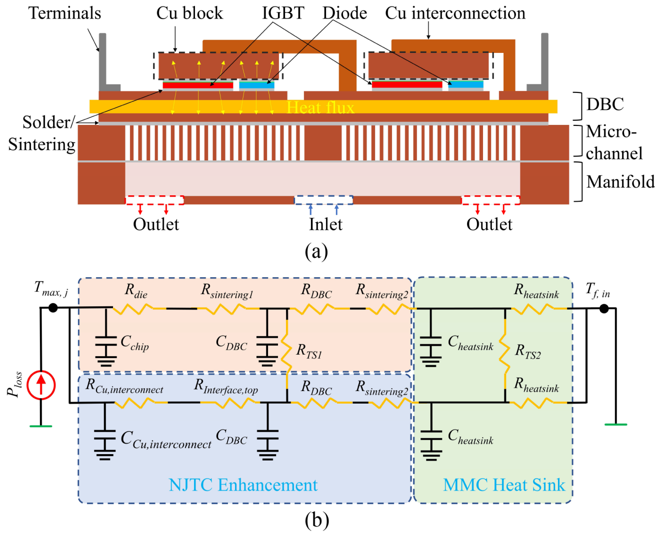

Fig. 4. (a) Structure and (b) thermal network model of the proposed module.

flux entering and leaving the top and bottom surfaces of that structure following the onset of OC.

Following an OC event, the DBC substrate rapidly absorbs heat due to its direct thermal contact with the IGBT device, enabling an immediate response to junction temperature rise. However, the limited thermal capacitance of the DBC causes its heat absorption capability to degrade sharply over time, ultimately failing to mitigate the junction temperature rise effectively. The IGBT junction temperature reaches 175 °C within 408 ms. During the first 1 s of the OC event, the DBC absorbs only 46.9 J, accounting for a mere 11% of the total excess energy generated by the OC.

This stark mismatch between transient heat generation and the thermal buffering capacity of DBC highlights a critical bottleneck in the liquid-cooled integrated packaging method under OC conditions.

III. Overcurrent-Capable IGBT Module Design

As analyzed in Section II, the limited OC capability of typical pin-fin-based direct liquid-cooled modules stems from two critical factors: the thermal resistance bottleneck of the heatsink and insufficient transient thermal buffering. This article proposes a new packaging structure with enhanced NJTC and adopts a manifold microchannel heatsink to reduce thermal resistance.

A. Structure of the Proposed Module

Fig. 4(a) illustrates the structural schematic of the proposed power module. In contrast to a typical pin-fin module, this design integrates two synergistic thermal management strategies: enhancement of NJTC through copper block interconnects and high-efficiency convective cooling via a substrate-embedded MMC heatsink.

In traditional pin-fin modules, heat is primarily conducted downward from the devices and dissipated through convective cooling. In contrast, the proposed module introduces dual heat conduction paths. Copper block interconnects offer significant advantages in both steady-state heat conduction and transient heat absorption due to their high thermal conductivity and volumetric heat capacity. Under steady-state conditions, the copper interconnects provide an additional upward thermal path from the device to the coolant. Heat conducted through the copper interconnect flows into the DBC and is ultimately extracted by the coolant in the MMC heatsink. Since the copper interconnect region is spatially separated from the main downward heat path, this parallel configuration effectively reduces the total junction-to-fluid thermal resistance. Under transient conditions, the copper interconnects function as a local thermal buffer. During OC events, they rapidly absorb excess heat, enabling temporary thermal energy storage. This mitigates the junction temperature rise rate and extends the safe operating duration under OC conditions.

The MMC heatsink is designed to significantly improve convective cooling performance. Its large specific surface area, high cooling efficiency, and excellent temperature uniformity outperform traditional Pin-fin heatsink [23]. Importantly, the heat removed through the upward and downward paths is ultimately carried away by the coolant in different flow areas of the MMC heatsink. This means that the MMC heatsink will simultaneously reduce the thermal resistance of both paths.

Fig. 4(b) presents the thermal network model of the proposed module, illustrating the dual heat dissipation paths from the power device. $R_{\mathrm{Cu,interconnect}}$ represents the thermal resistance of the copper interconnect. $R_{\mathrm{interface,top}}$ includes the thermal resistance of the sintered layer between the copper interconnect and the active region of the chip, as well as the soldering layer between the interconnect and the DBC. The copper interconnects not only serve as efficient upward thermal conductors but also significantly enhance the NJTC. Heat flowing through both the upward and downward paths is ultimately removed by the MMC heatsink. It is important to note that these two thermal paths are not completely independent. As heat is transferred into the DBC and the heatsink, lateral thermal spreading causes interaction between the two paths. To account for this coupling effect, R_{TS1} and R_{TS2} are introduced in the model to represent the lateral thermal spreading resistances in the DBC and the heatsink, respectively.

B. NJTC Enhancement Design

The power module employing copper interconnects instead of aluminum wire bonding is shown in Fig. 5(a). A vertical clearance of 2 mm must be maintained in the copper block region connected to the device's active area to meet electrical isolation requirements and reserve space for gate wire bonding. Considering the packaging volume constraints and cost factors, the height of the copper block, which is used to enhance the NJTC, needs to be carefully optimized.

For the pin-fin heatsink under water cooling conditions (coolant flow rate: 2 L/min), the achieved heat transfer coefficient (HTC) is approximately 30 000 W/(m^2·K). As shown in Fig. 5(b), simulation results using this HTC as a boundary condition demonstrate an excellent agreement with both full

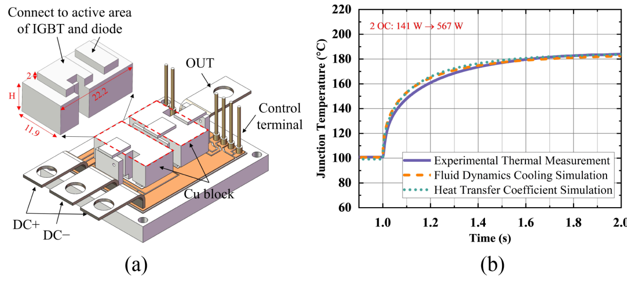

Fig. 5. (a) Schematic structure of a power module using copper interconnects. (b) Experimentally and numerically calculated junction temperature versus time at 2 p.u. OC.

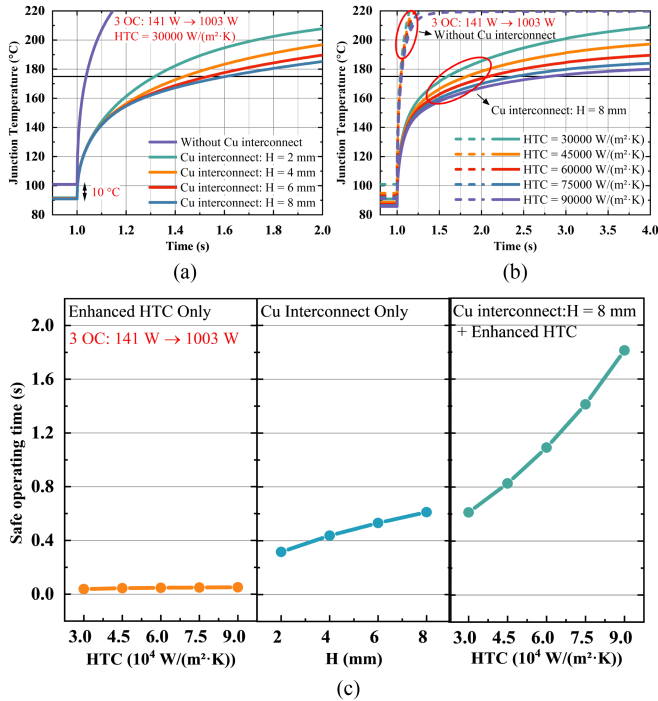

Fig. 6. (a) Junction temperature variation over time for modules with varying heights of copper blocks under 3 p.u. OC condition. (b) Junction temperature variation over time at different HTCs. (c) Safe operating time of power modules with different structures and HTCs at 3 p.u. OC.

fluid dynamics simulations and experimental measurements. Therefore, to obtain reasonably accurate simulation results with reduced computational resources, all simulations in this section are conducted using the HTC as the boundary condition.

Fig. 6(a) demonstrates the junction temperature variation over time for modules with top-side interconnect copper blocks of varying heights and those without copper interconnects under 3 p.u. OC condition. Under the same HTC, the proposed module achieves a 10 °C reduction in junction temperature under nominal operating current owing to the additional heat dissipation paths enabled by the top-side copper interconnects.

While increasing the copper block height extends the OC withstand duration, the thermal buffering effect saturates above a critical height threshold, with additional height increases demonstrating diminishing returns in suppressing the junction temperature rise rate. This limitation stems from inadequate thermal diffusion time during short overcurrent transients, which reduces heat absorption in the distal regions of copper block and consequently constrains thermal buffering capacity. Through comprehensive consideration of module manufacturing cost, dimensional constraints, and thermal performance enhancement, the copper block height of H = 8 mm is determined as the optimal design parameter, striking an optimal balance between transient thermal buffering capacity, material utilization efficiency, and system compactness.

As illustrated in Fig. 6(b), the junction temperature profiles under varying HTCs reveal critical limitations of typical modules without Cu interconnects. Although increasing the HTC reduces steady-state junction temperatures, it fails to effectively delay the temperature rise during the initial phase of OC events. The inherently low NJTC results in a smaller thermal time constant ($\tau = R_{th} \cdot C_{th}$), causing the junction temperature to rapidly approach the failure susceptibility region (safe operation duration < 50 ms). Within the first 50 ms, the heat has not yet fully reached the heatsink, resulting in negligible divergence among the junction temperature rise curves under different HTCs. Consequently, variations in HTC have minimal impact on the safe operating duration under OC events.

For modules with enhanced NJTC, the thermal buffering effect delays the junction temperature rise, allowing the junction temperature curves under different HTCs to diverge before entering the critical region. A higher HTC results in a lower steady-state postovercurrent temperature and a smaller transient temperature rise within the same OC duration, thereby extending the safe operating duration under OC conditions.

Fig. 6(c) quantitatively compares the effects of enhancing HTC, NJTC, and the combined application on the OC capability of the module. While improving HTC alone increases the module's current-carrying capacity, it offers limited benefits under severe overcurrent conditions (e.g., 3 p.u.), with a safe operating time of less than 50 ms. Increasing NJTC significantly extends the safe operating time to approximately 600 ms. However, this improvement is constrained by the limited thermal conductivity and volumetric capacity of thermal buffering materials, making further extension difficult.

By contrast, the synergistic enhancement of both NJTC and HTC enables a much more substantial increase in safe operating time, extending from less than 0.6 s with NJTC alone to nearly 2 s under 3 p.u. conditions, demonstrating a more-than-additive effect. This synergy highlights the effectiveness of combining NJTC design with advanced cooling technologies (HTC $>$ 30,000 W/m^2·K) as a promising strategy to improve the overload tolerance of power modules.

C. Structure of MMC Heat Sink

To achieve a higher HTC, an MMC heat sink is designed and implemented. A comprehensive comparison of MMC heat sinks with different manifold designs reveals that the U-shaped manifold demonstrates superior overall performance in terms of heat transfer efficiency, temperature uniformity, and pressure drop [24]. Meanwhile, considering the requirements for reliable

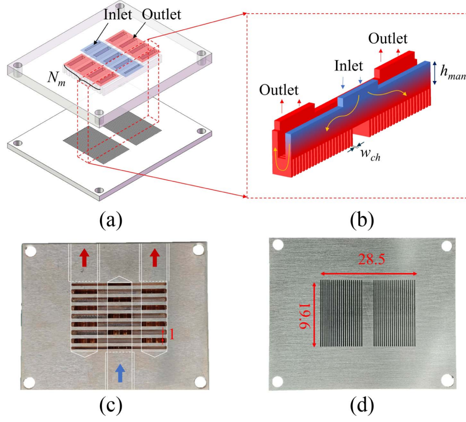

Fig. 7. (a) Exploded-view diagram of MMC heat sink. (b) Schematic diagram of coolant flow path in MMC heat sink. Photograph of (c) manifold and (d) microchannels.

mounting and scalability in power module cooling applications, this article proposes an area expandable manifold microchannel structure based on a U-type flow path, which balances thermal performance with engineering adaptability for module integration.

The structure and coolant flow paths of the MMC are shown in Fig. 7. The heat sink consists of two layers, which are bonded together using a silver sintering process. A special double-layer crossover manifold reduces the pressure drop while obtaining a high HTC by minimizing the flow length in the microchannels. In addition, multiple inlets in the manifold allow for a more uniform fluid distribution. Meanwhile, the connection ports between the manifold and the cooling loop can also be integrally machined as threaded holes directly on the manifold, as shown in Fig. 7(c), thereby minimizing the risk of coolant leakage. The microchannel is strategically divided into two independent zones to separately cool the upper and lower switch arm devices, thereby optimizing coolant flow distribution and maximizing thermal efficiency under high-power operation.

As shown in Fig. 7(b), the coolant enters through the inlet, makes a right-angle turn, flows along the microchannels, and exits from the outlet. The complex 3-D flow, combined with impingement effects and the high specific surface area of microchannels, achieves excellent heat transfer efficiency. Our previous work provides a more detailed description of this structure [25].

D. Microchannel and Manifold Design Using CFD Simulations

The manifold structure directly influences fluid distribution within the microchannels. An optimized manifold design ensures uniform coolant flow across all microchannels, effectively minimizing hot spots and enhancing thermal stability. Furthermore, well-structured manifolds contribute to the effective utilization of the coolant, ensuring that each microchannel participates actively in heat dissipation. Under identical microchannel aspect ratios, narrower microchannel dimensions can achieve higher heat transfer efficiency. However, this improvement is accompanied by increased manufacturing costs.

TABLE III
GEOMETRICAL AND OPERATING CONDITIONS FOR MANIFOLD MICROCHANNEL

Parameter	Value range
Manifold height h_{man} (mm)	1, **3**, 5
Manifold number N_m	3, **4**, 5
Microchannel aspect ratios	7:1
Microchannel width w_{ch} (μm)	100, **300**, 500
Flowrate	2 L/min
Coolant	Water
Fluid inlet temperature T_{in} (°C)	70
Heat source	280 W×2 IGBTs

TABLE IV
NUMERICAL THERMO-HYDRODYNAMIC RESULTS OF DIFFERENT MMC CONFIGURATIONS

h_{man}	ΔT_j/K	dT_j/K	ΔP/kPa
1 mm	54.38	0.22	5.05
3 mm	**44.92**	**0.17**	**2.37**
5 mm	44.31	0.43	1.56
N_m	ΔT_j/K	dT_j/K	ΔP/kPa
3	45.36	0.93	1.68
4	**44.92**	**0.17**	**2.37**
5	45.00	0.43	3.31
w_{ch}	ΔT_j/K	dT_j/K	ΔP/kPa
100 μm	33.11	0.33	2.81
300 μm	**44.92**	**0.17**	**2.37**
500 μm	49.59	0.03	2.29
	ΔT_j/K	dT_j/K	ΔP/kPa
Pin-Fin	64.34	2.94	2.84

The parameters to be optimized and their corresponding values are summarized in Table III, and the values selected based on the results are highlighted in bold. Due to the larger heat transfer surface area and higher fin efficiency, a microchannel with an aspect ratio of 7 exhibits optimal thermo-hydraulic performance [26]. The manifold height, the manifold number, and the microchannel width are selected as the optimization parameters. When modifying the microchannel width, the depth is adjusted accordingly to maintain a constant aspect ratio.

Table IV summarizes the junction temperature rise ΔT_j, temperature nonuniformity dT_j, and pressure drop ΔP across the heat sink for different MMC heat sink configurations. The values of ΔT_j and dT_j are calculated using the following equations:

$$\Delta T_j = T_{j,ave} - T_{f,\text{in}} \tag{2}$$

$$dT_j = T_{j,\max} - T_{j,\min} \tag{3}$$

where $T_{j,ave}$, $T_{j,\max}$, and $T_{j,\min}$ represent the average, maximum, and minimum junction temperatures of the two IGBT chips, respectively. The proposed manifold design enables all MMC configurations to maintain exceptionally low pressure drops. The choice of a 3 mm manifold height represents a tradeoff between heat transfer efficiency and module miniaturization. The change in the number of manifolds has a minimal impact on the overall heat transfer performance. A configuration

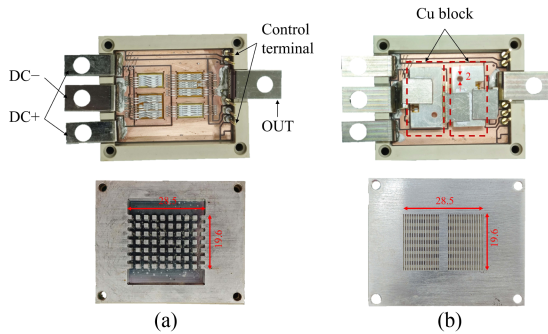

Fig. 8. (a) Photograph of the typical pin-fin module. (b) Proposed module.

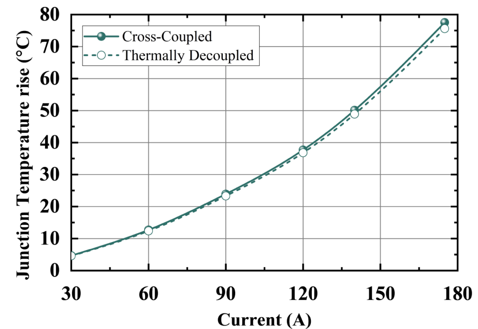

Fig. 10. Comparison of junction temperature rise with and without thermal cross-coupling under HTC = 90 000 W/m^2·K and an 8 mm NJTC copper block.

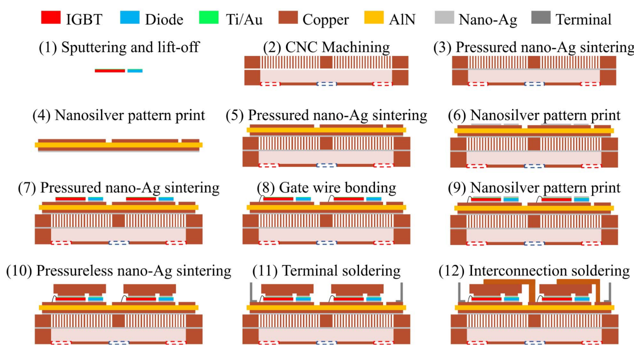

Fig. 9. Fabricating process of the proposed power module.

with four manifolds is selected to achieve good temperature uniformity between the chips. It can be observed that the smaller the microchannel width, the higher the heat transfer efficiency, highlighting the strong cooling potential of the MMC-structured heat sink. However, after evaluating the manufacturing complexity and cost considerations, a microchannel width of 300 μm was selected for fabrication and implemented in the power modules.

E. Manufacturing Processes

Fig. 8 presents the photograph of the typical pin-fin module and the proposed module. Both modules are composed of 1200 V / 100 A IGBTs and diodes configured in a half-bridge topology. They share the same DBC substrate, and the footprint area of the microchannel and pin-fin structures is identical, allowing for a direct performance comparison. A 2 mm diameter hole is created in Cu blocks to enable real-time monitoring of the IGBT's surface temperature using thermography. It is worth noting that the NJTC is locally reduced due to the fabrication of holes in the copper block. Therefore, the transient performance of the proposed module shall be even better in practical applications.

Detailed manufacturing processes are illustrated in Fig. 9. To ensure reliable silver sintering between the copper block and the chip, a 50 nm/100 nm Ti/Au thin film is sputtered onto the active area of the chip. The microchannels (300 μm in width and 2 mm in depth), manifolds, and copper block are all fabricated using computer numerical control (CNC) machining. To ensure sintering compatibility, a 1 μm silver layer is electroplated onto all metal surfaces.

The heatsink is fabricated by precisely aligning the manifold with the corresponding microchannel layer and bonding them through a silver sintering process. Specifically, a 200 μm nanosilver paste layer (Heraeus, ASP 338) is stencil-printed on the manifolds and soft-baked at 100 °C for 30 min, followed by high-pressure sintering at 35 MPa and 260 °C for 10 min. This process provides reliable metallurgical bonding under applied pressure and temperature. Subsequently, nano-silver sintering is similarly applied to bond the DBC onto the heat sink (25 MPa, 260 °C, 5 min) and the chips onto the DBC (15 MPa, 260 °C, 5 min). To avoid interference, gate wire bonding is performed first, followed by pressureless silver sintering on top of the chip (Heraeus, DA295A). Finally, terminals and copper interconnects are reflow-soldered using SAC305 solder at 260 °C.

IV. Thermal Testing and Result Analysis

A. Test Conditions and Setup

In converter design, reserving a 30% –50% safety margin is common practice [6]. Hence, the normal operating current of inverters fabricated using the proposed module is typically 70 A. Since the dc link voltage under normal operating conditions is relatively high, proper insulation, and encapsulation would be required for safe operation. To reasonably simplify the experimental setup and facilitate accurate real-time junction temperature monitoring using an infrared camera, a single IGBT is driven in the ON-state by a continuous 15 V gate signal and powered by a programmable dc source (IT-M3912D-32-480).

To validate this simplification, the thermal cross-coupling between the two IGBT chips in the proposed module layout is evaluated through simulation. The results are shown in Fig. 10, where the junction temperature rise of the upper-arm IGBT is compared under two conditions: 1) both upper-and lower-arm IGBTs are connected in series and conduct current I (cross-coupled) and 2) only the upper-arm IGBT conducting current I (thermally decoupled). The simulation methodology is implemented as follows: in the cross-coupled case, power P (corresponding to the power loss when a single chip conduct current I) is applied to both chips, resulting in a total power of $2P$. In the thermally decoupled case, power P is applied only to the upper arm chip. The results reveal a negligible difference between the two cases, with a maximum temperature deviation

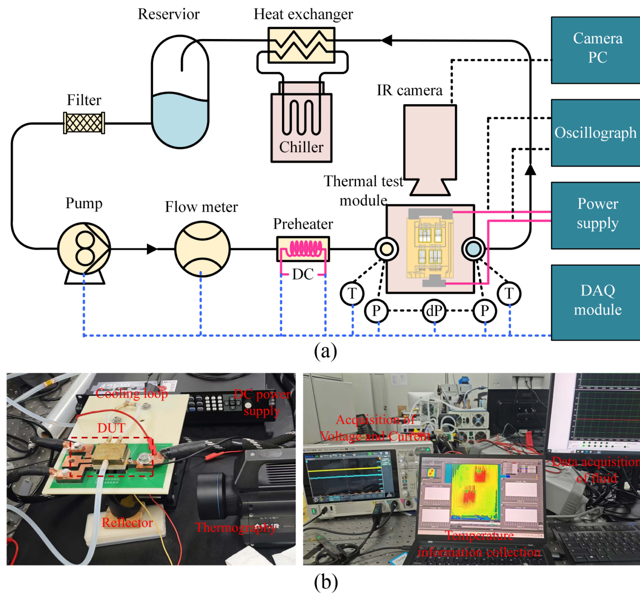

Fig. 11. (a) Schematic diagram. (b) Physical figure of the experimental setup for overcurrent experimental measurements.

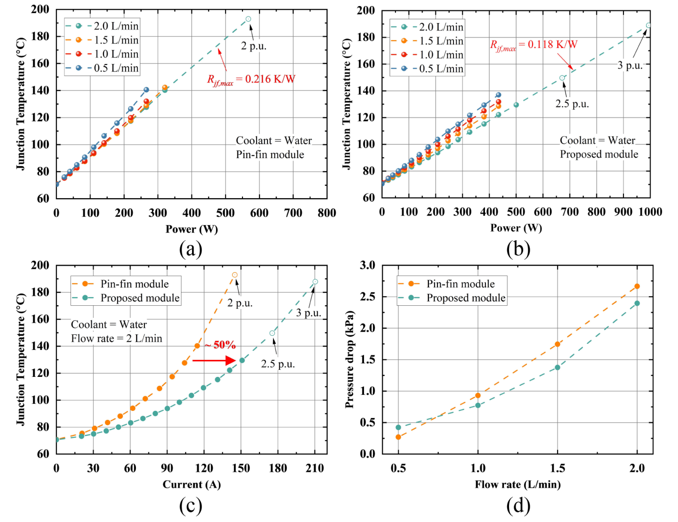

Fig. 12. Variation of junction temperature versus chip power dissipation for (a) the pin-fin module and (b) the proposed module. (c) Comparison of junction temperature variation versus current at a flow rate of 2 L/min. (d) Pressure drop comparison at different flow rates.

below 2.5%. This confirms that, under the present layout and cooling conditions, thermal cross-coupling is minimal and the measured temperature from a single IGBT is representative of its actual thermal behavior during overcurrent events.

The baseline current of the IGBT is set to 70 A dc, and the overcurrent is also dc. The OC event is triggered after the device reaches a steady-state condition at 70 A, ensuring that the thermal response to overcurrent is evaluated based on a well-defined initial state. Deionized water at 70 °C serves as the coolant to maintain controlled thermal boundary conditions. This temperature is selected based on IGBT datasheets, where the rated continuous collector current is typically specified at relatively high case temperatures. Utilizing a higher coolant temperature enables a more equitable and insightful comparison of overcurrent capability across diverse packaging configurations. Furthermore, it imposes more stringent thermal conditions, demonstrating the effectiveness of the proposed thermal management strategy under realistic, potentially harsh operating environments.

Fig. 11 illustrates the experimental setup. A Coriolis mass flowmeter positioned downstream of the pump measured real-time flow rates, while an in-line electrical heater controlled the coolant inlet temperature. For the test samples, inlet and outlet temperatures, along with pressure differences between them, were measured using two T-type thermocouples and a differential pressure transducer, respectively. After absorbing heat from the samples, the coolant was chilled via a plate heat exchanger and recirculated through a filter. To ensure accurate readings, a black coating with an emissivity of approximately 0.94 is applied to the chip surface. A calibrated infrared camera captures the chip temperature via a reflective mirror at a sampling frequency of 500 Hz. Simultaneously, current and voltage across the chip are recorded using a high-speed oscilloscope.

B. Steady-State Thermal Analysis

Fig. 12 presents the thermal performance and pressure drop of the modules under steady-state operation. As shown in Fig. 12(a) and (b), both modules are tested under four different flow rates (0.5–2 L/min) with gradually increasing power to obtain the junction temperature under various load conditions. The relationship between junction temperature and power is linear, and its slope represents the junction-to-fluid thermal resistance $R_{jf,\max}$. It can be observed that for the same module, increasing the flow rate reduces the thermal resistance. However, for the pin-fin module, the reduction in thermal resistance becomes marginal after reaching 2 L/min. In contrast, the proposed module demonstrates sustained cooling capacity enhancement with increasing flow rates. For safety precautions, experimental validation is limited to presteady-state conditions during OC conditions. Hollow circles indicate the steady-state temperatures achievable under OC conditions without failure, derived from heat dissipation and thermal resistance. At a flow rate of 2 L/min, the proposed module achieves a single-chip junction-to-fluid thermal resistance as low as 0.118 K/W, representing a 45% reduction in thermal resistance compared to the pin-fin module.

Fig. 12(c) presents the junction temperatures of both modules under varying load currents at a flow rate of 2 L/min. The proposed module can increase the chip current-carrying capacity by 50% while maintaining almost the same junction temperature and pressure drop. This implies that under prolonged 2 p.u. OC conditions (140 A), the chips in the typical pin-fin module exceed the safe operating temperature range ($T_j > 190\,°\mathrm{C}$), while the proposed module maintains a junction temperature around 130 °C, ensuring long-term reliable operation. Meanwhile, the enhanced thermal performance of the proposed module does not result in increased pumping power. As illustrated in Fig. 12(d), both module structures maintain low pressure drops across

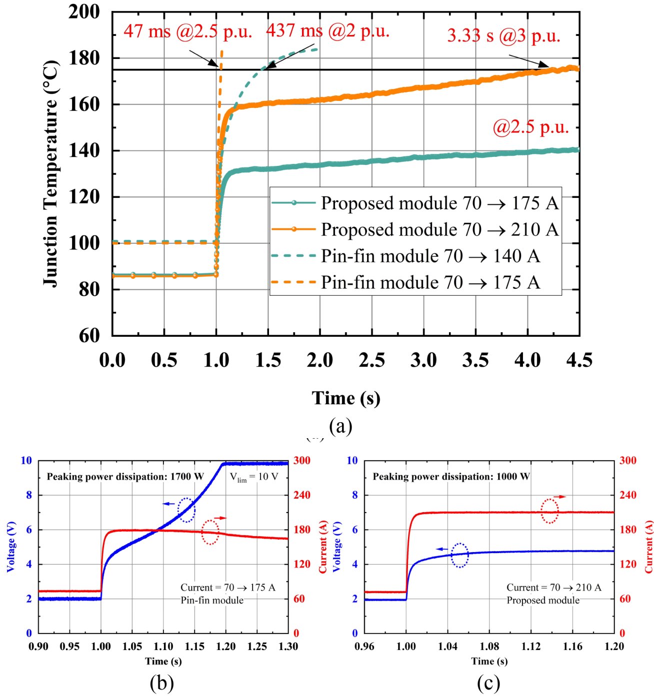

Fig. 13. (a) Comparison of junction temperature variation over time under different OC conditions at a flow rate of 2 L/min. IGBT current and voltage during OC for (b) the pin-fin module at 2.5 p.u. OC and (c) the proposed module at 3 p.u. OC.

various flow rates, enabling the potential for miniaturization of the coolant loop.

This improvement reduces the need for parallel modules in converters of equivalent specifications, minimizes parasitic parameters, and shrinks the size of converters, valves, and related equipment, thereby lowering manufacturing, operation, and maintenance costs. Furthermore, it offers enhanced safety margins under extreme conditions, mitigating risks of device breakdown or thermal failure.

C. Transient-State Thermal Analysis

OC tests are performed on both modules at 2 L/min flow rate. The variation of the junction temperature with elapsed time after the OC occurrence is shown in Fig. 13(a). The pin-fin module reaches 175 °C in 437 ms at 2 p.u. and 47 ms at 2.5 p.u., failing to meet grid OC tolerance requirements. Compared with the pin-fin module, the proposed module, benefiting from enhanced NJTC and heat transfer efficiency, exhibits significantly reduced temperature rise rate and target temperature under OC conditions. For the proposed module, the junction temperature is stabilized at approximately 150 °C under 2.5 p.u. OC conditions, enabling prolonged continuous operation. At 3 p.u., the junction temperature is elevated to 175 °C within 3.33 s, demonstrating compliance with transient overcurrent requirements for state-of-the-art grid-connected converters, validating the robust OC capability of the proposed module packaging.

Fig. 13(b) and (c) comparatively presents the terminal voltage and current waveforms of the pin-fin module under 2.5 p.u. and the proposed module under 3 p.u. OC conditions, respectively.

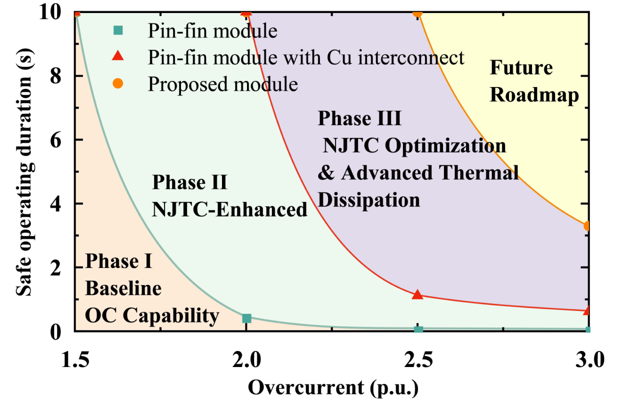

Fig. 14. Comparison of safe operating duration under different OC conditions for various packaging structures.

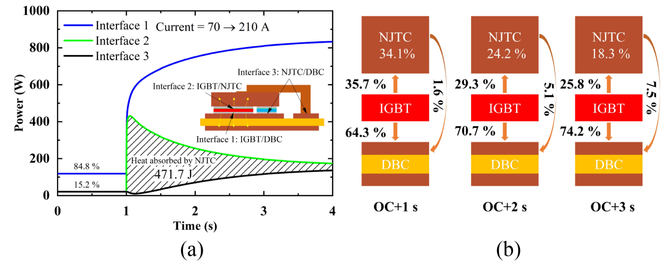

Fig. 15. (a) Power across interfaces before and during 3 p.u. OC. (b) Distribution of the additional energy generated by IGBT at 3 p.u. OC at different elapsed times (OC+1 s, OC+2 s, and OC+3 s correspond to 857 J, 1722.7 J, and 2578.6 J, respectively).

As shown in Fig. 13(b), thermal runaway is observed in the pin-fin module at 2.5 p.u. OC, characterized by the uncontrolled escalation of IGBT chip power dissipation following OC initiation. This positive feedback mechanism originates when the rise in junction temperature increases the IGBT's ON-state resistance, causing greater thermal power dissipation. This self-reinforcing cycle further elevates junction temperature, ultimately leading to catastrophic device failure. The experimental configuration incorporated a power supply voltage limit of 10 V, with the voltage ceiling being reached within 200 ms, corresponding to a peak thermal power dissipation of 1700 W. The proposed module maintains safe operation for over 3 s under 3 p.u. OC conditions. As demonstrated in Fig. 13(c), following OC initiation, the chip power dissipation is rapidly stabilized at 1000 W with complete suppression of thermal runaway.

As evidenced by the comparative analysis of Figs. 12(c) and 13(a), the pin-fin module at 2 p.u. and the proposed module at 3 p.u. demonstrate comparable steady-state junction temperatures, whereas their OC sustainability durations differ by nearly an order of magnitude. This comparison conclusively demonstrates that enhanced NJTC by reducing the rate of junction temperature rise plays an important role in OC capability improvement.

Based on simulation and experimental data, the safe operating duration of power modules with different packaging structures

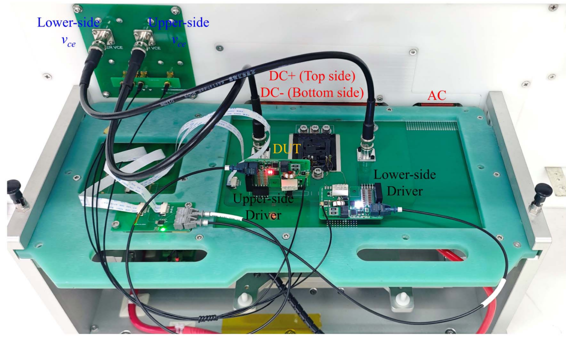

Fig. 16. Double-pulse test setup.

under various OC conditions is shown in Fig. 14 . If the safe operating duration exceeds 10 s, the module is considered capable of long-term steady-state operation under those conditions. It is evident that with the enhancement in NJTC and heat dissipation, the OC capability of the module can be significantly improved. In scenarios requiring only a 2.5 p.u. OC capacity, the standalone enhancement of NJTC is sufficient to meet the demand, avoiding the additional costs associated with improved cooling structures. However, for modules demanding a 3 p.u. OC capability, it is necessary to combine enhanced NJTC with advanced cooling strategies.

D. Simulation Analysis

This section quantitatively analyzes the impact of enhanced NJTC and advanced heat dissipation methods on OC performance based on simulation results. The accuracy of the simulation results has been validated by prior experimental results.

Fig. 15(a) illustrates the power variation over time across three interfaces in the proposed module under 3 p.u. OC conditions. The upward thermal path accounts for 15.2% of the power in the steady state. The power difference between Interface 2 and Interface 3 represents the power absorbed by the NJTC. When the 3 p.u. OC occurs, the NJTC rapidly absorbs heat, and the shaded area represents the energy absorbed by the NJTC, which is 471.7 J over the 3 s OC duration.

Fig. 15(b) illustrates the proportion of energy absorbed by the NJTC to the additional energy generated by IGBT at different elapsed times. Part of the energy absorbed above the chip is stored in the NJTC and the remainder passes through the NJTC to the heat sink. Due to its high thermal conductivity, copper absorbs a large amount of energy within a short time, i.e., 34.1% of the additional energy within 1 s of OC occurrence. This proves the importance of NJTC, and better results will be achieved by using materials with better thermal conductivity and higher heat capacity as NJTC.

E. Comparison With Existing SOA-Enhancement Approaches

The transient SOA performance of the proposed IGBT module is benchmarked with representative packaging technologies reported in the literature, as summarized in Table V. The OC level is normalized to the rated current, and the current type (dc, ac peak, or ac rms) specifies the reference used to define OC conditions. These distinctions are critical for fair benchmarking, as the power loss is strongly influenced by the current waveform characteristics. While many previous studies have aimed to extend the SOA by integrating PCMs or microchannel cooling structures either above or below the semiconductor devices, most of these approaches focus solely on either enhancing NJTC for heat absorption or implementing active cooling for heat extraction. However, the effectiveness of thermal capacitance enhancement is inherently constrained by the physical volume of the module, restricting the amount of excess heat that can be absorbed during OC events. As a result, such methods are often insufficient for high-power devices. In contrast, the proposed module achieves over 30 s of safe operation at 2.5 p.u., and 3.33 s at 3 p.u. under a single-chip power loss of 1000 W, while maintaining junction temperatures consistently below critical thresholds. This superior performance is attributed to the synergistic combination of passive NJTC enhancement and active heat extraction through advanced cooling. The proposed approach achieves a well-balanced integration of SOA extension, experimentally validated thermal performance, and practical manufacturability, making it a highly competitive solution for future high-reliability, grid-connected power conversion systems.

V. Electrical Characteristics Analysis and Discussion

A. Double Pulse Test

To investigate the impact of copper blocks as top interconnections on the electrical performance of power modules, the dynamic characteristics of the pin-fin module and the proposed module are measured through DPT, using the PRime-rel AVATAR-HD platform, as illustrated in Fig. 16. The current sensor used in the double-pulse test is integrated internally within the measurement equipment and is not externally visible. The lower arm of the half-bridge power module was switched with an inductive load across the upper switch.

Fig. 17 presents the DPT waveforms of the pin-fin module and the proposed module under a 220 V dc link voltage and a 75 A load current. The turn-ON and turn-OFF waveforms of both modules are nearly identical. The parasitic inductances of the pin-fin module and the proposed module are calculated as 26.38 nH and 25.91 nH, respectively, according to the following equation:

$$v_{ce,\text{spike}} = L_s \cdot {}^{di}/_{dt}. \tag{4}$$

It should be noted that the calculated inductance value includes both the DPT board and the components of the additional test circuit parasitics. This demonstrates that replacing traditional bonding wires with integrated top-side copper interconnections significantly enhances the power module's overcurrent capability while maintaining nearly identical electrical characteristics.

TABLE V
OVERVIEW OF POWER MODULE PACKAGING STRUCTURES FOR SOA EXTENSION

Reference	Packaging Method	Methodology	Device Size (mm^2) / type	OC Level (p.u.)	Power Loss (W)	SOA Extension
Present study	Cu interconnect with substrate-embedded MMC	Experiment and Simulation	9.6 × 10.26 / Si IGBT	2.5 / 3 (dc)	140–671 / 140–1003	>30 s @ 2.5 p.u., T_j < 150°C 3.33 s @ 3 p.u., T_j < 175°C
[2], [32]	PCM integrated below device	Experiment and Simulation	/ Si IGBT	3 (ac peak)	31.1–110.3	3 s, T_j < 130°C
[33]	Nano-enhanced PCM integrated below device	Experiment and Simulation	/ Si IGBT	2 / 2.5 (ac peak)	120–250 / 120–330	10 s @ 2 p.u., T_j < 133°C 10 s @ 2.5 p.u., T_j < 155°C
[34]	Microchannels embedded in DBC	Experiment	12 × 12 / Si IGBT	/ (dc)	~208.8 / ~244.8	30 s, T_j < 164°C 30 s, T_j < 185°C
[14]	PCM integrated into the press-pack module	Experiment and Simulation	14.1 × 14.1 / Si Diode	2 / 2.4 (ac rms)	96–229 / 96–280	3 s @ 2 p.u., T_j < 135°C 3 s @ 2.4 p.u., T_j < 150°C
[16]	PCM container as top interconnect	Simulation	6.44 × 4.04 / SiC MOSFET	/	125–250	20 s, T_j < 196°C
	Copper serving as top interconnection	Simulation	6.44 × 4.04 / SiC MOSFET	/	125–250	20 s, T_j < 199°C
[18]	Microchannels on top of device	Simulation	9.1 × 9.1 / SiC MOSFET	2 / 3 (ac rms)	104.4–505.65 / 104.4–1069.01	20 s @ 2 p.u., T_j < 250°C 1 s @ 3 p.u., T_j < 250°C

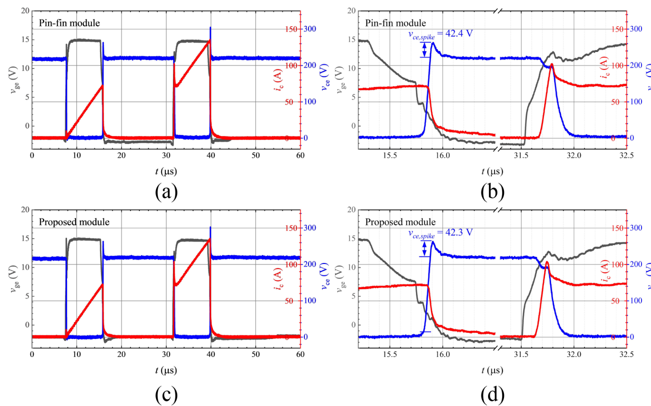

Fig. 17. Waveforms of DPT at 220 V/75 A. Full waveforms of (a) pin-fin module and (c) proposed module. Zoomed-in turn-ON and turn-OFF waveforms of (b) pin-fin module and (d) proposed module.

B. Comparison Between Experimental Setup and Inverter Operating Conditions

To evaluate the relevance between the experimental conditions and actual inverter overload scenarios, the IGBT power losses under typical switching operation and dc conduction conditions are calculated and compared, as summarized in Table VI. The loss estimation follows the methodology outlined in [12], which is commonly used to evaluate IGBT power dissipation under real-world inverter operating conditions. For the same rms output current, the power loss under dc test conditions is significantly higher than that under typical inverter operation. This indicates that the power dissipation applied during our experiments is conservative and even more severe than in practical inverter applications, thereby validating the robustness of the proposed module under extreme power loss.

C. Reliability Considerations and Future Work

While the proposed IGBT module demonstrates excellent thermal and overcurrent performance by integrating a copper block for NJTC enhancement, the use of such a thick copper block raises notable reliability concerns, primarily associated with the thermomechanical mismatch between copper and silicon. The substantial difference in the coefficients of thermal expansion (CTE) between Cu and Si may introduce significant thermomechanical stress during thermal cycling, potentially compromising long-term mechanical integrity.

To address this issue, prior studies have explored multiple mitigation strategies. One effective approach is replacing copper with materials such as molybdenum [27] or AlSiC [28], which offer better CTE compatibility with silicon while maintaining adequate thermal conductivity. Another promising solution is the use of porous sintered silver as a compliant interposer [29]; its low elastic modulus allows for stress absorption and deformation under load, thereby reducing interfacial stress. In addition, modifying the geometry of the interposer or spacer—such as adopting octagonal or structured surfaces—can help redistribute stress more uniformly across the bonding interface [30]. These techniques have all demonstrated measurable improvements in thermomechanical reliability, such as lower stress gradients, reduced warpage, and extended cycling life, while preserving thermal performance. In our current design, the copper block

TABLE VI
COMPARISON OF IGBT POWER LOSS UNDER INVERTER OPERATION AND EXPERIMENTAL TEST CONDITIONS ($T_j = 125\,^{\circ}$C)

Dc link voltage (V)	Current of converter I_o (A, rms, per IGBT)	Operating frequency (kHz)	Modulation index M	Grid power factor cosφ	Power loss P_{loss} (W)			Current of Dc supply I_{dc} (A)	Power loss P_{test} (W)
					conduction	switching	total		
600	70	7.5	0.9	0.9	60.4	42.1	102.6	70	138.6
600	140	7.5	0.9	0.9	197.4	84.3	281.7	140	434.0
600	210	7.5	0.9	0.9	411.0	126.4	537.4	210	886.2

is sintered onto the IGBT surface using a pressureless sintering process, forming a high-conductivity interface. Prior analysis indicates that residual stress and warpage associated with this bonding process can be significantly mitigated through careful control of sintering parameters and joint geometry [31].

Although this work primarily focuses on thermal design and performance validation, future work will incorporate insights from these advanced packaging strategies to improve the mechanical reliability of the proposed structure.

VI. CONCLUSION

This work presents a power module featuring enhanced NJTC and advanced thermal management technologies, which is fabricated via silver sintering. The results demonstrate that the synergistic combination of NJTC enhancement and high-efficiency convective cooling achieves a more-than-additive improvement in SOA extension. Compared with the traditional pin-fin module, the proposed module enables significantly longer safe operating time under severe overcurrent while maintaining manufacturability, offering a promising solution for high overcurrent capability power electronics. The main conclusions are summarized as follows.

1) At a flow rate of 2 L/min, the proposed module achieves a thermal resistance as low as 0.118 K/W, which is a 45% reduction in the junction-to-fluid thermal resistance compared to the pin-fin module. Additionally, the pressure drops for both modules remain at an extremely low level of less than 5 kPa at 2 L/min.
2) Under the same junction temperature, the proposed module achieves nearly a 50% increase in steady-state current-carrying capability, which plays a crucial role in reducing the number of parallel modules and lowering system costs.
3) Under transient OC conditions, the proposed module sustains stable operation for 3.33 s at 3 p.u. OC (1000 W per IGBT), outperforming pin-fin modules (47 ms at 2.5 p.u. OC) by nearly two orders of magnitude. The critical role of NJTC and the dual thermal path are quantitatively demonstrated through simulations, showing that within 1 s after the OC event, they account for 35.7% of the energy absorption.
4) Double-pulse test results reveal that replacing wire bonds with copper interconnects does not impact the module's electrical performance. Including the parasitics from the DPT board and the additional test circuit components, the proposed module exhibits a parasitic inductance of 25.91 nH.
5) While the proposed module demonstrates strong thermal and overcurrent capabilities, its mechanical reliability can be further enhanced by adopting advanced packaging strategies—such as stress-buffering interlayers, compliant interposers, and geometry optimization—to address challenges associated with thick copper structures.

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