Resonant Switched-Capacitor Multilevel Inverter

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***Abstract*—For almost a decade, switched-capacitor multilevel inverters (SCMLIs) have been a prominent research topic in power electronics due to their attractive features, including inductor-less voltage boosting capability, ease of control and implementation, as well as self-voltage balancing of capacitors. However, a major shortcoming of SCMLIs is the imperative parallel charging process of the capacitors from a dc source or another internal SC-based unit, which causes unwanted inrush currents, electromagnetic interference generation, and excessive current stress posing a critical challenge for high power applications. Consequently, the deployment of SCMLIs in future photovoltaic and motor drive applications remains uncertain. To address these critical issues, this article introduces a novel class of SCMLIs featuring an integrated resonant (Res)-based charging operation with a soft-switching and soft-charging procedure. For the first time, this innovative concept is applied to an active boost neutral point-clamped (ABNPC)-based five-level (5L) converter, enabling full dc-link utilization at the ac output through a resonant network without any inrush or current stress issues. The 5L-ABNPC-based variant of the proposed Res-SCMLI, which can be modulated through both phase-shifted or level-shifted standard pulsewidth modulation strategies, consists of four bidirectional and four normal FETs, two dc-link capacitors, and one floating self-balanced capacitor. Extensive analysis, a comparative study, and validation through simulation and experimental results from a 3 kW SiC-based single-phase laboratory-built prototype for both open-loop and grid-connected conditions confirm the effectiveness of this approach.**

***Index Terms*—And soft-Switching operation, full dc-link utilization, multilevel inverter (MLI), resonant network, soft-charging, switched-capacitor.**

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I. Introduction

THE next generation of power electronic converters requires ultra-efficient designs that optimize overall efficiency, power density, and overall cost with additional circuit functionality to support net-zero emission targets in many developed countries [1]. The emergence of new wide-band-gap (WBG) devices, i.e., SiC or GaN-FETs, significantly facilitates this goal, enabling high-frequency power electronics converters that reduce the size of passive elements, i.e., the electromagnetic interference (EMI) filters as the bulkiest system components [2], [3].

Concurrently, for applications such as photovoltaic (PV) grid-connected systems, bidirectional electric vehicle (EV), and induction motor drives, when dc–ac power conversion is a prime focus, further topological advancements in existing methodologies are still necessary [4]. This originates from the fact that traditional three-level (3L) converter architectures face limitations in scalability and efficiency, making the exploration of advanced multilevel inverter (MLI) topologies crucial for improving power quality and minimizing filtering requirements [4], [5].

Among many variants of MLIs, mid-point-clamped-based topologies like stacked-multicell (SMC) [6], active neutral-point-clamped (ANPC) [7], [8], [9], and T-Type-based structures [10] become more popular in grid-connected applications and variable speed hydro drives as they can be established with reduced stress WBGs, while providing a virtual ground with respect to the output voltage for leakage current mitigation. Ability to be modulated with a phase-shifted (PS)-pulsewidth modulation (PWM) strategy is another interesting feature of them, where the provided redundant switching states (RSSs) can be efficiently exploited to increase the output apparent switching frequency with respect to the effective switching frequency for a reduced EMI or output filters [11], [12]. A smooth current stress drawn from the dc supply is also another appealing feature as these class of MLIs need a minimal effort for double-line frequency mitigation in a single-phase application with a passive-based solution [12].

Even though giving such impactful opportunities, mid-point-clamped-based MLIs are all buck-based topologies meaning that due to their half voltage conversion gain, an input dc voltage of at least 800 V is necessary to achieve a successful power injection into a 230–245 V rms grid [13]. Their operation highly relies on the flying-capacitor (FC) technique and RSSs to generate

output voltage levels, which requires careful balancing of the dc-link voltage and FCs [12]. As the number of output voltage increases, i.e., inclusion of more FCs, the neutral-point of dc-link capacitors needs more stiff and robust control. In addition, for input dc or battery packs voltages that are around 400 V, an additional power processing stage is needed to meet the minimum requirement of the load/grid voltage for power injection [14]. Moreover, due to lack of any reactive network, the switching operation of all the high-switching frequency devices in such FC-based MLIs is hard, while this can hinder their WBG-based utilization in higher range of switching frequency owing to excessive switching losses [15].

Alternatively, integration of switched-capacitor (SC) technique into the MLIs created a new class of MLIs called SCMLIs, where the capacitor(s) are directly charged by the dc source or another voltage-level creator unit, and then without involving any other energy storage elements, i.e., boost inductors, they can deliver their charged voltage to the output. This makes new opportunity for realization of inductor-less boost-based converters within an acceptable power density, when smaller range of input dc voltage, e.g. 400 V, is available to feed a standard grid [16]. Self-voltage balancing of the capacitors makes their application much easier than FC-based MLIs, as well since there is no need for active voltage balancing of dc-link capacitors and FCs [17].

Five-level (5L) ABNPC-MLIs presented in [18], [19] and [20] with unity voltage conversion gain, and the one proposed in [21], with half voltage conversion gain, as well as their derivations in larger number of output voltage levels realization such as [22], [23], and [24], are among the most popular ones SCMLIs in this context. Even though having such a popularity in the research topic during the latest decade, the inrush current and the large current stress concern of devices are among two major drawbacks of the SCMLIs, which cause a great deal of uncertainty for their application-oriented design [16], [22]. This high current stress issue at full modulation index of operation is more problematic as the SC charging process is associated with flowing the load current at the same time with a hard switching action of the involved SC loop devices. This leads to EMI concerns and poor efficiency at relatively high output power [16].

Inspired by the idea of integrating a resonant network into the SC charging path, there is a potential to define a new class of SCMLIs as this has been a well-known approach in dc-dc SC-based converters [25]. In this special case, which is the scope of this article, the resonant network is charged to the input dc voltage within a specific switching scheme corresponding to its resonant frequency. Subsequently, during the remaining portion of this resonant period, the stored energy is transferred to the FCs. Through this, the aggressive and discontinuous nature of the input current can be alleviated, while the FC can possess much smaller values than the original SCMLIs. This partial soft-charging operation has been already applied in [26], and [27], at low power; however, they have never widely been elaborated in SCMLIs.

Regarding the above mentioned contributions, a new class of resonant (Res)-based SCMLIs over the mid-point-clamped-based circuit architecture is proposed in this work, which mainly provides the following substantial features:

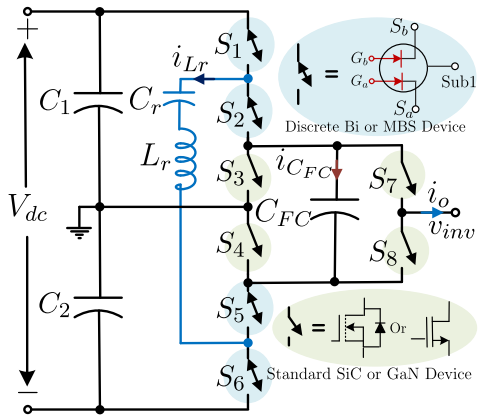

Fig. 1. Proposed 5L-Res-based-ABNPC converter.

1) Full dc-link voltage utilization at the ac output, while giving 5L output voltage.
2) Significant reduction in current stress profile of devices even at full modulation index with an integrated passive resonant tank.
3) Soft-switching action of the devices that are involved in the charging path of FC.
4) Bidirectional power flow operation and full reactive power support.
5) Flexibility in modulation where both PS- and level-shifted (LS)-PWM can be exploited.
6) Ability for practical realization using low voltage stress WBGs and reasonable FC capacitance.

The rest of the article is organized as follows. Details of working principle and modulation strategies of the novel Res-SCMLI concept applied to a 5L-Res-based-ABNPC converter given in Section II. Design guidance of the passive elements is discussed in Section III. Detailed simulation results over the PLECS are presented in Section IV. In following, a comprehensive comparative study over the state-of-the-art topologies is conducted in Section V. Extensive experimental results obtained from a 3 kW single-phase laboratory-built prototype using SiC-based WBGs are then presented in Section VI. Finally, Section VII concludes this article.

II. Proposed Res-SCMLI

The 5L-Res-based-ABNPC variant of the proposed Res-SCMLI topology is illustrated in Fig. 1. As can be seen, apart from the dc-link capacitors, C_1 and C_2, this novel class of SCMLIs is comprised of four bidirectional/four-quadrant devices, i.e., S_1, S_2, S_5, and S_6, and four standard GaN or SiC-based FETs formed as a classical back-end H-bridge, i.e., S_3, S_4, S_7, and S_8. While, the bidirectional devices are used to block a stress voltage in both polarities and to conduct a symmetric current in both directions, they can be provided through different circuitry configurations, i.e., common-drain or common-source with discrete- or monolithic-based FETs [28], [29]. As per the current state-of-the-art status, their common-drain GaN-based version providing whole the device in a single-chip called as

monolithic bidirectional switch (MBS) is getting manufactured by Navitas, Infineon, and Transphorm/Rensas [28], [29].

As depicted in Fig. 1, their symbol is slightly different with respect to the normal FETs as they need two gate-source leads per device, with an isolated gate-driver per each gate-source lead [29]. Hence, if common-source-based configuration is to be considered for the bidirectional devices, the total number of gate drivers for the proposed 5L-Res-based-ABNPC converter is eight, while if their MBS version is to be realized, then this number is turned to 12.

The proposed 5L-Res-based-ABNPC converter needs a resonant tank including L_r and C_r as well to provide a smooth charging/discharging profile for the FC. With a proper design procedure for this resonant tank, the soft-switched operation of the devices that are involved the charging path of the FC can also be guaranteed. As can be realized from Fig. 1, the proposed topology needs only an input dc voltage equals to V_{dc} to provide 5L output voltage with full dc-link voltage utilization at the ac output. This comes from the fact that both the resonant tank and the FC voltages are balanced at V_{dc}. In the following sections, its detailed operation is discussed.

A. Working Principles

Different switching states of the proposed 5L-Res-based-ABNPC converter have been depicted in Fig. 2, where the green and red traces represent the charging/discharging path of the resonant tank, and the load current, respectively. As can be understood, per each output voltage level, there are two RSSs in which, the resonant tank is charged directly by the input dc voltage through one RSS, and then it gets discharged its energy to the FC with the other RSS path. Here, the standard normal FETs formed as a H-bridge only carry the load current. However, bidirectional devices are in charge of handling the charging/discharging current of the resonant tank. As per "State A and B" for +1 output voltage-level and "State G and H" for -1 output voltage-level, three out of four bidirectional devices are either in charging path of resonant tank/FC or the ac load, while either S_7 or S_8 is ON to translate the ac polarity. Per remaining output voltage levels, only two bidirectional devices are in the charging path of resonant tank/FC, and two normal FETs from the H-bridge part are involved in the ac load current flowing path.

Admittedly, the maximum voltage level of the converter denoted as "State E and F" for +2 voltage-level and "State K and L" for -2 voltage-level in Fig. 2, is created by the help of the FC voltage solely. Considering this, the resonant tank current not only regulates the FC voltage, but also supports part of the load current during these top-level output voltage states. As the proposed 5L-Res-based-ABNPC converter offers a full dc-link utilization at its ac output, these maximum output voltage levels are equal to $\pm V_{\text{dc}}$, which implies the same unity voltage gain ratio as the conventional SC-based-5L-ABNPC converter.

One can also notice is the role of the dc-link capacitors, i.e., C_1, and C_2, which are only in charge of delivering the voltage to the ac output during the middle voltage levels generations, i.e., $\pm V_{\text{dc}}/2$. Concurrently, the maximum voltage stress (MVS) of all the bidirectional devices is equal to $\pm V_{\text{dc}}/2$, while this value for the idea presented in [10], the proposed 5L-Res-based-ABNPC converter can be further generalized if an additional T-cell is to be added before the dc-link capacitors. Under this assumption, a seven-level Res-based ABNPC inverter is derived, in which its overall voltage gain is 1.5.

B. Resonant Network Analysis

This section presents an analytical framework to estimate the maximum value of the resonant current, $I_{Lr,m}$, passing through the resonant tank using a Thevenin-based model of the FC charging/discharging time interval. Determination of this maximum value is crucial to realize the current stress mitigation capability of the proposed Res-based SCMLI. Fig. 3 illustrates the simplified resonant tank behavior during a single FC charging event in the proposed converter, while Fig. 4 shows the typical waveforms including the load current, i_o, the resonant tank passing through current, i_{Lr}, the voltage across the FC, v_{FC}, the current passing through the FC, i_{FC}, and the instant voltage across the resonant tank, v_{res}.

The analysis is based on a 50% charging duty cycle of the resonant tank, D, which defines the resonant charging/discharging interval to be exactly half of each resonant switching period, t_{res}. This fixed duty cycle is selected to ensure symmetric resonant operation, simplifying both the waveform analysis and modulation scheme. The 50% allocation of D allows the FC to efficiently exploit both RSSs provided per each output voltage level, while it can guarantee a proper zero-crossing for i_{Lr}, which is critical for soft switching operation of the involved devices in the charging/discharging path of the FC.

As shown in Fig. 3, the excitation voltage, v_{res}, applied across the resonant tank (comprising of L_r, C_r, and R_r) is approximated by a bipolar pulse waveform, v_p, derived from the switching pattern of the converter. This voltage can be roughly calculated using the first harmonic approximation method as follows:

$$v_p(t) = v_{\text{res}}(t) \approx \frac{V_{\text{dc}} - v_{\text{FC}}(t)}{2} + \frac{2(V_{\text{dc}} - v_{\text{FC}}(t))}{\pi} \sin(\omega_{\text{d}} t) \tag{1}$$

where, ω_d is the damped natural frequency equals to

$$\omega_d = \sqrt{\omega_{\text{res}}^2 - \alpha^2} = \sqrt{\frac{1}{L_r C_r} - \left(\frac{R_r}{2L_r}\right)^2}. \tag{2}$$

where $\omega_{\text{res}} = 2\pi f_{\text{res}}$ is the angular resonant frequency and α is the damping factor.

Considering (1) and Fig. 4, the resonant tank current, i_{Lr}, exhibits a damped sinusoidal shape at every instance reaching a peak before reversing as energy is exchanged between L_r and the FC capacitance, C_{FC}. As illustrated in Fig. 4, this resonant waveform is terminated at the zero-crossing point of current, which occurs at $t = 0.5t_{\text{res}}$, and its relationship is expressed as:

$$i_{Lr}(t) \approx \frac{2(V_{\text{dc}} - v_{\text{FC}}(t))}{\pi R_r} \sin(\omega_{\text{d}} t). \tag{3}$$

where $v_{\text{FC}}(t)$ is the instant voltage across the FC.

Referring to (3), the maximum value of i_{Lr} can be found when

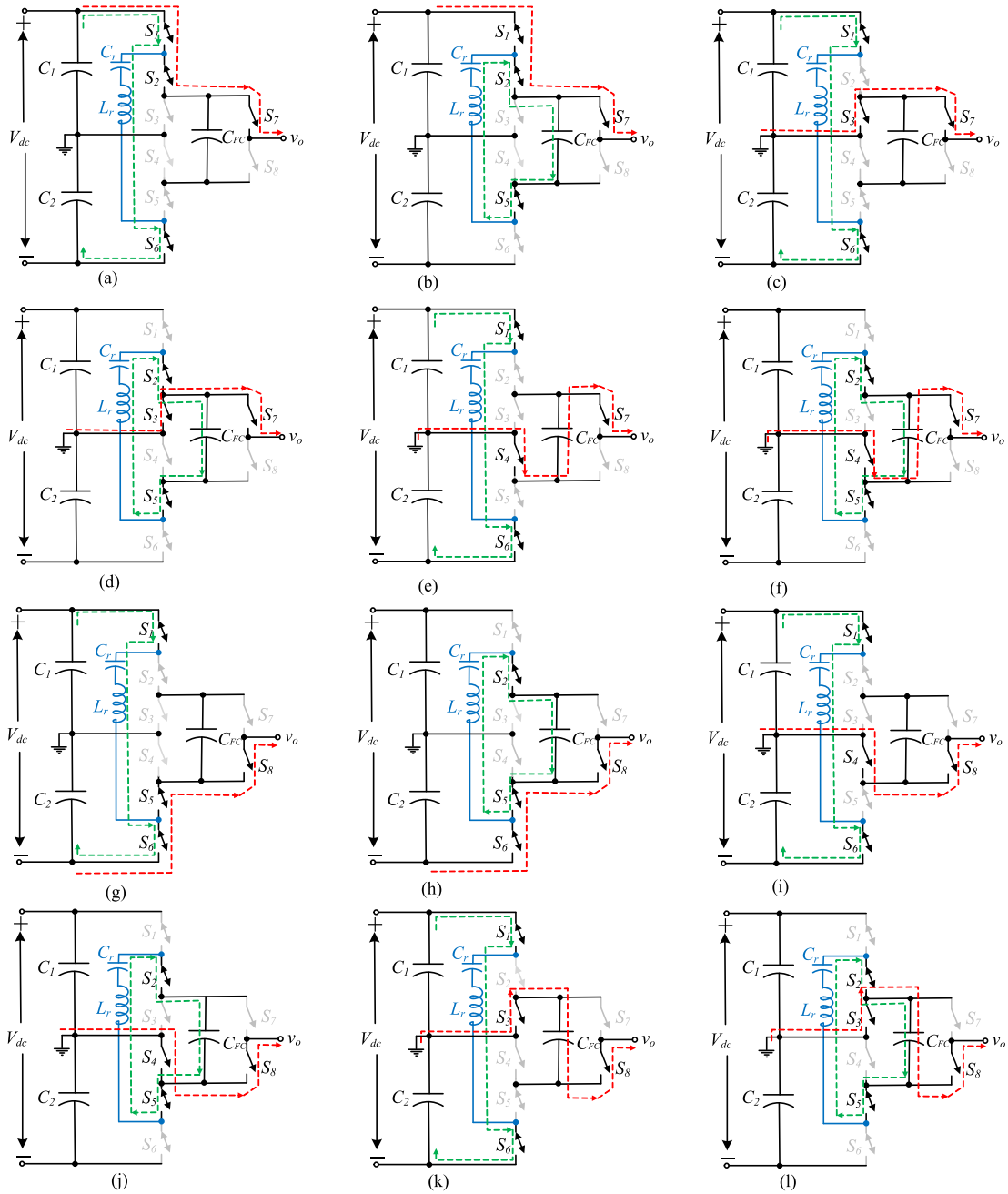

Fig. 2. Different switching states of the proposed 5L-Res-based-ABNPC converter. (a) State A (+1). (b) State B (+1). (c) State C (0). (d) State D (0). (e) State E (+2). (f) State F (+2). (g) State G (−1). (h) State H (−1). (i) State I (0). (j) State J (0). (k) State K (−2). (l) State L (−2).

v_{FC} in Fig. 4). To find out $v_{\mathrm{FC}}(t)$, Thevenin equivalent circuit per each charging/discharging resonant event of the FC shown in Fig. 3 is helpful. Hence the FC and resonant tank time constant can be attained. Here, the open-circuit voltage, V_{oc} seen at the input of the FC charging path represents the Thevenin equivalent voltage, $V_{\mathrm{th,eq}}$. Contemporary, $R_{\mathrm{th,eq}}$ is the Thevenin equivalent resistance, which accounts for the energy dissipation and the effective damping during the charging period. It is determined by the ratio of V_{oc}, and I_{sc} observed at the same port. Here, I_{sc} is the short-circuit current of the resonant network when the FC voltage is assumed to be zero. Regarding the estimated relationship of i_{Lr} expressed in (3), I_{sc} is calculated as follows:

$$i_{\mathrm{sc}}(t) = \begin{cases} \frac{2V_{\mathrm{dc}}}{\pi R_r}\sin(\omega_{\mathrm{d}} t), & 0 < t \le 0.5t_{\mathrm{res}} \\ 0. & 0.5t_{\mathrm{res}} < t \le t_{\mathrm{res}} \end{cases} \tag{4}$$

$$I_{\mathrm{sc}} = \frac{1}{t_{\mathrm{res}}}\int_0^{t_{\mathrm{res}}} |i_{\mathrm{sc}}(t)|\, dt = \frac{2V_{\mathrm{dc}}}{\pi^2 R_r}. \tag{5}$$

Hence, considering $V_{\mathrm{oc}} = V_{\mathrm{dc}}$, we would have

$$R_{\mathrm{th,eq}} = \frac{V_{\mathrm{oc}}}{I_{\mathrm{sc}}} = \frac{\pi^2 R_r}{2} \approx 4.935 R_r. \tag{6}$$

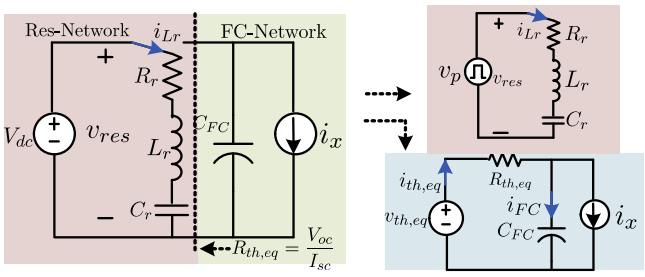

Fig. 3. Resonant and FC loop equivalent circuit with Thevenin-based model, where i_x is the contribution of the ac load current on FC current at top positive/negative output voltage levels of the proposed 5L-Res-based-ABNPC converter.

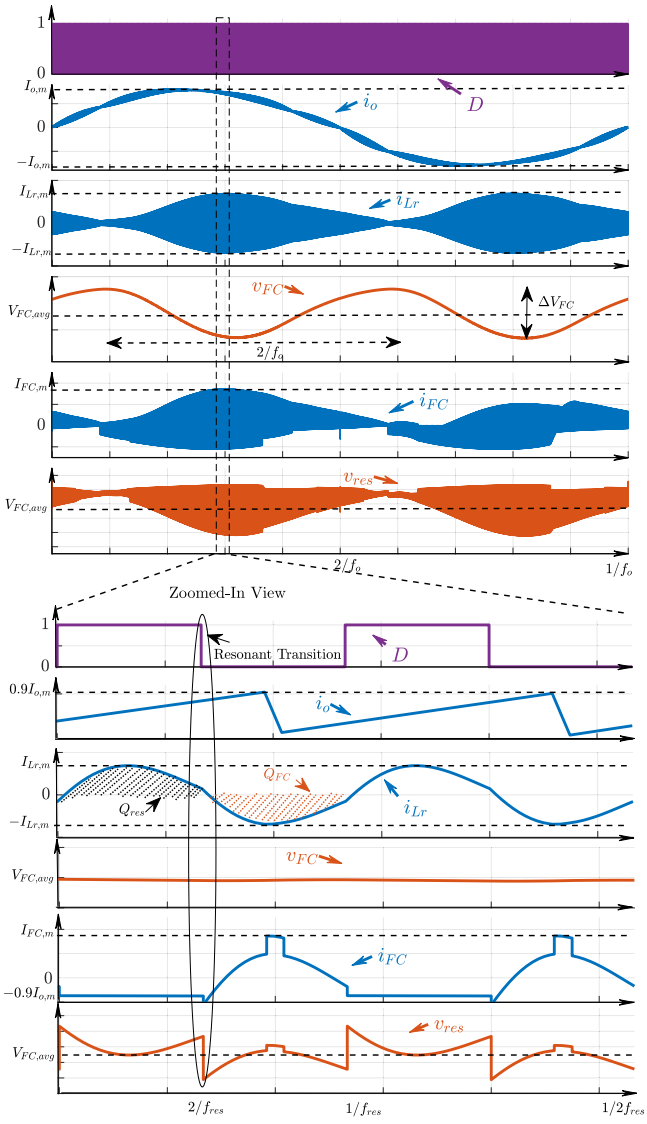

Fig. 4. Typical waveforms of the proposed 5L-Res-based-ABNPC converter for the resonant tank analysis and its affect over the FC at full modulation index. All analytical results are based on a grid-connected case with unity PF, i.e., purely resistive loading.

This value directly defines the resonant time constant of the FC charging process via

$$\tau = R_{\text{th,eq}} C_{\text{FC}}. \tag{7}$$

On the contrary, a simplified expression for the Thevenin-equivalent current, $i_{\text{th,eq}}$, which captures the combined effect of the FC charging current, i_{FC}, and the influence of the load current drawn from the inverter's top-level output voltage, $i_x(t)$ is of importance. Hence, we can write

$$i_{\text{th,eq}}(t) = i_{\text{FC}}(t) + i_x(t) = \frac{V_{\text{th,eq}} - v_{\text{FC}}(t)}{R_{\text{th,eq}}}. \tag{8}$$

Having considered, $V_{\text{th,eq}} = V_{\text{oc}} = V_{\text{dc}}$, $v_{\text{FC}}(t)$ can be found out by solving the following differential equation.

$$\frac{V_{\text{dc}} - v_{\text{FC}}(t)}{\tau} = \frac{i_x(t)}{C_{\text{FC}}} + \frac{dv_{\text{FC}}(t)}{dt}. \tag{9}$$

As is clear from (9), finding $i_x(t)$ that is the contribution of the load current during discharging period of the FC, is necessary to solve (9). To find this, having the instant voltage of the proposed inverter output voltage is helpful as

$$v_{\text{inv}}(t) = \text{M}V_{\text{dc}} \sin(\omega_{\text{o}} t) = \text{ac}(t) V_{\text{dc}} \tag{10}$$

where M is the modulation index, ω_{o} is the angular frequency of the load voltage, and $\text{ac}(t)$ is the ac modulation reference.

On the other hand, the general sinusoidal form of the ac load current can be written as follows:

$$i_o(t) = I_{o,m} \sin(\omega_{\text{o}} t + \varphi) \tag{11}$$

where φ is the power factor (PF) angle between the inverter output voltage and load current, and $I_{o,m}$ is the peak value of the load current.

Now, to calculate $i_x(t)$, the duty cycle of the inverter output voltage during top positive/negative output voltage levels should be calculated as follows:

$$\text{ac}_{12}(t) = \begin{cases} 2\text{ac}(t) - 1, & \theta_1 < \omega_{\text{o}} t \le \theta_2 \\ 0. & \text{otherwise} \end{cases} \tag{12}$$

where

$$\begin{cases} \theta_1 = \sin^{-1}(\frac{1}{2M}) \\ \theta_2 = \pi - \sin^{-1}(\frac{1}{2M}) \end{cases}. \tag{13}$$

Hence, taking (10), (11), (12), and (13) into account, $i_x(t)$ can be found as follows:

$$i_x(t) = \text{ac}_{12}(t) i_o(t) = I_{o,m}(2\text{ac}(t) - 1) \sin(\omega_{\text{o}} t + \varphi). \tag{14}$$

Taking $i_x(t)$ into consideration and subsequently replacing this in (9), $v_{\text{FC}}(t)$ is attainable. Hence, a closed-form analytical solution for $I_{Lr,m}$ can be indirectly found through the maximum value of the described expression given in (3). By solving this relationship numerically over a range of practical operating points, the variation of $I_{Lr,m}$ with respect to different peak values of load current, modulation indexes, and load PF angle can be systematically visualized as demonstrated in Fig. 5(a) and (b). All results are based on realistic hardware choices as: $C_{\text{FC}} = 470\ \mu$F, $L_r = 4\ \mu$H, $C_r = 1.17\ \mu$F, and $R_r = 0.1\ \Omega$

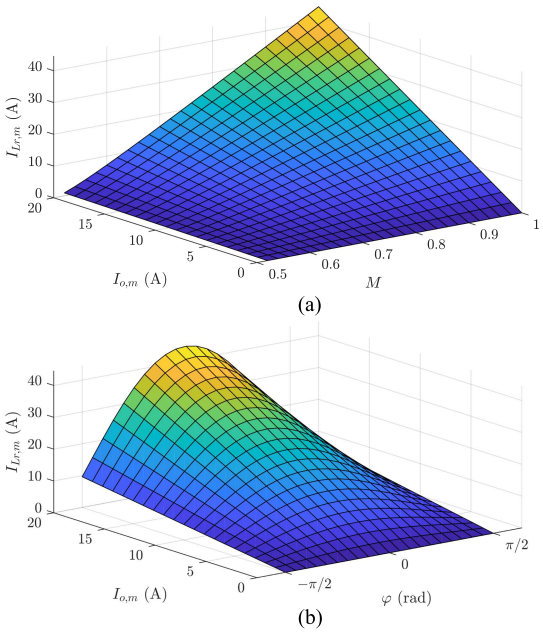

Fig. 5. Peak resonant current $I_{Lr,m}$ as a function of modulation index M and load conditions: (a) dependency on M and $I_{o,m}$ under unity PF operation, revealing worst-case current stress conditions and (b) variation of $I_{Lr,m}$ with M and PF angle φ, confirming that the largest resonant current occurs at unity PF. Results obtained for $C_{\text{FC}} = 470$ μF, $L_r = 4$ μH, $C_r = 1.17$ μF, $R_r = 0.1$ Ω, $f_{\text{sw}} = 75$ kHz, and $V_{\text{dc}} = 400$ V.

with a switching frequency of 75 kHz corresponded to the resonant frequency and a dc link voltage of $V_{\text{dc}} = 400$ V.

As per Fig. 5(a), the dependency of $I_{Lr,m}$, on M, and $I_{o,m}$ at unity PF can be realized. The surface reveals that at full modulation index $M = 1$ and for 15 A peak of load current, the resonant current peaks is 35 A, which corresponds to 2.2–2.4 times the load current amplitude. Fig. 5(b) further expands this analysis by incorporating the load phase angle, φ offering insight into how reactive power conditions affect the resonant tank behavior. As can be understood, when φ increases (i.e., moving away from unity PF), $I_{Lr,m}$ tends to reduce slightly. Therefore, it can be concluded that the worst-case scenario in terms of resonant current stress and $I_{Lr,m}$ occurs at unity PF. This observation supports using unity PF as a conservative design case for sizing the resonant tank.

C. Modulation Strategies

One interesting feature of the proposed Res-SCMLI applied to the 5L-Res-based-ABNPC converter is its flexibility to choose either LS-PWM or PS-PWM strategy. This prominent feature is not possible for the conventional SCMLIs including the 5L-ABNPC converter proposed in [19] and [20], as they need a dedicated carrier to charge/discharge the FC during the middle output voltage level generations. Fig. 6(a) and (b) shows the details of these modulation strategies as for the proposed 5L-Res-based-ABNPC converter, where to generate all the distinctive output voltage levels, two carries either with LS or PS arrangement are required, i.e., C_1, and C_2 in Fig. 6. As can be

TABLE I
PS-PWM PRINCIPLE APPLIED TO THE PROPOSED 5L-RES-BASED-ABNPC

ac Sign	PS-PWM Condition	Res-Charging Condition	v_{inv}
P	$\lvert ac\rvert \geq C_1, C_2$	$D > C_2$	State "E"
	$\lvert ac\rvert \geq C_1, C_2$	$D < C_2$	State "F"
	$C_1\ (C_2) \leq \lvert ac\rvert < C_2\ (C_1)$	$D > C_2$	State "A"
	$C_1\ (C_2) \leq \lvert ac\rvert < C_2\ (C_1)$	$D < C_2$	State "B"
N	$\lvert ac\rvert \geq C_1, C_2$	$D > C_2$	State "K"
	$\lvert ac\rvert \geq C_1, C_2$	$D < C_2$	State "L"
	$C_1\ (C_2) \leq \lvert ac\rvert < C_2\ (C_1)$	$D > C_2$	State "G"
	$C_1\ (C_2) \leq \lvert ac\rvert < C_2\ (C_1)$	$D < C_2$	State "H"
-	$\lvert ac\rvert \leq C_1, C_2$	$D > C_2$	State "C(I)"
	$\lvert ac\rvert \leq C_1, C_2$	$D < C_2$	State "D(J)"

realized, in both types of the modulation, there have been an ac and a dc modulation reference, i.e., ac and D, which are in charge of generating the output voltage levels and charging/discharging operation of the resonant tank, respectively.

Alternatively, the bidirectional devices require both the ac and dc modulation signals as based on the working principle of the proposed 5L-Res-based-ABNPC converter shown in Fig. 2, they are involved in both the charging/discharging path of the resonant tank and the load current. On the contrary, all the four standard FETs located in the H-bridge side of the proposed converter need only an ac modulation reference to transfer the voltage levels to the output. Obviously, S_7, and S_8 are just being ON/OFFfor the positive/negative half cycle of the inverter output voltage, which means their switching losses is negligible.

As can also be deduced from Fig. 6(a) and (b), the 5L output voltage switching frequency of the proposed converter, i.e., the apparent switching frequency, in both the LS- and PS-PWM techniques are equal. However, the effective switching frequency of the devices for the PS-PWM technique is half compared to the LS-PWM one, which can significantly reduce the switching losses for the hard-switched-based devices. Details of the PS-PWM strategy shown in Fig. 6(b) has also been tabulated in Table I.

It is worth noting that, the proposed topology is inherently scalable to three-phase applications, similar to conventional ANPC-based structures. A three-phase implementation would share a common dc-link with a midpoint, and each leg would operate with the same modulation strategy described earlier, using ac references PS by 120°. Each phase would also require an independent resonant tank synchronized to the same resonant frequency, with a dc duty cycle maintained at 50% across all phases to preserve symmetrical soft-charging behavior.

III. DESIGN GUIDELINES

The proper design of the resonant tank elements (L_r, C_r), FC (C_{FC}), and the dc-link capacitors (C_1, C_2) is critical to ensure soft-charging operation, capacitor voltage balancing, and minimal device stresses in the proposed 5L-Res-based-ABNPC converter. This section provides the design methodology based on the operational principles illustrated in Fig. 4 and the analytical relationships derived in Section II.

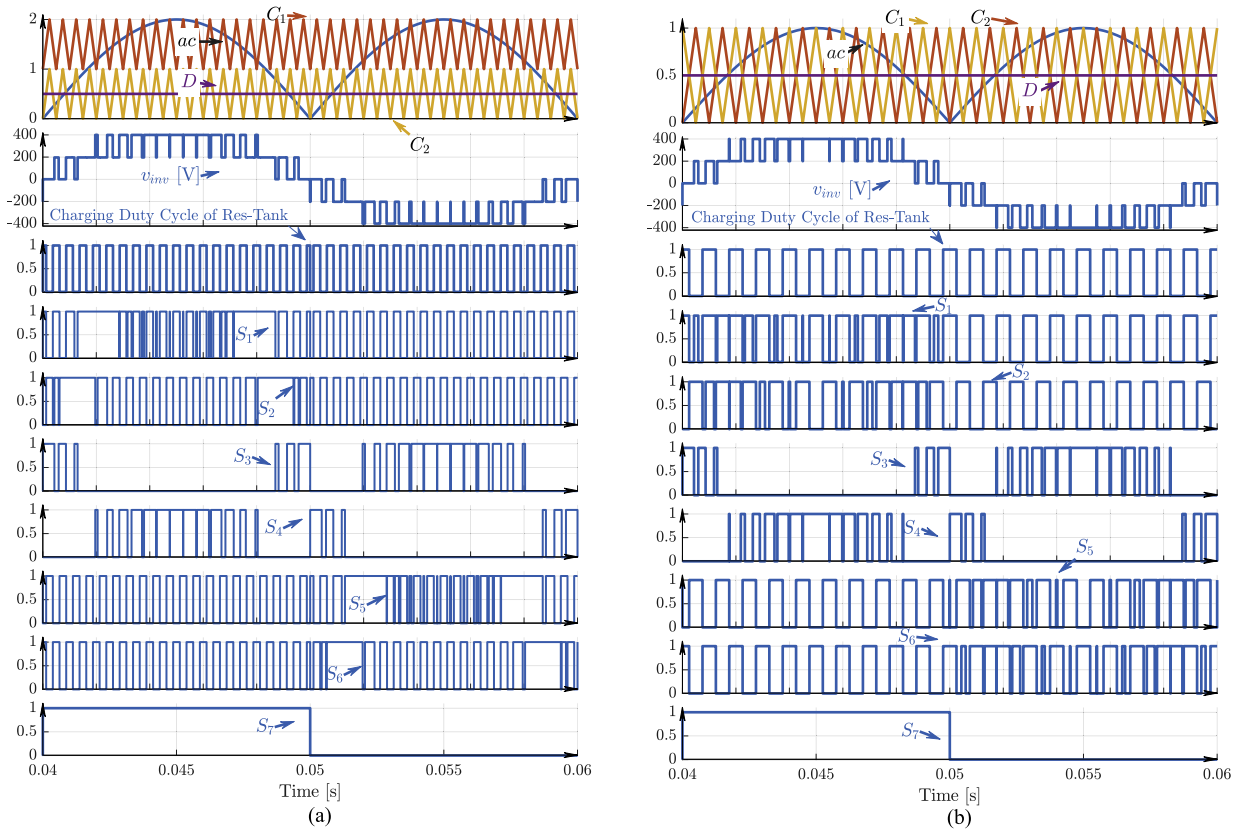

Fig. 6. Modulation strategies applied to 5L-Res-based-ABNPC converter based on (a) LS-PWM and (b) PS-PWM.

A. *Resonant Tank Design*

The resonant tank includes parasitic resistance, R_r, associated with the inductor and switching devices, as well. This resistance leads to a finite quality factor, Q, given by

$$Q = \frac{1}{R_r}\sqrt{\frac{L_r}{C_r}}. \tag{15}$$

The resonant tank must satisfy the following design goals:

1) Achieve a sufficiently high resonant frequency f_{res} to allow fast FC charging within each PWM switching cycle.
2) Maintain a moderate Q to minimize resonant losses and guarantee a symmetric, sharp sinusoidal, i_{Lr}, profile for efficient soft-charging, and soft-switching.
3) Minimize the effect of parasitic resistance, R_r, of the inductor and switching devices.

The resonant tank parameters are then selected to satisfy

$$\omega_{\text{res}} = \frac{1}{\sqrt{L_r C_r}}. \tag{16}$$

Fig. 7 showcases the dependency of $I_{Lr,m}$ versus $I_{o,m}$, and Q at the fixed resonant frequency. A moderate Q value ($Q \approx 2-4$) is targeted by minimizing R_r through appropriate selection of low-resistance inductors and careful PCB layout design. This moderate value of Q ensures the sinusoidal nature of $i_{Lr}(t)$ at each resonant switching event; hence, it can offer soft-switching transitions, i.e., zero voltage switching (ZVS) at turned-ON, and zero current switching (ZCS) at turned-OFF

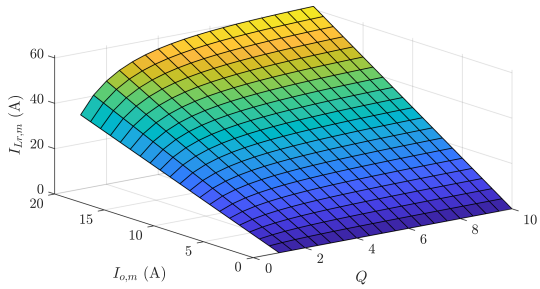

Fig. 7. Dependency of $I_{Lr,m}$ on $I_{o,m}$ and Q of the resonant tank at unity PF, full modulation index, and fixed resonant frequency, i.e., 75 kHz.

for the bidirectional devices that are involved in the charging loop of FC. As earlier discussed, the resonant duty cycle is chosen as $D = 0.5$, corresponding to a half-period charging followed by a half-period discharging. As shown in Fig. 4, this symmetry guarantees zero-crossing of $i_{Lr}(t)$, which is critical to minimize device stress and ensure smooth charge transfer to the FC.

It is worth highlighting that the proposed converter is designed such that the resonant current peak, $I_{Lr,m}$, is larger than the peak load current, $I_{o,m}$, by a factor of 2 or more under full modulation index as shown in Fig. 5. As a result, even at light loads, the resonant tank inductor has sufficient energy to discharge the output capacitance, C_{oss}, of the bidirectional devices, ensuring

ZVS turned-ON. The natural zero-crossing of this current also leads to ZCS turned-OFF, achieving full soft-switching behavior over a wide operating range.

B. FC Design

The FC must be sized to limit the voltage ripple ΔV_{FC} during the operation while supporting the load current contribution at full modulation index. To do so, its total charge value, Q_{FC}, must be equal to the charge transferred by the resonant tank, Q_{res} (see the shaded area in Fig. 4). Hence, we can write

$$C_{\text{FC}}\Delta V_{\text{FC}} = Q_{\text{res}} \tag{17}$$

To calculate Q_{res}, the following relationship can be considered as

$$Q_{\text{res}} = \int_0^{\frac{\pi}{\omega_{\text{d}}}} i_{Lr}(t)dt = \frac{4(V_{\text{dc}} - V_{\text{FC,avg}})}{\pi\omega_{\text{d}}R_r} \tag{18}$$

where $V_{\text{FC,avg}}$ is the average voltage across the FC as shown in Fig. 4. Allocating 5% to 10% ripple for ΔV_{FC} and regarding the analysis compiled in Fig. 5, $I_{Lr,m}$ remains within 2 to 2.5 times larger than $I_{o,m}$. Given $V_{\text{dc}} = 400$ V and a nominal 3 kW single-phase power output, the FC was selected as $C_{\text{FC}} = 470$ μF to satisfy the voltage ripple constraint without excessive capacitance, thereby optimizing size and cost.

C. DC-Link Capacitor Design

The dc-link capacitors C_1 and C_2 are primarily responsible for supplying the intermediate voltage levels ($\pm V_{dc}/2$) to the ac output during the middle states. Their design considerations include the following:

1) Stabilizing the intermediate dc voltage levels against load pulsations and switching actions.
2) Providing sufficient energy storage to absorb current ripples generated by the inverter switching.
3) Avoiding excessive voltage fluctuation at $V_{\text{dc}}/2$ points, especially during fast load transients.

Each dc-link capacitor can be sized based on the allowable voltage ripple ΔV_{dc} at $V_{\text{dc}}/2$ and the worst-case load current swing, typically using

$$C_1 = C_2 = \frac{I_{o,m}}{2\pi f_o \Delta V_{\text{dc}}}. \tag{19}$$

IV. Detailed Performance Evaluation Via PLECS

To further investigate the performance of the proposed 5L-Res-based-ABNPC converter, the detailed simulation results obtained from the PLECS are presented in this Section. The input dc voltage is considered as 400 V, while the resonant tank parameters are chosen to achieve 75 kHz resonant frequency to strike a balance between minimizing the size of passive components.

The FC value was selected as $C_{\text{FC}} = 470$ μF to handle the voltage ripple requirements under rated conditions with $D = 0.5$. The other specification of this simulation is $P = 3$ kW nominal output power in a single-phase configuration at $M = 1$, while its detailed results are shown in Fig. 8(a) and (b) based on PS- and LS-PWM techniques, respectively. As can be seen, all the 5L output voltage levels in both types of modulations with full dc-link utilization factor at the ac output are generated.

TABLE II
Maximum Voltage and Current Stress of Devices

Devices	MVS	MCS	Type of Switching/f_{sw}
S_1, S_2, S_5, S_6	$\pm 0.5V_{dc}$	$I_{Lr,m}$	Soft-Switched @ f_{res}
S_3, S_4	V_{dc}	$I_{o,m}$	Hard-Switched @ f_{sw}
S_7, S_8	V_{dc}	$I_{o,m}$	Hard-Switched @ f_o

Following the resonant network analysis detailed in Section II and shown in Fig. 5, it can be confirmed that $I_{Lr,m}$ is around 35 A. From zoomed-in view of v_{inv}, and i_o, it can also be deduced that the apparent switching frequency of the ac output for the PS-PWM technique is two times larger than the LS-PWM strategy, i.e., 150 versus 75 kHz. This feature is also reflected to the quality of the load current as larger current ripple can be observed in i_o when LS-PWM is to be used. One can further emphasize is the voltage across the FC, v_{FC}, which is oscillating with the double-line frequency, while its average value is around 360 V.

To evaluate the voltage and current stress behavior of the devices involved in the proposed 5L-Res-based-ABNPC converter, Fig. 9(a) and (b) can be taken into account. Here, the 5L output voltage of the inverter, v_{inv}, the load current, i_o, the resonant tank current, i_{Lr} besides the voltage and current stresses of S_1, S_2, and S_3 have been highlighted. Due to symmetry of the proposed topology, the behavior of S_4, S_5, and S_6 also are the same. As S_7, and S_8 are both low frequency devices and their major role is for polarity generation of the ac waveforms, their stresses have not been shown in Fig. 9; however, the MVS and maximum current stress (MCS) of all the devices as well as their type of switching action are summarized in Table II.

As can be observed from Fig. 9(a) and (b), the MVS for the bidirectional devices, S_1, and S_2 is $\pm 0.5\text{V}_{\text{dc}}$, while their MCS is equal to $I_{Lr,m}$. Even though passing such a large resonant current compared to $I_{o,m}$, their switching performance is fully soft as per Fig. 9(b). Due to the moderate value of quality factor chosen for the resonant tank that is greater than one, they have an intrinsic ZVS during the turned-ON process, while due to the zero-crossing of i_{Lr}, their switching transition possesses a ZCS action during the turned-OFF, as well. This creates a unique feature for the proposed Res-SCMLI as the FC charging process is not only fully soft in terms of current stress, but also the devices involved in the charging loop of the FC possess a fully soft-switched performance as well. Obviously, the normal FETs, i.e., S_3, and S_4 are still hard-switched as the low frequency load current is passing through them.

To demonstrate the three-phase scalability of the proposed Res-based SCMLI, Fig. 10(a) shows the steady-state per phase 5L output voltage, load current, resonant tank current, and the FC voltage waveforms under balanced conditions at 10 kW output power and $V_{\text{dc}} = 400$ V. As seen, each phase operates independently without any inrush or transient distortion, thanks to the resonant tank in each leg being driven at the fixed switching frequency with a 50% duty cycle. The ac modulation reference of each phase follows a three-phase sinusoidal profile with 120° phase shift, applied through PS-PWM technique earlier

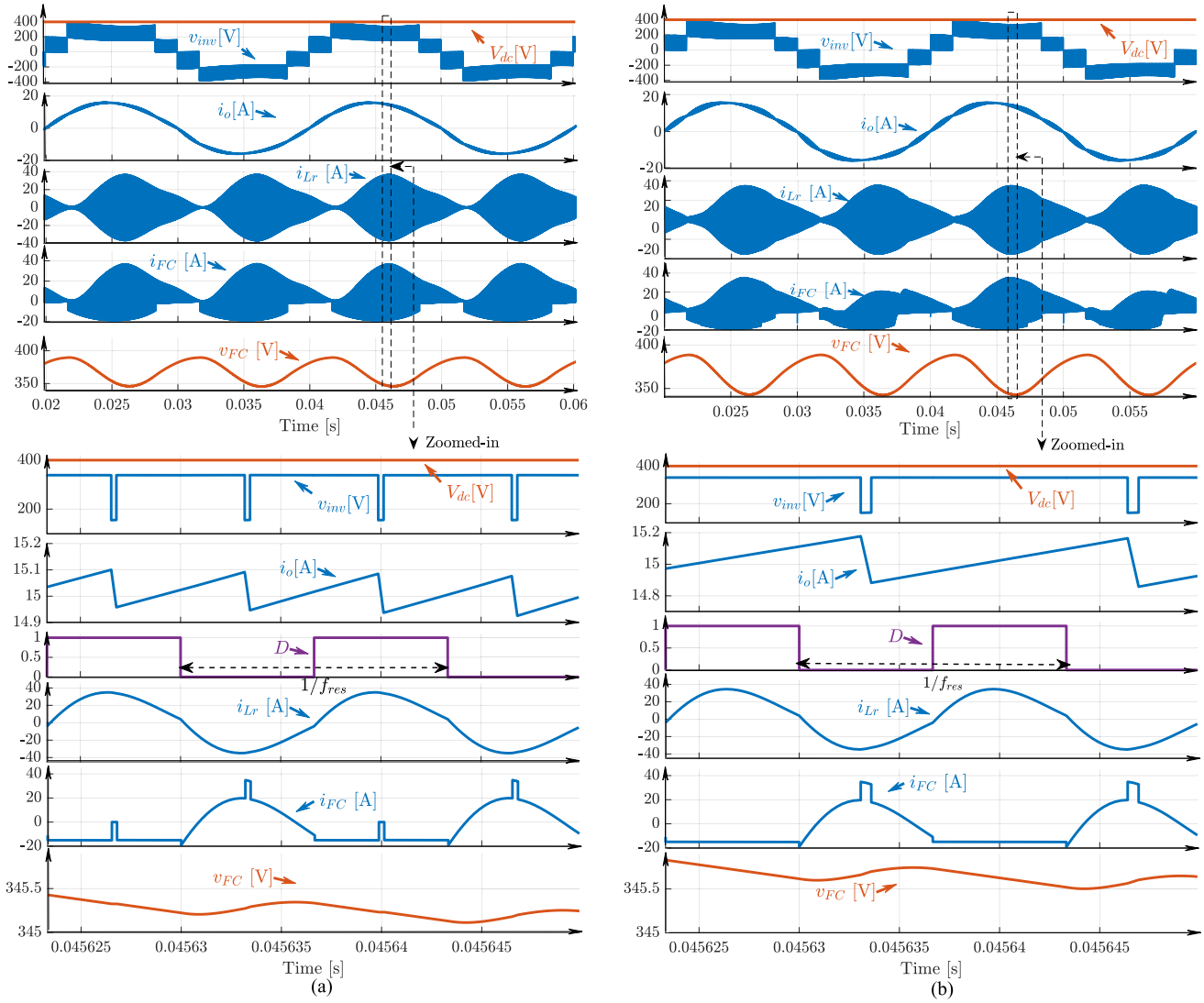

Fig. 8. PLECS results of the proposed Res-SCMLI showing from the top: the input DC voltage, the 5L inverter output voltage, the load current, the resonant tank current, the current passing through the FC and the voltage across the FC at 3 kW power, full modulation index, $f_{sw} = f_{res} = 75$ kHz and $V_{dc} = 400$ V, with (a) PS-PWM and (b) LS-PWM strategies.

discussed. Importantly, $I_{Lr,m}$ in each phase reaches approximately 2.2 times the corresponding $I_{o,m}$, which confirms that the resonant path carries sufficient energy to support FC charging without stress or imbalance.

Fig. 10(b) highlights the case where the load current in phase-a is unbalanced with respect to phases b and c. The results confirm that the operation of each phase remains unaffected, as the working principle is dictated locally by its own resonant tank. This modular architecture ensures that even under unbalanced loading, each phase maintains stable FC voltage with minimal ripple and no cross-phase interference. This validates the robustness and scalability of the proposed converter in realistic three-phase environments.

V. Comparative Study With State-of-the-Art Topologies

As per the comparative study, two following sections have been provided to showcase the main features of the proposed 5L-Res-based-ABNPC converter in respect to its major counterparts from qualitative, quantitative, and numerical modeling point of view. The compared topologies belong to both original FC-based MLIs family as well as conventional ABNPCs.

A. Quantitative, and Qualitative Comparison

As per Table III, the terms of "S," "D," "C," and "G," respectively, denote for the number of required active devices, diodes, capacitors, and gate drivers. Moreover, TSV index refers to the total standing voltage of active devices.

Unlike conventional SCMLIs or FC-based converters where inrush current and hard switching severely limit high-frequency and high-power operations, the proposed topology achieves ZVS during turn-ON and ZCS action during turn-OFFfor the bidirectional devices. This feature enables a drastic reduction in switching losses and EMI propagation, making the proposed

TABLE III
COMPARISON BETWEEN THE PROPOSED 5L-RES-BASED-ABNPC AND SOME OTHER 5L ANPC/ABNPC INVERTERS/CONVERTERS

Type of Converter	No. of Components				Output Gain	MVS/V_{dc} TSV/V_{dc}	FC Balancing Method	Bidirectional?/ MVS on FCs	Modulation Strategy	Efficiency (%)	Inrush Current @M=1?/ Soft-Switching?
	S	D	C	G							
ANPC [8]	8	0	3	8	0.5	0.5/3	FC-based	Yes/0.25V_{dc}	PS and LS	99@1kW	No Inrush/No
ANPC [9]	6	2	3	6	0.5	0.75/3.5	FC-based	No/0.25V_{dc}	PS and LS	NA@1kW	No Inrush/No
Type I-DM-ANPC [13]	10	0	3	6	0.5(1)	0.75(1)/5(6)	FC(SC)-based	Yes/V_{dc}	PS(FC) and LS(SC)	98.3@2.2kW	Very Large in SC/No
Type II-DM-ANPC [13]	10	0	3	8	0.5(1)	0.5(1)/5(6)	FC(SC)-based	Yes/V_{dc}	PS(FC) and LS(SC)	98.5@1.6kW	Very Large in SC/No
Type III-DM-ANPC [13]	10	0	4	7	0.5(1)	0.5(1)/5.5(6.5)	SC-based	Yes/0.5V_{dc}	Only LS	97.9@1.6kW	Very Large/No
ABNPC [18], [19]	6	2	3	6	1	1/5	SC-based	No/V_{dc}	Only LS	97.8@1.5kW	Very Large/No
ABNPC [20]	8	0	3	8	1	1/5	SC-based	Yes/V_{dc}	Only LS	98.3@3kW	Very Large/No
ABNPC [21]	6	2	4	5	0.5	0.5/5	SC-based	Yes/0.25V_{dc}	Only LS	97@1.2kW	Very Large/No
ABNPC [22]	10	0	4	9	1	1/5.5	SC-based	Yes/0.5V_{dc}	Only LS	NA@300W	Very Large/No
Proposed Res-Based ABNPC	12(8)	0	3	8(12)	1	1/6	Res-based	Yes/V_{dc}	PS and LS	98.2@3kW *	No/Both ZVS and ZCS

* Based on PLECS model at the maximum modulation index. The measured efficiency at the rated power is around 97.5%.

TABLE IV
QUALITATIVE COMPARISON BETWEEN FC-BASED MLIS, AND THE PROPOSED RES-BASED SCMLI

Feature	FC-Based MLIs, i.e., [6], [8], [11], [12]	Proposed Res-based SCMLI
Output Voltage Gain	Limited (typically less than 0.5–1); input must be greater than 800V for 230V rms output.	Unity gain with 400V input; supports full DC-link utilization at AC output.
FC Balancing	Needs RSSs and complex sensor-based balancing loops. FC value can be relatively small compared to ABNPCs.	Naturally balanced; no sensors required; FC value can be smaller than ABNPCs but larger than ANPCs.
Component Count	Usually driven with standard FETs and MLCCs. SMC-based MLIs need still bidirectional devices.	Requires low MVS rating bidirectional devices. Both MLCCs and film capacitors can be used as the FC.
Control and Modulation Strategy	Requires active DC-link control; both LS-and PS-PWM are feasible.	No need to control DC-link; supports both LS- and PS-PWM due to symmetric design and resonant tank.
Device Stresses	Fraction of load current is passing through the devices with low MVS.	Significant MCS reduction in comparison to conventional SCMLIs, i.e., MCS ≈2–2.5×load current.
Soft-Switched Capability	All of them are hard-switched; Induces high switching loss and EMI at high switching frequency.	Intrinsic soft-charging and soft-switching (ZVS/ZCS) for all resonant path devices.
Power Density	Very high in case of using MLCCs and GaN-TOLT devices but at the cost of low reliability.	2.14 kW/L (prototype) with air-cooled system; higher with GaN or TOLT devices.
Efficiency	Typically very high as they are buck-based topologies, i.e., RMS current passing through the devices is minimal.	98.2% peak; greater than 97% across full load range at full modulation index.

converter highly suitable for WBG devices, especially at large power ratings.

Another unique advantage is the elimination of inrush current during full load operation ($M = 1$). Conventional SCMLIs such as standard ABNPC structures suffer from very large current spikes at high modulation indices, often requiring larger capacitors and resulting in poor efficiency. In contrast, the proposed Res-based SCMLI exhibits no inrush current even at maximum modulation index, thanks to the soft-charging profile of the FC offered by the resonant tank. Ability to be modulated using any of standard modulations, i.e., LS- or PS-PWM is also a unique feature of the proposed converter as no existing SCMLIs offer this interesting feature.

From a hardware realization perspective, a tradeoff exists between device count and gate driver complexity depending on the choice of bidirectional switch implementation. If MBS devices are utilized for the four-quadrant switches, only eight power devices are needed but 12 isolated gate drivers are required. Conversely, using discrete FETs to build the bidirectional switches requires 12 devices but only eight gate drivers.

As summarized in Table IV, the proposed Res-based SCMLI topology addresses several key limitations of existing FC-based MLIs such as those presented in [6], [8], [11], and [12], as well. While FC-MLIs inherently suffer from limited voltage gain and require high input voltages for standard 230 V rms output, the proposed topology achieves unity gain with only 400 V input, making it more suitable for low-voltage dc sources such as PV or battery systems. The proposed resonant-based structure naturally ensures FC voltage balancing without the need for redundant states, sensors, or closed-loop balancing control, which are often required in FC-based inverters.

Although FC-based MLIs can achieve very high power densities, they typically rely on ultra-compact layouts using multilayer ceramic capacitors (MLCCs), GaN TOLT devices, and aggressive thermal management. This comes at the cost of increased system complexity, as active capacitor voltage balancing with sensors and feedback loops is essential to maintain stable operation. In contrast, the proposed Res-based SCMLI prototype, given in next Section, delivers a power density of 2.14 kW/L using an air-cooled, rack-mounted layout. Even though the current density is moderate, with future integration of GaN-based bidirectional devices, TOLT packaging, and cold-plate cooling, it is expected to scale well beyond 3 kW/L while retaining the converter robustness, efficiency, and EMI-friendly characteristics.

B. Numerical Comparison Via PLECS

In order to numerically evaluate the operation performance of conventional 5L-ANPC, and 5L-ABNPC converters, a standard

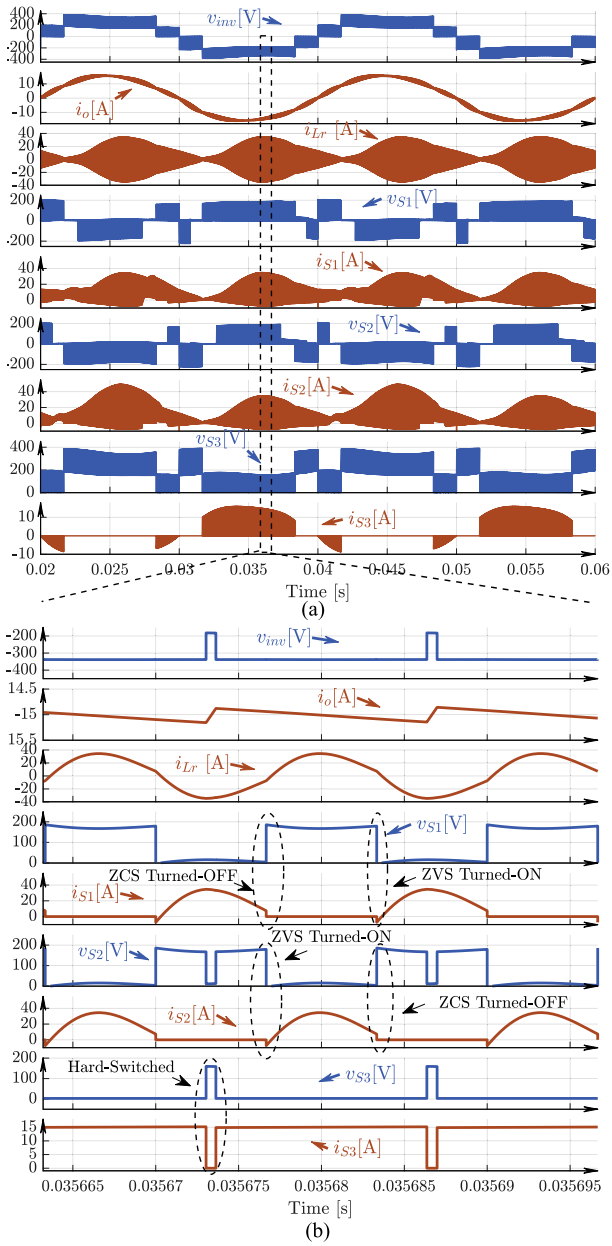

Fig. 9. Standard PLECS results at 3 kW output power, full modulation index with $V_{dc} = 400$ and LS-PWM technique showing (a) voltage and current stress profiles of S_1, S_2, and S_3 of the proposed 5L-Res-based-ABNPC and (b) its zoomed-in view emphasizing on soft-switched performance of S_1, and S_2, and hard-switched action of S_3 at peak charging current area.

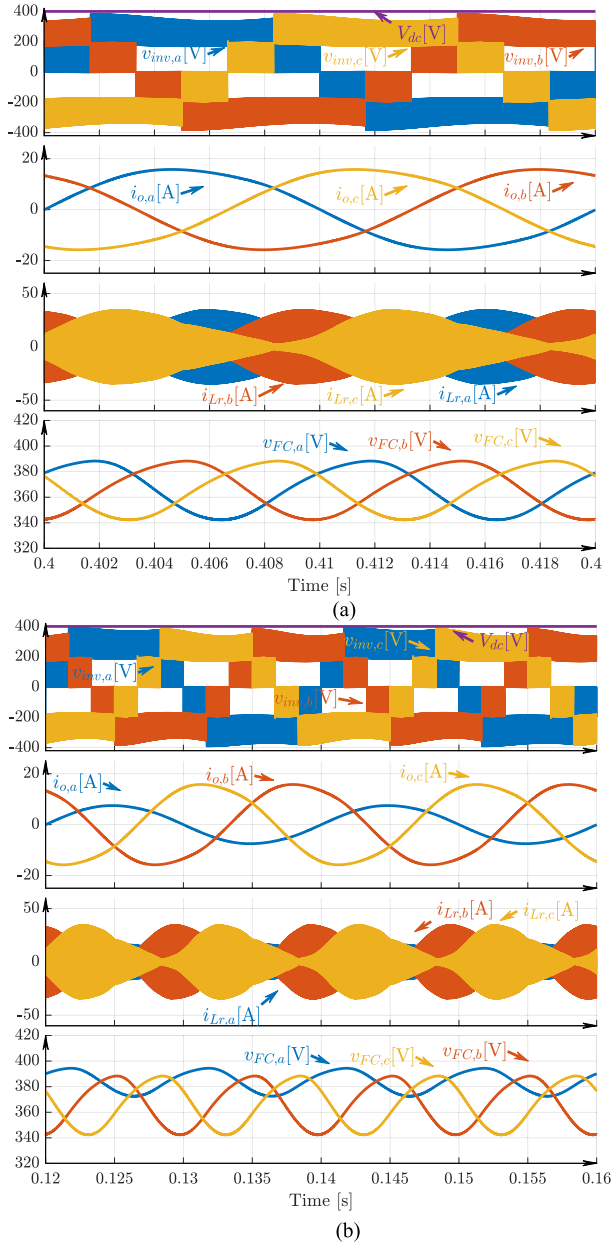

Fig. 10. Standard PLECS results for the three-phase extension of the proposed 5L-Res-based-ABNPC converter at full modulation index with $V_{\rm dc}$ =400 and PS-PWM technique for a system with (a) 10 kW balanced load and (b) unbalanced load when the phase b and c are injecting 3 kW per each and the power of phase a is set at 1.5 kW.

PLECS model is developed at the same power level (3 kW), and at the same switching frequency, 75 kHz for each and their detailed simulation results with the main circuit topology are shown in Fig. 11(a), and (b).

Owing to half voltage conversion gain provided by conventional 5L-ANPC-based converters, 800 V input dc voltage is considered to feed a 230 V rms grid/load voltage [6], [8]. On the contrary, 5L-ABNPC converter follows the SC-based charge balancing process with a unity voltage conversion gain. Hence, its input dc voltage is considered as 400 V to feed the same grid/load voltage. In both cases, a full modulation index is taken into account. As has also been known, the conventional 5L-ANPC converter requires eight standard FETs, in which the MVS value for S_1, S_2, S_3, and S_4 is equal to $V_{\rm dc}$ (considering $2V_{\rm dc}$ as the input dc voltage), while as for the rest, their MVS is $0.5V_{\rm dc}$. On the other hand, S_1, and S_4 are both bidirectional/four-quadrant device in 5L-ABNPC-based structure given in [18] and [19] with an MVS equals to the input dc voltage, $V_{\rm dc}$, while the rest of devices are standard FETs. Its counterpart presented in [20] needs also eight devices but all based on the standard FETs, with the same SC-based charging process.

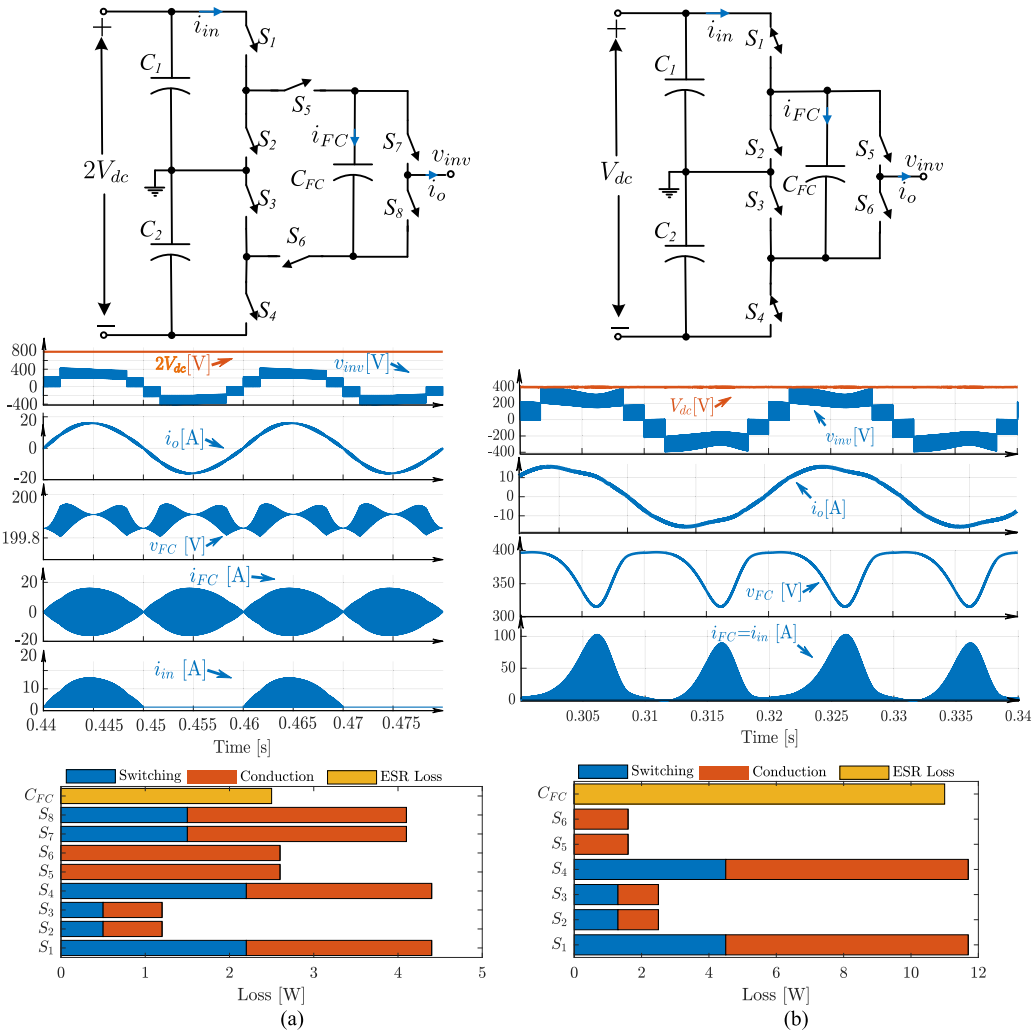

Fig. 11. Performance evaluation of conventional FC- and SC-based topologies based on PLECS at 3 kW power, full modulation index with 75 kHz effective switching frequency in (a) 5L-ANPC structure [7] with a PS-PWM technique and 800 V input DC voltage and (b) 5L-ABNPC structure [18], [19] with a LS-PWM technique and 400 V input DC voltage.

As can be seen from Fig. 11(a), the FC voltage for 5L-ANPC converter is balanced at around 200 V, i.e., one-quarter of the input dc voltage, while its passing through current is the switching current of the ac load, with maximum 15 A. Here, dc link-capacitors, C_1 and C_2 are in charge of the top output voltage level generation, i.e.,$\pm 0.5\mathrm{V_{dc}}$, and they need an active voltage balancing described in details in [13]. FC charge balancing in this converter is on the basis of two RSSs used in PS-PWM technique as well, where in a more accurate mode, a closed-loop control system is used to provide better dynamics for the FC [13].

As opposed to this, the SC-based 5L-ABNPC converter does not have any RSSs as the FC is charged only during the middle output voltage levels, i.e., $\pm 0.5\mathrm{V_{dc}}$, with a LS-PWM strategy and, thus, it delivers its charged voltage to the load at top voltage positive and negative levels, $\pm \mathrm{V_{dc}}$. Even though requiring half input dc voltage compared to 5L-ANPC converter, the FC passing though current of 5L-ABNPC converter, i_{FC}, which is equal to the input current, i_{in}, drawn from the input dc supply, possesses a large discontinuous inrush spike and its peak is around 8-time larger than the load current peak at full modulation index.

This excessive current stress induces a large EMI as well, while due to the hard-switched nature of the FC charging path devices, i.e., S_1, and S_4, the overall efficiency is significantly compromised at full power. As has been suggested in [18], and [16], there have been two approaches put forward to alleviate such current stress issue, in which the first one is to apply a larger C_{FC} compared to C_1, and C_2, and the second one is to reduce the maximum modulation index to 0.85 or 0.9. The latter approach becomes more popular as the 5L-ABNPC converter achieves more than 98% overall efficiency at full power according to [13], [19], and [20].

A comparative loss analysis between these two conventional topologies under identical operating conditions (3-kW, full modulation index, 75-kHz switching frequency, and the same SiC devices, i.e., UJ4C075018K4S) has also been conducted in Fig. 11(a), and (b). The gate resistances to control the dv/dt of devices are chosen as per the data sheet of the SiC-FETs. As

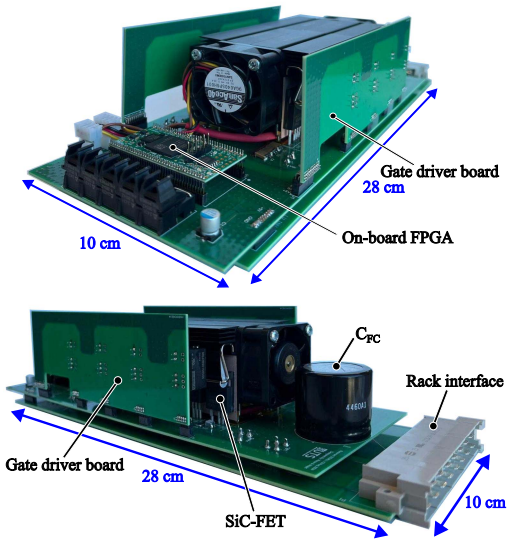

Fig. 12. 3 kW single-phase prototype of the proposed 5L-Res-based-ABNPC converter with SiC-FETs technology and an on-board FPGA, while the MLCCs and L_r of the resonant branch are placed at the bottom side of the power board.

per these, both converters exhibit hard-switched behavior, with no soft-charging mechanism in their FC paths. This causes a significant switching loss for the SC loop devices in ABNPCs, but due to lower range of current stress for ANPC, the switching losses still are in an acceptable range. In both cases, 470μF electrolyte capacitors were selected for the FC to ensure a fair basis for comparison. As seen in Fig. 11(b), this value proves insufficient for the ABNPC under full-load conditions, resulting in a large FC voltage ripple and distortion in the ac load current waveform, indicating that the FC cannot fully support the top-level voltage states. This is a direct consequence of the hard-charging action, which causes severe inrush currents. In contrast, the 5L-ANPC topology shown in Fig. 11(a) maintains a cleaner current waveform due to its more stable FC behavior. Despite lacking any voltage boosting capability, the ANPC achieves very high efficiency, mainly due to its minimal conduction losses and relatively simple switching operation.

In summary, compared to existing 5L inverters, the proposed 5L-Res-based-ABNPC converter uniquely combines high efficiency, soft-switching operation, no inrush current at full modulation, full dc-link utilization, bidirectional operation, and practical implementation flexibility, establishing itself as a strong candidate for next-generation high-frequency, high-density power electronics systems.

VI. Experimental Results

To validate the performance of the proposed 5L-Res-based-ABNPC converter, a 3 kW/110 kHz laboratory-built prototype using discrete SiC-FETs and on-board FPGA is developed as shown in Fig. 12. The designed converter consists of two same gate-driver boards placed into two sides of the power board with a 2.14 kW/L power density. Each of the gate driver boards can drive four SiC-FETs, i.e., S_1, S_2, S_3, and S_7, and S_5, S_6, S_4, and S_8. The current design of the proposed 5L-Res-based-ABNPC converter has followed the industrial rack mounted standard dimension with a careful layout consideration. Conducted EMI in the low-frequency range of 9–150 kHz is becoming a critical concern for grid-connected power converters due to recently introduced standards such as CISPR 11 and BDEW recommendations [30]. Hence, EMI and thermal considerations were prioritized in the hardware layout. The resonant tank loop was tightly routed and locally shielded to minimize parasitic inductance and radiated noise. High-frequency MLCCs were placed near critical switching nodes, and isolated gate drivers were used with short signal paths to limit common-mode noise coupling. Due to the soft-switching nature of the resonant charging path, high-frequency EMI is inherently reduced compared to hard-switched SCMLIs. However, as the resonant frequency (110 kHz) falls within the regulated band, careful design of the input EMI filter and damping networks is still essential to suppress narrowband EMI tones [30].

TABLE V
Main Parameters Used for the Experimental Prototype

Element	Type and Description
Switching Frequency/Rated Power	110 kHz/ 3 kW
SiC-FETs	750 V/UJ4C075018K4S
MLCCs for Res-Tank	5×470nF/2220Y1K00474KXRWS2
MLCCs as HF DC-Link	220nF/GRM55DR7LW224KW01L
Microprocessor	DSP-TMS320F28379D
On-board FPGA	TE0890-02-P1C-5-A
C_{FC}	470uF/450V/LGL2W471MELC35
L_r for Res-Tank	2uH/40A/SER2011-202MLD
Gate Drivers	UCC21520
Isolated dc/dc ICs	MGJ2D121505SC

Thermal design followed a forced air-cooled strategy using a finned aluminum heat sink, with thermal vias and copper pours added beneath high-loss devices. Measured case temperatures remained within safe limits at full load, confirming effective thermal management under rated conditions. The resonant tank parameters are also chosen to ensure 110 kHz resonant frequency with a moderate value of Q as per Fig. 7, while the details of components used in the prototype are tabulated in Table V. The selection of L_r is based on the expected $I_{Lr,m}$ at full power in terms of its maximum saturation current. LS-PWM strategy is selected as for the modulation strategy, as well. Considering the above specifications, the experimental results are presented in following sections addressing the performance of the proposed 5L-Res-based-ABNPC converter in both open- and closed-loop grid-connected conditions.

A. Open-Loop Results

The steady-state experimental results of the proposed 5L-Res-based-ABNPC converter, when a resistive load at open-loop condition is exploited, are shown in Fig. 13(a), and (b), while 400 V input dc voltage is applied to the converter. As per Fig. 13(a), 3 kW power is injected to a single-phase load at $M = 0.95$, while all the expected output voltage levels of the converter are clearly generated with full dc-link voltage utilization at the ac output. The peak of ac load current is around 15 A, the voltage across the dc-link capacitors is perfectly balanced at 200 V without

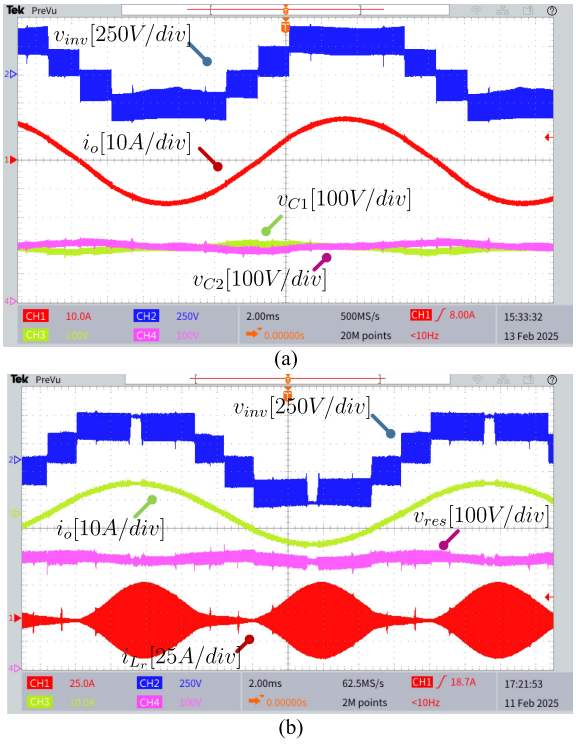

Fig. 13. Experimental results of the proposed 5L-Res-based-ABNPC converter at the steady-state condition showing, (a) 5L output voltage, the load current and the balanced voltage across the DC-link capacitors at 3 kW output power and $M = 0.95$ and (b) emphasizing on the resonant tank current at 2.8kW power with full modulation index, and the voltage across the resonant tank.

exploiting any external sensors. The same experimental results at full modulation index and 2.8 kW power have also been shown in Fig. 13(b) emphasizing on 400 V balanced voltage across the resonant tank, and the current passing through it. As can be seen, with almost 15 A peak of the load current, $I_{Lr,m}$ is around 32 A confirming the analysis given in Fig. 5. This is the breakthrough feature of the proposed topology, as it operates within a full modulation index, while the MCS of the bidirectional devices and resonant tank is slightly greater than two times the peak load current.

In following, the performance of the proposed converter is verified through the experiment under a step change in the load power, i.e., from 1.3 to 2.3 kW at $M = 0.95$, and under a sudden change in M from 0.75 to 1. Details of these results are demonstrated in Fig. 14(a)–(d), respectively. The zoomed-in view of these results showing the peak current passing through the resonant tank can again confirm the soft-charging operation of the FC at the rated voltage and high power.

In order to show the voltage stress of devices, Fig. 15(a) and (b) can be considered, where the bidirectional devices, S_1, and S_2 are blocking $\pm$ 200 V at 400 V input dc voltage. On the other hand, the normal FETs, S_3, and S_7, are blocking 400 V stress voltage at high and low switching frequency, respectively. As per the symmetry of the proposed converter, the stress voltage of other involved four devices has not been shown. Fig. 16(a) and (b) also demonstrated the voltage and current stresses of S_1, and

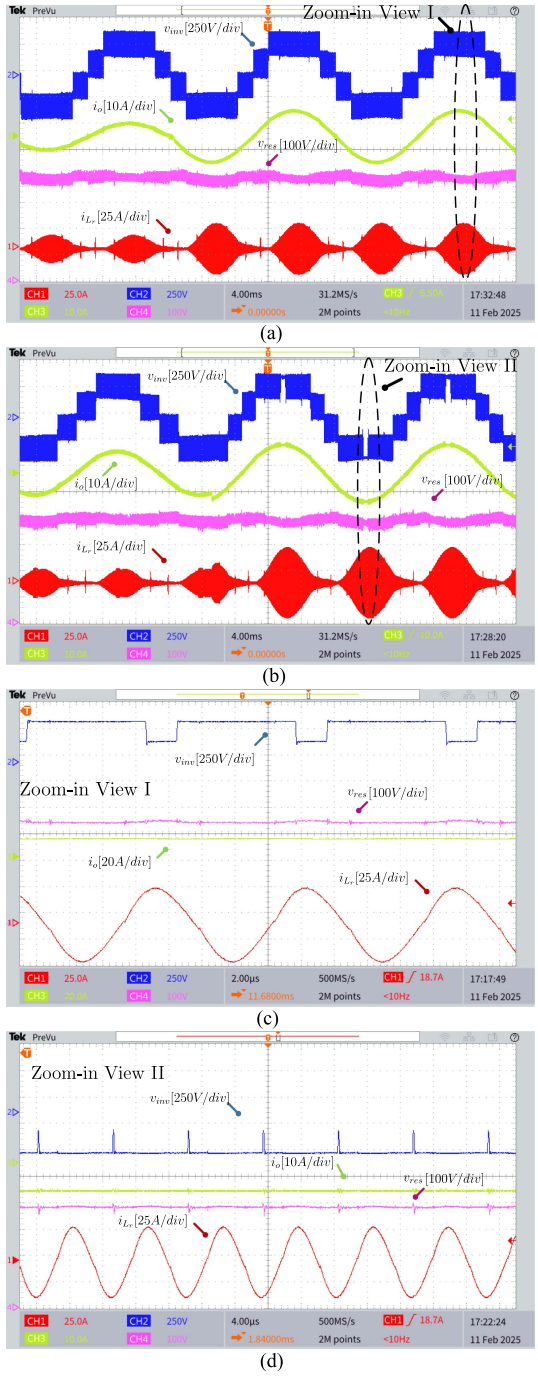

Fig. 14. Experimental results of the proposed 5L-Res-based-ABNPC converter at transient in maximum modulation index and load step-change showing 5L output voltage, the load current, the resonant tank voltage, and the current passing through the resonant tank, when (a) M is fixed at 0.9 and the power is changed from 1.2 to 2.3 kW, (b) M is changed from 0.75 to 1 at constant load, (c) zoomed-in-view of the results under the load change at 2.3 kW power, and (d) zoomed-in view of the results at 2.8 kW and $M = 1$.

S_2 in presence of the 5L output voltage of the proposed converter and the load current at full modulation index and 2.8 kW power. In this case, a 30 MHz N7041A Rogowski ac current probe is used to capture the bidirectional devices current, where due to the soft-charging operation, their MCS is roughly higher than

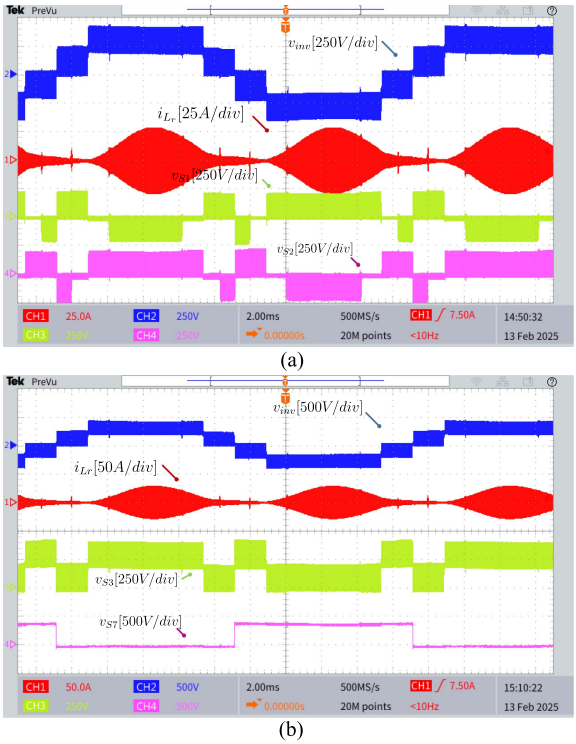

Fig. 15. Experimental results of the proposed 5L-Res-based-ABNPC converter showing the 5L inverter output voltage, and the resonant tank current at $M = 0.95$ with (a) stress voltage across S_1, and S_2 and (b) stress voltage across S_3, and S_7.

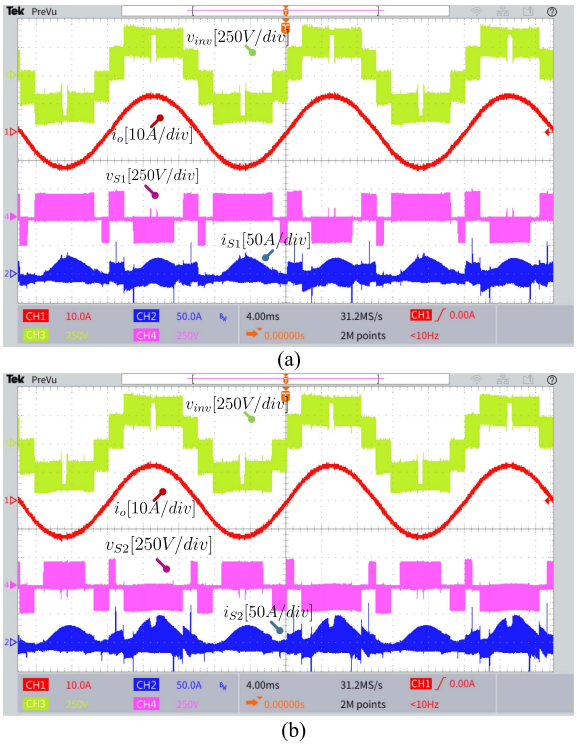

Fig. 16. Experimental results of the proposed 5L-Res-based-ABNPC converter showing the 5L inverter output voltage, and the load current at 2.8 kW power and full modulation index with (a) stress voltage across S_1, and current stress of S_1 and (b) stress voltage across S_2, and current stress of S_2.

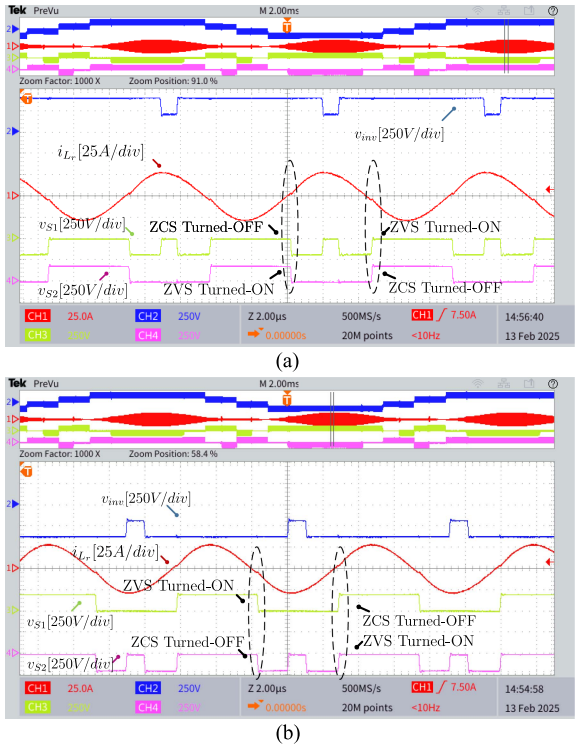

Fig. 17. Experimental results of the proposed 5L-Res-based-ABNPC converter emphasizing on soft-switched performance of bidirectional devices with $M = 0.95$ at (a) positive half cycle of the 5L inverter output voltage and (b) negative half cycle of the 5L inverter output voltage.

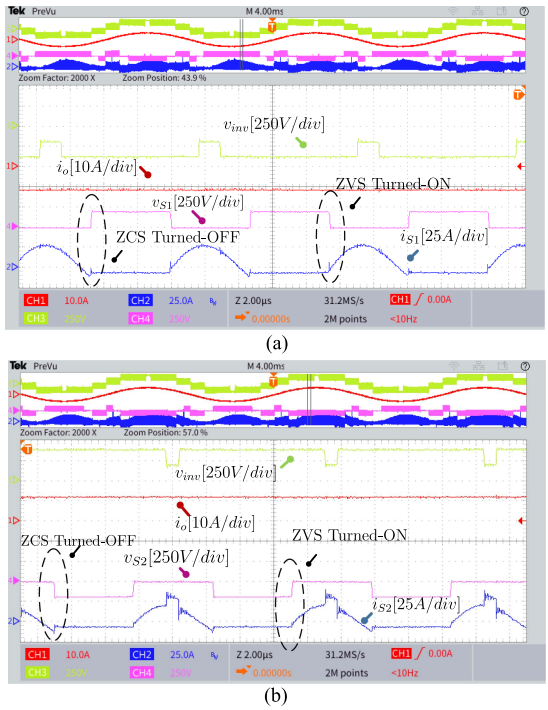

Fig. 18. Experimental results of the proposed 5L-Res-based-ABNPC converter at full modulation index ($M = 1$) and 2.8 kW power emphasizing on soft-switched performance of bidirectional devices (a) S_1 stress at negative half cycle of the 5L inverter output voltage and (b) S_2 stress at positive half cycle of the 5L inverter output voltage.

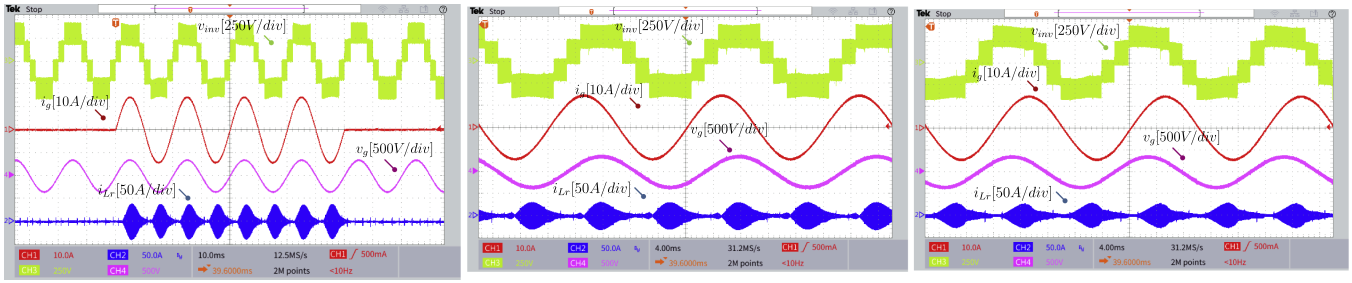

Fig. 19. Experimental grid-connected operation showing (a) the results with a dynamic change of the injected active power at unity PF from zero to full power, and vice versa, (b) steady-state reactive power support result at full apparent power with a leading PF, and (c) steady-state reactive power support result at full apparent power with a lagging PF.

32A without inducing any aggressive spikes. These results can confirm the MCS and MVS analysis given in Table II.

In order to highlight the soft-switching feature of these bidirectional devices, Fig. 17(a) and (b) can be taken into account. Thanks to the sinusoidal nature of the resonant tank current with a moderate Q leading to a perfect zero crossing, all bidirectional devices take ZVS turned-ON and ZCS turned-OFF feature at the same time, which can remarkably increase the overall efficiency of the converter with a reduced EMI propagation issue. The zoomed-in view of the voltage and current stresses for bidirectional devices, S_1, and S_2, in presence of the 5L output voltage and the load current at full modulation index and 2.8 kW power can also be seen in Fig. 18(a) and (b). The results are highlighted when the inverter is generating its top positive and top negative output voltage levels. As per 14 A of the load peak current, the MCS of the devices is roughly around 30 A with a proper zero crossing ensuring the soft-switched performance of the bidirectional devices both in turned-ON and turned-OFFinstances.

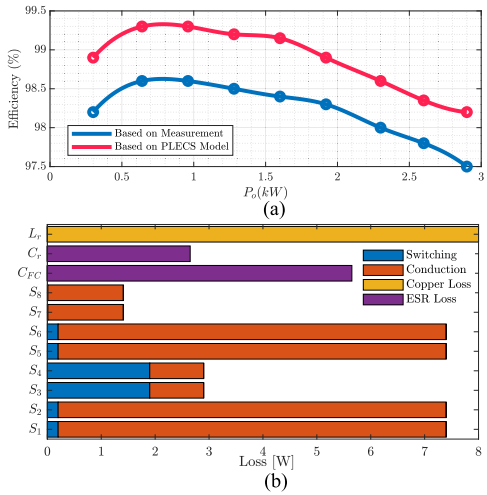

Fig. 20. (a) Efficiency results of the proposed 5L-Res-based-ABNPC converter at full modulation index based on PLECS and experiment and (b) loss breakdown results of the involved components at the rated power, full modulation index, and based on PLECS model.

B. Closed-Loop Grid-Connected Results

As per the grid-connected results, the proposed 5L-Res-based-ABNPC converter is connected directly to a 50 Hz grid emulating by Regatron TC30.528.43 via an interface L -type filter. The input dc voltage is provided by a Elektro-Automatik PV emulator (model EA-PSI-9750-12). The grid peak voltage is considered 340 V, while the input dc voltage is set at 400 V. This results in a maximum modulation index, M equals to 0.85, and hence for 15 A peak of the injected grid current, the maximum injected active power would be around 2.6 kW. AMC3330 and AMC3301 ICs as the precision, isolated amplifier with a fully integrated isolated dc–dc converter are used as per the grid voltage, v_g, and the injected grid current, i_g, sensors, respectively. The same grid voltage observer technique with a proportional resonant controller explained in details in [13] is used with a DSP to generate the reference current, while the adjusted sampling time is based on 110 kHz resonant frequency of the proposed converter.

Under the above assumptions, stable grid-connected operation of the proposed 5L-Res-based-ABNPC converter at unity PF within a dynamic result, i.e., zero to full power and vice versa, can be confirmed in Fig. 19(a). The result showcases the 5L inverter output voltage, v_{inv}, the injected grid current, i_g, the grid voltage, v_g, and the resonant tank current, i_{Lr}, where $I_{Lr,m}$ is around 30 A. Concerning, $M = 0.85$, and 15 A peak of the grid current, $I_{o,g}$, this value of $I_{Lr,m}$ can again confirm the analysis presented in Fig. 5. Within the same amount of $I_{o,g}$, Fig. 19(b), and (c) shows the successful reactive power support operation of the proposed converter within leading and lagging PF, respectively. As can be seen, $I_{Lr,m}$ in nonunity PF shows a smaller value, i.e., roughly around 25A, in comparison to unity PF operation confirming again the analysis developed in Section II and illustrated in Fig. 5(b).

C. Loss and Efficiency Analysis Based on PLECS and Experiment

Considering Fig. 20(a), the efficient performance of the proposed 5L-Res-based-ABNPC converter at full modulation index over a wide range of output power can also be confirmed. Notably, due to soft-charging and soft-switching nature of high frequency devices, i.e., bidirectional devices, the overall

efficiency of the proposed topology confirming by both PLECS and measurement is more than 97.6%. Concerning the reasonable value of the passive components, reaching this amount of efficiency through conventional SCMLIs at full modulation index is not attainable owing to large current stress and significant voltage drop across the FC. The loss breakdown details of the involved components based on $R_{\mathrm{ds,on}}$ of the selected devices, and equivalent series resistance (ESR) of the passive elements have also be shown in Fig. 20(b). These results have been captured by the detailed model of the proposed 5L-Res-based-ABNPC converter in PLECS.

VII. Conclusion

This article introduced a novel class of resonant switched-capacitor multilevel inverters (Res-SCMLIs) by integrating a resonant network into the charging path of the FC. Focusing on the 5L ABNPC topology, the proposed approach successfully addresses key challenges associated with conventional SCMLIs, including large inrush currents, high device stress, and limited modulation flexibility. By employing a carefully designed resonant tank, the proposed converter achieves soft-charging and soft-switching of the involved devices even at full modulation index, significantly reducing current stress and EMI propagation without compromising full dc-link voltage utilization at the ac output. Furthermore, the flexibility to operate under both PS and level-shifted PWM strategies enhances modulation options and system efficiency. The theoretical findings were thoroughly validated through detailed simulations and experimental results from a 3 kW SiC-based prototype, demonstrating superior steady-state and dynamic performance, robust voltage balancing, and excellent stress management with around 98% measured efficiency.

Future work will focus on improving the converter's power density and scalability by replacing the discrete bidirectional switches with monolithic or TOLT-based devices, which offer reduced parasitics and better thermal integration. In addition, realizing the resonant inductor L_r using PCB-based or planar magnetic structures will enable higher saturation currents and more compact construction, supporting higher output power. Decoupling the resonant and switching frequencies is also under consideration, as the H-bridge side devices are hard-switched and not constrained by the resonant tank dynamics allowing optimization of both stages independently for better EMI and efficiency.

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