Pseudo Partial Power Processing Multilevel Modular High Gain Switched Tank Converter for Data Center Intermediate Bus Converter

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***Abstract*—In this article, a pseudopartial power processing (P-PPP) multilevel modular high step-down gain switched tank converter (HGSTC) is proposed for data center application. The proposed HGSTC comprises high step-down gain multilevel modules, a low-voltage-side rectifier, and a nonisolated autotransformer, of which the autotransformer is the key to realize the P-PPP structure. Compared with full power conversion, the topology reduces the processing power by 12.5% . A detailed operation principle analysis of the converter is conducted, including derivation of voltage gain and soft-switching analysis. Furthermore, systematic configuration methods for the topology family are established, along with generalized expressions for voltage gain. The comparison with existing topologies reveals the advantages of the proposed converter. A 6 mm-high planar autotransformer design and optimization methodology is presented for ultrathin intermediate bus converters in data center application. A 1 MHz 46–50 V input 5.75–6.25 V / 84 A output prototype is built for verification. The peak efficiency of the proposed converter reaches 96.03%, and the power density reaches 816 W / in^3.**

***Index Terms*—DC transformer, high step-down gain, multilevel modules, pseudo partial-power-processing, switched tank converter.**

I. Introduction

ARTIFICIAL intelligence and cloud computing have driven the development of high-performance processors such as data center graphics processing units and central processing units. Data center power supplies are facing changes to cope with the increasingly stringent power requirements of these processors. Advanced power supplies can not only reduce energy consumption and operating costs, but also better adapt to the power needs of large data centers [1], [2], [3], [4]. Data centers are beginning to abandon the conventional 12 V bus architecture and adopt a 48 V bus architecture to reduce conduction losses, as shown in Fig. 1, which requires support from high step-down ratio and high-density power solutions. The present challenge is how to achieve efficient energy conversion in a limited space [5], [6]. To overcome the contradiction between high input voltage and high output current in 48 V-1 V point of load power supplies, two-stage design is a promising solution, in which the first stage intermediate bus converter (IBC) is implemented as a dc transformer (DCX) with constant voltage gain, and the second stage implements voltage regulation and fast response. Due to functional separation, each part can be optimized and designed according to its own characteristics. Through reasonable division of labor and collaboration, the complexity of the overall design is reduced and the reliability and flexibility of the system are improved [4], [7], [8].

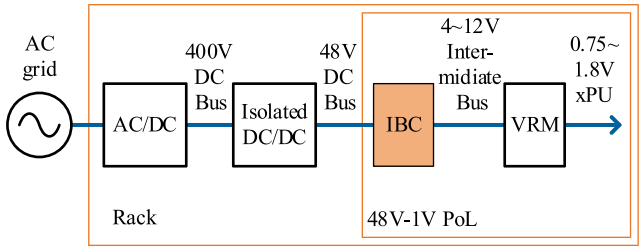

Fig. 1. Data center 48 V bus architecture with intermediate bus.

Transformer-based solutions, especially resonant converters such as *LLC* and SRC, are widely used in IBC. The resonant characteristics make it easy to achieve zero-voltage switching (ZVS) on the primary switches and zero-current switching (ZCS) on the secondary switches. Moreover, the voltage gain of the converter can be easily enhanced by changing the turns ratio of the transformer. The high-turns ratio transformer design and high voltage stress of the switches are the main technical limitations of this type of converters. In addition, the size and power consumption of the transformer need to be compromised. The power consumption of the transformer mainly includes core loss and winding loss. The core loss is negatively correlated with the effective core cross-sectional area, and the winding loss is negatively correlated with the window area of the core. Therefore, the transformer loss can be reduced by increasing the effective cross-sectional area and window area, but this runs counter to the design goal of high power-density.

Switched capacitor converter (SCC) based solutions, as a type of power electronic converter with nonmagnetic or few

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magnetic components, completely or partially eliminate the abovementioned problems introduced by transformers [9], [10]. SCC topologies leverage the strategic combination of switching networks and capacitor arrays to achieve voltage gains as high as several tens of times (including both step-up and step-down operations) while relying exclusively on capacitors and semiconductor switches, thereby demonstrating distinctive advantages in power density. The conventional SCC architecture is characterized by two intrinsic limitations. First, the hard-charging characteristics of capacitors induce abrupt voltage step transitions, subjecting capacitive components to stress levels exceeding the system's power rating. Second, the hard-switching operation of semiconductor devices generates substantial switching losses and electromagnetic interference, collectively restricting their applicability in high-performance power electronic systems.

To address these challenges, the resonant switched capacitor converter has been proposed. Distributed or centralized inductors are used to form an *LC* resonant network with capacitors, enabling switches to achieve ZCS operation and avoid hard charging of the capacitors, thereby significantly reducing switching losses [11]. Building upon these advancements, the flying capacitor multilevel dc–dc converter has demonstrated promising potential in low-voltage applications [12], [13]. By employing multilevel modulation strategies, this architecture constrains switching voltage stress to 1/N of the input voltage (where N denotes the number of voltage levels). However, its nonmodular architecture introduces scalability limitations, while intricate modulation schemes restrict its viability in high-current scenarios. To address structural scalability challenges, the multilevel modular switched capacitor converter (MMSCC) has emerged. This configuration adopts a modular design, and reduces switch voltage stress to 1/M of the system voltage (where M represents the number of modules). Distributed inductors can be integrated into MMSCC to realize ZCS of switches, forming the ZCS-MMSCC topology that enables high-efficiency and high-power-density implementations [14]. Google LLC subsequently developed the switched tank converter (STC) based on ZCS-MMSCC architecture, eliminating nearly half of the inductive components while commercializing this technology in 48 V–12 V power supplies for data centers [15]. Nevertheless, constrained by fundamental charge transfer principles, its voltage gain remains positively correlated with component quantity.

With artificial intelligence accelerator chips now requiring power supply voltages as low as 0.75 V, intermediate bus voltages are transitioning from conventional 12 V to 6 V or lower levels. However, in switched capacitor-based IBCs, increased step-down gain necessitates proportional augmentation of switching components, capacitors, and inductors, resulting in significant degradation of both conversion efficiency and power density. To address the above contradictions and achieve high step-down gain and low component voltage stress, this article proposes a pseudo partial power processing (P-PPP) multilevel modular high step-down gain switched tank converter (HGSTC). The direct connection between the expandable modules and the output transfers partial power directly to the output port without passing through magnetic component or rectifier, making the proposed HGSTC have characteristics similar to PPP and is, therefore, called P-PPP [16], [17], [18].

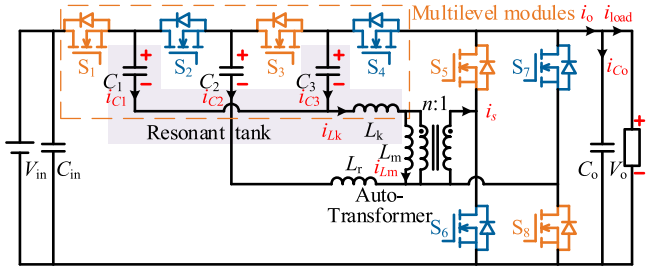

Fig. 2. Schematic of the proposed HGSTC.

The proposed HGSTC not only inherits the merits of SCCs and uses extendable multilevel modules to relieve device voltage pressure, but also inherits the merits of transformer-based converters by employing autotransformer to eliminate the need for exponentially increasing components—a critical limitation of SCCs—to achieve additional step-down gain. Furthermore, compared to conventional transformers with identical conversion ratios, the autotransformer enables a significant reduction in winding count, thereby directly minimizing transformer losses. Moreover, leveraging the P-PPP structure, a portion of the power bypasses the autotransformer and rectifier and flows directly to the output, effectively reducing the power rating required for the autotransformer. The contributions of this article are as follows.

1) A new topology suitable for high step-down voltage gain and high output current is proposed, and the use of autotransformer solves the inherent drawback that SCC needs a large number of devices to achieve high gain.
2) The specialized autotransformer is designed, which can effectively reduce the turns and volume of transformer windings compared with the traditional transformer.
3) The P-PPP structure is employed to reduce the power flowing through the magnetic component, which helps to reduce the design power capacity of autotransformer and improve the efficiency of the converter.

The rest of this article is organized as follows. In Section II, the steady-state working principle and voltage gain of the topology are analyzed in detail, and its topology family is introduced. Section III discusses the detailed design of converter, including ZVS analysis, and detailed magnetic design steps. Section IV is a comparative study of the HGSTC and the state-of-art converters, and the excellent theoretical performance of the proposed converter is revealed. The built prototype of HGSTC and the experimental result are shown in Section V. Finally, Section VI concludes this article.

II. Proposed High Step-Down Gain Switched Tank Converter

A. Proposed Converter

The schematic of the proposed HGSTC with fixed 4nX gain is shown in Fig. 2, where 4nX refers to the input and output voltage ratio of 4n:1. It consists of 4:1 multilevel modules and an n:1 autotransformer. Capacitors C_1 and C_3 form a pair of equally valued split capacitors, which, in conjunction with inductor L_k, constitute a resonant tank. Capacitor C_2 and inductor L_r, constitute a resonant tank. The autotransformer is depicted

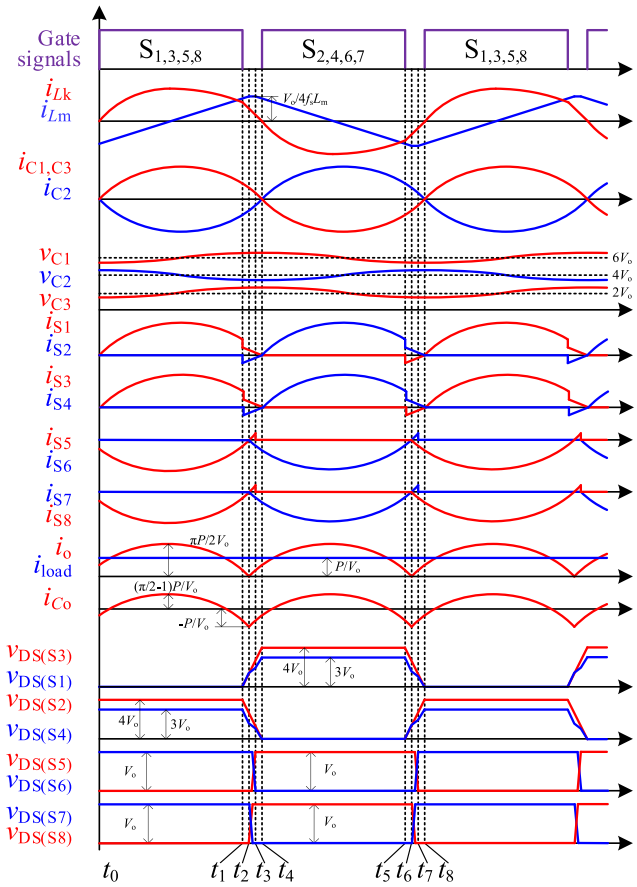

Fig. 3. Key waveforms of the converter in one switching period, $n = 2$.

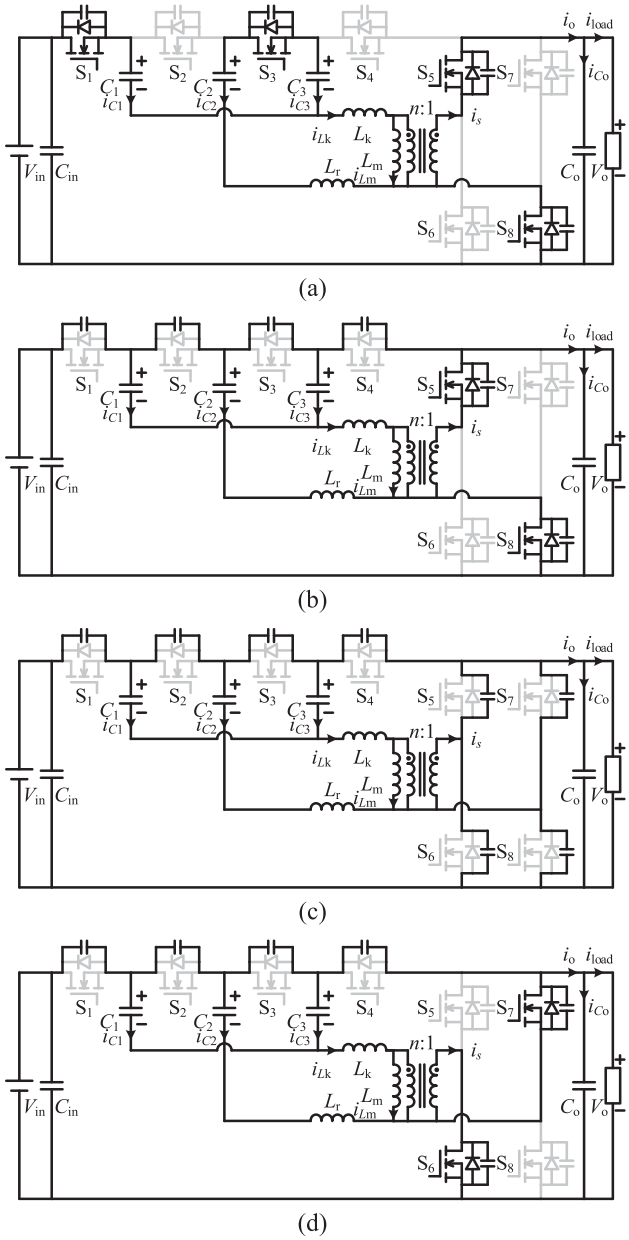

Fig. 4. Simplified equivalent circuits of the proposed converter during half period. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

as an n: 1 transformer with primary leakage inductance L_k, magnetic inductance L_m, and short-circuited windings, where L_k is reused as the resonant inductance. The specific configurations for transformer are discussed in detail in Section III. S_1–S_4 are main switches, while S_5–S_8 are synchronous rectifier switches, with S_7 and S_8 serving as resonant tank circuit switches simultaneously. The positive current direction and voltage polarity are shown in Fig. 2.

Similar to common fixed voltage gain switched capacitor-based converters, all switches use a pair of complementary drive signals with dead time. When S_1, S_3, S_5, and S_8 are ON and the other switches are OFF, the state of the converter is called Phase A; When S_2, S_4, S_6, and S_7 are ON and other switches are OFF, the state of the converter is called Phase B. The resonant frequencies of the three resonant tanks are configured to be equal, and the switching frequency is set to the resonant frequency. The HGSTC operates as a DCX with fixed voltage gain of $4n$:1.

In the analysis of the operating principle in this section, in order to present the characteristics of the converter more intuitively and clearly, the following simplifications are followed.

1) The input and output capacitors are infinitely large, and the corresponding ports voltages remain constant during steady-state operation.
2) The switches are ideal MOSFETS. All parasitic parameters are ignored except for the components shown in the schematic.
3) Capacitors C_1 and C_3 have the same capacitance value. The switching frequency matches the resonant frequency, that is, $C_1 = C_2$, and $\omega_r = 2\pi f_r = 2\pi f_s = (2L_kC_1)^{-1/2} = (2L_kC_3)^{-1/2} = (L_rC_2)^{-1/2}$, where ω_r is the resonant angular frequency, f_r is the resonant frequency, and f_s is the switching frequency.

Within one switching cycle, the converter has 8 operating modes. The main waveform of the circuit is depicted in Fig. 3, where S_A, S_B, i_{Lk}, i_{Lm}, i_{C1}–i_{C3}, i_{S1}–i_{S8}, i_o, i_{load}, i_{Co}, and $v_{DS(S1)}$ –$v_{DS(S8)}$ are driving signal for S_1, S_3, S_5, and S_8, driving signal for S_2, S_4, S_6, and S_7, current through L_k, current through L_m, current through C_1–C_3, current through S_1–S_8, output current before C_o, load current, current through C_o, and voltage across S_1–S_8, respectively.

Mode 1 (t_0–t_1): At t_0, S_1, S_3, S_5, and S_8 are soft turned ON, S_2, S_4, S_6, and S_7 keep OFF, and the converter enters the steady-state Phase A. The equivalent circuit is shown in Fig. 4(a). There are two main power paths, the first one charging from the input side to C_1 and then flowing through the transformer to the output side, and the second one charging from C_2 to C_3 and then flowing through the transformer to the output side.

Mode 2 (t_1–t_2): At t_1, S_1 and S_3 are turned OFF, S_5 and S_8 are driven to turn OFF but current flows through the body diodes. The equivalent circuit is shown in Fig. 4(b). The C_{oss} of S_2 and S_4 begin to be discharged, the C_{oss} of S_1 and S_3 begin to be charged, the current of resonant tanks remain positive. When i_{Lm} is greater than i_{Lk}, the secondary winding current i_s reverses, S_5 and S_8 are OFF, and this interval ends.

Mode 3 (t_2–t_3): At t_2, S_5 and S_8 are OFF, and the equivalent circuit is shown in Fig. 4(c). The C_{oss} of S_6 and S_7 start to be discharged, and the C_{oss} of S_5 and S_8 start to be charged. According to the aforementioned simplified assumption, this process is faster than the charging and discharging process of the C_{oss} of S_1–S_4, so the body diodes of S_6 and S_7 begin to conduct, and this interval ends.

Mode 4 (t_3–t_4): The C_{oss} of S_2 and S_4 remain being discharged, while the C_{oss} of S_1 and S_3 remain charged. The equivalent circuit is shown in Fig. 4(d). When this process ends, the body diodes of S_2 and S_4 begin to conduct, and this interval ends.

The above intervals cover half of the switching cycle of the converter. In the following half cycle, each resonant tank will operate with opposite polarity. The equivalent circuits will not be analyzed one by one. All switches are soft turned ON. Based on above analyses, the HGSTC operates symmetrically between two steady-state phases A and B with dead time, and can achieve fixed voltage gain energy conversion without closed-loop control.

B. Voltage Gain Analysis

In this part, ignoring the dead time, assume that the interval of Phase A is t_0–t_A and the interval of Phase B is t_A–t_B, where $t_A - t_0 = t_B - t_A = T_s/2$. By solving the state of the resonant tanks, the voltage gain of the converter can be obtained.

In Phase A, the state equations of the circuit are expressed as

$$\begin{cases} v_{c1}(t) + L_k\frac{di_{Lk}(t)}{dt} + nV_o - V_{in} = 0, \\ v_{c3}(t) + L_k\frac{di_{Lk}(t)}{dt} + nV_o - v_{c2}(t) = 0, \\ C_1\frac{dv_{C1}(t)}{dt} + C_3\frac{dv_{C3}(t)}{dt} - i_{Lk}(t) = 0, \\ C_2\frac{dv_{C2}(t)}{dt} = -C_3\frac{dv_{C3}(t)}{dt}. \end{cases} \tag{1}$$

At t_0, the voltages of capacitors C_1 and C_3 reach their minimum values v_{C1min} and v_{C3min}, the voltage of capacitor C_2 reaches its maximum value v_{C2max}, and the currents of inductor L_k is zero. Therefore, the initial capacitor voltage and inductor current can be expressed as

$$\begin{cases} i_{c1}(t_0) = v_{c1min} \\ i_{c2}(t_0) = v_{c2max} \\ i_{c3}(t_0) = v_{c3min} \\ i_{Lk}(t_0) = 0. \end{cases} \tag{2}$$

In Phase B, the state equations of the circuit are expressed as

$$\begin{cases} v_{C2}(t) - v_{C1}(t) + nV_o - L_k\frac{di_{Lk}(t)}{dt} = 0 \\ v_{C3}(t) + nV_o - L_k\frac{di_{Lk}(t)}{dt} = 0 \\ C_1\frac{dv_{C1}(t)}{dt} + C_3\frac{dv_{C3}(t)}{dt} - i_{Lk}(t) = 0 \\ C_2\frac{dv_{C2}(t)}{dt} = -C_1\frac{dv_{C1}(t)}{dt}. \end{cases} \tag{3}$$

At t_A, the voltages of capacitors C_1 and C_3 reach their maximum values v_{C1max} and v_{C3max}, the voltage of capacitor C_2 reaches its minimum value v_{C2min}, and the currents of inductor L_k is zero. Therefore, the initial capacitor voltage and inductor current can be expressed as

$$\begin{cases} i_{c1}(t_A) = v_{c1max} \\ i_{c2}(t_A) = v_{c2min} \\ i_{c3}(t_A) = v_{c3max} \\ i_{Lk}(t_A) = 0. \end{cases} \tag{4}$$

The relationship between the output current and the inductor current within a switching period can be expressed as

$$I_o = \frac{n\int_{t_0}^{t_A} i_{Lk}(t)dt - n\int_{t_A}^{t_B} i_{Lk}(t)dt}{T_s}. \tag{5}$$

By bring (1)–(4) into (5), it can be simplified as

$$\begin{cases} v_{c1max} - v_{c1min} = v_{c3max} - v_{c3min} = \frac{I_o T_s}{8C_1} \\ v_{c2max} - v_{c2min} = \frac{I_o T_s}{8C_2}. \end{cases} \tag{6}$$

Combining (6) with (1)–(4), the simplified time domain expressions of the inductor current and capacitor voltage in T_s can be expressed as follows:

$$\begin{cases} v_{C1}(t) = 6V_o + \frac{I_o T_s}{16C_1}\sin\omega_r(t - t_0 - \frac{T_s}{4}) \\ v_{C2}(t) = 4V_o + \frac{I_o T_s}{16C_2}\sin\omega_r(t - t_0 + \frac{T_s}{4}) \\ v_{C3}(t) = 2V_o + \frac{I_o T_s}{16C_1}\sin\omega_r(t - t_0 - \frac{T_s}{4}) \\ i_{Lk}(t) = \frac{\pi I_o}{4}\sin\omega_r(t - t_0). \end{cases} \tag{7}$$

Finally, the voltage gain is obtained as

$$G = \frac{V_o}{V_{in}} = \frac{1}{4n}. \tag{8}$$

In summary, the HGSTC overcomes the drawback of SCC and STC that require a large number of switching devices to achieve high step-down gain through a simple-structured autotransformer.

C. Family of the Topologies

Distinct connection configurations of transformers can modify the total voltage gain of the converter. Four transformer configurations are depicted in Fig. 5(a)–(d), where configurations (a) and (c) leverage short-circuit connections of the same-polarity terminals and can be optimized into autotransformers, where the primary and secondary sides share a single winding. This configuration provides two major advantages: First, the cancellation effect between oppositely directed primary and secondary currents reduces current stress on the winding conductors, directly minimizing copper losses in the magnetic components. Second, the elimination of isolation gaps and the reduction of

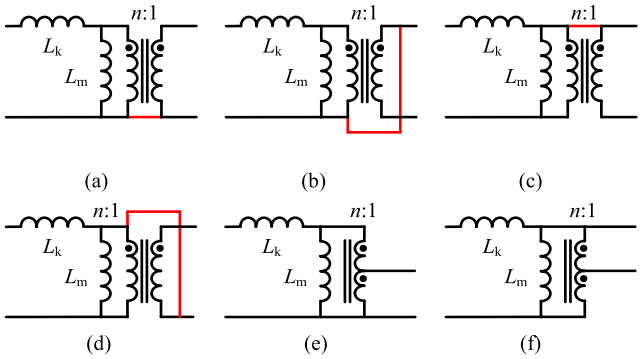

Fig. 5. Transformer configurations. (a) Configuration 1. (b) Configuration 2. (c) Configuration 3. (d) Configuration 4. (e) Configuration 5. (f) Configuration 6.

TABLE I
VOLTAGE GAIN OF DISTINCT TRANSFORMER CONFIGURATIONS

Transformer configuration	Voltage gain	
Fig. 5(a)	$G=\begin{cases}\frac{1}{m\cdot n} \\ \frac{1}{m\cdot n-n+1}\end{cases}$	m=2,4,6.... m=3,5,7...
Fig. 5(b)	$G=\frac{1}{m\cdot n+2}$	m=2,4,6...
Fig. 5(c)	$G=\begin{cases}\frac{1}{m\cdot n-2n+2m} \\ \frac{1}{m\cdot n-n+1}\end{cases}$	m=2,4,6.... m=3,5,7...

one terminal significantly enhance the design and implementation feasibility of the transformer. The corresponding autotransformer models for configurations (a) and (c) are depicted in Fig. 5(e) and (f), respectively. With reference to (1)–(8), the relationship between the converter gain, the modular number m of the multilevel modules, and the transformer turns ratio n under various transformer and circuit configurations is systematically derived and summarized in Table I, excluding situations where the voltage at both ends of the resonant cavity is 0 or there is a voltage mismatch between multilevel modules.

Based on the aforementioned derivation of voltage gain, topologies with distinct voltage gains have been derived. Analogous to Fig. 2, two additional representative topologies are presented in Fig. 6. The configuration in Fig. 6(a) employs the configuration of Fig. 5(b), achieving a voltage gain of 1/10, whereas Fig. 6(b) employs the configuration of Fig. 5(c), achieving a voltage gain of 1/9. Considering the integration potential of magnetic components such as autocoupling and miniaturization, the subsequent analysis in this article focuses on the topology illustrated in Fig. 2 for further investigation.

III. CONVERTER DESIGN CONSIDERATIONS

A. Soft Switching Analysis

The switches of the proposed converter are divided into main switches S_1–S_4, and rectifier switches S_5–S_8, but in each switching process, the turn-ON process of all switches can be considered

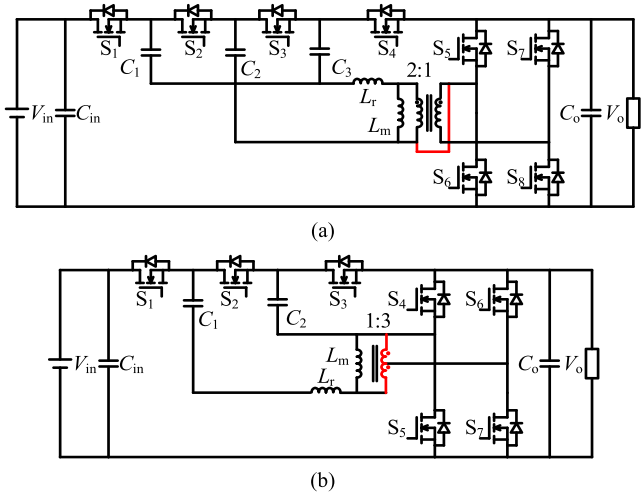

Fig. 6. Two representative topologies of the family. (a) Topology with voltage gain of 1/10. (b) Topology with voltage gain of 1/9.

to start simultaneously. Taking the switching from Phase A to Phase B as an example, the resonant tank current remains positive after S_1 and S_3 are turned OFF until S_2 and S_4 are turned ON, so that all C_{oss} are fully charged or discharged. According to the principle of energy conservation, the resonance process between the magnetic components and the output capacitance of the switches should ensure the following relationship:

$$\begin{aligned} &L_{\mathrm{k}}\left(i_{Lr(t1)}+i_{Lk(t1)}\right)^2+\frac{1}{2}\left(L_{\mathrm{r}}+2L_{\mathrm{k}}\right)i_{Lr(t1)}{}^2 \\ &\geq C_{oss(\mathrm{S1,S4})}V_{\mathrm{ds(S1,S4)}}{}^2+C_{oss(\mathrm{S2,S3})}V_{\mathrm{ds(S2,S3)}}{}^2 \\ &+2C_{oss(\mathrm{S5-S8})}V_{\mathrm{ds(S5-S8)}}{}^2 \end{aligned} \tag{9}$$

where $i_{Lk(t1)}$, $V_{\mathrm{ds(S1,\ S4)}}$, $V_{\mathrm{ds(S2,\ S3)}}$ refer in particular to current through L_{k}, the drain-source voltage of S_1 and S_4, and the drain-source voltage of S_2 and S_3 at the beginning of dead time, respectively. By substituting (10) into (9), the soft switching condition is simplified to (11)

$$\begin{cases} V_{\mathrm{ds(S1,S4)}}=2nV\mathrm{o}, \\ V_{\mathrm{ds(S2,S3)}}=(2n-1)\,V\mathrm{o}, \\ i_{Lk}(t_1)=-2i_{C2}(t_1)=\frac{nV\mathrm{o}}{4f_{\mathrm{s}}L\mathrm{m}} \end{cases} \tag{10}$$

$$\begin{aligned} &\frac{4L_{\mathrm{k}}+L_{\mathrm{r}}}{\mathrm{L_m}^2}\geq\frac{128{f_{\mathrm{s}}}^2}{n^2} \\ &\left[(2n-1)^2C_{oss(\mathrm{S1,S4})}+4n^2C_{oss(\mathrm{S2,S3})}+2C_{oss(\mathrm{S5-S8})}\right]. \end{aligned} \tag{11}$$

Inequality (11) describes the ZVS boundary regarding hardware parameters. Fig. 7 visually illustrates the ZVS constraints of the relevant variables at a constant switching frequency ($f_{\mathrm{s}}=f_{\mathrm{r}}$). It can be seen that the smaller k_1, the wider the ZVS frequency range; The larger k_2, the wider the ZVS frequency range. Under high resonance frequency conditions, the resonant inductance is very small, and due to the high rms value of the primary side current, it is difficult to reduce the inductance ratio k_1 by reducing the magnetizing inductance. This is similar to

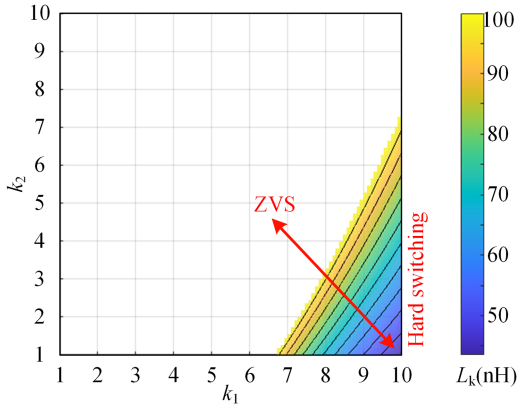

Fig. 7. ZVS boundary at a constant switching frequency ($f_s = f_r$). $k_1 = L_m / L_k$, $k_2 = L_r / L_k$.

the classical *LLC* converter, which is also one of the reasons why such converters are always designed as DCX that operate at a fixed frequency at high switching frequencies and have unregulated voltage gain.

According to (7), ensure that the peak-to-peak value of the sinusoidal fundamental component of the voltage across resonant capacitors C_1–C_3 is not greater than a certain value V_{Cp}

$$\begin{cases} \frac{P_o}{8V_oC_1f_s} \le V_{Cp} \\ \frac{P_o}{8V_oC_2f_s} \le V_{Cp}. \end{cases} \tag{12}$$

According to the series *LC* resonance equation, (12) is transformed into

$$\begin{cases} L_k \le \frac{V_oV_{Cp}}{\pi^2 f_s P_o} \\ L_r \le \frac{2V_oV_{Cp}}{\pi^2 f_s P_o}. \end{cases} \tag{13}$$

The constraint of L_k is given by (13), and the constraint of L_m is obtained from (11).

For switches S_5–S_8, the soft-switching transitions differ from those of conventional MMSCC due to the presence of transformers. The resonant tank current direction remains asynchronous with the secondary-side transformer current direction, and their differential current flows through the magnetizing inductance L_m. Specifically, the zero-crossing time of i_s precedes that of i_{Lk}. Prior to achieving ZVS turn-ON for S_2/S_4 (or S_1/S_3), the charging of C_{oss} in S_5/S_8 (discharging in S_6/S_7), and discharging of C_{oss} in S_6/S_7 (charging in S_5/S_8) have already commenced. Consequently, a transient period exists where all switches S_1–S_8 operate in resonant states. Assuming constant input capacitor voltage V_{in} and output capacitor voltage V_o, the circuit comprises 6 current loops and 12 nodes. Notably, the voltage v_p at the common node shared by S_2, S_3, and C_2 varies dynamically with the secondary-side resonant process

$$v_p(t) = v_{C2}(t) + L_r\frac{di_{Lr}(t)}{dt} + v_{ds(S8)}(t). \tag{14}$$

During the interval t_2–t_3, $v_{DS(S8)}(t)$ rises from 0 to V_o, which drives the node voltage v_p to increase from $2n$ V_o to $(2n+1)$ V_o. This dynamic voltage transition enables soft commutation between paired switches through coordinated voltage stress redistribution: S_1 (rated for $(2n\text{-}1)$ V_o) commutates with S_2 (rated for $2nV_o$), whereas S_3 (rated for $2nV_o$) commutates with S_4 (rated for $(2n\text{-}1)$ V_o). The progressive voltage elevation across v_p ensures sequential ZVS activation by precisely aligning the voltage stresses and resonant transitions across these switch pairs, thereby maintaining topological symmetry and stress balancing critical for reliable high-frequency operation.

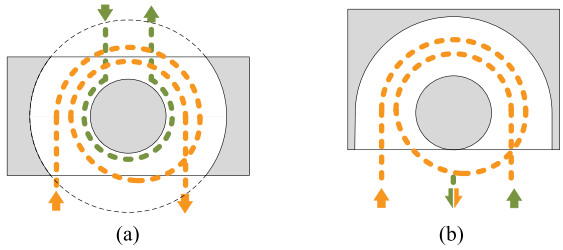

Fig. 8. Two winding structures of 2:1 transformer. (a) Generic 2 turns:1 turn configuration. (b) Center tap autotransformer terminated on the same side.

B. Magnetic Design

According to the design constraints in the previous section, given the resonant frequency f_r, the electrical parameters of the transformer, such as L_k and L_m, can be easily obtained. The task of this section is to design its physical structure. In this work, a planar transformer is designed to operate at 1 MHz to achieve high power density. In order to carry a large output current, the number of turns on the secondary side of the transformer is set to 1, so according to the voltage gain expression, the number of turns on the primary side is 2.

1) Step 1. Core Outline and Termination: In addition to electrical parameters, the most important consideration for this transformer is its box volume. However, before achieving the goal of minimizing its volume, its termination and installation will have a significant impact on the overall power density of the transformer. Therefore, this section will first determine its outline.

To construct a 2:1 transformer, the typical method involves winding two coils on EE- or EER-type magnetic cores, as shown in Fig. 8(a). In Fig. 8(b), all terminals are repositioned to one side of the core, forming a 2-turn:1-turn autotransformer configuration, while the opposite side of the core remains closed. This design enables the realization of an EP core with narrowed edge legs. The advantages of this structure lie in: 1) The autotransformer essentially shares the copper of the primary and secondary sides, the total number of windings is reduced from 3 turns to 2 turns, and the reverse current offsets each other in the same conductor, which significantly reducing the conduction loss; 2) The primary and secondary devices can be distributed on the same side of the magnetic component, which is conducive to reducing PCB conduction loss and reducing the converter volume. Subsequent designs will adopt this optimized structural configuration.

2) Step 2. Magnetic Material and Effective Cross-Sectional area: The minimum effective cross-sectional area of magnetic

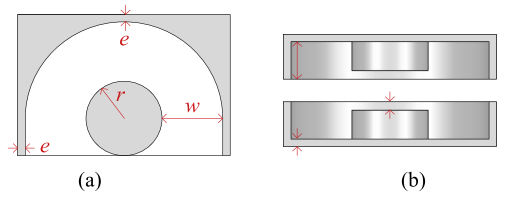

Fig. 9. Core dimensions definition. (a) Top view (only one piece of a pair is shown). (b) Side view.

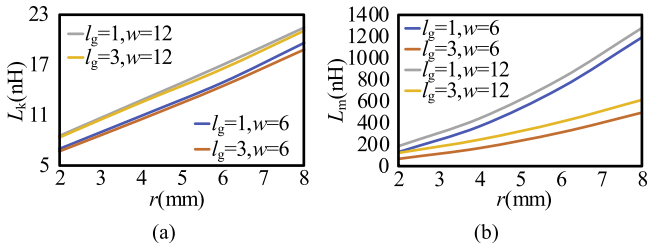

Fig. 10. Relationship between electrical parameters and dimensions of the transformer. (a) Leakage inductance L_k versus r, l_g and w. (b) Magnetizing inductance L_m versus r, l_g, and w.

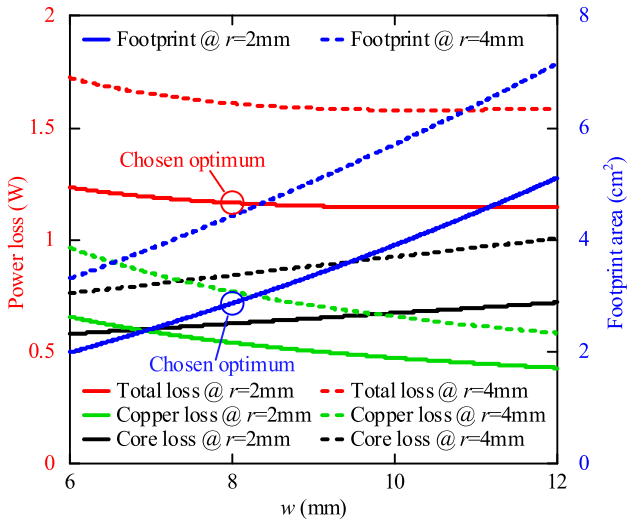

Fig. 11. Relationship between power loss, footprint area, and dimension variables.

core can be expressed as

$$A_{e(\min)} = \frac{DV_o}{N_s f_r B_m} \tag{15}$$

where D is the excitation duty cycle of the transformer, taken as 0.5; N_s is the number of turns ON the secondary side of the transformer, which is set to 1; B_m is the maximum magnetic density. High-frequency ferrite DMR51W from DMEGC is selected for transformer core material. The maximum flux density is set to 50 mT. The volumetric core loss at 1 MHz is 115 mW/cm^3, which remains sufficiently low to prevent local magnetic core loss caused by uneven flux.

3) Step 3. Relationship Between Core Dimensions and Electrical Parameters as Well as Magnetic Flux Density: The magnetic core of the autotransformer is composed of two identical EP cores with air gap in the central column. The core size is defined, as shown in Fig. 9. In order to achieve the flattest profile, the window height h_w should be equal to the thickness of the winding PCB, which is set to 4 mm. The radius of the central column r, the width of the window w and the length of the total air gap l_g determine L_k and L_m. In addition, the thickness of the top and bottom plane h_i, the width of the side legs, e, and r, directly affect the maximum magnetic flux density of the core. Its initial value can be estimated by $A_{e(\min)}$ and optimized based on the flux density through magnetic simulation. Both e and h_i are initialized to 1 mm. Finally, w is related to the average current density of the windings. To avoid confusion, the electrical parameters are still based on the original isolation transformer model, as shown in Fig. 2.

Based on the equivalent circuit and dimensions definition, finite element simulation was conducted to obtain the relationship between its electrical parameters and dimensions, as drawn in Fig. 10. Obviously, whether r or w increases, there will be more leakage flux directly passing through the conductor without passing through another winding. The main influencing factor for L_m is l_g. The larger the l_g, the smaller the magnetic permeability of the magnetic path, and the smaller the L_m. r and w, respectively, affect the magnetic conductivity of the central column and other parts, and also have a certain impact on L_m.

4) Step 4. Tradeoff Between Power Loss and Footprint: In the final step of design, a tradeoff should be made between the power loss and volume of the transformer, while meeting the basic electrical parameters. Because the height of the transformer is already limited by the thickness of the PCB, this step uses footprint to characterize the volume of the transformer.

Fig. 11 illustrates the relationship between the footprint, copper loss, core loss, and the total loss and the core dimensions w and r. The solid line represents the result when $r = 2$ mm, and the dotted line represents the result when $r = 4$ mm. According to the result of the last step, r is limited to within 4 mm. Although this will result in the local cross-sectional area of the central column of the EP core being smaller than $A_{e(\min)}$, in fact, in order to achieve a smaller magnetizing inductance, the length of the air gap accounts for a large proportion of the height of the central column, which means that most of the magnetic circuit with a smaller cross-section is air. Therefore, setting r to 2–4 mm is allowed. Obviously, smaller r has more advantages in both power loss and footprint, as w increases, the copper loss and core loss show different trends, so in general, the total of the two may first decrease and then increase, but in this work, footprint is a vital factor affecting the overall power density of the converter. Therefore, considering that the total loss does not change significantly when $w = 8$–12 mm, w was ultimately set to 8 mm. The winding is composed of two identical 2oz 10-layer PCBs, with the shape and structure shown in Fig. 12. The layers are connected using vias, pads, and copper foils. The odd-numbered layers and the even-numbered layers are, respectively, connected in parallel and form one turn.

Finite element analysis was used to verify the magnetic field density and current density of the designed transformer, and the results are shown in Fig. 13. As can be seen in Fig. 13(a),

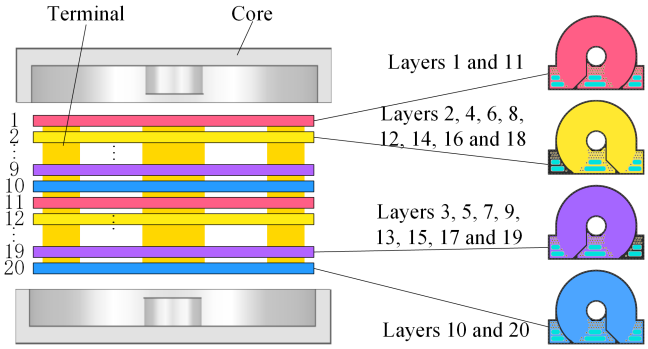

Fig. 12. PCB winding structure of the autotransformer.

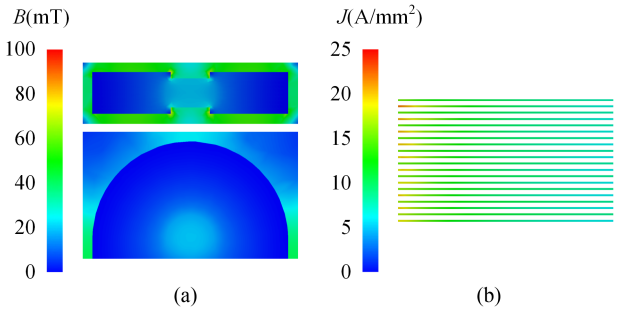

Fig. 13. Finite element simulation results of magnetic density and winding current density. (a) Magnetic density on the vertical and horizontal section of the central cylinder. (b) Winding current density on the vertical section of the winding center.

the magnetic flux in the core is uniform, with a maximum flux density of about 50 mT except for local crowding, which meets the design goal. The performance of current density in PCB is shown in Fig. 13(b). Although the average current density is limited to 10 A/mm^2 according to design, hotspots of 20 A/mm^2 appear locally. The simulated leakage inductance is 12 nH, which can act as a resonant inductor in the resonant tank.

IV. Comparative Study of the HGSTC and State-of-Art Converters

In the design of DCX for IBC applications, achieving high efficiency and power density constitutes the primary objectives. Both *LLC* converter and STC have been extensively studied and adopted in IBC implementations due to their excellent performance [1], [15]. This section conducts a comparative study between the proposed HGSTC and *LLC*/STC topologies with same voltage gain to demonstrate the performance superiority of HGSTC. To highlight the differences between the three converters, the loss parts with difference are the main research objects, and the same parts are ignored. The discussion in this section is based on simplified models, including waveform calculations without high-order harmonics, ideal switch models with linear C_{oss}, ideal diode and constant R_{dsON}, constant resonant capacitors and dc capacitors, and lines without parasitic parameters.

Fig. 14 shows 48 V to 6 V *LLC*, STC, and the proposed HGSTC topologies. The rectifier side of *LLC* converter and HGSTC can be implemented as full-wave rectifier and bridge

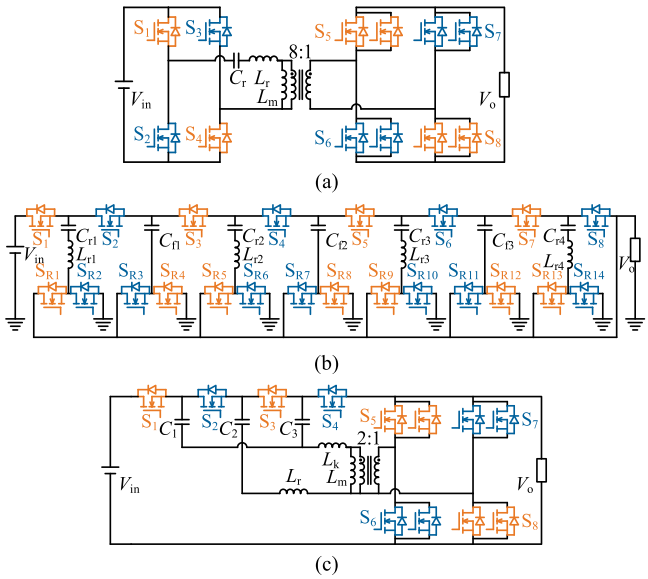

Fig. 14. 48 V to 6 V *LLC*, STC, and the proposed HGSTC topologies. (a) *LLC*. (b) STC. (c) Proposed HGSTC.

TABLE II
Voltage and Current Stress of Secondary SR Switches

Topology	Voltage stress	Current stress (sum)
LLC with bridge rectifier	6V	πI_o
LLC with full-wave rectifier	12V	πI_o
STC	6V	$7/8\ \pi I_o$
HGSTC with bridge rectifier	6V	$7/8\ \pi I_o$
HGSTC with full-wave rectifier	12V	$7/8\ \pi I_o$

rectifier, but given that STC is inherently limited to bridge rectification configurations, all topologies in this comparative study employ bridge rectifier to maintain methodological consistency. The synchronous rectifier (SR) switches in Fig. 14(a) and (c) adopt multiple MOSFETS in parallel to carry high current output.

A. Secondary Side SR Switches

Table II shows the voltage and current stresses of SR switches for three converters under rated input/output voltage conditions. All the SR switches' voltage stress of the three converters with bridge rectifiers is 6 V. The voltage stress of *LLC* and HGSTC with full-wave rectifier will be doubled to 12 V, but the number of synchronous rectifier switches will be halved. When the output current of the converter is I_o, the current stress of each switch from S_5 to S_8 of *LLC* (multiple parallel MOSFETS are regarded as one switch) is $(\pi/4)\ I_o$, and the sum of the current stress of the four switches is πI_o. The current stress of S_{R1} to S_{R14} of STC is $(\pi/16)\ I_o$, and the total current stress of the 14 switches is $(7\pi/8)\ I_o$. The current stress of S_5 and S_6 of HGSTC is $(\pi/4)\ I_o$, and the current stress of S_7 and S_8 is $(3\pi/4)\ I_o$. The total current stress of the 4 switches is $(7\pi/8)\ I_o$.

According to above results, it can be seen that under the same conditions, the current stress of HGSTC and STC is 12.5% smaller than that of *LLC*, which is determined by the P-PPP

TABLE III
VOLTAGE AND CURRENT STRESS OF PRIMARY SWITCHES

Topology	Voltage stress	Current stress
LLC	S_1–S_4: 48V	$(\pi/32)\ I_o$
STC	S_1, S_8: 6V; S_2–S_7: 12V	$(\pi/16)\ I_o$
HGSTC	S_1, S_4: 18V; S_2, S_3: 24V	$(\pi/16)\ I_o$

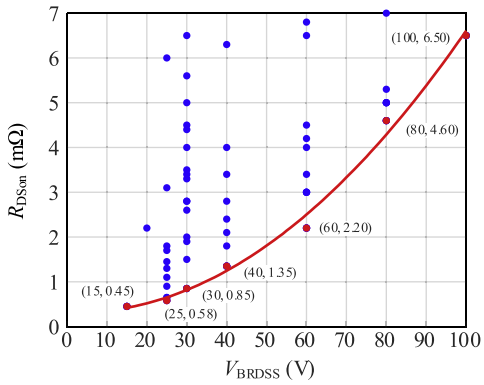

Fig. 15. Relationship between R_{DSON} and V_{BRDSS} of all 102 Infineon PQFN 3.3 mm×3.3 mm packaged OptiMOS power MOSFET products under 100 V.

structure of the former two. This structure directly transmits 12.5% of the power from the primary side to the output without flowing through transformers, inductors, or rectifiers. For voltage stress, HGSTC has the same characteristics as *LLC*, which is related to the specific implementation of rectifier.

This result shows the superiority of the proposed HGSTC's secondary side structure. More importantly, its secondary side, like *LLC*, can be flexibly implemented in various forms, such as bridge rectifier and full-wave rectifier.

B. Primary Side Switches

Table III shows the voltage and current stresses of the primary switches of the three converters. The primary switch voltage stress of *LLC* converter is 48 V, which is equal to the input voltage, and the current stress is $(\pi/32)\ I_o$. The current stress of all switches ON the primary side of STC is $(\pi/16)\ I_o$, the voltage stress of S_1 and S_8 is 6 V, and the voltage stress of S_2–S_7 is 12 V. The current stress of all switches ON the primary side of HGSTC is $(\pi/16)\ I_o$, the voltage stress of S_1 and S_4 is 18 V, and the voltage stress of S_2 and S_3 is 24V. Since the switch voltage stresses of these three converters are different, Infineon's OptiMOS power MOSFET is selected as a reference device to further evaluate the performance of the primary switches of these three converters. A standardized component selection criteria was applied uniformly to calculate conduction losses, enabling direct comparative analysis under identical operating conditions. This series of MOSFET is widely used in IBC design because of its extremely low ON-state resistance (R_{DSON}), high current carrying capacity and small package area. Fig. 15 shows the relationship between R_{DSON} and drain-source breakdown voltage (V_{BRDSS}) of PQFN 3.3 mm×3.3 mm packages with V_{BRDSS} less than 100 V, covering all 102 products. Obviously, under similar process levels, the minimum R_{DSON} is approximately quadratic with the V_{BRDSS}.

TABLE IV
PRIMARY SWITCHES SELECTION AND TOTAL CONDUCTION LOSS OF ALL PRIMARY SWITCHES

Topology	MOSFET	V_{BRDSS}	R_{DSon}	Total conduction loss
LLC [1]	IQE046N08LM5	80V	4.6mΩ	1.24W
STC [15]	IQE004NE1LM7	15V	0.45mΩ	1.18W
	IQE006NE2LM5	25V	0.58mΩ	
The proposed HGSTC	IQE008N03LM5	30V	0.85mΩ	1.18W
	IQE013N04LM6	40V	1.35mΩ	

Based on the above rules, the conduction losses of the three converters are calculated, respectively. In the selection of switches, a 1.5-fold safety margin is added on the basis of the basic voltage stress. The selection of primary switches of the three converters and the total conduction loss of all primary switches are shown in Table IV. The primary switches conduction loss of *LLC* is 1.24 W, and the loss of STC is comparable to that of HGSTC, which is about 1.18 W, which is about 4.8% lower than that of *LLC*. Furthermore, the number of primary switches of HGSTC is half of that of STC, and it has a simpler structure.'

In summary, the proposed HGSTC demonstrates significant advantages over both *LLC* and STC topologies across primary and secondary sides, characterized by reduced component count, simplified structural configuration, and optimized electrical stress distribution. These combined merits establish it as a promising topology for advanced power conversion systems requiring high efficiency and compact form factors.

C. Concept of P-PPP and Comparison of HGSTC and State-of-Art Converters

PPP converters, also known as differential power converters, establish a special connection between the source and load sides compared to conventional full power processing converters. Due to its high efficiency, low power, and low cost, PPP converters are promising in many applications.

The converter proposed in this article is different from the conventional PPP structure, but its special connection structure gives it similar characteristics to PPP, mainly manifested in voltage conversion ratio and current stress.

Fig. 16 shows a variant of the proposed converter, where there is no direct connection between the primary side and output side. In this variant, switch S4 is connected to GND, the voltage conversion ratio will change from (4*n*: 1) to (4*n* - 1: 1), which is consistent with the gain characteristics in PPP [19].

From another perspective, the current stress of the primary switches is the same with that of full power processing converters. Therefore, it can be considered that all the load power flows through the main switches, but only a portion of the power flows through the rectifier, resulting in lower current stress of rectifier switches, which is similar to the concept of PPP.

In summary, the proposed converter is regarded as a P-PPP converter due to its (1) unique connection method that affects

TABLE V
COMPARISON OF HGSTC AND STATE-OF-ART CONVERTERS

Topology	Input/output voltage	Output current	Power density	Peak efficiency	Switching frequency	Magnetic components	Driver circuit	Expandable
STC 2019[15]	48V/12V	50A	-	98.90%	320kHz	SMD	Bootstrap	Yes
LLC-DCX 2021[20]	48V/6V	150A	300W/in^3	97.8%	1MHz	PCB winding	Isolated	No
LEGO 2022[21]	48V/1V	450A	294W/in^3	88.40%	1MHz	General	Bootstrap	No
Multiphase LLC 2023[22]	48V/6V	160A	240W/in^3	96.70%	500kHz	PCB winding	Bootstrap	No
SC Buck 2023[23]	24V/6V	15A	-	93.00%	200kHz	General	Bootstrap	Yes
Hybrid SCC 2024[24]	48V/12V	16.6A	481W/in^3	96.79%	500kHz	SMD	Bootstrap	No
SCC+SRC 2024[7]	48V/12V	25A	346W/in^3	97.23%	1MHz	PCB winding	Bootstrap	No
SCC+SRC 2025[2]	48V/12V	20A	300W/in^3	97.12%	1MHz	PCB winding	Bootstrap	No
HGSTC This work	48V/6V	84A	816W/in^3	96.03%	1MHz	PCB winding	Bootstrap	Yes

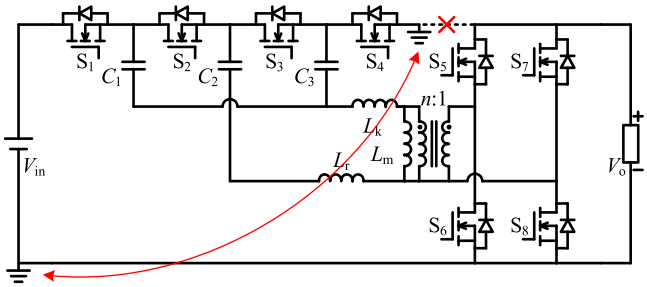

Fig. 16. Variant of the proposed converter. The direct connection between main switches and load is cut off, with the voltage conversion ratio changes from (4n: 1) to (4n - 1: 1).

the voltage conversion ratio characteristics, and (2) reduced current stress on some switches. This concept highlights its similar properties to PPP and emphasizes its differences using the "pseudo-" prefix.

Table V listed a performance comparison of solutions applied to voltage regulator modules in data centers. The efficiency of the (4:1) solutions is generally higher than 96%, with some exceeding 98% ; On the contrary, that of (48:1) converters is difficult to break through 90% ; (8:1) is at an intermediate level, therefore the proposed HGSTC has satisfactory efficiency and power density performance. Furthermore, it is worth noting that only a few solutions are expandable, highlighting the advantages of the HGSTC's family framework.

V. EXPERIMENTAL VERIFICATIONS

A hardware prototype of the proposed HGSTC is built to validate theoretical analyses. The key parameters and specifications of the prototype are summarized in Table VI. The prototype operates at a nominal input voltage of 48 V (46–50 V range) and output voltage of 6 V (5.75–6.25 V range) with a rated current

TABLE VI
PARAMETERS AND SPECIFICATIONS OF THE PROTOTYPE

Parameter and specifications	Rated value
Input voltage, V_i	46 – 50 V
Output voltage, V_o	5.75 – 6.25 V
Output current, I_o	84 A
Rated power, P_o	500 W
Switching frequency, f_s	1 MHz
Resonant capacitance, C_1, C_3	1.01 μF
Resonant inductance, L_k	12.5 nH
Switches S_1, S_4	IQE008N03LM5CGSC
Switches S_2, S_3	IQE013N04LM6CGSC
Switches S_5 – S_8	IQE004NE1LM7CGSC
Magnetic core	DEMEG DMR51W

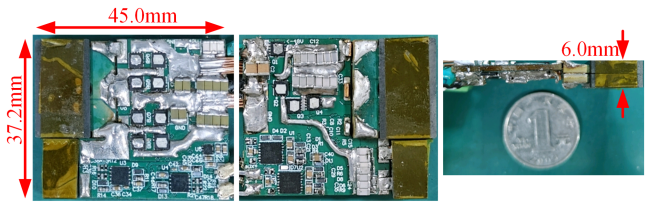

Fig. 17. Photograph of the prototype. (a) Front. (b) Back. (c) Side.

of 84 A. Fig. 17 provides photographs of the prototype, with a box volume of 45.0 × 37.2 × 6.0 mm³, resulting in a maximum power density of 816 W/in^3.

The experimental key waveforms are presented in Figs. 18 and 19. Fig. 18(a)–(d) shows the gate-source voltages and drain-source voltages of switches S_1–S_8 under rated input voltage and 29 A output current, whereas Fig. 19(a)–(d) shows the gate-source voltages and drain-source voltages of switches S_1–S_8

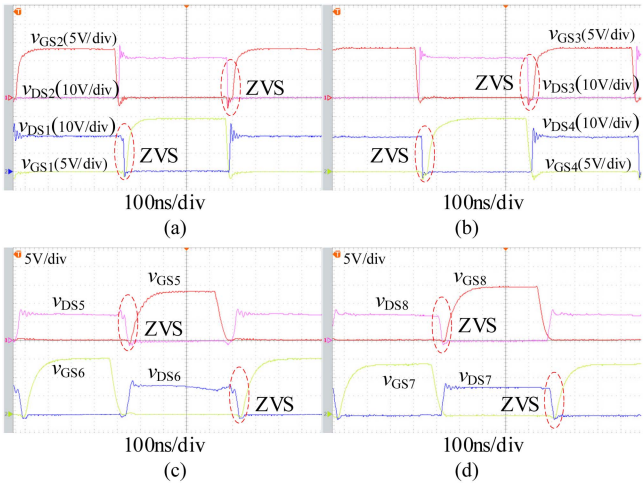

Fig. 18. Experimental key waveforms under rated input voltage and 29 A output current. (a) Gate-source and drain- source voltage of S_1, S_2. (b) S_3, S_4. (c) S_5, S_6. (d) S_7 and S_8.

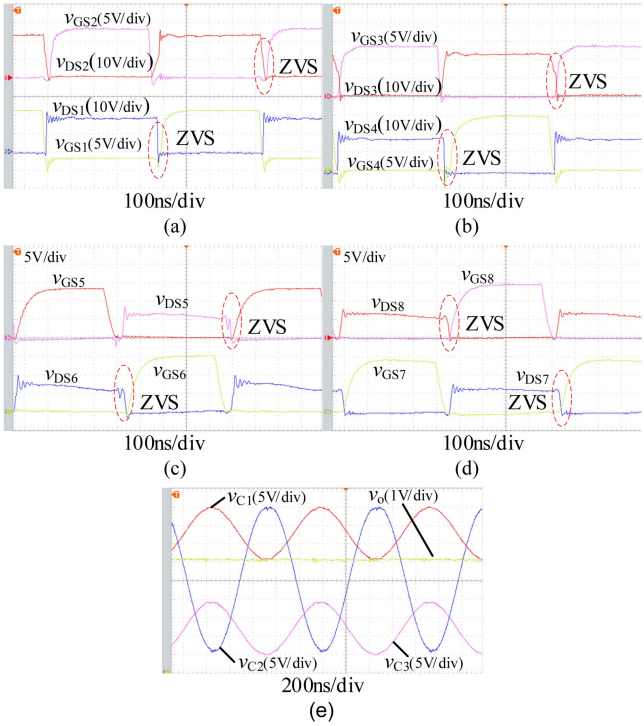

Fig. 19. Experimental key waveforms under rated input voltage and 84 A output current. (a) Gate-source and drain-source voltage of S_1, S_2. (b) S_3, S_4. (c) S_5, S_6. (d) S_7 and S_8. (e) Output voltage and resonant capacitors voltage at full load.

under rated input voltage and 84 A output current, where $v_{GS1} - v_{GS8}$ and $v_{DS1} - v_{DS8}$ represent gate-source voltages and drain-source voltages of S_1–S_8, respectively. These waveforms confirm that all switches achieve soft-switching operation under light and heavy load. The output voltage and the voltage of the resonant capacitors under full load are shown in Fig. 19(e).

The transient response when the load decreases from full load (84 A) to one-third load (29 A) and when the load increases from one-third load to full load is shown in Fig. 20. The experimental

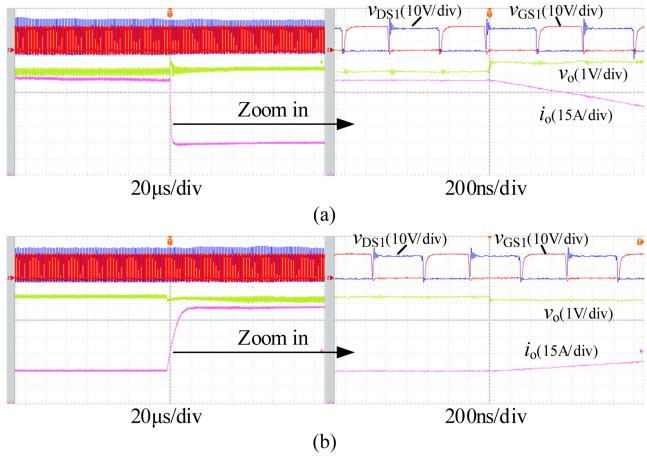

Fig. 20. Transient response experimental waveform. (a) From 84 A to 29 A. (b) From 29 A to 84 A.

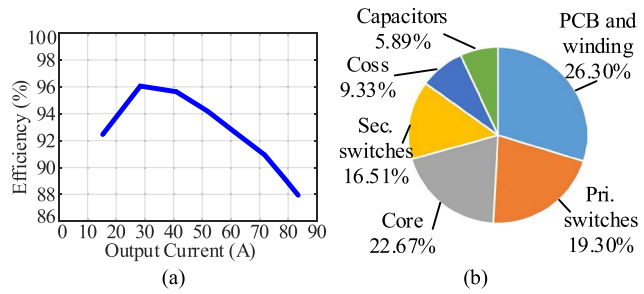

Fig. 21. Measured efficiency and power loss breakdown at peak efficiency point. (a) Efficiency. (b) Power loss breakdown.

waveform includes the output voltage v_o and output current i_o before and after the load change event, as well as the driving voltage v_{GS1} and drain-source voltage v_{DS1} of one main switch S_1, to reflect the soft switching characteristics of the converter under transient conditions. According to the experimental results, the maximum current drop rate is about 15.0 A/μs, and the maximum current rise rate is about 4.7 A/μs.

The measured efficiency curve of the prototype from 15 to 84 A output current is shown in Fig. 21(a). The peak efficiency is 96.03% at 29 A. Under light load, core loss and gate driver loss are the main parts of the total power loss. Under heavy load, conduction loss becomes the dominant part of the total power loss, among which PCB loss is an important component. Detailed power loss breakdown of the HGSTC prototype is plotted in Fig. 21(b). The largest proportion is PCB and winding losses, as transformers use PCB windings, so these two are grouped together. Due to the high current and pursuit of the lowest possible prototype cost, the current density of PCB is inevitably high, which leads to high copper losses. Second, there is the loss of the switches, including conduction loss and turn-OFF loss. In order to achieve lower R_{DSON}, the junction capacitance of low-voltage Si MOSFET is large. In addition, although they achieve ZVS operation, there are still turn-OFF losses. Better PCB layout or using more advanced PCB manufacturing processes may improve the efficiency performance of this converter under heavy load.

VI. Conclusion

This article proposes a P-PPP multilevel modular HGSTC for data center IBCs, featuring a topology based on high step-down gain multilevel modules. By integrating P-PPP techniques and specialized autotransformer configuration, the design achieves both high step-down gain and high output current capabilities. Furthermore, a family of topologies is introduced with generalized voltage gain expressions derived to unify their operational principles. The converter inherits the low-voltage-stress characteristic of SCC switches, enabling the use of low-voltage Si MOSFETS with optimized figure-of-merit. A detailed theoretical analysis and key component design guidelines are provided. A 1 MHz 500 W 8:1 DCX prototype was built, with a maximum output current of 84 A, a power density of 816 W/in^3, and a peak efficiency of 96.03% . The experimental results verified the feasibility of the theoretical model and design.

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