Power and Signal Dual Modulation in DC/DC Converters Using FSK-Based DSSS for High Anti-Interference Performance

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***Abstract*—Power and signal dual modulation (PSDM) enables simultaneous power control and data transmission in dc microgrid (DCMG). However, the communication signal degrades during long-distance transmission and be disrupted by noise on the transmission line, posing challenges for the anti-interference capability. This article proposes a novel PSDM method using symmetrical binary frequency shifting-direct sequence spread spectrum (SBFS-DSSS) to address these challenges. By integrating frequency shift keying (FSK) with DSSS, SBFS-DSSS technique improves communication sensitivity and anti-interference capabilities. During demodulation, binary FSK signals (40/50 kHz) encoded with DSSS and carried by switching ripple are converted to low-frequency binary phase shift keying (PSK) signals (5 kHz) with DSSS through a two-step process, preserving high autocorrelation. To ensure reliable communication, a synchronization mechanism is incorporated and periodically refreshed during communication, guaranteeing consistent alignment between transmitter and receiver. To evaluate the performance of SBFS-DSSS technique, the signal-to-noise ratio and processing gain of the system are analyzed and compared with conventional FSK. In a 1 kW DCMG prototype system, the performance of the proposed scheme is assessed. SBFS-DSSS achieves an 11.5 dB processing gain and maintains reliable communication up to 500 m, thereby demonstrating the advantages.**

***Index Terms*—DC microgrid, direct sequence spread spectrum (DSSS), power and signal dual modulation, symmetrical binary frequency shifting (SBFS), talkative power conversion.**

I. Introduction

As a vital component of the energy internet [1], dc microgrid (DCMG) is increasingly reliant on robust communication links to ensure the secure operation, energy scheduling, and protection of power transactions [2], [3], [4]. Consequently, the integration of power electronic equipment with reliable communication connections is a future development trend.

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Power and signal dual modulation (PSDM) technology, also referred to as talkative power conversion (TPC), is a method in which power converters simultaneously achieve power control and information modulation without requiring additional devices [5], [6], [7]. Moreover, a dual verification mechanism for power and information can be designed based on PSDM technologies, which improves system security [8] and makes it an attractive option for DCMG to realize reliable energy and information transmission. Recent studies have significantly expanded the scope of TPC. Leng et al. [9] implemented variable zero vector position modulation in three-phase dc–ac converters, while Placzek et al. [10] integrated a low-bandwidth frequency shift keying (FSK) link into an inductive power transfer stage. These works demonstrate the applicability of PSDM across various topologies and highlight the increasing maturity of the field.

PSDM technologies can be classified into two categories based on the relationship between power and data modulation, encoded switching carrier (PSDM-ESC) and encoded control ripple (PSDM-ECR) [11], [12], [13]. In the PSDM-ESC system, the information carrier is the same as the primary harmonic ripple [11], with its amplitude determined by power conversion and circuit parameters. This means the amplitude of the information carrier cannot be regulated and is prone to being affected by power fluctuations. In contrast, PSDM-ECR systems allow regulation of the information carrier's amplitude due to the independence of data and power carriers [12], [13]. This adaptability allows the PSDM-ECR to maintain signal integrity during long-distance transmissions, making it more robust against signal attenuation [13], [14], [15]. However, PSDM-ECR introduces more complex output power harmonics and complicates power control.

Given the PSDM-ESC system's susceptibility to signal attenuation and power noise, enhancing its interference resistance is highly desirable for reliable communication. As shown in Table I, spread spectrum (SS) techniques are widely employed in converters to mitigate EMI harmonics and reduce communication interference [16], [17], [18]. The two most popular SS methods are direct sequence spread spectrum (DSSS) and frequency-hopping spread spectrum (FHSS).

In [19], a phase locked loop employing a SS technique is implemented to minimize EMI harmonics and voltage ripple in

TABLE I
APPLICATIONS OF SS TECHNOLOGIES IN PSDM SYSTEMS

Ref.[a]	Conf.[b]	Modu.[c]	Freq.[d]	SSTe.[e]	Comm.[f]
[19],[20]	/	FSK	/	FHSS	/
[21]	/	FSK	/	SS-FSK	/
[22]	/	BPSK	/	DSSS	/
[23]	PSDM-ESC	DPSK	Yes	DSSS	Yes
[26]	PSDM-ECR	DQPSK	Yes	/	Yes
[25]	PSDM-ESC	FH-DPSK	/	/	Yes
[14]	PSDM-ESC	FHSS-4FSK	/	FHSS	Yes

[a]Cited Reference, [b]Configuration of TPC, [c]Modulation Technique, [d]Frequency Switching Impact, [e]SS Techniques, [f]Communication function.

buck converters. Kundrata and Adrija [20] achieved FHSS by randomly hopping among 256 switching frequencies ranging from 900 kHz to 1.1 MHz, mitigating interference and diminishing EMI peaks. In [21], the SS frequency modulation is applied to dc–dc converters using time-based control, reducing EMI by 11.2 dB without affecting the duty cycle. In [22], a novel key-based DSSS technique utilizing binary phase shift keying (BPSK) modulation is implemented to enhance the security and reliability of communications-based train control systems against EMI. To reduce EMI, these SS-based techniques usually spread the frequencies or the phase of at long-line transmission pulse width modulation (PWM) carrier, which have the potential to achieve PSDM techniques as well.

Conventionally, DSSS is paired with phase shift keying (PSK) modulation [23], whereas FHSS is often associated with FSK [14], [24], [25]. However, applying these SS-based methods to PSDM-ESC systems poses inherent challenges for power electronic converters. Direct PSK modulation of power carrier may disrupt the charge-discharge balance of capacitors and inductors during power conversion, resulting in output voltage fluctuations that degrade the power quality. In contrast, FSK has a negligible impact on the output voltage, making it more appropriate for SS-based solutions [25]. However, FHSS introduces additional complexities in converters. According to [20], FHSS requires higher clock rates and complex digital logic to manage rapid frequency hops. Leng et al. [14] demonstrated FHSS with 4FSK for PSDM communication, but limiting to four frequencies restricts FHSS's full potential. Precise timing for each frequency hop is critical to avoid duty-cycle errors, necessitating sophisticated compensation mechanisms that further complicate converter design.

The above review shows three critical limitations related to the integration of SS techniques into PSDM-ESC systems.

1) Conventional FSK is incompatible with DSSS, as DSSS depends on sequence autocorrelation, which FSK lacks.
2) Conventional PSK-DSSS, when applied in PSDM-ESC systems, may cause duty cycle disturbances in DCMG, compromising power quality.
3) FHSS requires complex timing, making it difficult to maintain power quality in PSDM systems. These limitations highlight the need for a technique that combines FSK's simplicity with DSSS's robustness without impacting power transfer performance.

To address the aforementioned limitations, this study proposes a novel PSDM-ESC method that uses specialized FSK to transform FSK-modulated signals into PSK-modulated signals. This approach, termed the symmetrical binary frequency shifting-direct sequence spread spectrum (SBFS-DSSS) technique, effectively mitigates the identified challenges as follows:

1) It ensures compatibility between FSK-modulated signals and DSSS during demodulation.
2) It preserves the simplicity of FSK while significantly reducing voltage fluctuations.
3) It eliminates the hardware complexity associated with frequent and rapid frequency hopping.

The primary contributions of this article are outlined as follows.

1) SBFS-DSSS technique is proposed, integrating FSK and DSSS to enhance the anti-interference performance of PSDM-ESC modulation. For PWM-based converters, transitioning from constant to variable frequency requires minimal programming changes, with negligible impact on dynamic performance and power conversion efficiency.
2) During demodulation, the SBFS-DSSS signal undergoes a two-step process: it is first converted from a high-frequency (40 kHz or 50 kHz) FSK-modulated signal to a low-frequency (5 kHz) PSK-modulated signal, followed by filtering through a bandpass filter. This conversion effectively minimizes the interference from local power switching.
3) A detailed analysis of system noise demonstrates that the SBFS-DSSS technique achieves the same processing gain equivalent to that of PSK-DSSS, as experimentally validated.

The rest of this article is organized as follows. Section II introduces the general principle of PSDM-ESC modulation, spread spectrum technique and the limitations of Applying DSSS in FSK-based PSDM-ESC. In Section III, the modulation and demodulation principles of SBFS-DSSS are discussed in detail. The code and carrier synchronization mechanism is analyzed. Section IV analyzes the anti-interference performance of the system by calculating G_{p}. In Section V, the experimental and theoretical analyses are validated. Finally, Section VI concludes this article.

II. PSDM-ESC MODULATION AND SPREAD SPECTRUM TECHNIQUE

A. PSDM-ESC Modulation Principle

This section introduces the modulation principle of PSDM-ESC. In a PWM-based converter, the power pulse has three degrees of freedom: frequency, phase, and duty cycle [15]. In PSDM-ESC, duty cycle is used for power modulation, while frequency and phase are used for data modulation [11], [25].

Fig. 1 depicts the block diagram of PSDM-ESC system, in which "data modulation" block often employs either FSK or PSK modulation techniques. As depicted in Fig. 1(a) and (b), the frequency or phase of power carrier $v_{\mathrm{tri}}(t)$ are modulated by baseband data to generate encoded power carrier $v_{\mathrm{c}}(t)$. For instance, in binary modulation, each bit (0 or 1) is associated with one of two unique frequency or phase states.

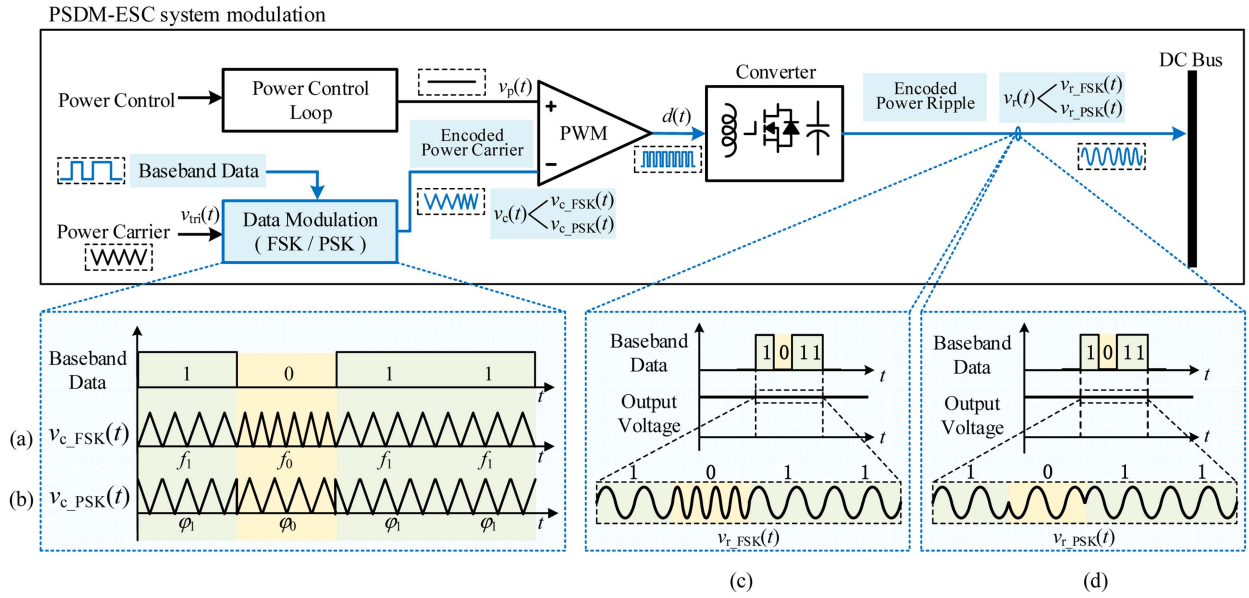


Fig. 1. Block diagram of PSDM-ESC system modulation in DCMG. (a) FSK-modulated power carrier waveform $v_{c\_FSK}(t)$. (b) PSK-modulated power carrier waveform $v_{c\_PSK}(t)$. (c) FSK-modulated power ripple waveform $v_{r\_FSK}(t)$. (d) PSK-modulated power ripple waveform $v_{r\_PSK}(t)$.

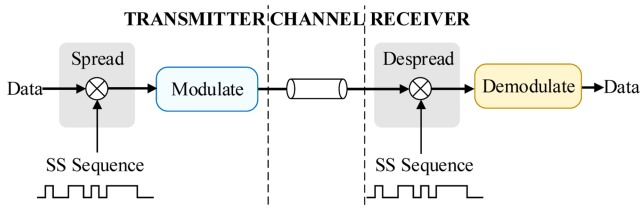


Fig. 2. Block diagram of SS communication system.

Binary FSK (BFSK) shifts the frequency of the power carrier, bit 0 selects f_0, and bit 1 selects f_1

$$v_{c\_FSK}(t) = \begin{cases} v_{tri}(2\pi f_0 t), & \text{when bit } = 0 \\ v_{tri}(2\pi f_1 t), & \text{when bit } = 1. \end{cases} \quad (1)$$

BPSK shifts the phase of a single-frequency power carrier, bit 0 keeps the reference phase, bit 1 adds a phase shift π

$$v_{c\_PSK}(t) = \begin{cases} v_{tri}(2\pi f_s t), & \text{when bit } = 0 \\ v_{tri}(2\pi f_s t + \pi), & \text{when bit } = 1 \end{cases} \quad (2)$$

where f_s is the carrier frequency for BPSK.

Fig. 1(c) and (d) illustrates the encoded power ripple $v_r(t)$ that emerges at the converter output and propagate onto the dc bus. These ripples are subsequently sampled and demodulated by other converters in the dc bus.

B. Principles of DSSS Modulation and Demodulation

DSSS is a technique that uses a pseudorandom (PN) sequence to spread the data signal over a wider bandwidth than the original baseband signal, thereby enhancing the anti-interference capability. The block diagram of an DSSS communication system is illustrated in Fig. 2.

In DSSS, bit "1" is typically represented by an *m*-sequence (e.g., {1, 0, 1, 1, 0, 0, …0, 1, 1}), while bit "0" is represented by its inverted sequence (e.g., {0, 1, 0, 0, 1, …1, 0, 0}). The elements of these sequences are referred to as chips. For autocorrelation and despreading purpose, the chip values are often mapped from binary {01}to bipolar {−1,+1} form (e.g., {1, −1, 1, 1, −1, −1, …−1, 1, 1}, enabling the correlation properties required for reliable signal recovery.

For the *m*-sequence $\{c(i)\}$, $i = 0, 1, \ldots, N-1$, of length N, the autocorrelation function $R(\tau)$ at lag τ, is given by

$$R(\tau) = \sum_{i=0}^{N-1} c(i)\, c[(i+\tau) \bmod N]\ . \quad (3)$$

At the receiver, the incoming signal is multiplied by the same spreading sequence to generate a despread signal. This despread signal can then be demodulated to recover the original baseband signal [27]. The high autocorrelation of the spreading sequence greatly reduces system interference during this decoding process, enhancing signal clarity, and robustness [28], [29].

It is important to note that the desirable autocorrelation properties of the *m*-sequence depend on its bipolar representation, as illustrated in Fig. 3(a). When a unipolar form is used instead, the autocorrelation performance degrades significantly, as shown in Fig. 3(b). This discrepancy poses challenges when integrating DSSS with FSK modulation.

C. Limitations of Applying DSSS in PSDM-ESC Technology: FSK versus PSK

The BPSK modulated signal can be expressed as

$$s(t) = A\cos(2\pi f_c t + \pi d_u(t)) = -A d_b(t)\cos(2\pi f_c t) \quad (4)$$

where A is the amplitude of the carrier, $d_u(t) \in \{0, 1\}$ is the unipolar data sequence, and $d_b(t) \in \{-1, 1\}$ is the corresponding bipolar representation. Equation (4) shows that the BPSK signal is generated by multiplying a bipolar baseband sequence

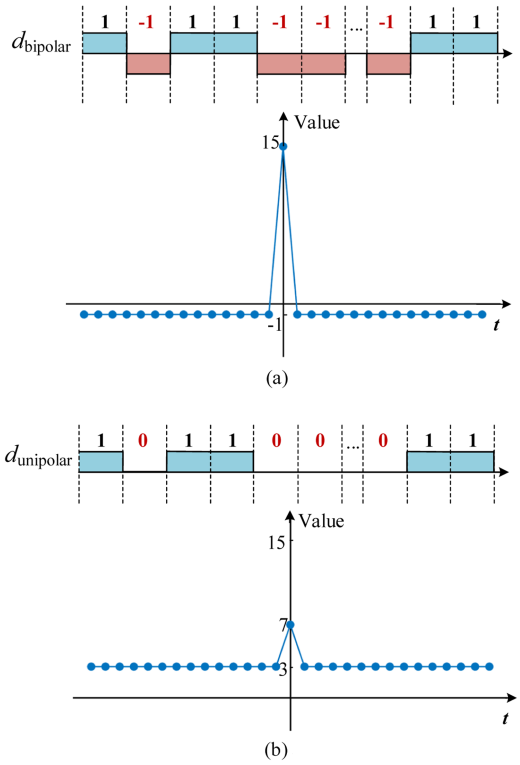


Fig. 3. Autocorrelation properties of (a) a bipolar *m*-sequence, (b) a unipolar *m*-sequence.

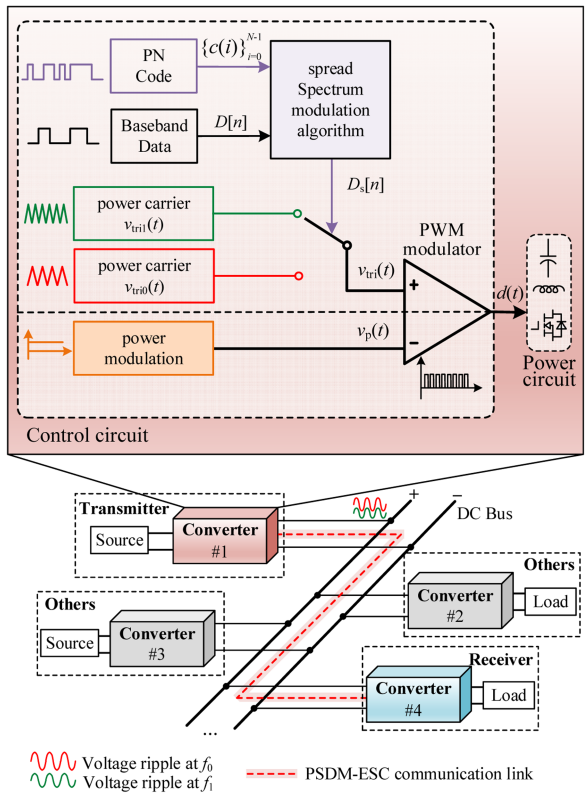


Fig. 4. Block diagram of modulation principle of SBFS-DSSS in DCMG: the single-transmitter scenario.

with the carrier waveform. At the receiver, the bipolar sequence $d_b(t)$ can be recovered through BPSK demodulation.

In BFSK modulation, the data is encoded by shifting the carrier frequency between f_1 and f_0, which can be expressed as

$$s(t) = Ad_u(t)\cos(2\pi f_1 t) + A(1 - d_u(t))\cos(2\pi f_0 t). \tag{5}$$

Equation (5) shows that the BFSK signal is formed by multiplying two complementary unipolar baseband sequences with independent carrier waveforms. At the receiver, the unipolar data sequence $d_b(t)$ cannot be directly converted to a bipolar sequence.

To address the challenges of applying DSSS to FSK signals in PSDM-ESC system, SBFS-DSSS is proposed. This technique involves converting the original FSK-modulated signals to a mid-frequency carrier, thereby enabling their transformation into BPSK-DSSS signals for more efficient despreading and demodulation. The SBFS-DSSS technique achieves a high processing gain, as analyzed in Section IV and validated through experimental results in Section V. A detailed description of the proposed method is provided as follows.

III. SBFS-DSSS Modulation and Demodulation Principles

A. Modulation Principle

This section presents the modulation principle of SBFS-DSSS in DCMG. The modulation diagram of SBFS-DSSS is shown in Fig. 4, where converter #1 serves as the data transmitter and converter #4 acts as the data receiver. The remaining converters do not participate in the communication link but emit ripple and harmonics that may interfere with communication.

In the proposed SBFS-DSSS strategy, the transmitter operates at its normal frequency f_n when not communicating. During data transmission, modulation alternates between two frequencies, f_0 and f_1, which are symmetrically offset from f_n to represent chip "0" and "1", respectively. The frequencies conform to

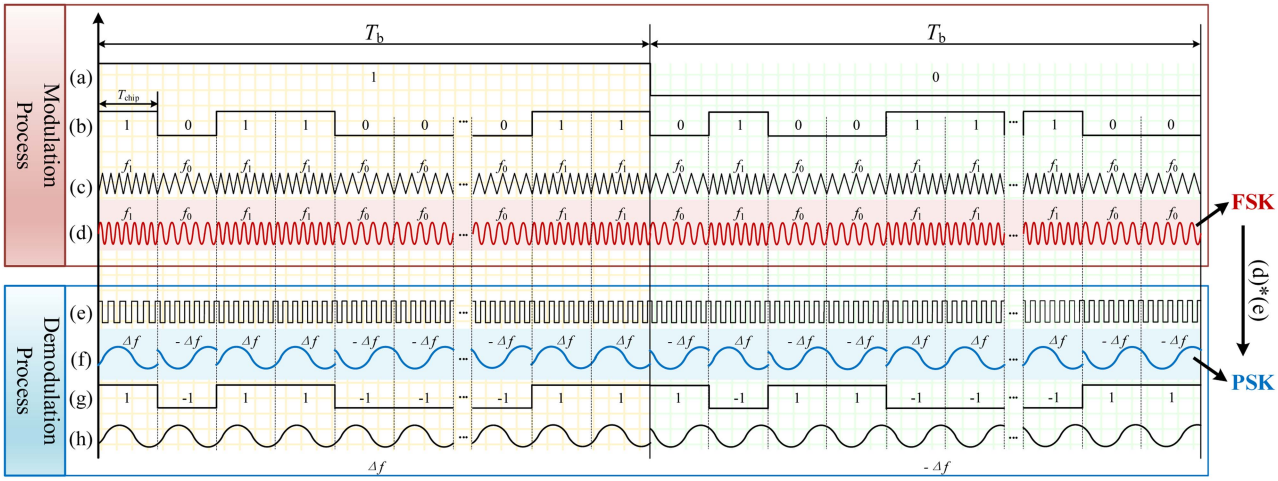
$$\begin{cases} \frac{1}{2}(f_0 + f_1) = f_n \\ n_0 / f_0 = n_1 / f_1 = T_{chip} \\ f_1 - f_n = f_n - f_0 = \Delta f \end{cases} \tag{6}$$

where T_{chip} is the duration of a chip, n_0 and n_1 are integers, ensuring that the frequencies are orthogonal in a chip period. The mean value of f_0 and f_1 equals f_n, indicating that they are symmetry about f_n with a frequency difference of Δf. This character enables the conversion of an FSK-DSSS signal into a BPSK-DSSS signal, as illustrated in Fig. 5.

During transmission at the transmitter, each bit of the baseband data sequence $D[n]$ is spread by representing it with a unipolar *m*-sequence $\{c_u(i)\}_{i=0}^{N-1}$, resulting in the spread data sequence $D_s[n]$ expressed as

$$D_s[n] = \{D[n] \oplus c_u(i)\}_{i=0}^{N-1}. \tag{7}$$

Table II illustrates the relationship between $D[n]$ and the corresponding $D_s[n]$, using an example of *m*-sequence $\{c_u(i)\} = \{1, 0, 1, 1, 0, 0, 1, 0, 1, 0, 0, 0, 0, 1, 1\}$.



(a) $D[n]$, (b)$D_s[n]$, (c) $v_{tri}(t)$, (d) $v_{PCC}(t)$, (e) $v_{ref}(t)$, (f) $v_{mix}(t)$, (g) $c_b(t)$, (h) $v_d(t)$

Fig. 5. SBFS-DSSS modulation and demodulation process.

TABLE II
MAPPING BETWEEN $D[n]$ AND $D_s[n]$

$D[n]$	$D_s[n]$
1	{1, 0, 1, 1, 0, 0, 1, 0, 1, 0, 0, 0, 0, 1, 1}
0	{0, 1, 0, 0, 1, 1, 0, 1, 0, 1, 1, 1, 1, 0, 0}

As shown in Fig. 4, according to the sequence of $D_s[n]$, the power carrier $v_{tri}(t)$ is produced by selecting either $v_{tri0}(t)$ or $v_{tri1}(t)$. Then, the gate signal $d(t)$ is generated by comparing $v_{tri}(t)$ to the power reference $v_p(t)$, which is calculated by the power control loop. Thus, the data is modulated in the output bus voltage ripple $\tilde{v}_{PCC}(t)$, and the other converters on the dc bus can receive the data by detecting the bus voltage ripple and demodulating it. The key waves of modulation are shown in Fig. 5(a)–(d). $D_s[n]$ is the spread data sequence determined by $D[n]$ in Table II. The output voltage ripple $\tilde{v}_{PCC}(t)$ has the same frequency as $v_{tri}(t)$. The communication frequencies f_1 and f_0 are chosen to be in close proximity, typically with a Δf ranging from 1 kHz to 10 kHz. Due to this narrow frequency band, the variation in ripple amplitude between f_1 and f_0 is very small. Therefore, for simplicity and clarity in the analysis, the ripple amplitude is considered to be constant at A_s in Fig. 5 and in the subsequent formula derivations.

B. Despread and Demodulation Principle

As previously discussed, PSK is compatible with DSSS and facilitates efficient despreading. Therefore, converting SBFS-modulated signals into their PSK-equivalent forms the core principle of demodulation in SBFS-DSSS systems.

Fig. 6 illustrates the demodulation diagram of SBFS-DSSS at the receiver, with the corresponding waveforms shown in Fig. 5(e)–(h). The signal $\tilde{v}_{PCC}(t)$ represents the amplified and filtered bus voltage ripple, which is first processed by a band-pass filter that passes the 40–50 kHz SBFS carrier band. An equalizer is then applied to compensate for amplitude and phase

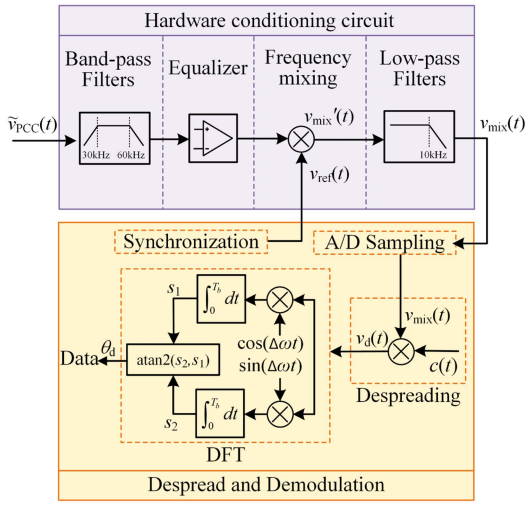


Fig. 6. Despread and demodulation principle of SBFS-DSSS.

distortions caused by the transmission impedance between the transmitter and receiver, including the effects of EMI filters. The conditioned signal is subsequently multiplied by a 45 kHz local reference $v_{ref}(t)$, generating $v'_{mix}(t)$. This mixed signal is then filtered by a low-pass filter with a 10 kHz cutoff frequency to extract a 5 kHz despread signal, denoted as $v_{mix}(t)$ in Fig. 5(f). Finally, the resulting waveform is sampled by a DSP to enable reliable despreading and demodulation.

Assuming the received ripple signal $\tilde{v}_{PCC}(t)$ is

$$\tilde{v}_{PCC}(t) = \begin{cases} A_s \sin(\omega_1 t), & \text{if } c_u(t) = 1 \\ A_s \sin(\omega_0 t), & \text{if } c_u(t) = 0 \end{cases} \tag{8}$$

where A_s is the amplitude $\omega_1 = 2\pi f_1$, $\omega_0 = 2\pi f_0$.

The local mixing signal $v_r(t)$ is

$$v_r(t) = \sin(\omega_n t + \varphi) \tag{9}$$

where $\omega_n = 2\pi f_n$, φ is the phase difference between $v_r(t)$ and $\tilde{v}_{PCC}(t)$.

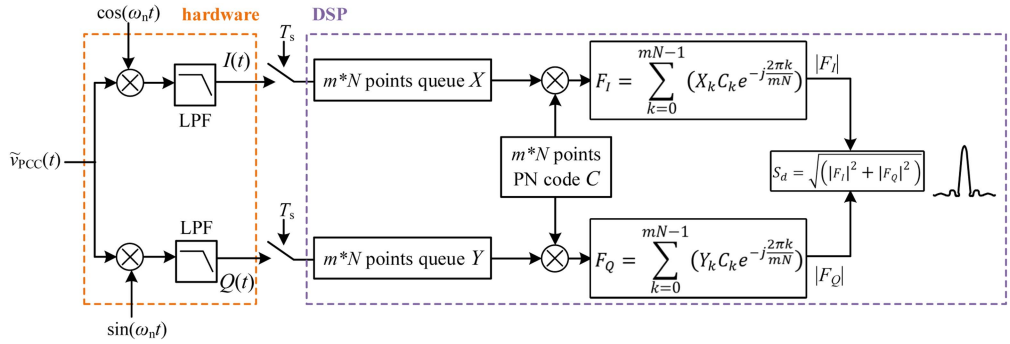


Fig. 7. Implementation of code and carrier synchronization.

The mixed signal $v'_{\mathrm{mix}}(t)$ is derived as

$$\begin{cases} v'_{\mathrm{mix1}}(t) = -\frac{A_{\mathrm{s}}}{2}\left\{\cos\left[(\omega_1+\omega_{\mathrm{n}})t+\varphi\right]-\cos\left(\Delta\omega t-\varphi\right)\right\} \\ v'_{\mathrm{mix0}}(t) = -\frac{A_{\mathrm{s}}}{2}\left\{\cos\left[(\omega_0+\omega_{\mathrm{n}})t+\varphi\right]-\cos\left(\Delta\omega t+\varphi\right)\right\} \end{cases} \tag{10}$$

where $\Delta\omega = 2\pi\Delta f$, v'_{mix0} and v'_{mix1} are the signals when transmitting chip "0" and "1", respectively.

The mixed signal $v'_{\mathrm{mix}}(t)$ consists of a low frequency Δf component and a high-frequency component. The high frequency component can be filtered after passing through an LPF, and the output can be expressed as

$$\begin{cases} v_{\mathrm{mix1}}(t) = \frac{A_{\mathrm{s}}}{2}\cos\left(\Delta\omega t-\varphi\right) \\ v_{\mathrm{mix0}}(t) = \frac{A_{\mathrm{s}}}{2}\cos\left(\Delta\omega t+\varphi\right). \end{cases} \tag{11}$$

If the transmitting side and the receiving sides are synchronized and $\varphi = \pi/2$ is satisfied, it can be seen that the SBFS signals have converted to BPSK signals. The BPSK signal $v_{\mathrm{mix}}(t)$ is then multiplied by a local bipolar *m*-sequence $c_{\mathrm{b}}(t)$ to produce a despread signal $v_{\mathrm{d}}(t)$. When $c_{\mathrm{b}}(t)$ is perfectly aligned with $D_{\mathrm{s}}[n]$, as depicted in Fig. 5(h), $v_{\mathrm{d}}(t)$ will be a sine wave with a frequency of Δf and a constant phase. In the subsequent step, the signal after despreading $v_{\mathrm{d}}(t)$ is demodulated by discrete Fourier transform (DFT) algorithm, and the phase θ_{d} is calculated and converted to original data.

The period during which the receiver performs the despreading and demodulation algorithms is referred to as the decoding stage.

C. Synchronization Principle

As discussed in the preceding analysis, the effectiveness of the decoding process relies on precise synchronization between the transmitter and receiver, including both carrier synchronization and code synchronization. Accordingly, the receiving process is divided into two distinct phases: 1) the synchronization stage and 2) the decoding stage. To facilitate synchronization, a dedicated synchronization bit is transmitted before the data frame. This section introduces a synchronization mechanism used in the SBFS-DSSS technique, which integrates code synchronization and carrier synchronization into a unified process.

Fig. 7 illustrates the synchronization process of the SBFS-DSSS technique. In this diagram, $\tilde{v}_{\mathrm{PCC}}(t)$ is defined as in (8) and can also be expressed as

$$\tilde{v}_{\mathrm{PCC}}(t) = A_{\mathrm{s}}\sin\left(\omega_{\mathrm{n}}t + c_{\mathrm{b}}(t-t_0)\Delta\omega t\right) \tag{12}$$

where $c_{\mathrm{b}}(t)$ is the bipolar *m*-sequence, and t_0 is the code delay between the transmitter and the receiver.

Two quadrature waveforms with frequency ω_{n} are generated by the local DSP, expressed as

$$\begin{cases} v_{\mathrm{rI}}(t) = \cos\left(\omega_{\mathrm{n}}t+\varphi\right) \\ v_{\mathrm{rQ}}(t) = \sin\left(\omega_{\mathrm{n}}t+\varphi\right) \end{cases} \tag{13}$$

where φ is the phase difference between the transmitter and the receiver.

$\tilde{v}_{\mathrm{PCC}}(t)$ is multiplied by the two quadrature waveforms and subsequently filtered by low-pass filters to extract the $\Delta\omega$ frequency components, denoted as $I(t)$ and $Q(t)$, respectively. The resulting signals are derived as follow:

$$\begin{cases} I(t) = \frac{A_{\mathrm{s}}}{2}\sin\left(c_{\mathrm{b}}(t-t_0)\Delta\omega t-\varphi\right) \\ Q(t) = \frac{A_{\mathrm{s}}}{2}\cos\left(c_{\mathrm{b}}(t-t_0)\Delta\omega t-\varphi\right). \end{cases} \tag{14}$$

The resulting mixed signals are passed through a low-pass filter implemented in hardware. This design reduces the signal bandwidth, enabling DSP to perform the despreading algorithm at a lower sampling rate.

Since $c_{\mathrm{b}}(t) = 1$ or $c_{\mathrm{b}}(t) = -1$, it follows that:

$$\begin{cases} \sin\left(c_b(t-t_0)\Delta\omega t\right) = c_b(t-t_0)\sin\left(\Delta\omega t\right) \\ \cos\left(c_b(t-t_0)\Delta\omega t\right) = \cos\left(\Delta\omega t\right). \end{cases} \tag{15}$$

Then, (14) can be expanded as

$$\begin{cases} I(t) = \frac{A_{\mathrm{s}}}{2}\left[\underbrace{c_{\mathrm{b}}(t-t_0)\sin\left(\Delta\omega t\right)\cos\varphi}_{\mathrm{BPSK-DSSS\ sine}} - \underbrace{\cos\left(\Delta\omega t\right)\sin\varphi}_{\mathrm{Continuous\ sine}}\right] \\ Q(t) = \frac{A_{\mathrm{s}}}{2}\left[\underbrace{\cos\left(\Delta\omega t\right)\cos\varphi}_{\mathrm{Continuous\ sine}} + \underbrace{c_{\mathrm{b}}(t-t_0)\sin\left(\Delta\omega t\right)\sin\varphi}_{\mathrm{BPSK-DSSS\ sine}}\right]. \end{cases} \tag{16}$$

It can be observed that $I(t)$ and $Q(t)$ are both composed of the superposition of a BPSK-DSSS sine wave and a continuous sine wave, with the signal intensity of the DSSS components determined by φ.

The subsequent processes are executed digitally within the DSP. The digital implementation of code and carrier synchronization, referred to as a sliding-window synchronization (SWS) method, is described below.

Initially, the signals $I(t)$ and $Q(t)$ are sampled at a sampling interval T_{s}. The sampled data within a window corresponding to one code length are stored in two queues of length $m \cdot N$, denoted as

$$\begin{cases} X = \{X_0,\ X_1, \ldots,\ X_{m\cdot N-1}\} \\ Y = \{Y_0,\ Y_1, \ldots,\ Y_{m\cdot N-1}\} \end{cases} \tag{17}$$

where m represents the length of the *m*-sequence, and N is the number of samples per chip duration.

Assuming the latest sampling time is $t = (mN-1)T_s$ with the most recent sample placed at the end, the sampled signal can be expressed as

$$\begin{cases} X_k = I\left(kT_s\right) \\ Y_k = Q\left(kT_s\right). \end{cases} \tag{18}$$

Subsequently, the queues$X$ and Y are independently multiplied by the local discrete *m*-sequence C to obtain the despread signal sequence $\hat{X}$ and $\hat{Y}$, expressed as

$$\begin{cases} \hat{X}_k = X_k\, C_k, & k = 0, 1, \ldots, mN-1 \\ \hat{Y}_k = Y_k\, C_k, & k = 0, 1, \ldots, mN-1. \end{cases} \tag{19}$$

Here, C is the discrete-time representation of $c_{\mathrm{b}}(t)$, and is expressed as

$$\begin{aligned} C &= \left\{c_{\mathrm{b}}\left(kT_s\right),\ k = 0, 1, \ldots,\ mN-1\right\} \\ &= \{C_0,\ C_1, \ldots,\ C_{mN-1}\} \\ &= \left\{\underbrace{c_0, \ldots,\ c_0}_{N}, \underbrace{c_1, \ldots, c_1}_{N}, \ldots, \underbrace{c_{m-1}, \ldots,\ c_{m-1}}_{N}\right\}. \end{aligned} \tag{20}$$

Finally, the demodulation algorithm is implemented using DFT at frequency $\Delta\omega$ to obtain the synchronization value at the specified time, expressed as

$$\begin{cases} F_I = \sum_{k=0}^{mN-1} \hat{X}_k e^{-j\frac{2\pi k}{mN}} \\ F_Q = \sum_{k=0}^{mN-1} \hat{Y}_k e^{-j\frac{2\pi k}{mN}}. \end{cases} \tag{21}$$

From (16)–(21), F_I can be derived, as (22) shown at the bottom of this page.

Based on the autocorrelation characteristics of the spreading code sequence $c(kT_s)$, it can be deduced that when $t_0 = 0$, $|F_I|$ achieves its maximum amplitude

$$F_{I(\max)} = \frac{mNA_{\mathrm{s}}}{4}\cos\varphi. \tag{23}$$

Similarly, F_Q is derived as

$$\begin{aligned} F_Q &= \sum_{k=0}^{mN-1} Y_k C_k e^{-j\frac{2\pi k}{mN}} \\ &\approx \frac{A_{\mathrm{s}}}{2}\sin\varphi \sum_{k\,=\,0}^{mN-1} \left[c_{\mathrm{b}}(kT_s)\, c_{\mathrm{b}}\left(kT_s - t_0\right)\right]\sin\left(k\Delta\omega T_s\right) e^{-j\frac{2\pi k}{mN}}. \end{aligned} \tag{24}$$

$|F_Q|$ reaches the maximum amplitude when $t_0 = 0$

$$F_{Q(\max)} = \frac{mNA_{\mathrm{s}}}{4}\sin\varphi. \tag{25}$$

Based on the abovementioned analysis, code synchronization can be achieved by identifying the peak magnitude of $|F_I|$ and $|F_Q|$. Simultaneously, carrier synchronization can be accomplished by computing the phase of the complex $F_I + jF_Q$. The phase difference between the transmitter and receiver is given by

$$\varphi = \arg\left(F_I + jF_Q\right). \tag{26}$$

In this way, code and carrier synchronization are simultaneously established. The SWS method shares similarities with the despreading and demodulation processes. However, unlike conventional demodulation, the SWS algorithm must be executed at every sampling instant, imposing substantial computational demands on the DSP.

The receiver initially operates in the synchronization stage. Once synchronization is achieved, it transitions to the decoding stage, using the synchronization point as a temporal reference. Consequently, the DSP no longer needs to perform SWS algorithm at every sampling instance, thereby significantly reducing computational overhead. Owing to the accuracy of the DSP's crystal oscillator, the local clock can be used to maintain timing for short data frames. However, for longer data frames, periodic resynchronization is necessary during the decoding stage to ensure continued alignment.

IV. Anti-Interference Performance

A. Anti-Interference Performance of SBFS-DSSS

This section analyzes the noise classifications of the TPC systems, and then evaluates the anti-interference performance of SBFS-DSSS.

In a DCMG utilizing the PSDM method, the communication data in the dc bus may be corrupted by channel noise. The noise includes the following.

1) Fundamentals and harmonics components of the converters involved in the communication link.

$$\begin{aligned} F_I &= \sum_{k=0}^{mN-1} X_k C_k e^{-j\frac{2\pi k}{mN}} = \sum_{k=0}^{mN-1} \frac{A_{\mathrm{s}}}{2} C_k \left[c_{\mathrm{b}}\left(kT_s - t_0\right)\sin\left(k\Delta\omega T_s\right)\cos\varphi\right] e^{-j\frac{2\pi k}{mN}} - \underbrace{\sum_{k=0}^{mN-1} \frac{A_{\mathrm{s}}}{2} C_k \left[\cos\left(k\Delta\omega T_s\right)\sin\varphi\right] e^{-j\frac{2\pi k}{mN}}}_{\approx 0\left(\text{ Because } \sum_{k=0}^{mN-1} C_k \approx 0\right)} \\ &\approx \frac{A_{\mathrm{s}}}{2}\cos\varphi \sum_{k=0}^{mN-1} \left[c_{\mathrm{b}}(kT_s)\, c_{\mathrm{b}}\left(kT_s - t_0\right)\right]\sin\left(k\Delta\omega T_s\right) e^{-j\frac{2\pi k}{mN}}. \end{aligned} \tag{22}$$

2) Fundamentals and harmonics components of the other converters connected to the dc bus that are not involved in the communication link.
3) Noise from the control loops of converters and their dynamic transition process.
4) Gaussian white noise from electronic components.

The primary interference affecting the communication link arises from the fundamental and harmonic components of converters, both those participating in the communication link and those that are not. The noise within the communication band of SBFS-DSSS system, which is primarily caused by the fundamental and harmonic components of other converters, as well as the sideband components generated during dynamic transitions. This noise can be modeled as bandpass random noise, confined to one of two frequency bands. It can be modeled as $n(t)$, as referred to in Chapter 3.9 of the book [30]

$$n(t) = x(t)\sin(2\pi f_c t) + y(t)\cos(2\pi f_c t) \tag{27}$$

where $x(t)$ and $y(t)$ are two independent random noise sources in baseband, f_c is the carrier frequency. The noise intensity p_n is

$$\begin{aligned} p_n &= \lim_{T\to\infty}\frac{1}{2T}\int_{-T}^{+T} n^2(t)\,dt \\ &= \lim_{T\to\infty}\frac{1}{4T}\int_{-T}^{+T}\left[x^2(t)+y^2(t)\right]dt. \end{aligned} \tag{28}$$

The noise-affected bus voltage ripple $v_{rwn}(t)$ is the sum of ideal ripple $v_{PCC}(t)$ and noise $n(t)$. Considering the noise locates within the frequency ranges [f_0-B_c,f_0+B_c], and thus, $f_c = f_0$, it can be expressed as

$$\begin{aligned} v_{rwn}(t) &= v_{PCC}(t) + n(t) \\ &= [A_s + x(t)]\sin(2\pi f_0 t) + y(t)\cos(2\pi f_0 t) \end{aligned} \tag{29}$$

where A_s is the amplitude of the ideal ripple.

The frequency mixing output after LPF is

$$\begin{aligned} v_{mix}(t) &= \frac{1}{2}A_r A_s \sin(2\pi\Delta f t) \\ &\quad + \frac{1}{2}A_r\left[x(t)\sin(2\pi\Delta f t) + y(t)\cos(2\pi\Delta f t)\right] \end{aligned} \tag{30}$$

where A_r is a scaling factor associated with the mixing process.

The signal-to-noise ratio (SNR) of the frequency mixing output is

$$\begin{cases} p_s' = \lim\limits_{T\to\infty}\frac{1}{2T}\int_{-T}^{+T}\frac{1}{4}A_r{}^2A_s{}^2[1-\cos(4\pi\Delta f t)]dt = \frac{1}{4}A_r{}^2p_s \\ p_n' = \lim\limits_{T\to\infty}\frac{1}{2T}\int_{-T}^{+T}\frac{1}{4}A_r{}^2n^2(t)\,dt = \frac{1}{4}A_r{}^2p_n \\ (S/N)_{mix} = \frac{\frac{1}{4}A_r{}^2p_s}{\frac{1}{4}A_r{}^2p_n} = \frac{p_s}{p_n} = (S/N)_{rwn} \end{cases} \tag{31}$$

where p_s' is the signal power after mixing, p_n' is the noise power after mixing, p_s is the signal power of the ideal ripple, and p_n is the noise power of the system before mixing. $(S/N)_{mix}$ is the SNR of the mixed signal, and $(S/N)_{rwn}$ is the SNR of the bus voltage ripple.

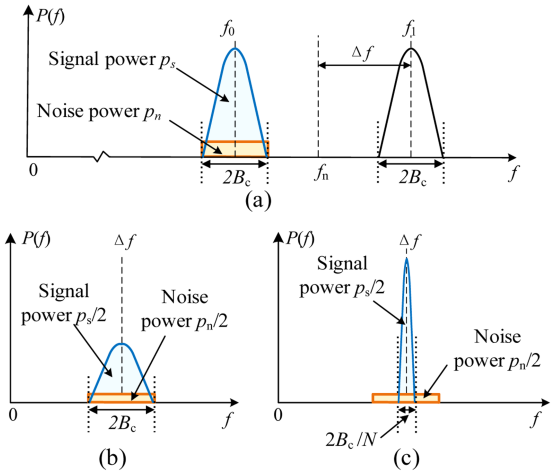


Fig. 8. Power spectral density of (a) received ripple signal, (b) mixed signal, and (c) despread signal.

After the mixing procedure, the SNR remains unchanged, as shown in Fig. 8(a) and (b). Besides, if the noise is within the frequency ranges [f_1-B_c, f_1+B_c], the conclusion is the same. Following this, the despreading algorithm is applied. The processing gain G_p, defined as the ratio of the signal bandwidths after and before DSSS, is defined as

$$G_p = W/B = N_s = R_c/R_b \tag{32}$$

where W and B are the signal bandwidths after and before DSSS, N_s is the length of the *m*-sequence, and R_c and R_b are the code rate of the *m*-sequence and baseband data, respectively.

The processing gain is the key factor in improving SNR [31], which can also be expressed as

$$G_p = \frac{(S/N)_{out}}{(S/N)_{in}} \tag{33}$$

where $(S/N)_{out}$ is the SNR of the processed signal after DSSS and $(S/N)_{in}$ is the SNR of the unprocessed signal before DSSS.

As shown in Fig. 8(c), the SNR of the despread signal is greatly improved. In this article, $N_s = 15$, so the processing gain of the SBFS-DSSS system is $G_p = 15$.

In summary, the SBFS strategy mitigates the interference through three sequential processes. First, components outside the communication band are attenuated by a band-pass filter prior to the frequency mixing stage. Second, the mixed signals are further processed by a low-pass filter, ensuring that only frequency components near the communication band are sampled by the DSP. Third, for noise components within the communication band that are sampled, the despreading process effectively randomizes and suppresses their energy, thereby significantly improving the SNR of the communication signal.

B. Impact of Power Conversion on Communication

The power conversion process is another concern that may affect communication. In a converter with closed-loop control, the transient response of the duty cycle can be modeled as a

damped oscillation [25], which is expressed as

$$d(t) = D + Ae^{-\beta t}\sin(\omega_d t) \tag{34}$$

where D is the steady-state duty cycle, A is the initial amplitude, β is the damping coefficient, and ω_d is the angular frequency of oscillation. These parameters are determined by the topology and power control loop.

For a square wave with amplitude $V = 1$, duty cycle d, and angular frequency f_c, the fundamental component at frequency f_c is given by

$$v_1(t) = \frac{4}{\pi}\sin(\pi d)\sin(2\pi f_c t) = \frac{4}{\pi}\sin(\pi d)\sin(\omega_c t). \tag{35}$$

Thus, in the transient response as in (34), the fundamental component at frequency ω_c can be expressed as

$$v_1(t) = \frac{4}{\pi}\sin\left[\pi\left(D + Ae^{-\beta t}\sin(\omega_d t)\right)\right]\sin(\omega_c t). \tag{36}$$

It is clear that $v_1(t)$ is an envelope modulated wave with carrier frequency ω_c. The envelope represents the information signal after its spectrum has been shifted to the baseband.

In steady state, the fundamental component $v_{\text{steady}}(t)$ is

$$v_{\text{steady}}(t) = \frac{4}{\pi}\sin(\pi D)\sin(\omega_c t). \tag{37}$$

The perturbation of the fundamental component is

$$\Delta v_1(t) = v_1(t) - v_{\text{steady}}(t)$$

$$= \frac{4}{\pi}\left\{\sin\left[\pi\left(D + Ae^{-\beta t}\sin(\omega_d t)\right)\right] - \sin(\pi D)\right\}\sin(\omega_c t). \tag{38}$$

The difference between the envelope of the perturbation response and the steady-state wave can be considered as noise and is expressed as

$$\Delta V_{\text{envelope}}(t) = \frac{4}{\pi}\left\{\sin\left[\pi\left(D + Ae^{-\beta t}\sin(\omega_d t)\right)\right] - \sin(\pi D)\right\}. \tag{39}$$

This perturbation noise can be considered as interference introduced into the code by the transmitter. It remains unchanged during the demodulation and despreading process and cannot be filtered out. To assess the impact of the noise, a set of parameters is assumed for the practical circuit, and the SNR is simulated accordingly.

For a practical circuit, $A = 0.4$, $D = 0.49$, $\beta = 1000\,\text{s}^{-1}$, $\omega = 1000\pi\text{rad/s}$, $\varphi = 0$. A transient begins at $T_1 = 6\text{ms}$ is depicted in Fig. 9.

During the code duration T_{code}, starting at T_i, the disturbance $\Delta v(t)$ is integrated as

$$\Delta V_{\text{code}}(i) = \int_{T_i}^{T_i+T_{\text{code}}} \frac{4}{\pi}\left\{\sin\left[\pi\left(D + Ae^{-\beta t}\sin(\omega_d t)\right)\right] - \sin(\pi D)\right\}. \tag{40}$$

The ripple amplitude during the transient process is

$$v(i) = \sin(\pi D) + \Delta V_{\text{code}}(i)/T_{\text{code}}. \tag{41}$$

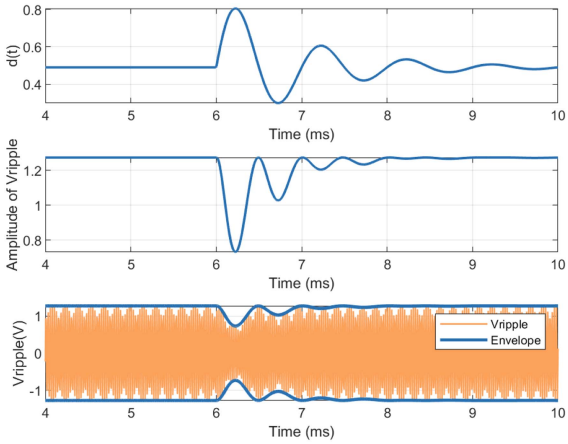


Fig. 9. Duty cycle variation $d(t)$ when $A = 1$ and $\beta = 1000\,\text{s}^{-1}$.

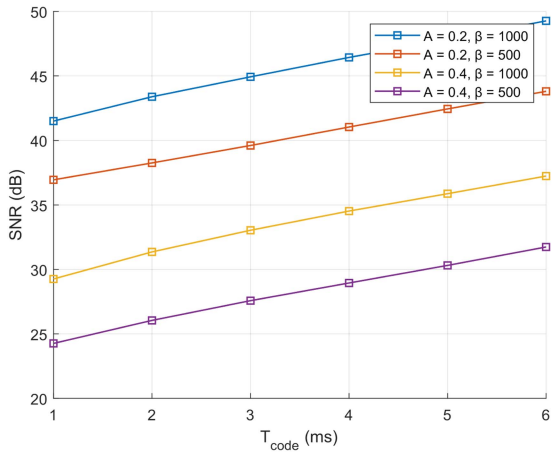


Fig. 10. SNR for different chip lengths.

The starting point of the code is randomly selected 1000 times within the total duration T, resulting in 1000 values of $v(i)$ being calculated. The mean a and variance $\sigma_n{}^2$ of $v(i)$ are then calculated to determine the SNR

$$\text{SNR} = \frac{a^2}{2\sigma_n{}^2}. \tag{42}$$

Fig. 10 shows the SNRs with varying code lengths. It is evident that increasing the code length enhances the SNR. The SBFS-DSSS technique, which extends code duration using spreading codes, offers better anti-interference performance during power-affected communication. However, longer code durations naturally reduce the communication rate.

In conclusion, the theoretical framework outlined in Sections III and IV has elucidated both the SBFS-DSSS modulation technique and its corresponding anti-interference. Section V will demonstrate how these methods perform under real operating conditions, thereby confirming the practical feasibility and robustness of the proposed system.

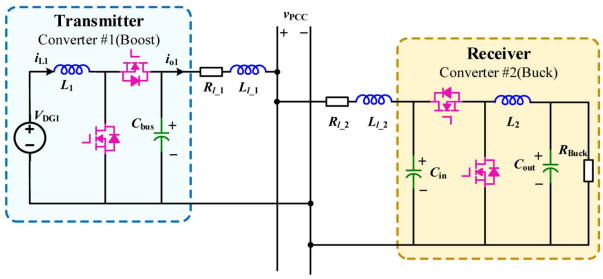


Fig. 11. Structure of the experimental platform.

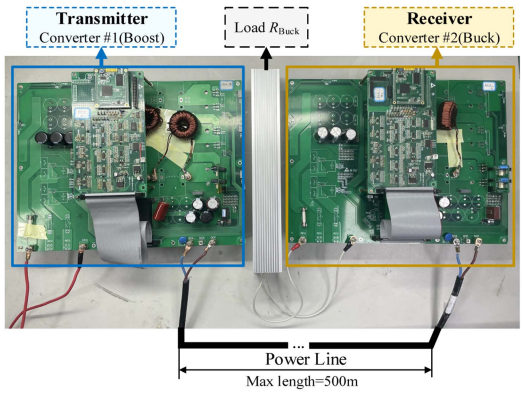


Fig. 12. Photo of the experimental platform.

TABLE III
SYSTEM PARAMETERS OF EXPERIMENTAL PLATFORM

Parameters	Name	Value
Input voltage of converter #1	V_{Boost}	200 V
Reference voltage of dc bus	V_{bus}	380 V
Output voltage of converter #2	V_{Buck}	200 V
Load resistance of converter #2	R_{l}	40 Ω
Output capacitor of converter #1	C_{bus}	100 μF
Input capacitor of converter #2	C_{in}	50 μF
Output capacitor of converter #2	C_{out}	300 μF
Inductors of converter #1 and #2	L_1, L_2	2 mH

V. EXPERIMENTAL VERIFICATION

A. Experimental Platform Design

To verify the correctness of theoretical analysis, a dc system with two 1 kW converters, which employs SBFS-DSSS modulation for communication, is constructed. The system structure is shown in Fig. 11 and the prototype photo is shown in Fig. 12. The experimental platform consists of a transmitter converter #1 using Boost topology and a receiver converter #2 using Buck topology. The parameters are shown in Table III. The selected parameters fulfill the accuracy requirements of SBFS-DSSS demodulation and the power quality standards.

B. Data Transmission Experiments

The experiment is conducted with the parameters shown in Table IV. The switching frequency without communication is set at $f_{\text{n}} = 45$ kHz. In communication, the switching frequency is shifted between 40 kHz and 50 kHz, with a 5 kHz band symmetrically around 45 kHz. The filter design is based on 40 kHz, which is the lowest one of the transmitter converter's switching frequencies.

TABLE IV
SBFS-DSSS COMMUNICATION PARAMETERS

Parameters	Name	Value
Switching frequency	f_{n}	45 kHz
Low frequency	Δf	5 kHz
Communication frequencies	f_0, f_1	40 kHz, 50 kHz
Communication baud rate	R_{B}	166.7 bps
Chip period	T_{chip}	400 μs
Number of chips	N_{chip}	15
Code period	T_{b}	6 ms
m-sequence	$\{c(i)\}_{i=0}^{14}$	{1, 0, 1, 1, 0, 0, 1, 0, 1, 0, 0, 0, 0, 1, 1}
Number of data	N_{data}	8
Data frame length	T_{frame}	54ms

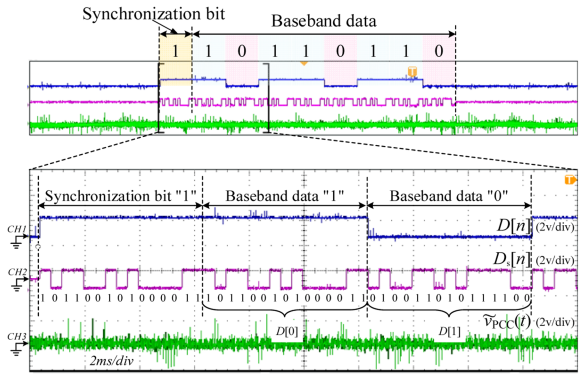


Fig. 13. Data transmission waveforms of SBFS-DSSS modulation.

In the experiment, a data frame consisting of a synchronization bit and eight data bits ("10110110") is transmitted. The waveforms when transmitter sends data are shown in Fig. 13, where $D[n]$ is the transmitted data, $D_{\text{s}}[n]$ is the spread sequence, and $\tilde{\text{v}}_{\text{PCC}}$ is the bus voltage ripple. It can be observed that the switching frequency changes are reflected on the dc microgrid bus voltage ripple $\tilde{\text{v}}_{\text{PCC}}$. Frequency fluctuations lead to a 4.5% variation in ripple amplitude and cause less than a 0.2% change in conversion efficiency. The average frequency is nearly unchanged. Such minimal deviations fall well within the standard DCMG limits, confirming that power conversion and efficiency remain almost unaffected during communication.

C. Synchronization and Data Decoding Experiments

The effectiveness of the synchronization method is verified. Two quadrature waveforms, as defined in (13), are generated by the DSP and multiplied with $\tilde{v}_{\text{PCC}}(t)$. The resulting signals are then filtered using low-pass filters, and the filter outputs are subsequently sampled by DSP for analysis. According to the SWS method, a sliding window of duration T_{b} is applied. The sampled data within this window is first multiplied by the local m-sequence $D_{\text{d}}[n]$, followed by a DFT, yielding the amplitude

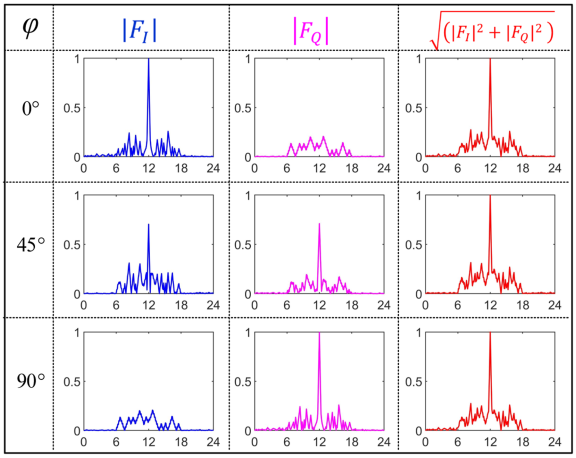


Fig. 14. Normalized magnitude of $|F_I|$, $|F_Q|$, and $\sqrt{(|F_I|^2+|F_Q|^2)}$ in different φ (x plot of each figure is "time(ms)", the y plot of each figure is "normalized magnitude").

$|F_I|$ and $|F_Q|$. In the process of sliding window, when $D_{\mathrm{d}}[n]$ and $D_{\mathrm{s}}[n]$ are completely aligned, $|F_I|$ and $|F_Q|$ reach their peak values. Otherwise, $|F_I|$ and $|F_Q|$ remain significantly low.

The experiment is conducted with only one synchronization bit transmitted. The phase offset between the transmitter and receiver is preset, and the despreading and DFT results are transmitted to a PC and normalized in MATLAB, as shown in Fig. 14. The figure shows the despreading and DFT results of $|F_I|$, $|F_Q|$ and $\sqrt{(|F_I|^2+|F_Q|^2)}$ under different phase offset φ between the transmitter and receiver. It can be observed that as φ varies, the normalized magnitude of $\sqrt{(|F_I|^2+|F_Q|^2)}$ remains nearly constant, while $|F_I|$ and $|F_Q|$ vary with φ. This confirms the validity of the synchronization mechanism.

In the decoding stage, the process of frequency mixing is shown in Fig. 15. To clearly observe the 40 kHz and 50 kHz ripple components, Fig. 15 is obtained under conditions where the Boost converter is connected to a purely resistive load. The received signal $\tilde{v}_{\mathrm{PCC}}$ is multiplied with the local mixing signal $v_{\mathrm{ref}}(t)$ and filtered by a low-pass filter to extract the expected signal $v_{\mathrm{mix}}(t)$, which is a phase-continuous sine wave with a frequency of 5 kHz. Specifically, enlarging the waveforms around the switching time t_0 of two chips, a π phase jump between two T_{chip} periods can be observed.

The demodulation result is shown in Fig. 16, where the recovered data matches the transmitted data. The observed communication delay is approximately 6 ms, which corresponds to the duration of one code sequence T_{b}.

D. Comparison of Anti-Interference Performance and Long-Line Transmission

To evaluate the anti-interference performance under long-line transmission conditions, a long transmission line is incorporated into the experimental system. The equivalent model of the long-line system, as shown in Fig. 17, includes an EMI filter.

Since the 45 kHz mixing reference and low-pass filter reduce the ripple of Buck, just the transmitter converter ripple is considered. The signal transfer function from the output voltage of the

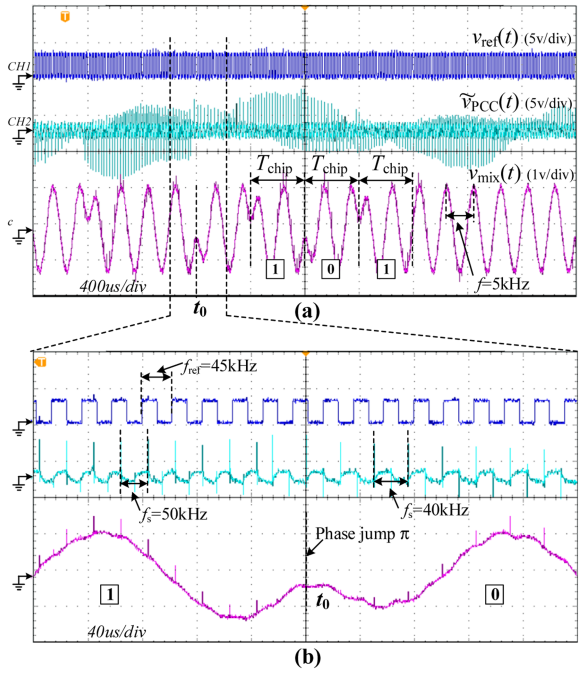


Fig. 15. SBFS-DSSS technique data demodulation process. (a) Multiplier waveform. (b) Partial enlarged view.

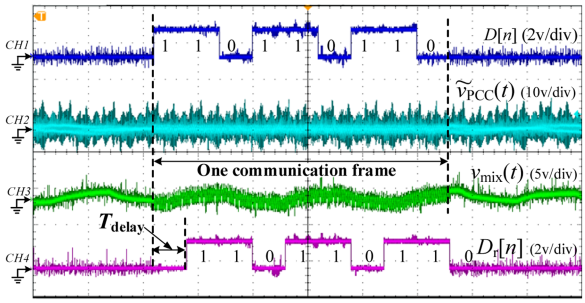


Fig. 16. Demodulation result.

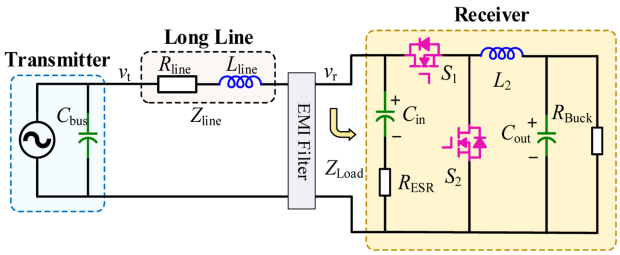


Fig. 17. Equivalent model for a long line.

transmitter (Boost converter) to the input voltage of the receiver (Buck converter) is

$$H(s)=H_{\mathrm{line}}(s)\,F_{\mathrm{EMI}}(s). \tag{43}$$

The effect of the EMI filter can be compensated by the equalizer, therefore, the model primarily focuses on the impact of the transmission line and neglects the influence of the EMI filter. The signal attenuation can be expressed as

$$H(s)=H_{\mathrm{line}}(s)=\frac{Z_{\mathrm{Load}}(s)}{Z_{\mathrm{line}}(s)+Z_{\mathrm{Load}}(s)} \tag{44}$$

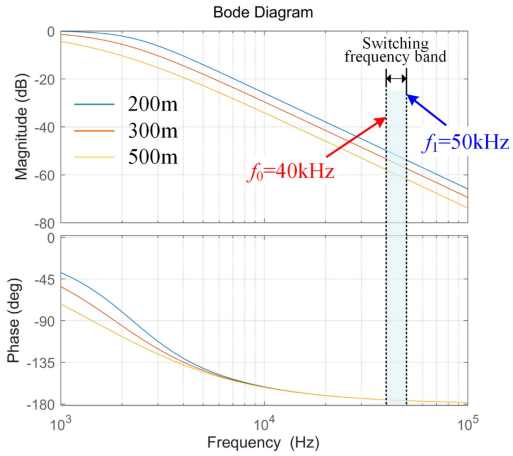


Fig. 18. Bode plot of the transfer function.

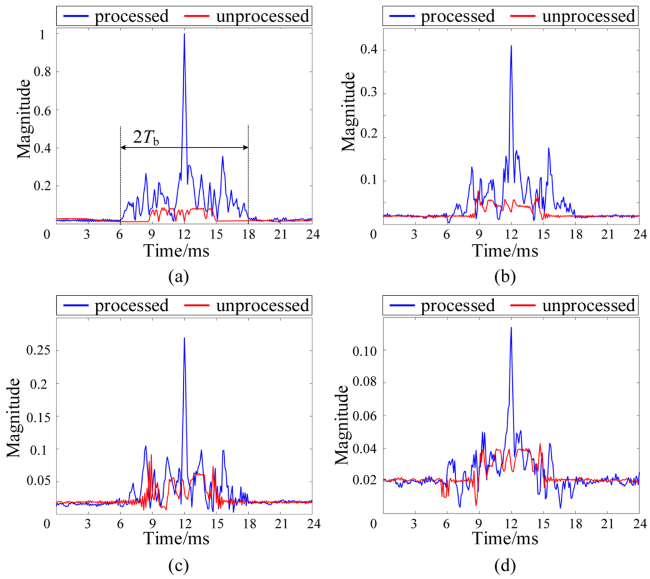


Fig. 19. Normalized sliding window despreading results for the transmission of a single bit over power lines with a length of (a) 0 m, (b) 200 m, (c) 300 m, and (d) 500 m.

$$Z_{\text{line}}(s) = R_{\text{line}} + L_{\text{line}}s. \tag{45}$$

At the switching frequency band, the voltage ripple primarily passes the input capacitor C_{in}. Consequently, the input impedance may be approximated as

$$Z_{\text{Load}}(s) = \frac{1}{sC_{\text{in}}} + R_{\text{ESR}} \tag{46}$$

where R_{ESR} is the ESR of the input capacitor C_{in}.

The bode plot of the transfer function $H(s)$ is shown in Fig. 18. The transmission line is a stranded copper wire with 4 mm^2 cross-sectional area, the equivalent resistor is about 11.2 Ω/km and inductance is about 480 μH/km. The bode plot illustrates that long-line transmission reduces the strength of the high frequency carrier signal. If the noise remains unchanged, SNR is consequently decreased.

Fig. 19 shows the normalized results of sliding window despreading and predespreading signal amplitudes for various power line lengths l_{p}. To highlight SNR, only one bit is transmitted during [6 ms, 12 ms]. Predespreading amplitudes are calculated using a sliding DFT with a window equal to the chip duration. [0, 6 ms] and [18 ms, 24 ms] represent noise-only intervals. The average amplitudes in these regions, denoted N_{out} and N_{in}, reflect despread and unprocessed noise powers, respectively. [6 ms, 18 ms] is the data region, lasting for $2T_{\text{b}}$. The maximum amplitudes in this region, S_{out} and S_{in}, indicate the power of the despread and unprocessed signals, respectively.

From Fig. 19(a), when $l_{\text{p}} = 0$ m, the processing gain G_{p} can be derived from (33) as

$$(G_{\text{p}})_{\text{SBFS}} = \frac{(S/N)_{\text{out}}}{(S/N)_{\text{in}}} = 14.13 = 11.5 \text{ dB}. \tag{47}$$

Fig. 19 shows that as l_{p} increases, the signal amplitude decreases rapidly, which would result in a high communication error rate. However, the SNR of the despread signal remains sufficiently high for reliable detection. Table V compares the processing gain G_{p} of SBFS-DSSS with conventional BFSK at four line lengths. Even at 500 m, SBFS-DSSS remains a significant 6.28 dB, compared to FSK's 1.89 dB. The experimental results demonstrate that the SBFS-DSSS technique enhances anti-interference performance and offers advantages in long-line transmission.

Additionally, an experiment is conducted to assess the communication dependability of SBFS-DSSS by changing the load during communication. The waveforms of the transmitted data, the received signal $\tilde{v}_{\text{PCC}}(t)$, the processed signal $v_{\text{mix}}(t)$, and the demodulated data are depicted in Fig. 20. It can be observed that a sudden change of load has a significant effect on the magnitude of output voltage ripple $\tilde{v}_{\text{PCC}}$, but does not lead to interrupt in communication. Fig. 21 shows the normalized sliding window despreading results during the sudden change. The autocorrelation property of the despreading results remain almost unaffected during the sudden voltage fluctuation, which

TABLE V
COMPARISON OF PROCESSING GAIN UNDER DIFFERENT LINE LENGTHS

Modulation	G_{p}(dB)			
	$l_{\text{p}} \approx 0$ m	$l_{\text{p}} = 200$ m	$l_{\text{p}} = 300$ m	$l_{\text{p}} = 500$ m
SBFS	11.50	9.20	7.35	6.28
BFSK	3.77	3.09	2.28	1.89

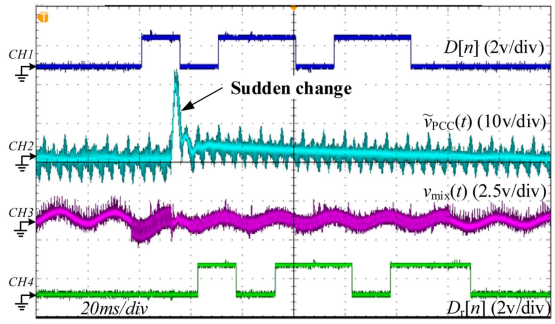


Fig. 20. Waveforms of communication during a sudden change.

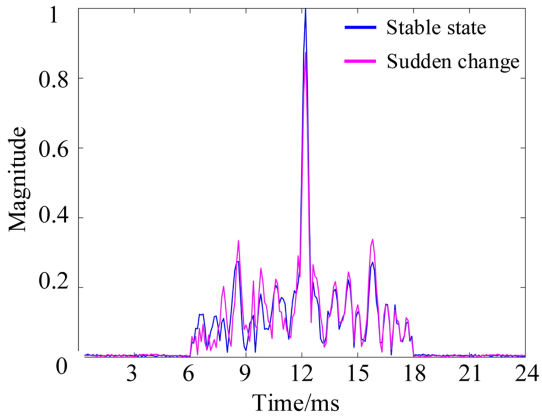


Fig. 21. Normalized sliding window despreading results during a sudden change.

demonstrates the reliability of SBFS-DSSS in maintaining anti-interference performance.

VI. Conclusion

This article proposes a PSDM-ESC modulation employing SBFS-DSSS technique in dc microgrids. By selecting the appropriate SBFS frequencies, the information carrier frequency is not only shifted away from the normal power frequency to minimize interference but also ensures that the power conversion efficiency of the converter remains unaffected during communication. DSSS is implemented by selecting the shifting pattern of SBFS frequencies based on the PN sequence. The anti-interference performance is significantly enhanced due to the autocorrelation properties of the PN sequence. Eventually, a 1 kW DCMG platform is constructed to demonstrate the effectiveness of this method. The performance of SBFS-DSSS is evaluated and compared with conventional BFSK modulation. Results show a significant improvement in processing gain and anti-interference capability, particularly under long-line conditions. The proposed SBFS-DSSS technique achieves a processing gain of 11.5 dB, and maintains reliable communication performance in transmission lines up to 500 m. This method offers a solution for talkative power converters in DCMG.

However, the data rate of this method is low because the spectrum of the carrier signal is constrained to a very narrow band in order to prevent switching noise. This design makes it particularly suitable for applications requiring reliable communication at low data rates, such as equipment identification and remote meter reading, but not suitable for control applications that demand high-speed communication links. Additionally, the method requires the converter to operate in continuous mode, as it does not support discontinuous modes, such as burst or skip-cycle modes. In high-SNR scenarios, alternative modulation techniques, such as multilevel FSK, quadrature amplitude modulation, or orthogonal frequency division multiplexing, can be employed in PSDM systems to enhance data rates and achieve higher spectral efficiency. Though their implementation requires careful consideration of power converter constraints. Furthermore, adaptive modulation strategies could be developed to dynamically adjust modulation parameters based on SNR levels, optimizing data throughput across varying channel conditions.

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