Partial Power Converter Based on the Gate Voltage Self-Balancing Supercascode Power Switch

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***Abstract*—To simplify the topology and control under medium-voltage dc input, a novel partial power dc transformer (DCX) based on gate voltage self-balancing supercascode power switches (GVSB-SCPSs) is proposed. The front stage of DCX is constructed by GVSB-SCPSs, which realize the medium-voltage dc input of a single module and a fixed voltage ratio. The closed-loop stabilized voltage output is achieved through the proposed partial power processing circuit, which handles a small portion of the output power. In the proposed converter, the high-frequency operation process of GVSB-SCPSs and the unique gate switching pattern during the dead time are analyzed. Based on this, the boundary condition of soft switching in the proposed converter is derived. Under this condition, the loss of the proposed converter is analyzed, and the dead time is optimally designed. Based on the proposed topology, a partial power converter experimental prototype is built. The prototype is constructed through the designed GVSB-SCPSs, which have been tested at 10 kV and demonstrate outstanding switching characteristics. The experimental results of the partial power converter prototype show that all the GVSB-SCPSs realize a ZVS soft switch at 4 kV, 20 kHz. Furthermore, the closed-loop stabilized voltage output is achieved, verifying the feasibility of the proposed PPP and DCX circuit.**

***Index Terms*—DC transformer (DCX), dead time, partial power processing (PPP), soft switch, supercascode power switch (SCPS).**

I. Introduction

POWER electronic converters for medium-voltage (MV) are widely used in MVdc distribution networks, undersea dc power distribution systems, high-speed train power systems, etc., [1], [2], [3], [4], [5], [6], [7], [8], [9]. However, the limited rated voltage of devices makes dealing with high input voltages difficult, while the topology and control of converters become complex. Utilizing devices in series to construct converters becomes the most direct and effective way to solve this problem [10], [11], [12], [13], [14].

Received 3 June 2025; revised 23 August 2025; accepted 23 September 2025. Date of publication 30 September 2025; date of current version 23 December 2025. This work was supported in part by the National Natural Science Foundation of China under Grant 52127901 and Grant 52407204. Recommended for publication by Associate Editor J. Lam. *(Corresponding author: Zongjian Li.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3616120.

Digital Object Identifier 10.1109/TPEL.2025.3616120

However, the issue of voltage imbalance exists in the series-connected devices, which needs various active and passive drive methods [15], [16]. Compared with other drive methods, the supercascode driver is very attractive due to its simple control, only one driving signal, and easy to achieve voltage balancing [17], [18], [19], [20], [21], [22], [23]. According to the device composition, supercascode power switches (SCPSs) can be classified into two primary configurations: the MOSFET and JFET hybrid configuration, as well as the fully normally-off device configuration.

For the MOSFET and JFET hybrid configuration, a supercascode topology is proposed in [18], where a 5-kV SCPS is constructed using five JFETs and one low-voltage MOSFET. The balancing network in [18] is improved by replacing the bottom low-voltage MOSFET with a SiC MOSFET in [19], enabling uniform voltage distribution across all devices. The SCPS constructed in [19] is further tested in boost and DAB converters in [20]. Another supercascode topology and control of the device voltage distribution are proposed in [21], while the overvoltage issue on the top JFET is analyzed.

For the fully normally-off device configuration, there is a better static voltage balance due to smaller leakage current than JFETs, and a 7.2-kV SuperMOS is reported in [22]. However, due to the problem of gate voltage drop in normally-off devices, the number of devices in series is limited. To solve the problem, a supercascode topology with gate voltage adaptive closed-loop regulation is proposed in [23], which also suppresses gate voltage overshoots and further expands the number of devices in series.

Both configuration topologies of SCPSs show outstanding switching characteristics and potential for MV applications, especially the topology proposed in [23], where the gate voltage closed-loop regulation is impressive. However, the devices in SCPSs have a unique switching process, which has a significant impact on the soft-switching realization of converters in the dead time. Due to limited research on SCPS-based converters, it is necessary to study the soft-switching realization methods and operation characteristics further.

Utilizing SCPSs to construct resonant converters not only simplifies the topology and control in MV conversion, but also achieves high efficiency [24]. The resonant converters achieve the highest efficiency when operating at the series resonant point and are widely used as DC transformers (DCXs) [25], [26], [27]. However, the output voltage of DCXs cannot be adjusted.

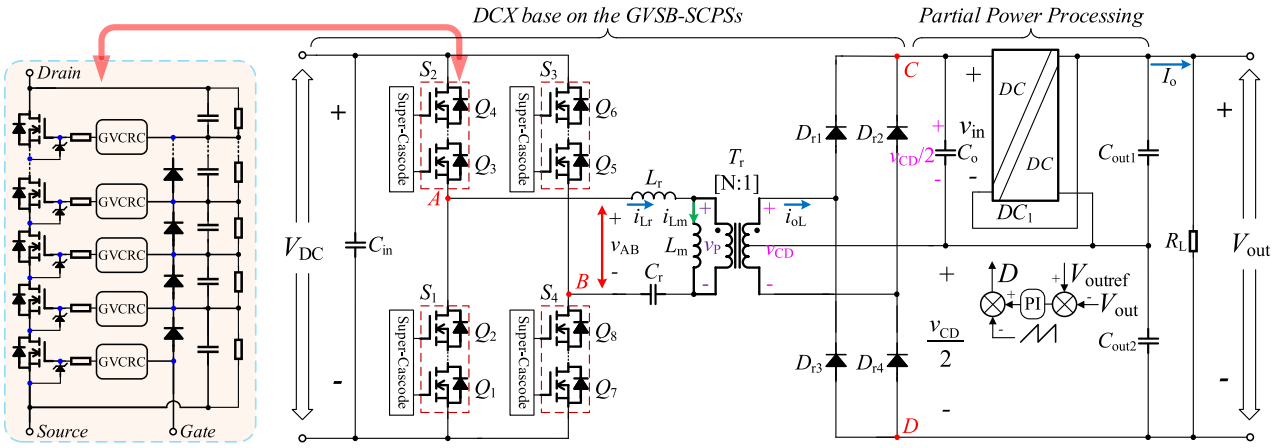

Fig. 1. Proposed PPP converter topology based on GVSB-SCPS.

To solve this problem, a two-stage scheme is proposed [26], [27].

The regulation of output voltage is realized by a front or post regulator module added. However, the added regulator module needed to handle the full load power, resulting in a complex circuit and heat dissipation design, while sacrificing converter efficiency.

This article proposes a novel partial power converter based on the GVSB-SCPSs and the proposed partial power processing (PPP) circuit. The front stage of the DCX employs the GVSB-SCPSs to achieve direct high-voltage input, which simplifies the topology and control of MVDC converters. The post stage of the DCX realizes stable voltage output and high efficiency in a wide input voltage range through a proposed PPP circuit.

The rest of this article is organized as follows. In Section II, the working principle of the proposed topology, high-frequency operation process of the GVSB-SCPSs, unique gate switching pattern during the dead time, soft-switching conditions of the proposed converter, and the losses combined with the dead time of the proposed converter are analyzed. In Section III, the gate voltage self-balancing results and switching performance of the constructed 10 kV GVSB-SCPS are introduced. Based on this, a partial power converter prototype is built, and the soft-switching test, PPP test, and operation test are carried out. The experimental results verify the effectiveness and feasibility of the proposed topology and analysis. Finally, Section IV concludes the article.

II. Topology and Operation Principle

A. Working Principle of the Proposed Partial Power Converter

Fig. 1 shows the proposed partial power converter topology based on the GVSB-SCPSs and the proposed PPP circuit. V_{DC}, v_{CD}, V_{out}, and I_o are the input voltage, the output voltage of the front stage, the output voltage of the post stage, and the output current, respectively. v_{AB} and i_{Lr} are the resonant voltage and resonant current. v_P, i_{Lm}, and i_{oL} are the primary voltage, exciting current, and secondary current of the transformer T_r, respectively. The turns ratio of T_r is N:1. v_{in} is the input voltage of the dcdc module DC_1. R_L is the load. D is the duty of DC_1.

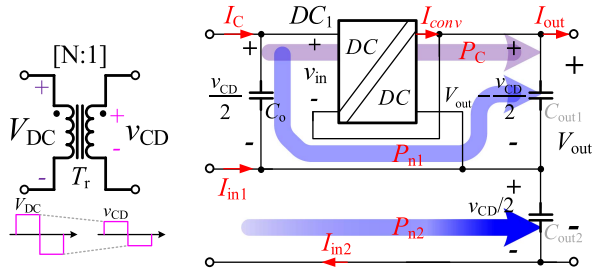

Fig. 2. Simplified schematic of the proposed topology.

The front stage of the proposed converter is a full-bridge *LLC* topology operating at the resonant frequency, acting as a DCX to achieve a fixed voltage ratio. The post stage is the proposed PPP circuit, which realizes the stable output of the converter. Fig. 2 shows the simplified schematic of the proposed topology. P_C is the active power processed by DC_1, and $P_{n1}+P_{n2}$ is the active power unprocessed by DC_1. Since the front-stage *LLC* operates at the resonant frequency point, the output voltage of T_r is determined by the V_{DC}/N. In addition, the voltages across C_o and C_{out2} are clamped at $v_{\mathrm{CD}}/2$, which equals the $V_{\mathrm{DC}}/(2N)$. According to the configuration shown in Fig. 2, there are

$$\begin{cases} v_{\mathrm{in}} = v_{\mathrm{CD}} - V_{\mathrm{out}} \\ V_{\mathrm{out}} = \frac{v_{\mathrm{CD}}}{2}(1+M_1) \end{cases} \tag{1}$$

where M_1 is defined as $(V_{\mathrm{out}}\text{-}v_{\mathrm{CD}}/2)/(v_{\mathrm{CD}}/2)$. The voltage gain M_C of DC_1 is defined as $(V_{\mathrm{out}}\text{-}v_{\mathrm{CD}}/2)/(v_{\mathrm{in}})$, which is related to D.

Combined with (1), the relationship between M_1 and M_C can be obtained by

$$M_1 = 2M_C \cdot (1 - NM) \tag{2}$$

Where M is the total gain of the converter and is defined as $V_{\mathrm{out}}/V_{\mathrm{DC}}$. By combining (1) and (2), the relationship between M and M_C can be obtained

$$M = \frac{V_{\mathrm{out}}}{V_{\mathrm{DC}}} = \frac{1+M_1}{2N} \Rightarrow M = \frac{1+2M_C}{2N(1+M_C)}. \tag{3}$$

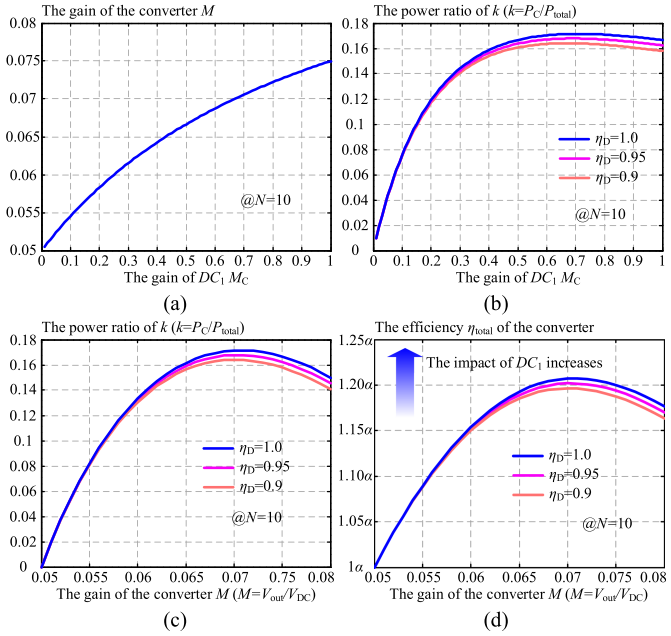

Fig. 3. Relationship between variables when $N = 10$. (a) M and M_C. (b) k and M_C. (c) k and M. (d) η_{total} and M.

Assuming that the efficiency of DC_1 is η_D, the relationship between P_C and P_C+P_{n1} can be obtained by

$$k_1 = \frac{P_C}{P_C + P_{n1}} = \frac{\eta_D v_{\text{in}}}{\eta_D v_{\text{in}} + (V_{\text{out}} - v_{\text{CD}}/2)}. \tag{4}$$

Combined with (1), (3), and (4), the relationship between P_C and P_C+P_{n1} in Fig. 2 is

$$k_1 = \frac{2\eta_D (1 - NM)}{2\eta_D (1 - NM) + (2NM - 1)} = \frac{\eta_D}{\eta_D + M_C}. \tag{5}$$

Assuming that the total output power of the converter is P_{total}, which equals $P_C+P_{n1}+P_{n2}$, the relationship between P_C and P_{total} can be obtained by combining (2), (3), and (5)

$$k = \frac{P_C}{P_{\text{total}}} = \frac{k_1 M_1}{1 + M_1} = \frac{\eta_D M_C}{(1 + 2M_C)(\eta_D + M_C)} \tag{6}$$

where k is the power ratio of P_C, and can also be obtained by combining (3) and (6)

$$k = \frac{\eta_D (2NM - 1)(1 - NM)}{NM[(2\eta_D - 1) + 2(1 - \eta_D) NM]}. \tag{7}$$

When $k>0$, the range that M needs to satisfy is $1/2N<M<1/N$. According to (3), (6), and (7), the relationship between M, k, and M_C is shown in Fig. 3(a)–(c). The efficiency of the $P_{n1}+P_{n2}$ component in the total input power P_{in} of the converter is defined as α. As a result, the relationship between the total efficiency η_{total} of the converter and α can be obtained by

$$\eta_{\text{total}} = \frac{P_C + P_{n1}}{P_{\text{in}}} + \frac{P_{n2}}{P_{\text{in}}} = \frac{\alpha}{1 - k}. \tag{8}$$

According to (7) and (8), the relationship between η_{total} and M is depicted in Fig. 3(d). As shown in Fig. 3, the output power of DC_1 only accounts for a small portion of the total output power

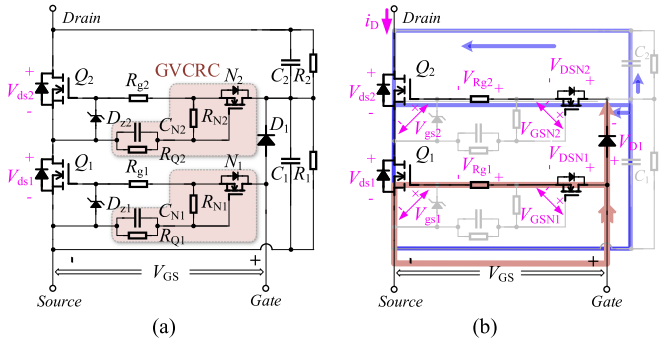

Fig. 4. Proposed GVSB-SCPS topology and turn-ON steady state. (a) Proposed topology including two SiC MOSFETs. (b) Turn-ON steady state.

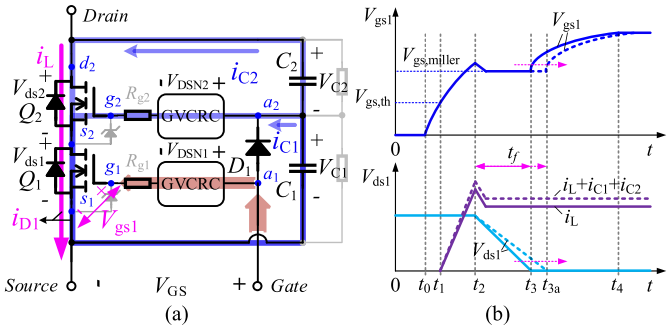

Fig. 5. Turn-ON process of the GVSB-SCPS. (a) Turn-ON state during the Miller plateau stage. (b) Theoretical turn-ON waveforms.

of the converter. Furthermore, as the power proportion processed by DC_1 in the total output power decreases, its impact on the efficiency of the converter is correspondingly reduced. When $k = 0$, η_{total} equals the efficiency of the front-stage DCX.

B. Principle and High-Frequency Operation Analysis of the Gate-Voltage Self-Balancing Super-Cascode Power Switch

Fig. 4(a) shows the proposed gate voltage self-balancing SCPS (GVSB-SCPS) topology including two SiC MOSFETs. Fig. 4(b) shows the simplified equivalent model of GVSB-SCPS in the turn-ON state. The blue lines represent the current paths of capacitors, and the red lines represent the external driving current paths. Q_j ($j\geq1$) is the SiC MOSFET. N_j is the N-channel depletion MOSFET. C_j is the capacitor for dynamic voltage balancing. R_j is the resistor for static voltage balancing. The operation principle of the topology in Fig. 4 has been explained and verified in [23]. In GVSB-SCPS, N_j, R_{Nj}, R_{Qj}, and C_{Nj} form a gate voltage closed-loop circuit (GVCRC), which is used to closed-loop regulate $V_{\text{gs}j}$ to keep it consistent and stable through $V_{\text{DSN}j}$. The principle of GVCRC has been explained in [23]. This article will focus on the switch operation of GVSB-SCPS.

Fig. 5(a) shows the turn-ON process of the GVSB-SCPS during the Miller plateau stage, where the load current i_L has been established, and C_j is discharging to Q_j. Fig. 5(b) shows the theoretical turn-on waveforms, where the dashed and solid lines, respectively, indicate the turn-ON process with and without the discharge currents i_{C1} and i_{C2}. t_f is the Miller plateau time,

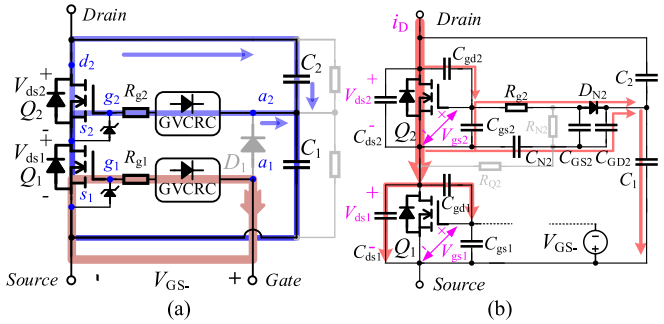

Fig. 6. Turn-OFF process and equivalent model of GVSB-SCPS. (a) Theoretical turn-OFF process. (b) Detailed parameter model of the drive branch.

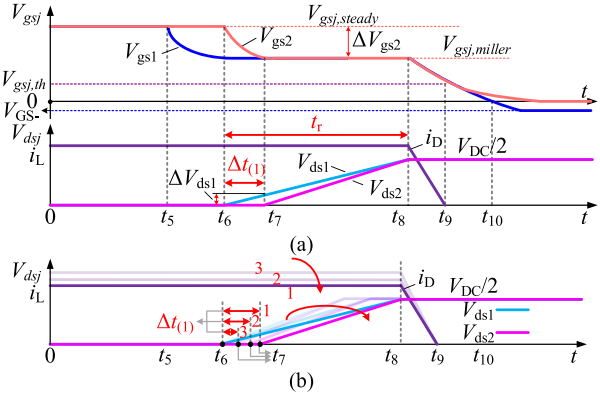

Fig. 7. Turn-off waveforms of the GVCB-SCPS. (a) Theoretical waveforms during the turn-OFF process. (b) Varying turn-OFF start points and turn-OFF time waveforms with the load current changes.

which is also the turn-ON time of device. $V_{\mathrm{gs\_miller}}$ is the Miller plateau voltage and remains constant during t_f, indicating that GVCRC has little effect on t_f, which is mainly impacted by i_{Cj}.

Before t_f, V_{C1} is approximately equal to V_{DC}/n due to voltage sharing, where V_{DC} is the total drain-source voltage of GVSB-SCPS. Considering that C_1 and C_2 need to be fully discharged during the t_f stage, the released charge can be expressed as

$$Q_{C1} = \frac{V_{\mathrm{DC}}}{n} \cdot C_1 = t_f \sum_{j=1}^{n} i_{Cj}. \tag{9}$$

According to Fig. 5, the current i_{D1} flowing through Q_1 is equal to i_L+i_{C1}+i_{C2}, and the t_f can be obtained by

$$t_f = (V_{\mathrm{DC}} \cdot C_1)/[n\,(i_{D1} - i_L)]. \tag{10}$$

During the t_f period, Q_1 is in the saturation region, where i_{D1} is controlled by $V_{\mathrm{gs\_miller}}$. Consequently, when $V_{\mathrm{gs\_miller}}$ remains constant, i_{D1} also remains unchanged. According to (10), when V_{DC} and i_L are constant, t_f will be affected by C_1. Furthermore, the larger the value of C_1, the longer t_f will be.

Fig. 6(a) shows the turn-OFF processes of GVSB-SCPS. When GVSB-SCPS is driven by V_{GS} to turn OFF, Q_j turns OFF in sequence, while the current flows through the body diode of N_j. Fig. 6(b) shows a detailed parameter model of the drive branch when V_{ds1} rises. Fig. 7(a) shows the theoretical waveforms during the turn-OFF process. Fig. 7(b) shows the varying turn-OFF start points and turn-OFF time waveforms with the load current i_L changes. Fig. 6(b) corresponds to the $\Delta t_{(1)}$ period in Fig. 7. $C_{\mathrm{gs}j}$, $C_{\mathrm{gd}j}$, and $C_{\mathrm{ds}j}$ are the gate-source capacitor, gate-drain capacitor, and drain-source capacitor of Q_j, respectively. $C_{\mathrm{GS}j}$, $C_{\mathrm{GD}j}$, and D_{Nj} are the gate-source capacitor, gate-drain capacitor, and body diode of N_j, respectively. During turn-OFF process, the moment when $V_{\mathrm{ds}j}$ starts to rise is the start turn-OFF point, which depends on the time of entering the Miller plateau.

Due to the sequential turn-OFF, the turn-OFF starting point of Q_j varies and is related to the load current i_L. Assuming the difference in the turn-OFF start points between Q_i ($1 \le i \le n$-1) and $Q_{(i+1)}$ is Δt_i, the sum of Δt_i can be obtained according to Fig. 6

$$\sum_{i=1}^{n-1} \Delta t_i = \frac{1}{i_L} \sum_{i=1}^{n-1} k_{(i+1)} \tag{11}$$

Where $k_{(i+1)}$ is the constant related to the driving branch of $Q_{(i+1)}$, and can be obtained by KVL and KCL

$$k_{(i+1)} = \left(C_{ossi}\left[C_{\mathrm{eq}(i+1)} + C_i\right]/C_i + C_{\mathrm{eq}(i+1)}\right) \cdot \left|\Delta V_{\mathrm{gs}(i+1)}\right| \tag{12}$$

Where C_{ossi} is the output capacitor of Q_i and equals to $C_{\mathrm{gd}j}$+$C_{\mathrm{ds}j}$. $\Delta V_{\mathrm{gs}(i+1)}$ is the difference between the Miller plateau voltage and the gate steady-state voltage of $Q_{(i+1)}$. $C_{\mathrm{eq}(i+1)}$ in (12) is

$$C_{\mathrm{eq}(i+1)} = C_{\mathrm{iss}(i+1)} + C_{Ni} \cdot C_{\mathrm{ISS}(i+1)}/\left[C_{Ni} + C_{\mathrm{ISS}(i+1)}\right] \tag{13}$$

Where $C_{\mathrm{iss}i}$ is the sum of $C_{\mathrm{gs}i}$ and $C_{\mathrm{gd}i}$, $C_{\mathrm{ISS}i}$ is the sum of $C_{\mathrm{GS}i}$ and $C_{\mathrm{Gd}i}$. From (11), (12), and (13), it can be known that Δt_i will increase as i_L decreases, as shown in Fig. 7(b).

During the $\Delta t_{(1)}$ period, the change of V_{ds1} for Q_1 is

$$\Delta V_{\mathrm{ds1}} = -\Delta V_{\mathrm{gs2}} \cdot \left[\frac{C_1 + C_{\mathrm{iss2}}}{C_1} + \frac{C_{N2} C_{\mathrm{ISS2}}}{C_1\,(C_{N2} + C_{\mathrm{ISS2}})}\right]. \tag{14}$$

However, V_{ds2} remains unchanged during this period since i_D discharges the C_{iss2} instead of charging the C_{oss2}. Furthermore, the changes of C_{iss2} and C_{ISS2} are related to ΔV_{gs2}, which is associated with Q_2 itself. Therefore, the changes of C_{iss2} and C_{ISS2} are decoupled from the V_{DC} and i_D. According to (14), ΔV_{ds1} is also decoupled from the V_{DC} and i_D. Combining (12) and (13), since the change of C_{oss1} within Δt_i is related to ΔV_{ds1}, it can be inferred that $k_{(2)}$ does not change with V_{DC} and i_D. As a result, the $\sum_{i=1}^{n-1} k_{(i+1)}$ does not change with V_{DC} and i_D.

Since i_D discharges the $C_{\mathrm{iss}(i+1)}$ of $Q_{(i+1)}$ instead of charging the $C_{\mathrm{oss}(i+1)}$ of $Q_{(i+1)}$ within the Δt_i period, the total turn-OFF time t_r include Δt_i and can be expressed as

$$t_r\,(V_{\mathrm{DC}}) = \frac{V_{\mathrm{DC}}\left[C_{\mathrm{oss}n}\,(V_{\mathrm{DC}}/n) + C_n\right]}{n \cdot i_L} + \frac{1}{i_L} \cdot \sum_{i=1}^{n-1} k_{(i+1)} \tag{15}$$

where $C_{\mathrm{oss}n}(V_{\mathrm{DC}}/n)$ is the output capacitor of Q_n at $V_{\mathrm{ds}n} = V_{\mathrm{DC}}/n$.

Since i_D charges $C_{\mathrm{oss}n}$ and C_n after Q_n enters the Miller platform, the equivalent output capacitance of Q_n can be obtained

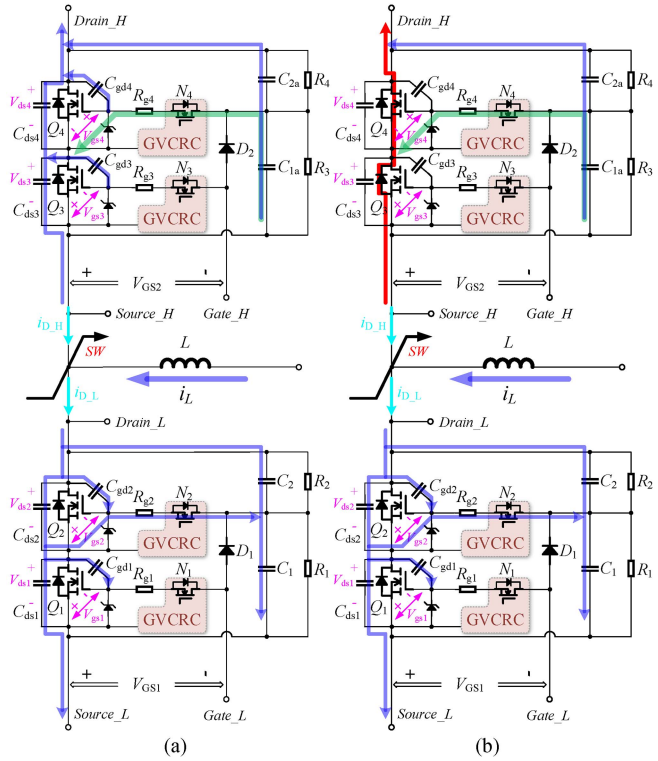

Fig. 8. GVSB-SCPS-based switching cell when the high-side switch achieves ZVS soft-switch. (a) Before the V_{ds3} and V_{ds4} drop to the minimized. (b) After the V_{ds3} and V_{ds4} drop to the minimized.

by the sum of $C_{\mathrm{oss}n}$ and C_n

$$C_{\mathrm{equal}(n)} = C_{\mathrm{oss}n} + C_n. \tag{16}$$

Due to the series relationship of C_j and KCL, (16) only applies to Q_n. Combined with (15) and (16), the total equivalent output capacitance of GVSB-SCPS can be obtained by

$$C_{\mathrm{oss\_eq}} = \frac{C_{\mathrm{equal}(n)}}{n} + \frac{1}{V_{\mathrm{DC}}} \sum_{i=1}^{n-1} k_{(i+1)}. \tag{17}$$

C. Switching Mode Analysis of the GVSB-SCPS Switching Cell During the Dead Time Under Soft-Switching Conditions

Based on the GVSB-SCPSs configuration with two devices in series, Fig. 8 shows the switching cell when the high-side devices achieve ZVS soft turn-ON during the dead time. Q_3 and Q_4 are the high-side devices, while Q_1 and Q_2 are the low-side devices. SW is the switching node. The blue lines represent the load current paths, and the green lines represent the current path for C_1 discharging to the gate of device. i_{D_H} and i_{D_L} are the currents flowing through the high-side devices and the low-side devices, respectively. Fig. 9 shows the theoretical waveforms.

As shown in Fig. 8, when the low-side devices are turned OFF, the voltage at the SW node rises, and i_L flows into the SW node. For the low-side devices, i_L will charge C_{ds1}, C_{ds2}, C_{gd1}, C_{gd2}, C_1, and C_2, resulting in the rise of V_{ds1} and V_{ds2} and the decrease of V_{gs1} and V_{gs2}. For the high-side devices, i_L will discharge C_{ds3}, C_{ds4}, C_{gd3}, C_{gd4}, C_{1a}, and C_{2a}. During this

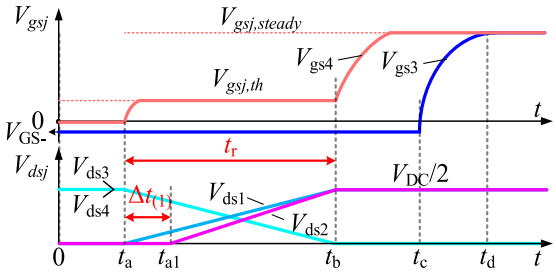

Fig. 9. Theoretical waveforms of high-side switch during soft turn-ON.

period, V_{gs3} is clamped by V_{GS2}, while C_{1a} charges the gate of Q_4 and V_{gs4} rises. However, once Q_4 turns ON, V_{ds3} will increase as V_{ds4} decreases, causing V_{gs4} to drop again. As a result, before C_{ds3} and C_{ds4} are fully discharged, V_{gs4} will remain close to the turn-ON threshold $V_{gsj,\mathrm{th}}$, as shown in Fig. 9. When V_{ds3} and V_{ds4} decrease to the minimum values, V_{gs4} will continue to rise to the steady-state value, causing Q_4 to be turned ON before Q_3. i_L eventually flows through the body diode of Q_3 and the channel of Q_4, creating the ZVS turn-ON condition of high-side devices.

During t_b–t_d period in Fig. 9, the current flows through the channel of Q_4 rather than its body diode. Since the conduction voltage drop of the channel is much smaller than that of the body diode, it will help to reduce the dead-time loss. Assuming that the conduction voltage drop of the body diode and the ON-state resistance of Q_j are V_{Drj} and $R_{\mathrm{ds}j,}$ respectively, the dead-time loss reduced by GVSB-SCPSs compared with the conventional series-connected devices is

$$P_{\mathrm{loss\_reduce}} = \int_{t_b}^{t_d} \left(\sum_{j=2}^{n} V_{Drj} \cdot i_{D\_H} - \sum_{j=2}^{n} R_{\mathrm{ds}j} \cdot i_{D\_H}^2 \right) dt. \tag{18}$$

The conclusion of (18) is also suitable for the cases where n>2. When n rises, GVSB-SCPS has smaller dead-time losses compared with the conventional series-connected device.

However, the GVSB-SCPS has an additional $\Delta t_{(1)}$ related to the load current. To ensure reliable turn-OFF of the low-side devices, the dead time should be greater than t_r. At the same time, i_L should fully discharge the output capacitance of high-side devices to create the condition of ZVS turn-ON.

D. Boundary Conditions for Soft Switching Realization of GVSB-SCPSs in the Proposed Converter

Since the efficiency of DCX is the highest when operating at resonant frequency, the analysis will be based on this condition. The conditions of the ZVS soft-switch for S_1-S_4 should be satisfied as follows.

1) The inductive input impedance exists in the resonant cavity, where the voltage changes direction before current.
2) Resonant current achieves complete charging and discharging of the output capacitors of devices during the dead time.
3) Resonant current cannot change the direction during the dead time.

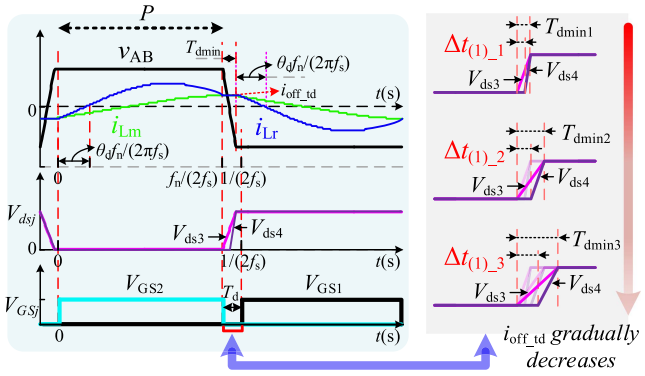

Fig. 10. Theoretical waveforms for ZVS realization in the proposed converter under the resonant point.

Since 1) is naturally satisfied at the resonant point, the realization of ZVS soft-switch is considered during the dead time as follows.

Fig. 10 shows the theoretical waveforms for ZVS realization in the proposed converter at the resonant point. f_n represents the normalized frequency and equals $2\pi f_s\sqrt{L_r/C_r}$, where f_s is the switch frequency. The P state is defined as the stage when v_P equals the Nv_{CD} and i_{Lr} is greater than i_{Lm}. In Fig. 10, when the OFF-state current $i_{\mathrm{off\_td}}$ during the dead time is smaller, the turn-OFF time will be longer, as shown in T_{dmin1}–T_{dmin3}. The turn-OFF time includes not only the time for charging the equivalent output capacitor of devices, but also the time difference when devices enter the Miller plateau, as shown in $\Delta t_{(1)\_1}$–$\Delta t_{(1)\_3}$. According to the previous analysis, $\Delta t_{(1)\_1}$–$\Delta t_{(1)\_3}$ is also related to $i_{\mathrm{off\_td}}$ and increases with the decrease of $i_{\mathrm{off\_td}}$. According to Fig. 1 and KVL, $i_{\mathrm{off\_td}}$ could be obtained by

$$i_{\mathrm{off\_td}} = \frac{Nv_{\mathrm{CD}}}{4L_m f_r} \tag{19}$$

Where f_r is the resonant frequency of L_r and C_r, and equals $1/2\pi\sqrt{L_rC_r}$. Assuming that the dead time is T_d and S_1–S_4 has the same parameters, since completely charge and discharge of the equivalent output capacitor $C_{\mathrm{equal}(n)}$ in S_1–S_4 during T_d period should be achieved, there is

$$i_{\mathrm{off\_td}}\cdot\left(T_d-\sum_{i=1}^{n-1}\Delta t_i|_{i_L=i_{\mathrm{off\_td}}}\right)>2C_{equal(n)}\cdot\frac{V_{\mathrm{DC}}}{n}. \tag{20}$$

Assuming that the minimum value of T_d is T_{dmin}, there is

$$T_{d\mathrm{min}}=\frac{2C_{equal(n)}V_{\mathrm{DC}}}{n\cdot i_{\mathrm{off\_td}}}+\sum_{i=1}^{n-1}\Delta t_i|_{i_L=i_{\mathrm{off\_td}}}. \tag{21}$$

Different from the conventional *LLC* topology, the T_{dmin} in (21) contains the time difference of turn-off starting points of each device and is related to $i_{\mathrm{off\_td}}$ in the dead time. However, when the T_d is too large, $i_{\mathrm{off\_td}}$ will cross zero in advance and reverse charge and discharge the $C_{\mathrm{equal}(n)}$ again, resulting in the loss of the ZVS condition. Therefore, the maximum dead time should be limited. According to Figs. 1 and 10 and periodic symmetry, the expression of excitation current and resonance current in P state can be obtained:

$$\begin{cases} i_{Lm\_P}(t) = -i_{\mathrm{off\_td}}+\frac{Nv_{\mathrm{CD}}}{L_m}\cdot t \\ i_{Lr\_P}(t) = I_{Lr\_pk}\sin\left(2\pi t\cdot f_s/f_n-\theta_d\right)\end{cases} \tag{22}$$

Where θ_d is the angle of i_{Lr} from the separation of resonance current and excitation current to just resonance to zero. I_{Lr_pk} is the peak value of i_{Lr}. Assuming that the efficiency of the post stage is η_p, the average current on the primary side of T_r and the total output current I_o should satisfy

$$2f_s\int_0^{f_n/(2f_s)}|i_{Lr}(t)-i_{Lm}(t)|\,dt=I_oV_{\mathrm{out}}/(\eta_pNv_{\mathrm{CD}}). \tag{23}$$

Since *LLC* only transfers energy in the P states, (22) can be brought into (23) to obtain

$$I_{Lr\_\mathrm{pk}}\cos(\theta_d)=\frac{P_o\pi}{2\eta_pNv_{\mathrm{CD}}f_n}-\frac{\pi i_{\mathrm{off\_td}}}{2}+\frac{\pi Nv_{\mathrm{CD}}f_n}{8L_mf_s} \tag{24}$$

Where P_o is the total output power. Moreover, according to the period symmetry, i_{Lm} and i_{Lr} are approximately equal at $t = 0$:

$$i_{Lm\_P}(t)|_{t=0}=I_{Lr\_\mathrm{pk}}\sin(-\theta_d)=-i_{\mathrm{off\_td}}. \tag{25}$$

Combine with (24) and (25), θ_d can be obtained as

$$\theta_d=\arctan\left[i_{\mathrm{off\_td}}\Big/\left(\frac{P_o\pi}{2\eta_pNv_{\mathrm{CD}}f_n}-\frac{\pi i_{\mathrm{off\_td}}}{2}+\frac{\pi Nv_{\mathrm{CD}}f_n}{8L_mf_s}\right)\right]. \tag{26}$$

Assuming that the maximum T_d to satisfy the $i_{\mathrm{off\_td}}$ without changing direction is T_{dmax}, T_{dmax} can be obtained according to (21) and (26)

$$T_{d\mathrm{max}}=\frac{2C_{equal(n)}V_{\mathrm{DC}}}{n\cdot i_{\mathrm{off\_td}}}+\sum_{i=1}^{n-1}\Delta t_i|_{i_L=i_{\mathrm{off\_td}}}+\frac{\theta_d}{2\pi f_r}. \tag{27}$$

Combined with (11), (15), (21), and (27), to ensure the realization of S_1–S_4 soft switching, the dead time T_d should satisfy

$$\begin{cases} T_d\ge\frac{2C_{equal(n)}V_{\mathrm{DC}}}{n\cdot i_{\mathrm{off\_td}}}+\sum_{i=1}^{n-1}\Delta t_i|_{i_L=i_{\mathrm{off\_td}}} \\ T_d\le\frac{2C_{equal(n)}V_{\mathrm{DC}}}{n\cdot i_{\mathrm{off\_td}}}+\sum_{i=1}^{n-1}\Delta t_i|_{i_L=i_{\mathrm{off\_td}}}+\frac{\theta_d}{2\pi f_r}\end{cases}. \tag{28}$$

E. Power Loss Analysis and Dead Time Design

In order to study the effects of T_d and $\sum_{i=1}^{n-1}\Delta t_i$ on the loss of the proposed converter, it is necessary to obtain the relationship between these parameters with the i_{Lr}. Since the RMS value $I_{\mathrm{rms\_}p}$ and the peak value I_{Lr_pk} of i_{Lr} satisfy $i_{Lr\_\mathrm{pk}}=\sqrt{2}\,I_{\mathrm{rms\_}p}$, it can be obtained according to (19), (23), and (25)

$$I_{\mathrm{rms\_}p}=\frac{\pi P_o}{2\sqrt{2}\eta Nv_{\mathrm{CD}}}\sqrt{\frac{N^4v_{\mathrm{CD}}^4\eta^2}{4\pi^2L_m^2P_o^2f_n^2f_r^2}+4(f_rT_d+f_r^2T_d^2)+1}. \tag{29}$$

According to (29), the $I_{\mathrm{rms\_}p}$ decreases with L_m increases, which is beneficial to reduce the conduction loss. However, the

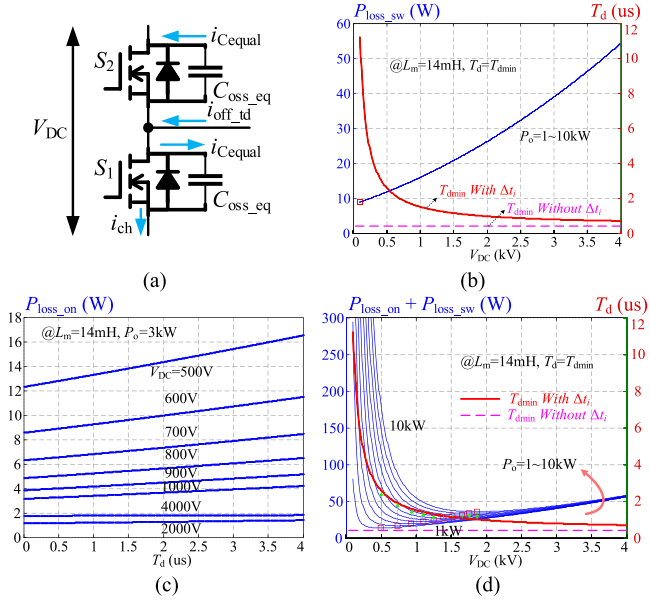

Fig. 11. Relationship between the switching loss, conduction loss, primary total loss, V_{DC}, and dead time of converter. (a) Turn-OFF simplified model. (b) Switching loss. (c) Conduction loss. (d) Primary total loss.

selection of L_m requires making i_{Lr} achieve complete charging and discharging of the output capacitors of devices during T_d period. Combining with (19)–(21), and $V_{\mathrm{DC}} = Nv_{\mathrm{CD}}$ at the resonant point, the range of L_m can be obtained by

$$L_m \le n\left(T_{d\min} - \sum_{i=1}^{n-1} \Delta t_i|_{i_L = i_{\mathrm{off\_td}}}\right) \Big/ \left(8C_{equal(n)} f_r\right). \tag{30}$$

Fig. 11(a) shows the simplified model when S_1 turns off during T_d, where i_{ch} and $i_{C\mathrm{equal}}$ are the channel current of S_j and the current flowing through the equivalent output capacitance C_{equal}, respectively. To simplify the analysis, it is assumed that i_{ch} is linearly turned off during this period, and there is

$$i_{\mathrm{ch}}(t) = i_{\mathrm{off\_td}}\left(1 - t/T_{d\min}\right). \tag{31}$$

Assuming that $P_{\mathrm{loss\_sw}}$, $P_{\mathrm{loss\_on}}$, and P_{loss} are the switching loss, conduction loss, and primary total loss of the converter, there is

$$\begin{cases} P_{\mathrm{loss\_sw}} = 4f_s \int_0^{T_{d\min}} i_d(t)\, V_{\mathrm{ds}}(t)\, dt = i_{\mathrm{off\_td}}^2 T_{d\min}^2 f_s / \left(12C_{\mathrm{oss\_eq}}\right) \\ P_{\mathrm{loss\_on}} = I_{\mathrm{rms}\_p}^2 R_{\mathrm{ds}} \\ P_{\mathrm{loss}} = P_{\mathrm{loss\_sw}} + P_{\mathrm{loss\_on}} \end{cases}. \tag{32}$$

According to (19), (21), and (32), the relationship between $P_{\mathrm{loss\_sw}}$, $P_{\mathrm{loss\_on}}$, P_{loss}, T_d, and $\sum_{i=1}^{n-1} \Delta t_i$ can be obtained, as shown in Fig. 11(b)–(d). The reference of R_{ds}, N, $C_{\mathrm{oss\_eq}}$, and f_s are 0.25 Ω, 20, 190 pF, and 20 kHz, respectively. It can be seen from (32) and Fig. 11(b) that as V_{DC} increases, the switching loss gradually increases, conduction loss gradually decreases, while the primary total loss P_{loss} has a minimum value. According to (13), (21), and (32), if V_{DC}, $i_{\mathrm{off\_td}}$, and f_s remain unchanged, adding T_d larger than T_{dmin} does not change the $P_{\mathrm{loss\_sw}}$. As

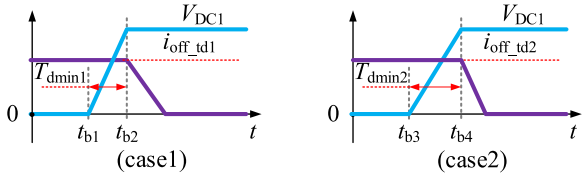

Fig. 12. Turn-off transient waveforms in a double pulse tester when $m = 2$.

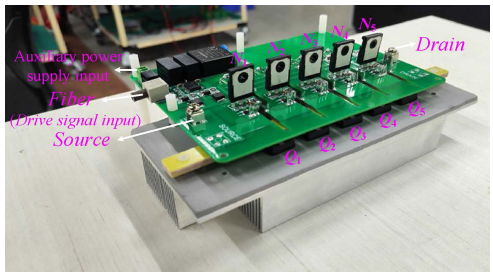

Fig. 13. Picture of the designed 10 kV GVSB-SCPS.

shown in Fig. 11(c), since $P_{\mathrm{loss\_on}}$ decreases with the reduction in T_d, it is beneficial to reduce the conduction loss when T_d decreases. Therefore, $T_d = T_{\mathrm{dmin}}$ was selected as the optimal dead-time control coordinate in the dead-time design.

However, obtaining the T_{dmin} and selecting appropriate L_m in (30) require to know $\sum_{i=1}^{n-1} \Delta t_i$. According to (11), (12), and (13), $\sum_{i=1}^{n-1} \Delta t_i$ is related to $\sum_{i=1}^{n-1} k_{(i+1)}$, which contains the voltage dependent junction capacitance of devices. According to the analysis in Section II-B, $\sum_{i=1}^{n-1} k_{(i+1)}$ will not change with V_{DC} and i_D. Therefore, T_{dmin} can be predicted through $\sum_{i=1}^{n-1} k_{(i+1)}$.

Combing with (11) and (21), T_{dmin} can be expressed as

$$T_{d\min} = \left[2C_{equal(n)} V_{\mathrm{DC}}/n + \sum_{i=1}^{n-1} k_{(i+1)}\right] \Big/ i_{\mathrm{off\_td}}. \tag{33}$$

As shown in Fig. 12, through m double pulse tests under different $i_{\mathrm{off_tdx}}$s and same V_{DC1}, $\sum_{i=1}^{n-1} k_{(i+1)}$ can be obtained as

$$\sum_{i=1}^{n-1} k_{(i+1)} = \frac{\sum_{x=1}^{m} i_{\mathrm{off\_tdx}} T_{\mathrm{dminx}} - mQ_{ossn}\left(V_{\mathrm{DC1}}/n\right)}{m} \tag{34}$$

Where $Q_{ossn}(V_{\mathrm{DC1}}/n)$ is the equivalent output charge of Q_n at V_{DC1}/n, which can be obtained by combining (15) and (16)

$$Q_{ossn}\left(V_{\mathrm{DC1}}/n\right) = \frac{V_{\mathrm{DC1}}\left[C_{ossn}\left(V_{\mathrm{DC1}}/n\right) + C_n\right]}{n}. \tag{35}$$

III. Experimental Results

To construct the proposed converter, a 10 kV GVSB-SCPS prototype based on the GVSB-SCPS topology is built using five SiC MOSFETs (WM2A050330L) in series, as shown in Fig. 13. The key experimental parameters of the designed GVSB-SCPS are listed in Table I.

TABLE I
PROTOTYPE PARAMETERS OF THE DESIGNED GVSB-SCPS

Variable	Symbol	Values
N-channel depletion MOSFETs	N_j	IXTH16N50D2
Avalanche diodes	D_j	SF1600 (two in series)
Resistors for static voltage balancing	R_1–R_5	3.4 MΩ
Capacitors for static voltage balancing	C_1–C_5	[1.5 nF, 1.2 nF, 1 nF, 850 pF, 800 pF]
Feedback resistances	R_{N1}–R_{N5}	[386.2, 398.3, 386.1, 376.5, 388 Ω]
	R_{Q1}–R_{Q5}	1522.1 Ω

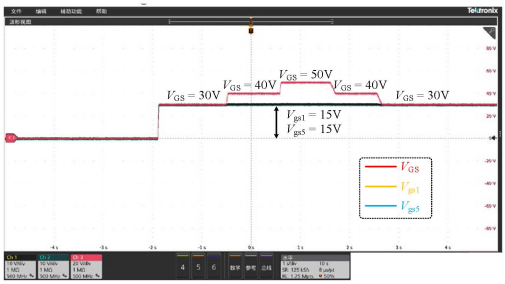

Fig. 14. Experimental waveforms of gate-source voltages for SiC MOSFETs in the designed 10 kV GVSB-SCPS under varying driving voltages.

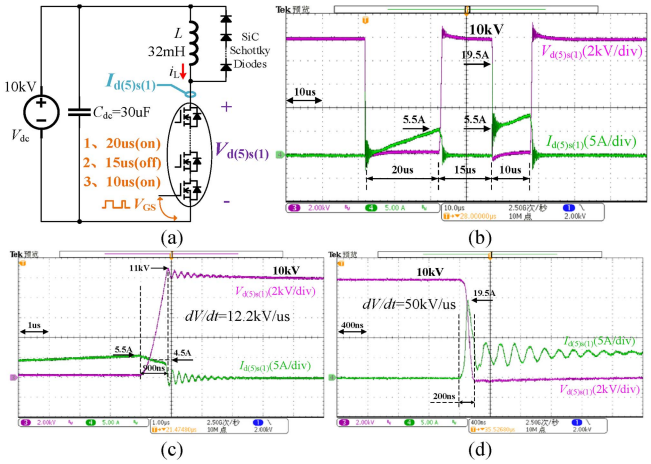

Fig. 15. Waveform test results of the designed 10 kV GVSB-SCPS in the DPT at 10 kV. (a) Schematic of DPT. (b) Waveform test results under two pulses. (c) Turn-OFF waveforms. (d) Turn-on waveforms.

A. *Experiment Results of the 10 kV GVSB-SCPS Prototype Designed as the Main Power Device in the Proposed DCX Converter*

Fig. 14 shows the experimental waveforms of gate-source voltages in the designed GVSB-SCPS under varying driving voltages. The experimental results demonstrate that the V_{gs1} and V_{gs5} remain stable at 15 V under V_{GS} changing from 30 to 50 V. The gate voltage self-balancing function has been verified.

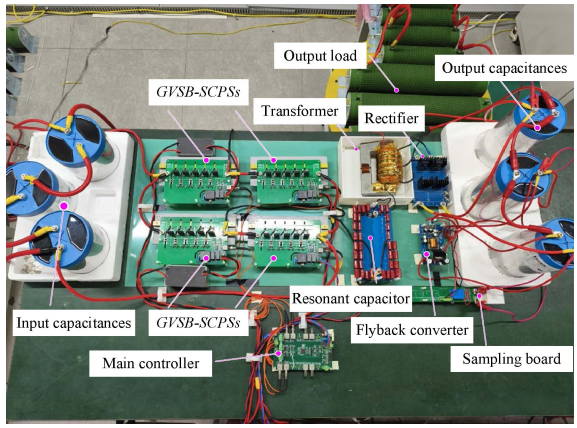

Fig. 16. Experimental prototype of the partial power converter based on the designed GVSB-SCPSs.

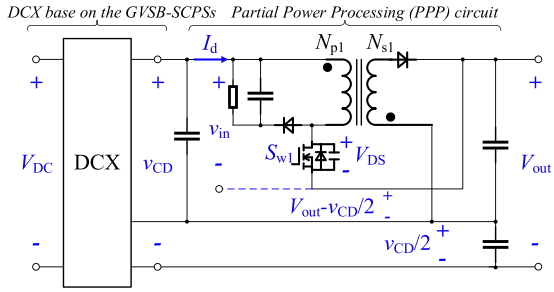

Fig. 17. Simplified equivalent model of the proposed converter topology.

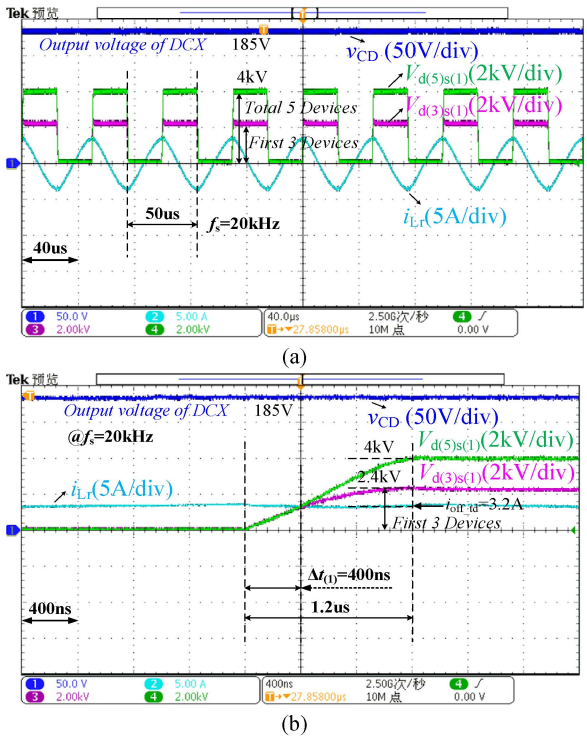

Fig. 18. Experimental results of DCX in the constructed converter. (a) Steady-state operation waveforms. (b) Turn-OFF transient waveforms.

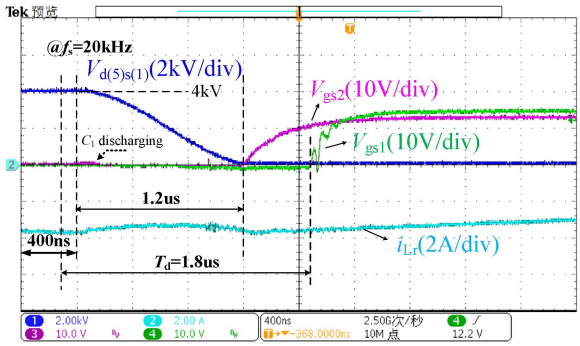

Fig. 19. Experimental results of gate voltages in the constructed converter.

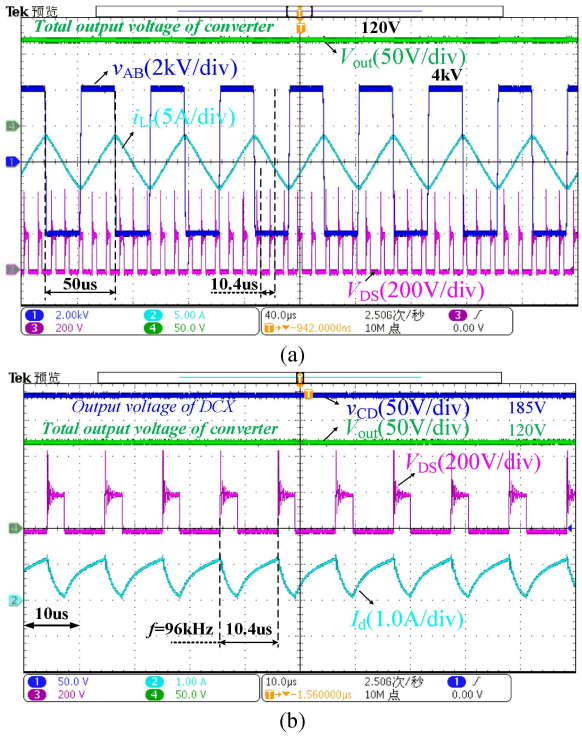

Fig. 20. Experimental results of the constructed converter. (a) V_{out}, v_{AB}, i_{Lr}, and V_{DS}. (b) v_{CD}, V_{out}, V_{DS}, and I_d.

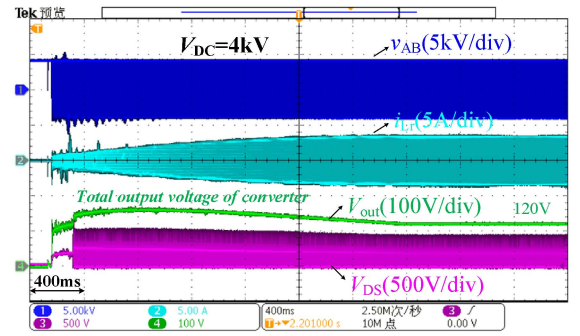

Fig. 21. Startup waveforms of the constructed converter at 4 kV.

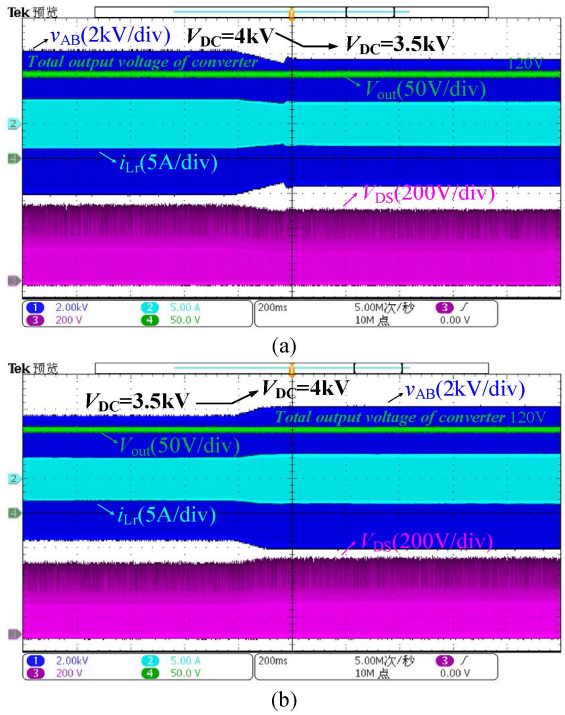

Fig. 22. Voltage and current waveforms under the condition of total input voltage V_{DC} variation. (a) The V_{DC} drops from 4kV to 3.5kV. (b) The V_{DC} rises from 3.5kV to 4kV.

Fig. 15 shows the waveform test results of the designed 10-kV GVSB-SCPS in the double pulse tester (DPT) at 10 kV. The input capacitor C_{dc} is 30 uF, and the input inductor L is 32 mH. Multiple series-connected Schottky diodes are connected in parallel at L to act as a freewheeling diode. The external driving signals are two pulses that last 20 and 10 µs, respectively, with an interval of 15 µs. $V_{d(j)s(1)}$ is the voltage difference between the drain of Q_j and the source of Q_1. I_{d5s1} is the current flowing through the designed GVSB-SCPS.

Fig. 15(c) shows the turn-OFF waveforms of the designed 10-kV GVSB-SCPS at 10 kV input. The drain-source voltage rises from 0 to 11 kV in 900 ns at 4.5 A, while the *dv*/*dt* is 12.2 kV/µs.

Fig. 15(d) shows the turn-ON waveforms of the designed 10-kV GVSB-SCPS at 10 kV input. The drain-source voltage falls from 10 kV to 0 in 200 ns at 19.5 A, while the *dv*/*dt* is 50 kV/µs. There is a 14 A current spike, which is caused by the reverse recovery current of the freewheeling diode and the charging current of the parasitic capacitors due to the fast *dv*/*dt*.

According to the experimental results from Figs. 14 and 15, the excellent performance of GVSB-SCPS has been verified.

B. Experiment Results of the Proposed Partial Power DCX With the GVSB-SCPS Prototype Designed

Based on the proposed converter topology, an experimental prototype of the partial power DCX utilizing the constructed GVSB-SCPSs is developed, as shown in Fig. 16. The key experimental parameters of the designed converter are listed in

TABLE II
PROTOTYPE PARAMETERS OF THE DESIGNED CONVERTER

Variable	Symbol	Values
Input voltage	V_{DC}	4 kV
Total output voltage	V_{out}	120 V
Switching frequency	f_{s}	20 kHz
Resonant capacitance	C_{r}	40.8 nF
Resonant inductance	L_{r}	1.577 mH
Excitation inductance	L_{m}	14.04 mH
Transformer turns ratio	N	20:1

Table II. The PPP unit is constructed by a flyback converter, as shown in Fig. 17. I_d is the current flowing through the main switch S_{w1}, and V_{DS} is the drain-source voltage of S_{w1}. v_{in} is the input voltage of the Flyback.

Fig. 18 shows the operation results of the built converter at 4 kV, 20 kHz. i_{Lr} is the resonant current and v_{CD} is the output voltage of the front-stage DCX. $V_{d(5)\,s(1)}$ is the total voltage (over Q_1–Q_5) across the drain and source of the GVSB-SCPS, while $V_{d(3)\,s(1)}$ is the voltage across the first three devices (over Q_1–Q_3). It is experimentally verified that the $V_{d(3)\,s(1)}$ is three-fifths that of $V_{d(5)\,s(1)}$, achieving a good voltage sharing. It can also be observed that when the turn-OFF current $i_{\mathrm{off\_td}}$ during the dead time is 3.2 A, the corresponding turn-off time is 1.2 µs, and the difference time $\Delta t_{(1)}$ between the turn-off start points is 400 ns. The sequential turn-OFF mechanism has been verified.

Fig. 19 shows the test results of the gate voltages in the constructed converter during the dead time T_d. When the drain-source voltage $V_{d(5)\mathrm{s}(1)}$ drops, the gate voltage V_{gs2} of the upper device first rises due to the discharge of the capacitor C_1, but is clamped below the threshold voltage. When $V_{d(5)\,s(1)}$ drops to 0, V_{gs2} continues to rise to the steady-state value. During the dead time, V_{gs1} is clamped to a low level by the external drive voltage V_{GS}. When the dead time T_d ends, V_{gs1} rises as the V_{GS} increases. The experimental results in Fig. 19 verify the analysis of the unique gate switching pattern during the dead time. Since V_{gs1} turns ON after $V_{d(5)\,s(1)}$ drops to 0, it also verifies the realization of ZVS soft switching of GVSB-SCPSs.

As shown in Fig. 20, under the conditions of an input voltage of 4 kV and a switching frequency of 20 kHz, v_{CD} and V_{out} are 185 and 120 V, respectively, while stable operation is achieved. At the same time, the operating frequency of the flyback is 96 kHz. The startup waveforms of the constructed converter at 4 kV are shown in Fig. 21. In this process, the output voltage V_{out} reaches and maintains a stable 120 V following a soft-start period lasting approximately 2.56 s.

As shown in Fig. 22, to test the voltage regulation function of the proposed PPP circuit, the total input voltage V_{DC} is varied between 3.5 and 4 kV. The experimental results show that when V_{DC} varies, v_{AB}, i_{Lr}, and the drain-source voltage V_{DS} of the S_{w1} in the flyback also varies accordingly. However, due to the closed-loop regulation of the proposed PPP circuit, the total output voltage V_{out} remains stable at 120 V. The voltage

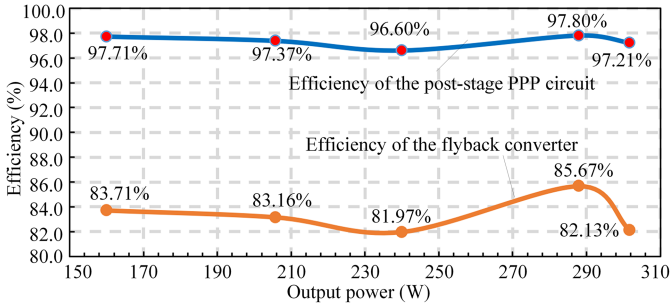

Fig. 23. Efficiency test results of the post-stage PPP circuit.

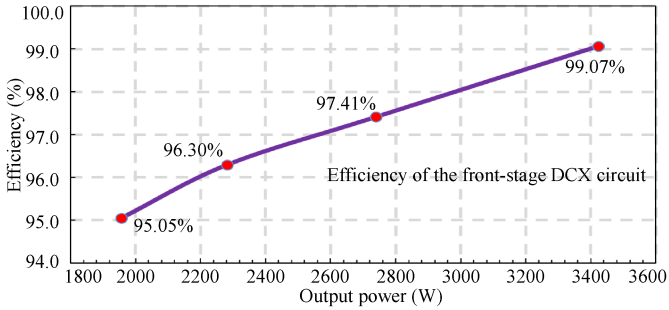

Fig. 24. Efficiency test results of the DCX circuit.

closed-loop regulation function of the proposed PPP circuit is verified.

In addition, the efficiency of the converter prototype under different output powers when $V_{\mathrm{DC}} = 4$ kV is tested, as shown in Figs. 23 and 24. As shown in Fig. 23, the efficiency of the flyback converter is around 83%, while the efficiency of the proposed post-stage PPP circuit reaches around 98%, with an increase of about 15%. As shown in Fig. 24, the efficiency of the DCX increases as the output power increases, reaching 99.07% when the output power is 3.42 kW.

C. Performance Comparison of the Proposed Topology and Method With Other State-of-the-Art Technologies

The comparison of the proposed topology and method with other state-of-the-art technologies is summarized in Table III.

In comparison with the topologies and methods proposed in [26], [28], [29], [30], and [31], the proposed method achieves a smaller number of driving signals and transformers, a higher voltage conversion ratio, and a higher test voltage on the basis of PPP, while the control strategy is very simple. The proposed topology adopts a two-stage architecture. The DCX achieves a fixed voltage ratio and soft switching for all devices, while the post stage uses the proposed PPP circuit for output voltage regulation. Based on the center-tapped design of the transformer and the PPP structure, most of the output power is directly transferred to the load, with only a small portion of the power processed by PPP, minimizing the power loss of the two-stage architecture. The proposed topology only requires four drive signals to drive the GVSB-SCPSs, enabling a single module to handle MV dc input. The converter uses PWM control on the

TABLE III
COMPARISON OF THE PROPOSED TOPOLOGY AND METHOD WITH OTHER STATE-OF-THE-ART TECHNOLOGIES

Comparison of the Proposed Topology and Method with Other State-of-the-Art Technologies

Technologies	Ref. [28]	Ref. [26]	Ref. [29]	Ref. [30]	Ref. [31]	Proposed
Topology	Half-bridge DCX	Full-bridge DCX+boost	Full-bridge DCX+buck	Full-bridge DCX+DAB	Half-bridge DCX+buck	Full-bridge DCX+PPP
Architecture type	Single-stage	Two-stage	Single-stage	Single-stage	Quasi-two-stage	Two-stage
Number of transformers	1	2	1	2(intergrate)	2	1★
Control strategy	Active clamping	Common-duty control	PWM control	Hybrid control	PWM control	PWM control
Number of drive signals	16	10	8	12	8	5★
Voltage conversion ratio	10:3	20:7	48:1	12:1	100:3	100:3★
Output isolation	Yes	Yes	No	Yes	Yes	Yes
Testing Voltage	2 kV dc	2 kV dc	48 V dc	60 V dc	400 V dc	4 kV dc★

low-voltage side for closed-loop regulation, without the need for high-isolation sampling and greatly simplifying the control.

IV. CONCLUSION

This article proposed a novel partial power converter based on the GVSB-SCPSs and the proposed PPP circuit. The GVSB-SCPSs were utilized to construct the DCX, directly achieving MVDC input of a single module. The proposed PPP circuit only needed to handle a small portion of the output power, while the high efficiency output of the converter was achieved. For the GVSB-SCPSs in the DCX, the influencing factors during continuous high-frequency operation were analyzed. At the same time, considering the unique gate switching pattern of the GVSB-SCPSs, the boundary condition for achieving soft switching during the dead time was provided. Under this condition, the loss of the proposed converter was analyzed, and the dead time was optimally designed. To construct the proposed converter, a 10 kV GVSB-SCPS was built and demonstrated outstanding switching characteristics in the testing results. Based on the proposed converter topology and the designed GVSB-SCPSs, a partial power converter prototype was built and stably operated at 4 kV, 20 kHz. The experimental results verified the realization of soft switching of GVSB-SCPSs. Furthermore, the proposed PPP circuit achieved closed-loop stability of the output voltage under the condition of total input voltage variation. The efficacy of the proposed topology and analysis was well verified.

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