Efficiency-Optimization Control Strategy With Real-Time Modulation Scheme for Three-Phase Single-Stage Matrix-Type Isolated AC–DC Converters

Zhiqiang Guo, *Senior Member, IEEE*, Zining Wang, Luming Liu, and Zhongyuan Chen

***Abstract*—This article proposes a control strategy for three-phase single-stage matrix-type isolated ac–dc converters. By introducing the global optimization modes of dual active bridge converters, the target current vector of the ac–dc converter is composed of the two working modes in the two adjacent switching periods, which can simplify the calculation of the modulation scheme. However, the scheme will generate a transient dc bias current during different current vector switching, which may lead to the loss of the zero-voltage switching (ZVS). Therefore, a control algorithm to suppress the transient dc bias current is proposed to achieve ZVS and reduce turn-ON switching loss. A simplified iteration algorithm is proposed to calculate the combined current vectors. The optimal working mode is calculated by a real-time modulation scheme without a lookup table. A single-loop control strategy without grid current sampling is presented to achieve the unity power factor. Finally, this control strategy is applied to a 1.5-kW three-phase single-stage matrix-type isolated ac–dc converter with 200-V/50-Hz line-to-line input voltage and 200-V output voltage. Experimental results demonstrate the performance of soft switching, fast dynamic response, and high efficiency.**

***Index Terms*—AC–DC converter, optimal working modes, space vector modulation (SVM), transient dc bias current suppression, unity power factor (PF).**

I. Introduction

In RECENT years, with the rapid development of renewable energy, energy storage, and electric vehicles, isolated ac–dc converters have witnessed widespread application and advancement [1], [2]. Traditionally, the isolated ac–dc converter is typically composed of multistage power conversions. The front stage is a nonisolated ac–dc converter, and the end stage is an isolated dc–dc converter. The intermediate dc bus requires large electrolytic capacitors [3]. Although this configuration enables the decoupling of output power and the regulation of input ac quality, the multistage power conversions result in significant power losses, low power density, and a shortened lifespan due to the presence of large electrolytic capacitors [4]. To improve the efficiency and power density in a wide voltage range, the single-stage isolated ac–dc converter has emerged as a new solution.

The single-stage ac–dc converter refers to the converter that features a single stage of high-frequency conversion, while other switches are driven by low-frequency gate signals to assist in commutation. A single-stage isolated ac–dc converter based on the matrix-type cycloconverter was proposed in the 2000s [5]. However, due to the hard switching and the high voltage stress exerted on the switches, it has not been widely adopted in engineering applications. The dual active bridge (DAB) converter can achieve a wide conversion ratio by using extended phase shift (EPS) [7], dual-phase shift (DPS) [7], and triple phase shift (TPS) [8], which are derived by the optimization method to achieve the minimum root mean square (rms) current or the peak current in the transformer. In [9], an efficiency-oriented automatic TPS modulation approach is proposed. This method utilizes the neural network combined with particle swarm optimization and fuzzy inference systems (FIS) to achieve the real-time TPS modulation. However, it requires considerable time to collect simulation and experimental data, and the optimal strategy for each specific operating condition must be derived individually through the optimization algorithm, resulting in a complex optimization process. In addition, online continuous modulation necessitates a supplementary FIS implementation stage. A five-degree-of-freedom (5-DOF) modulation scheme is proposed in [10] to improve the efficiency. Although the increased degrees of freedom provide more flexibility, the steady-state analysis and control of this method are extremely complicated. Meanwhile, it does not achieve a significant efficiency improvement compared to the TPS modulation. Therefore, a single-phase single-stage ac–dc converter composed of a DAB

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converter and an unfolder rectifier is proposed in [11], [12], [13], and [14]. In [11], the converter operates in multiple working modes for the zero-voltage switching (ZVS) and low conduction loss. However, the control strategy is based on a lookup table calculated offline. The triangle current modulation can achieve soft switching for the single-stage ac–dc converter [12], but the converter can only work in boost mode. A DPS control with variable switching frequency is proposed to achieve the unity power factor (PF) and soft switching [13]. Wide frequency variation poses difficulty in electromagnetic compatibility design. A TPS control combining four working modes is implemented in the DAB ac–dc converter for the ZVS and minimum conduction loss. The ac input current is controlled by the analytical expression without the need for current loop control [14]. The TPS control can achieve global optimal control with minimum current stress and wide ZVS performance. Compared to dc–dc converters, the modulation strategy for ac–dc converters involves significantly greater complexity. Implementing 5-DOF modulation schemes would further exacerbate control challenges in such topologies.

Based on the phase shift control in the DAB converter, a three-phase matrix-type single-stage ac–dc converter is presented in [15]. The phase shift control combined with the space vector pulse width modulation (SVPWM) can control the input grid current. The optimization of the three-phase single-stage isolated ac–dc converter mainly focuses on reducing conduction losses, minimizing switch losses, achieving unity PF, and improving power quality. The working mode featuring the four-level square waveform on the primary side and the two-level square waveform on the secondary side is presented in [15]. An analysis of the modulation scheme is carried out to enhance the efficiency. However, since the primary side waveform is a four-level square waveform, rather than a typical symmetrical two-level or three-level waveform, model optimization becomes more difficult compared to that in the single-phase DAB ac–dc converter. Consequently, it is challenging to obtain an analytical solution. To simplify the analytical modulation scheme, the current in the transformer is designed to operate in the discontinuous conduction mode (DCM) [16]. However, the current stress will become larger in high-power applications. In [17], the minimum rms of the transformer current is selected as the optimization objective. The optimal control trajectory is implemented by using a lookup table derived from the offline calculation, which lacks flexibility for wide output voltage regulation. In [18] and [19], the relationship between the modulation index and the phase shift angle under the current stress is obtained by establishing the mathematical model of the transformer current. In these control strategies, the duty cycle is fixed, so the conduction loss is not globally optimized. Hence, the efficiency is not high enough. The single-phase shift control is applied to the SVPWM [20]. However, the converter will experience large conduction losses and hard switching. In [21], a dual-period space vector modulation (SVM) based on the trapezoidal waveform modulation is proposed to decouple the transformer currents. The space vector is analytically calculated in real-time, but the converter fails to achieve ZVS. An improved control strategy for the matrix-type single-stage ac–dc converter is proposed to reduce the total harmonic distortion (THD) of the input side current and improve the current quality [22], [23]. In [24], a dedicated space-vector-modulation scheme and commutation method are proposed for safe operation of the matrix converter (MC) in wind energy conversion system. A novel PWM switching technique is proposed for a bidirectional MC in [25]. The proposed technique can control the input dc current and to inject a sinusoidal three-phase current to the grid at unity PF.

Based on the previous studies, it can be found that the control of three-phase single-stage isolated ac–dc converters merely focuses on one or two optimization objectives and thus fails to achieve multiobjective global optimization, which encompasses ZVS, minimum current stress, high power quality, etc. In the modulation scheme, only one or two working modes are implemented, preventing the attainment of higher efficiency. Moreover, the optimal working modes associated with the space vector cannot be analytically solved, so the precise optimal modulation and control strategies are difficult to calculate in real-time. These issues impede the further improvement of efficiency for three-phase single-stage isolated ac–dc converters.

In this article, the circuits of the three-phase single-stage matrix-type isolated ac–dc converter can be equivalent to the DAB converter under different working conditions. Therefore, the working modes in the matrix-type ac–dc converter can be simplified. The optimal working mode under the TPS control strategy is introduced, and the optimal analytical solutions for the duty cycle and phase shift angle corresponding to different working modes can be obtained. The contributions of this article are presented in the following.

1) This article proposes a current vector modulation scheme based on the optimized working modes for the DAB converters, which has not been implemented in the three-phase single-stage matrix-type isolated ac–dc converter before. Because of the complexity of the circuit and control strategy, most previous works have had difficulty in achieving ZVS for all the switches. The merits of transient dc bias current suppression and global ZVS are seldom discussed in other previous works on three-phase matrix ac–dc converters. The proposed control strategy can achieve ZVS for all the switches by reducing the transient dc bias current, thereby significantly reducing the switching loss.
2) Although the optimized working modes are applied in this article, it is also difficult to derive the expression of the working mode because of excessive working mode combinations for the current vector modulation. This is also the key issue in the other previous works, which is why the offline calculation was previously adopted for the modulation scheme of the three-phase single-stage matrix-type isolated ac–dc converter. To calculate the optimized working mode in real-time rather than relying on the look-up table calculated offline, an iteration algorithm is proposed in this article to simplify the modulation scheme. Furthermore, it is easy to implement this algorithm in the digital controller.

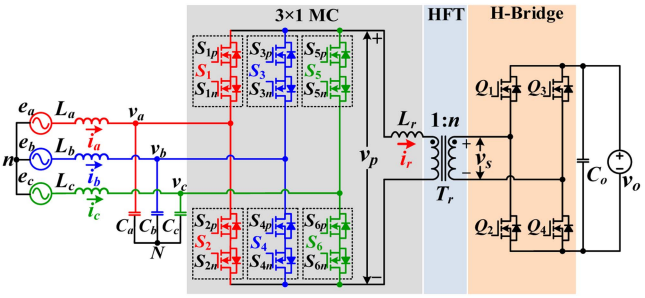


Fig. 1. Circuit topology of the three-phase single-stage matrix-type isolated AC–DC converter.

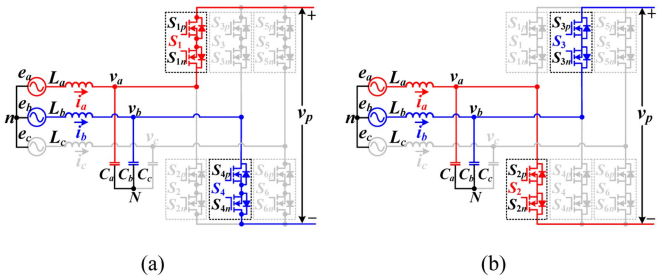


Fig. 2. Working state of the MC. (a) $v_p = v_{ab}$. (b)v_p = -v_{ab}.

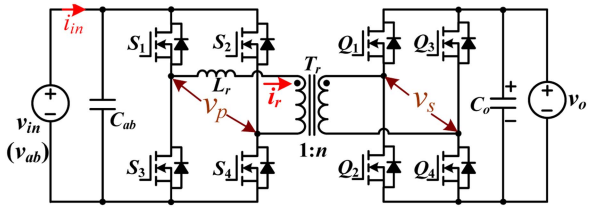


Fig. 3. Equivalent circuit of three-phase single-stage isolated AC–DC converter.

TABLE I
SPACE VECTORS IN MC

space vectors	Switching States						v_{in}
	S_1	S_2	S_3	S_4	S_5	S_6	
I_1	1	0	0	0	0	1	v_{ac}
I_2	0	0	1	0	0	1	v_{bc}
I_3	0	1	1	0	0	0	v_{ba}
I_4	0	1	0	0	1	0	v_{ca}
I_5	0	0	0	1	1	0	v_{cb}
I_6	1	0	0	1	0	0	v_{ab}
I_7	1	1	0	0	0	0	0
I_8	0	0	1	1	0	0	0
I_9	0	0	0	0	1	1	0

The organization of this article is as follows. In Section II, the current SVM is introduced, and the equivalent DAB circuit of the three-phase single-stage isolated ac–dc converter is presented. In Section III, the optimal working mode of DAB converters under the TPS control strategy is reviewed. Subsequently, a control strategy is proposed to achieve the vector combination of two adjacent switching periods, followed by an analysis of the dead zone logic for vector switching. In addition, a single voltage loop control strategy is proposed. In Section IV, the control of transient dc bias current suppression is reviewed, and an improved modulation scheme for achieving ZVS is proposed. Section V presents the experimental results and compares the efficiency of the two control strategies. The experimental results demonstrate the effectiveness and high efficiency of the improved modulation strategy. Finally, Section VI summarizes this article.

II. SVM CONTROL

A. Circuit of the Single-Stage Three-Phase AC–DC Converter Based on DAB

Fig. 1 illustrates the circuit of the three-phase single-stage matrix-type isolated ac–dc converter. This converter comprises a 3×1 MC, a high-frequency transformer (HFT) donated as T_r, a series inductor L_r, and an H-bridge converter. In the MC, each pair of switches consists of two switches connected in reverse series, which serves to control the bidirectional current flow. The MC transforms the input three-phase ac voltage into the high-frequency ac voltage v_p on the primary side of the HFT, and the voltage v_s is converted into the dc voltage v_o by the H-bridge converter. i_r represents the series inductor current.

To simplify the working mode, the current vector in the matrix-type ac–dc converter can be converted to a DAB converter. Taking the switches in phases A and B as an example for analysis in a switching period, Fig. 2 illustrates the working states of the MC. When the switches S_{1p}, S_{1n} S_{4p}, and S_{4n} are turned ON, v_p is equal to v_{ab}. When the switches S_{2p}, S_{2n}, S_{3p}, and S_{3n} are turned ON, v_p is equal to -v_{ab}. Therefore, the circuit depicted in Fig. 2 can be equivalent to a full bridge. The matrix ac–dc converter operating in the working mode shown in Fig. 2 is equivalent to a DAB converter, as illustrated in Fig. 3. When switches S_1 and S_4 are turned ON, the circuit is equivalent to Fig. 2(a). When S_2 and S_3 are turned ON, the circuit is equivalent to Fig. 2(b). In this case, the input voltage v_{in} is equal to v_{ab}.

When phases A and C are taken into account, the equivalent circuit can also be regarded as a DAB converter. In this case, the input voltage of the equivalent DAB converter is v_{ac}. The input voltage v_{in} can also be equal to v_{ba}, v_{ac}, v_{ca}, v_{bc}, and v_{cb}.

B. Space Vector Modulation

To guarantee the continuous flow path in the series inductor current and preclude the occurrence of short circuit between the phase voltage, only one upper bridge arm and one lower bridge arm must be turned ON. The state of the switches is presented in the following equation:

$$S_i = \begin{cases} 1, & \text{turn on} \\ 0, & \text{turn off} \end{cases} \quad \text{where } (i = 0, \ldots, 6)$$

$$\begin{cases} S_1 + S_3 + S_5 = 1 \\ S_2 + S_4 + S_6 = 1 \end{cases}. \tag{1}$$

The power input from ac to dc is defined as forward power. Table I shows the states of the switches corresponding to each current vector and the equivalent input voltage v_{in}.

The direction of the current vector space diagram is shown in Fig. 4. Each current vector corresponds to an input line-to-line

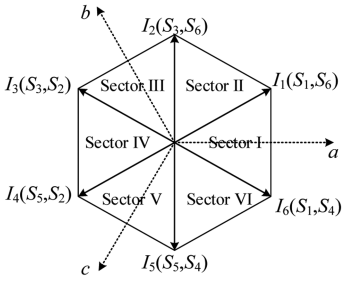


Fig. 4. Direction of the current space vectors.

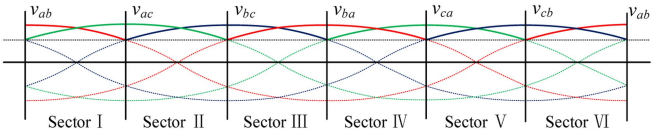


Fig. 5. Waveforms of AC-side input voltage in the entire line frequency period.

TABLE II
VECTOR ALLOCATION FOR EACH SECTOR

Sector	I	II	III	IV	V	VI
Vector I	I_6	I_2	I_2	I_4	I_4	I_6
Vector II	I_1	I_1	I_3	I_3	I_5	I_5

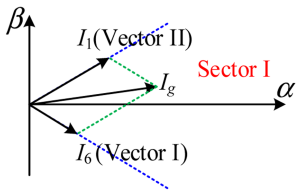


Fig. 6. Grid input current vector in Sector I.

voltage, so the effective voltage of the ac-side input voltage during the entire line frequency period is shown in Fig. 5.

The input grid current vector is obtained by the synthesis of two adjacent vectors shown in Table I. The two adjacent vectors in each sector are defined as Vector I and Vector II. To ensure the smooth transition of vectors during sector switching, the allocation of the current vectors in each sector is shown in Table II.

The vector diagram in Sector I is shown in Fig. 6. The grid input current vector I_g can be synthesized by controlling the amplitude of Vector I and Vector II. On the contrary, the amplitude of the Vector I and Vector II can be calculated by the grid input vector. Vector synthesis in other sectors is analyzed in the same method. Therefore, controlling the input grid current is equivalent to controlling the amplitude of the space vectors.

III. Single Loop Control of the Three-Phase Single-Stage Isolated AC–DC Converter

A. Optimal Working Mode of the DAB DC–DC Converter

TPS control in the DAB converter can achieve high efficiency and wide ZVS, thereby enabling the attainment of global optimal working modes [8]. In this article, the minimum peak current in

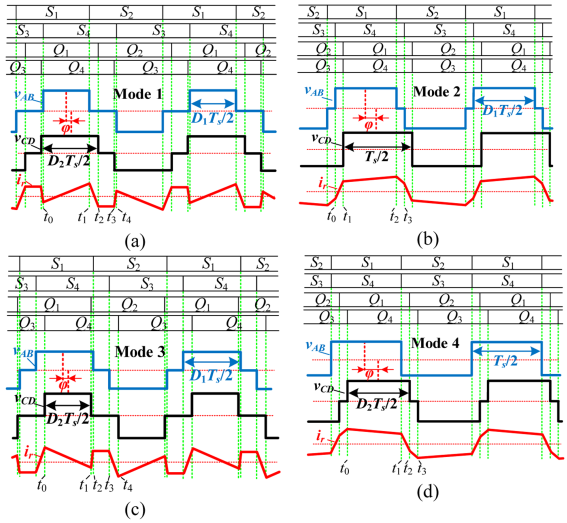


Fig. 7. Key waveforms of TPS. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

the transformer and ZVS of all the switches are the optimal objectives. With regard to the equivalent DAB dc–dc converter in Fig. 3, the previous research has demonstrated that the four working modes of DAB converters illustrated in Fig. 7 can fulfill the requirements of optimal working modes [8]. Specifically, these four working modes are capable of covering the entire range of load power, allowing the converter to achieve minimal conduction loss and extensive ZVS. The formula for the optimization of the minimum peak current can be expressed as in (2), i.e., the peak current in the transformer gets the minimum value on the premise that the output power meets the load requirement p^*. Simultaneously, the current amplitude in the transformer at the commutation time complies with the ZVS constraints. Previous studies have also indicated that the peak current is correlated with the conduction loss of the DAB converters [26]. In the TPS control for DAB converters, the conduction loss resulting from the implementation of the minimum peak current optimization is highly comparable to that obtained through the minimum rms current optimization [26]. However, the practical implementation of the minimum peak current optimization is simpler than that of the minimum rms current optimization. Consequently, the minimum peak current optimization is adopted in this article. I_{zvs1} and I_{zvs2} represent the minimum current amplitude required to charge and discharge the junction capacitors of the switches for the ZVS. The analysis of I_{zvs1} and I_{zvs2} can be found in [8] and [27]. Ignoring the nonlinearity of the junction capacitor of the switches, I_{zvs1} and I_{zvs2} can be approximately evaluated as$I_{\text{zvs1}} = 2v_{\text{in}}C_{\text{oss1}}/t_{\text{dead}}$ and $I_{\text{zvs2}} = 2v_oC_{\text{oss2}}/t_{\text{dead}}$, where C_{oss1} is the output capacitor of switches S_1–S_6, and C_{oss2} is the output capacitor of switches Q_1–Q_4. v_{in} is equal to the input voltage of the equivalent DAB converter shown in Fig. 3, and v_o is the output voltage of the DAB converter

$$\begin{cases} \text{Min}[i_{\text{peak}}(D_1, D_2, \varphi)] \\ \text{Subject to } P(D_1, D_2, \varphi) = p* \\ |i_r(Q_1 - Q_8)| \geq I_{\text{ZVS1}} \text{ or } I_{\text{ZVS2}} \end{cases}. \tag{2}$$

TABLE III
OPTIMAL TPS CONTROL STRATEGY

Working mode		Range of φ_s ($\varphi_s = 2\varphi/\pi$)	Expression of φ_s	Expression of D_1 and D_2
$M \leqslant 1$	Mode 1	$0 < \varphi_s \leqslant \varphi_{b1}$ where $\varphi_{b1} = 1 - M$	$\varphi_s = \sqrt{\left(\frac{2nL_rI_{ZVS1}}{v_oT_s}\right)^2 + \frac{1}{2}\cdot\frac{1-M}{M}y_i} - \frac{2nL_rI_{ZVS1}}{v_oT_s}$ (8)	$\begin{cases} D_1 = \frac{M}{1-M}\left(\varphi_s + \frac{4nL_rI_{ZVS1}}{v_oT_s}\right) \\ D_2 = \frac{D_1}{M} + \frac{4n^2L_rI_{ZVS2}}{v_oT_s} \end{cases}$ (7)
	Mode 2	$\varphi_{b1} < \varphi_s \leqslant 1$	$\varphi_s = 1 - \sqrt{\frac{1-y_i}{2-2/M+1/M^2}}$ (10)	$\begin{cases} D_1 = \frac{2M-1}{M} + \frac{1-M}{M}\varphi_s \\ D_2 = 1 \end{cases}$ (9)
$M > 1$	Mode 3	$0 < \varphi_s \leqslant \varphi_{b2}$ where $\varphi_{b2} = 1 - \frac{1}{M}$	$\varphi_s = \sqrt{\left(\frac{2L_rI_{ZVS2}}{v_{in}T_s}\right)^2 + \frac{1}{2}\cdot(M-1)y_i} - \frac{2L_rI_{ZVS2}}{v_{in}T_s}$ (12)	$\begin{cases} D_2 = \frac{1}{M-1}\left(\frac{4nL_rI_{ZVS2}}{v_{in}T_s} + \varphi_s\right) \\ D_1 = MD_2 + \frac{4L_rI_{ZVS1}}{v_{in}T_s} \end{cases}$ (11)
	Mode 4	$\varphi_{b2} < \varphi_s \leqslant 1$	$\varphi_s = 1 - \sqrt{\frac{1-y_i}{M^2-2M+2}}$ (14)	$\begin{cases} D_2 = (2-M) + (M-1)\varphi_s \\ D_1 = 1 \end{cases}$ (13)

The conversion ratio is defined as $M = v_o/(n\cdot v_{\text{in}})$, where v_{in} and v_o are the input and output voltages of the DAB converter, respectively. D_1, D_2, and φ represent the duty cycles and phase shift angle of the two full bridges, with φ ranging from $-\pi/2$ to $\pi/2$. T_s stands for the switching period. The DAB converter is capable of achieving bidirectional power flow. Fig. 7 only shows the key waveforms of the forward power flow. Because of the symmetry of the bidirectional power flow, there also exist four working modes in the reverse power flow, in which the phase shift angle φ is negative. In this article, the working modes in the forward power flow are taken as examples for the analyses. Because of the symmetry, the reverse power flow can be analyzed using a similar method. When $M \leq 1$, the converter operates in Mode 1 and Mode 2. When $M > 1$, the converter works in Mode 3 and Mode 4. The optimal formula can be solved by the Karush-Kuhn-Tucker method. The results of the optimal solutions for the four working modes are presented in the expressions of D_1 and D_2 in Table III, which can be referred to in [8]. Because of the space limitation, the detailed derivation of the optimal working modes will not be elaborated in this article. By controlling D_1, D_2, and φ, these four modes can achieve soft switching, reduce the peak of transformer current, and lower current stress.

Taking Mode 1 shown in Fig. 7(a) as an example, the input current of the equivalent DAB converter shown in Fig. 3 is defined as i_{in}, which is expressed as follows:

$$i_{\text{in}} = \frac{P}{v_{\text{in}}} = \frac{v_oT_s}{8nL_r}\cdot 2D_1\frac{2\varphi}{\pi}. \tag{3}$$

Defining $I_{\text{base}} = v_oT_s/(8nL_r)$, the normalized input current amplitude of the DAB converter in per unit (p.u.) is defined as y_i, which can be expressed as $i_{\text{in}}/I_{\text{base}}$. φ_s is defined as $2\varphi/\pi$ ($|\varphi| \leq \pi/2$). Equation (3) can be rewritten as follows:

$$y_i = 2D_1\varphi_s. \tag{4}$$

To achieve ZVS, it is necessary to control the minimum current value at the commutation time for the ZVS. The expressions of D_1 and D_2 of Mode 1 in optimal TPS control are expressed as (5), referred to in [14]

$$\begin{cases} D_1 = \frac{M}{1-M}\left(\varphi_s + \frac{4nL_rI_{\text{ZVS1}}}{v_oT_s}\right) \\ D_2 = \frac{D_1}{M} + \frac{4n^2L_rI_{\text{ZVS2}}}{v_oT_s} \end{cases}. \tag{5}$$

The phase shift angle in Mode 1 can be obtained by combining expressions (4) and (5), as shown in (6). If the normalized input current amplitude y_i is set, the working mode of the equivalent DAB converter can be determined

$$\varphi_s = \sqrt{\left(\frac{2nL_rI_{\text{ZVS1}}}{v_oT_s}\right)^2 + \frac{1}{2}\cdot\frac{1-M}{M}y_i} - \frac{2nL_rI_{\text{ZVS1}}}{v_oT_s}. \tag{6}$$

The derivation method of the phase shift angle expression for Mode 2, Mode 3, and Mode 4 is the same as that for Mode 1. The expressions for D_1, D_2, and φ_s in different working modes are shown in Table III. The expressions of φ_s in Table III build the relationship between the input current amplitude and the working modes of the DAB converter. Therefore, the normalized input current of the DAB converter in a switching period can be regarded as the current amplitude of the space vectors.

The detailed flowchart of the working mode selection for the equivalent DAB converter is shown in Fig. 8. The value of v_{in} can be referred to in Table I. The current vector in Sector I can be decomposed to I_6 and I_1. In this scenario, v_{in} is selected as either v_{AB} or v_{AC}. Based on the range of the calculated φ_s, the working mode of the equivalent DAB converter can be determined.

B. SVM Based on Optimal Working Modes

To apply the optimal working modes of the DAB converter to the SVM, the amplitude of Vector I and Vector II, which are obtained from the grid input current vector, are implemented in two adjacent switching periods, respectively. The distribution of Vector I and Vector II in different sectors is shown in Table II. The two vectors obtained through decomposition can be controlled by the equivalent DAB converter depicted in Fig. 3. Taking Sector I for example, the line-to-line voltage within Sector I is illustrated in Fig. 9(a), while the vector decompositions for

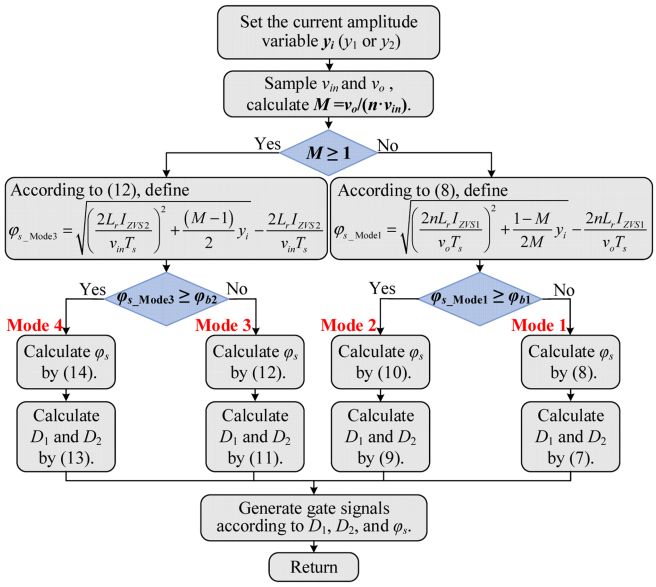


Fig. 8. Working mode selection for the equivalent DAB converter.

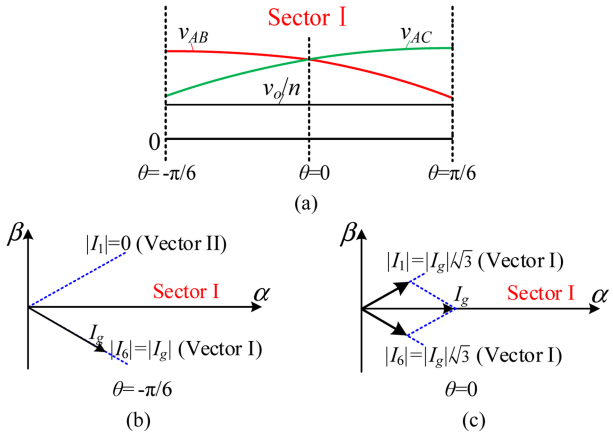


Fig. 9. Vector decomposition example in Sector I: (a) $\theta = -\pi/6$. (b) $\theta = 0$.

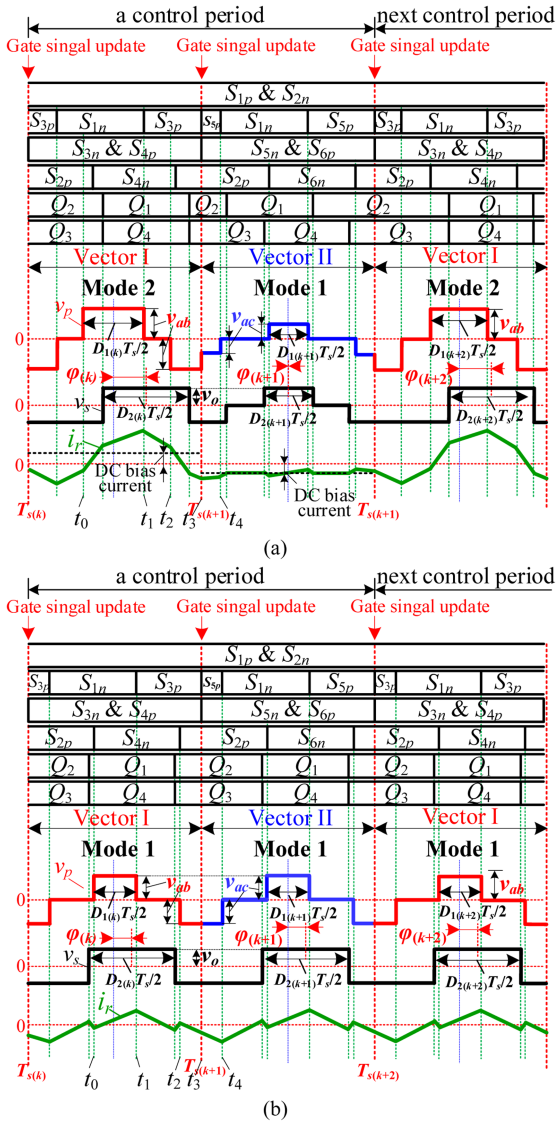


Fig. 10. Waveforms of the adjacent switching periods. (a) $\theta = -\pi/6$. (b) $\theta = 0$.

the phase of $-\pi/6$ and 0 are shown in Fig. 9(b) and Fig. 9(c), respectively. To simplify the subsequent analysis of the vector decomposition, it is assumed that v_o/n is less than v_{AB} and v_{AC} in Sector I, as illustrated in Fig. 9(a). Therefore, the equivalent DAB converter only works in Mode 1 or Mode 2. When the three-phase current vector is located in Sector I, it can be decomposed into I_6 and I_1. The current vector I_6 (Vector I) corresponds to the direction of the line-to-line voltage v_{ab}, and the current vector I_1 (Vector II) corresponds to the direction of the line-to-line voltage v_{ac}. Therefore, Fig. 9(a) only depicts the waveforms of v_{ab} and v_{ac}. θ represents the angle of the grid current vector I_g. The amplitude of I_6 and I_1 can be controlled by the working modes of the DAB converter in two adjacent switching periods. The magnitudes $|I_1|$ and $|I_6|$ can be regarded as the input current of the equivalent DAB converter shown in Fig. 3, respectively. The input voltage of the equivalent DAB converter can be set as v_{ab} and v_{ab} in the two adjacent switching periods, respectively. One control period is illustrated in Fig. 10. Every two adjacent switching periods are designated as a control period for synthesizing the grid current vector. When $\theta = -\pi/6$, the direction of I_g is identical to that of the current vector I_6. As depicted in Fig. 9(b), the amplitude of I_6 is $|I_g|$, and the amplitude of $|I_1|$ is 0. When the normalized amplitude of the grid current vector is 0.8, y_1 (normalized amplitude of Vector I) is 0.8 and y_2 (normalized amplitude of Vector II) is 0. The key waveforms of the isolated MC for $\theta = -\pi/6$ are presented in Fig. 10(a), where $\varphi_{(k)}$, $D_{1(k)}$, and $D_{2(k)}$ are the phase shift angle and duty cycles in kth switching period. Vector I (i.e., current vector I_6) may work in Mode 2, and Vector II (i.e., current vector I_1) may work in Mode 1. Since $|I_1|$ is equal to 0, the phase shift angle $\varphi_{(k+1)}$ is also equal to 0. As seen in Fig. 10(a), the amplitude of v_p in Vector I is v_{ab}, and that in Vector II is v_{ac}. When $\theta = 0$ as shown in Fig. 9(c), $|I_6|$ is equal to $|I_g|/\sqrt{3}$ and $|I_1|$ is also equal to $|I_g|/\sqrt{3}$. When the normalized amplitude of the grid current vector is equal to 0.8, $y_1 = y_2 = 0.4619$. The key waveforms of the isolated MC for $\theta = 0$ are presented in Fig. 10(b). As seen in Fig. 9(a), v_{AB} is equal to v_{AC} when $\theta = 0$. Therefore,

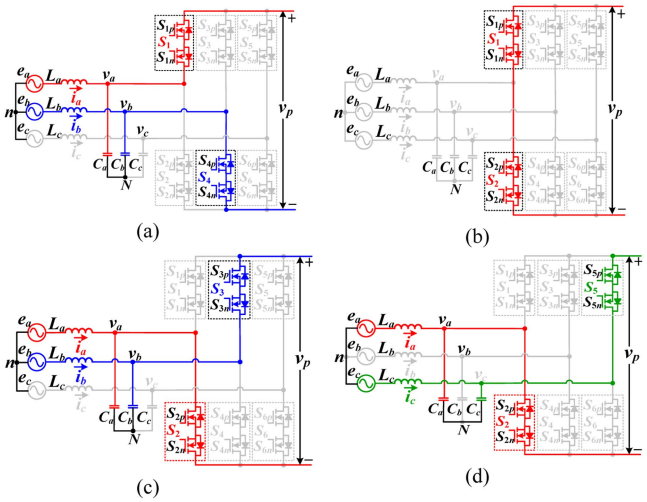


Fig. 11. Working state of the MC. (a) t_0–t_1. (b) t_1–t_2. (c) t_2–t_3. (d) t_3–t_4.

the amplitudes of v_p in Vector I and Vector II are the same. In Sector I, v_a is greater than v_b and v_c in Sector I, so v_{ab} and v_{ac} are greater than zero. Therefore, S_{1p} and S_{2n} can be conducted in the whole Sector I. Although S_{1p} and S_{2n} are turned ON in the whole Sector I, there will be no short circuit between the line-to-line voltages. In each sector, there are two switches conducted in the whole sector, which can also reduce the switching loss. The other switches are working at high switching frequencies.

Ignoring the deadband, the equivalent circuit diagram from t_0 to t_4 in Fig. 10 is shown in Fig. 11. At t_3, S_{3p}, S_{3n}, and S_{4p} are turned off, and S_{5p}, S_{5n}, and S_{6p} are turned ON. Vector I is switched to Vector II, and the amplitude of v_p is switched from $v_{a\ b}$ to $v_{a\ c}$. The input voltage of the equivalent DAB converter (shown in Fig. 3) is switched from $v_{a\ b}$ to $v_{a\ c}$. For the other sectors, the same analysis can be derived in the same method.

The aforementioned analysis is based on the premise that v_o/n is less than v_{AB} and v_{AC} in Sector I. When v_o/n is larger than v_{AB} or v_{AC}, the working mode in Vector I and Vector II can also operate in Mode 3 or Mode 4. The selection of the working mode has been elaborated in Fig. 8.

In Sector I, y_1 and y_2 are designated as (15), where I_{base} has been defined in Section III-A. y_1 and y_2 are obtained from the decomposition of the normalized input grid current vector, which is depicted in Fig. 6. In terms of the analysis presented in Section III-A, the working mode of Vector I and Vector II can be calculated by y_1 and y_2 (i.e., y_i as shown in Fig. 8)

$$\begin{cases} y_1 = |I_6|/I_{\text{base}} \\ y_2 = |I_1|/I_{\text{base}} \end{cases}. \tag{15}$$

When the input voltage is set at 200 V/50 Hz, along with $v_o = 200$ V, $L_r = 20\ \mu$H, $n = 0.98$, and $T_s = 20\ \mu$s. The working-mode indices of Vector I and Vector II in Sector I and Sector II for different output power are presented in Fig. 12. Fig. 12(a) shows the distribution of the mode for an output power of 750 W, where the normalized amplitude of the grid current vector y is 0.25. Fig. 12(b) shows the distribution of the mode for an output power of 1500 W, where y is 0.5. As the output power increases, Mode 1 is superseded by Mode 2.

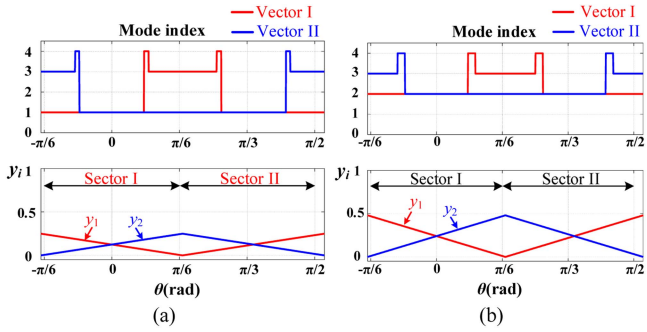


Fig. 12. Curves of the modes distribution for Vector I and Vector II. (a) 750 W ($y = 0.25$). (b) 1500 W ($y = 0.5$).

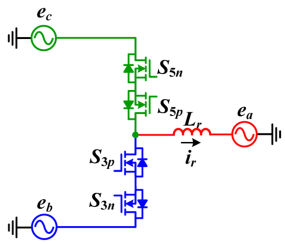


Fig. 13. Equivalent circuit diagram for vector switching.

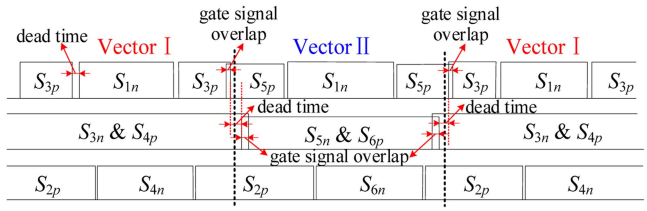


Fig. 14. Sequence of switches in the first half of Sector I.

C. Dead Zone for Vector Switching

During vector switching, the dead zone is necessary to preclude the short circuit between the phase voltage and the open circuit of the series inductor. Taking the instance of t_3 in Fig. 10 as an example, the working mode is switched from Vector I to Vector II. The upper bridge arm of Phase B is turned OFF, while the upper bridge arm of Phase C starts to turn ON. The equivalent circuit diagram is depicted in Fig. 13, and the gate signals of the switches are presented in Fig. 14. When v_b is lower than v_c in Sector I, S_{5p} is turned ON first. The body diode of S_{5n} is reverse-biased, and the current flows through S_{3p} and S_{3n}. Then, S_{3p} is turned OFF. When the series inductor current is positive, it flows through S_{3n} and the body diode of S_{3p}. When the series inductor current is negative, it flows through S_{5p} and the body diode of S_{5n}. After a deadband interval, S_{5n} is turned ON, and the voltage of the body diode of S_{3p} is reverse-biased. The current flows through S_{5p} and S_{5n}. Finally, after the overlap of the gate signals, S_{3n} is turned OFF, and the vector switching is completed. Fig. 14 also illustrates the switching from Vector II to Vector I. When Vector II is switched to Vector I, S_{3n} is turned ON

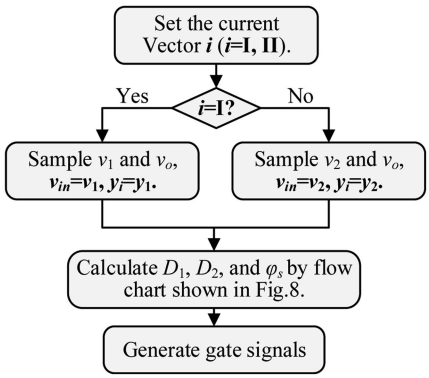


Fig. 15. Flowchart of the modulation scheme.

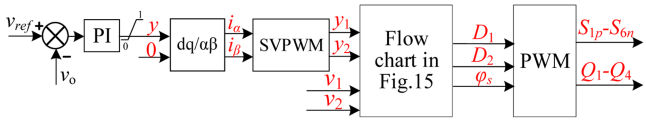


Fig. 16. Control diagram.

first, and the body diode of S_{3p} is reverse-biased. Subsequently, S_{5n} is turned OFF. When the series inductor current is positive, it flows through S_{3n} and the body diode of S_{3p}. When the series inductor current is negative, it flows through S_{5p} and the body diode of S_{5n}. After a deadband, S_{3p} is turned ON, and the current flows through S_{3p} and S_{3n}. After the overlap of the gate signals, S_{5p} is turned OFF. The vector switching from Vector II to Vector I is completed. The vector switching in the other sectors can be implemented in the same method.

D. Control Strategy

Fig. 15 shows the flowchart of the modulation scheme. The input voltage associated with Vector I is defined as v_1, while the input voltage associated with Vector II is defined as v_2. The input voltage of Vector I and Vector II can be referred to in Table I. The duty cycle and phase shift angle in the switching period are calculated by the flowchart shown in Fig. 8. Finally, the gate signals are generated.

Fig. 16 shows the control diagram, which represents a single-loop control without the need for the input current sample. The error between the output voltage and the voltage reference serves as the input of the proportional-integral (PI) controller. The output of the PI controller is defined as y, which is further defined as the normalized amplitude of the input grid current vector. The amplitudes y_1 and y_2 of Vector I and Vector II can be obtained by the inverse Park transform and SVM. In this process, the inputs of the d-q-axes in the inverse park transform are set as $i_d = y$ and $i_q = 0$. y_1 and y_2 correspond to the normalized input current of the DAB converter in two adjacent switching periods. D_1, D_2, and φ_s are calculated based on the flowchart of the control algorithm depicted in Fig. 15. Finally, the gate signals are obtained. By setting $i_q = 0$, the unity PF can be achieved, and the control strategy can be significantly simplified through the implementation of the single-loop control.

IV. Improved Modulation Scheme With Suppression of Transient DC Bias Current

A. Transient DC Bias Current Issue

As seen in Fig. 10(a), the series inductor current i_r at the end of Vector I serves as the initial current of Vector II at t_3. Because of the disparity in the initial series inductor currents of the two vectors, a transient dc bias current is induced during the vector transition. A control period is constituted by the two adjacent switching periods. The average current of the series inductor during the two adjacent switching periods should be equal to zero when the load power remains constant. Provided that the amplitudes of Vector I and Vector II are different, there must be a transient dc bias current in each switching period. As illustrated in Fig. 10(a), when the amplitude of Vector I is greater than that of Vector II, the transient dc bias current in Vector I is greater than zero and that in Vector II is less than zero. Conversely, when the amplitude of Vector I is less than that of Vector II, the transient dc bias current in Vector I is less than zero, and that in Vector II is greater than zero. In addition, this transient dc bias current cannot be mitigated by a dc-blocking capacitor in series with L_r. As shown in Fig. 10(a), if a dc-blocking capacitor is connected in series with L_r to block the dc bias current, the capacitor is charged with its voltage rising during the first switching period (Vector I) because of the positive dc bias current; while in the second switching period (Vector II), it is discharged because of the negative dc bias current, leading to a reduction in its voltage. Because the transient dc bias current in Vector I is equal to the negative of the transient dc bias current in Vector II, the average voltage of the dc-blocking capacitor must be equal to zero in a control period. Therefore, this transient dc bias current cannot be mitigated by a dc-blocking capacitor in series with L_r. The prior ZVS analyses of the working mode are based on the symmetric current waveform without a transient dc bias current in a switching period. Due to the presence of the transient dc bias current, some switches will lose the ZVS condition, thereby increasing the switching loss. As seen in the waveforms of Vector I in Fig. 10(a), $i_r(t_0)$ is greater than zero, so S_{4n} must work in hard switching. As seen in the waveforms of Vector II in Fig. 10(a), the currents at the commutation time are nearly all less than zero, so Q_1, Q_4, and S_{5p} work in hard switching in Vector II. Furthermore, the dc bias current will cause more conduction loss, thereby diminishing the efficiency of the converter. Analyzed in the same method, the transient dc bias current will exist in every switching period. The converter also loses the ZVS performance.

B. Suppression of Transient DC Bias Current for All ZVS

Authors' prior work in [28] has demonstrated that the series inductor current i_r at the beginning, middle, and end of a switching period is only determined by the phase shift angle φ. The key waveform for the DAB dc–dc converter without dc bias current in Mode 1, as illustrated in Fig. 17, is taken as an example for analysis. The starting time of the switching period is defined as t_0 and the midpoint time is t_{0m}.

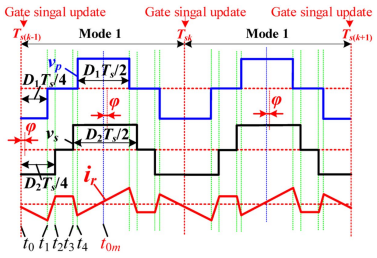


Fig. 17. Steady-state working waveform of Mode 1 for the DAB converter.

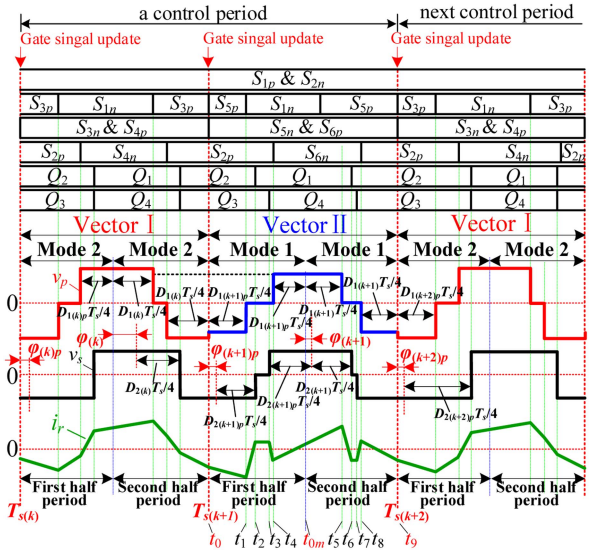


Fig. 18. Waveform of Mode 2 switching to Mode 1 without transient DC bias current in Sector I.

When the DAB dc–dc converter operates in a steady state, the transformer current is symmetry within a switching period. Consequently, the transformer current expression at t_0 and t_{0m} can be derived, as presented in (16) [28]. The same conclusion can be drawn for the other working modes

$$I_{r0m} = -I_{r0} = \frac{v_o T_s}{4nL_r}\left(\frac{2\varphi}{\pi}\right). \tag{16}$$

Fig. 18 shows the waveform of the mode transfer from Mode 2 to Mode 1 when the gate signal is updated at $T_{s(k+1)}$ without transient dc bias current in Sector I. The gate signals in the other sectors can be analyzed using the same method. To suppress the transient dc bias current, a switching period is partitioned into the first and second halves of the switching period, as depicted in Figs. 18 and 19. The transient dc bias current is suppressed in the first half period. In the second half period, the converter works in the working mode corresponding to the steady state. The duty cycle of the first half period in the kth switching period is defined as $D_{1(k)p}$ and $D_{2(k)p}$, and the phase shift angle is $\varphi_{(k)p}$. For the second half period in the kth switching period, the duty cycle is defined as $D_{1(k)}$ and $D_{2(k)}$, and the phase shift angle is $\varphi_{(k)}$. The duty cycle and phase shift angle of the first half period and the second half period are different, so they may work in different modes. It is assumed that the first and second half periods work in the same mode to simplify the analysis. In the absence of the

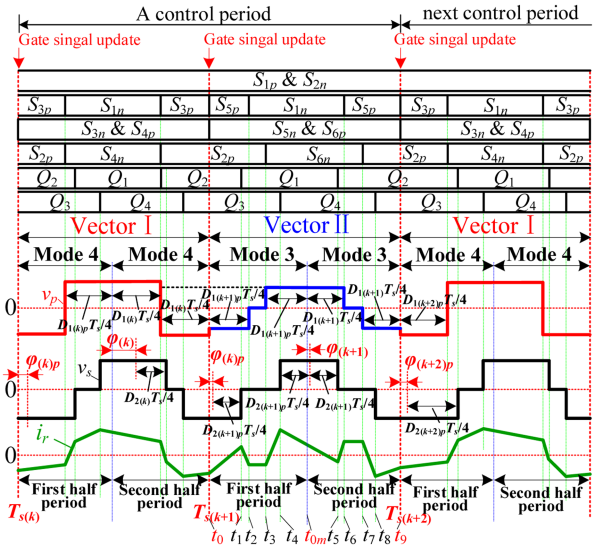


Fig. 19. Waveform of Mode 4 switching to Mode 3 without transient DC bias current in Sector I.

transient dc bias current, the current expressions I_{r0}, I_{r0m}, and I_{r9} at t_0, t_{0m}, and t_9 must be expressed as follows:

$$\begin{cases} I_{r0} = -\frac{v_o T_s}{4nL_r}\left(\frac{2\varphi_{(k)}}{\pi}\right) \\ I_{r0m} = -I_{r9} = \frac{v_o T_s}{4nL_r}\left(\frac{2\varphi_{(k+1)}}{\pi}\right) \end{cases}. \tag{17}$$

The current expression at time t_{0m} can be obtained according to the following equation:

$$\begin{aligned} I_{r0m} &= I_{r0} + \int_{t_0}^{t_{0m}} i_r(t) \\ &= I_{r0} - \frac{nv_{\text{in}} - v_o}{nL_r}(t_1 - t_0) + \frac{v_o}{nL_r}(t_2 - t_1) \\ &\quad - \frac{v_o}{nL_r}(t_4 - t_3) + \frac{nv_{\text{in}} - v_o}{nL_r}(t_{0m} - t_4) \\ &= \frac{v_o(2\varphi_{(k+1)p} - \varphi_{(k)})T_s}{2\pi nL_r}. \end{aligned} \tag{18}$$

Without the dc bias current, I_{r0m} in (18) must be equivalent to the expression presented in (17). Consequently, the expression of $\varphi_{(k+1)p}$ can be derived based on (17) and (18), as depicted in the following equation:

$$\varphi_{(k+1)p} = \frac{\varphi_{(k)} + \varphi_{(k+1)}}{2}. \tag{19}$$

Fig. 19 shows the waveform of mode transfer from Mode 4 to Mode 3 when the gate signals are updated at $T_{s(k+1)}$, provided that there is no transient dc bias current. Analyzed in the same method, the same constraint as that in (19) can be deduced for the mode transition from Mode 4 to Mode 3. In this case, the transient dc bias current can be suppressed. Without a transient dc bias current, the converter will meet the ZVS constraints. The other mode transition can be analyzed in the same manner, and the same conclusion can be drawn. Hence, they will not be elaborated on in detail.

C. ZVS Analysis in the First Half Period

Because of the disparity between the current value in the first and second halves of the switching period, the soft switching conditions of the first half period of Mode 1 and Mode 3 will be modified.

Fig. 18 illustrates Mode 1 without the transient dc bias current. In the absence of the transient dc bias current, the current value at time t_0 is I_{r0}, as presented in (17). The current expression of the series inductor at the commutation time in the first half of the switching period, ranging from t_0 to t_{0m}, is shown in the following equation:

$$\begin{cases} I_{r1} = -\frac{v_o\varphi_{(k)}T_s}{2\pi nL_r} - \frac{(n\cdot v_{in}-v_o)D_{1(k+1)p}T_s}{4nL_r} \\ I_{r2} = I_{r3} = \frac{v_o(\varphi_{(k+1)p}-\varphi_{(k)})T_s}{2\pi nL_r} + \frac{(v_oD_{2(k+1)p}-n\cdot v_{in}D_{1(k+1)p})T_s}{4nL_r} \\ I_{r4} = \frac{v_o(2\varphi_{(k+1)p}-\varphi_{(k)})T_s}{2\pi nL_r} + \frac{D_{1(k+1)p}(v_o-nv_{in})T_s}{4nL_r} \\ I_{r0m} = \frac{v_o(2\varphi_{(k+1)p}-\varphi_{(k)})T_s}{2\pi nL_r} \end{cases}. \tag{20}$$

As depicted in Fig. 18, the expression for the average input current during the first half period is presented in (21), where $\varphi_{s(k+1)p} = 2\varphi_{(k+1)p}/\pi$

$$i_{\text{in\_}(k+1)p} = \frac{v_oT_s}{16nL_r}\cdot 2D_{1(k+1)p}\varphi_{s(k+1)p}. \tag{21}$$

By defining $I_{\text{base\_}kp} = v_oT_s/(16nL_r)$, the normalized input current during the first half period in kth switching period is designated as $y_{(k)p}$, which is expressed as $i_{\text{in\_}(k)p}/I_{\text{base\_}kp}$. Therefore, (21) can be rewritten as follows:

$$y_{(k+1)p\_\text{Mode1}} = 2D_{1(k+1)p}\varphi_{s(k+1)p}. \tag{22}$$

The value of i_r at t_2 and t_3 should be less than -I_{zvs1} for the switches of the MC to achieve ZVS, and the value of i_r at t_4 should be greater than n·I_{zvs2} for the switches of the H-bridge to achieve ZVS. The ZVS conditions of Mode 1 in the first half switching period are presented in the following equation:

$$\begin{cases} I_{r4} = \frac{v_o(2\varphi_{(k+1)p}-\varphi_{(k)})T_s}{2\pi nL_r} + \frac{D_{1(k+1)p}(v_o-nv_{in})T_s}{4nL_r} \le -I_{zvs1} \\ I_{r2} = I_{r3} = \frac{v_o(\varphi_{(k+1)p}-\varphi_{(k)})T_s}{2\pi nL_r} + \frac{(v_oD_{2(k+1)p}-nv_{in}D_{1(k+1)p})T_s}{4nL_r} \\ \quad \ge n\cdot I_{zvs2} \end{cases}. \tag{23}$$

The increased current required for achieving ZVS may lead to additional conduction loss. As indicated in (23), to achieve ZVS while minimizing conduction loss, I_{r4} should be equal to -I_{zvs1}, and I_{r2} should be equal to n·I_{zvs2}. Therefore, the expressions of duty cycle $D_{1(k+1)p}$ and $D_{2(k+1)p}$ in the first half of the switching period can be expressed as presented in (24), where $\varphi_{s(k)} = 2\varphi_{(k)}/\pi$

$$\begin{cases} D_{1(k+1)p} = \frac{M}{1-M}\left(\frac{4nL_rI_{\text{zvs1}}}{v_oT_s} + \varphi_{s(k+1)}\right) \\ D_{2(k+1)p} = \frac{D_{1(k+1)p}}{M} + \frac{4n^2L_rI_{\text{zvs2}}}{v_oT_s} - (\varphi_{s(k+1)p} - \varphi_{s(k)}) \end{cases}. \tag{24}$$

The deduction process for Mode 3 without transient dc bias current in the first half of the switching period is similar to Mode 1. The expressions of current amplitude and duty cycle in the first half of the switching period of Mode 3 are presented in (25) and (26). The detailed derivation will not be elaborated on

$$y_{(k+1)p\_\text{Mode3}} = 2D_{2(k+1)p}\varphi_{s(k+1)p} \tag{25}$$

$$\begin{cases} D_{1(k+1)p} = M\cdot D_{2(k+1)p} + \frac{4L_rI_{\text{zvs1}}}{v_{in}T_s} + M(\varphi_{s(k+1)p} - \varphi_{s(k)}) \\ D_{2(k+1)p} = \frac{1}{M-1}\left(M\cdot\varphi_{s(k)} + \frac{4nL_rI_{\text{zvs2}}}{v_{in}T_s}\right) - \varphi_{s(k+1)p} \end{cases}. \tag{26}$$

Mode 2 and Mode 4 without the transient dc bias current possess inherent ZVS performance. Provided that the transient dc bias current is suppressed, the converter operating in Mode 2 and Mode 4 can meet the ZVS in wide output power. Therefore, the duty cycle expressions of Mode 2 and Mode 4 in the first half of the switching period are identical to those in the steady state analyses, as presented in (9) and (13), respectively. The current amplitude expressions of Mode 2 and Mode 4 in the first half period of k-th switching period are shown in (27) and (28)

$$y_{(k)p\_\text{Mode2}} = 2D_{1(k)p} - D_{1(k)p}^2 - (\varphi_{s(k)p} - 1)^2 \tag{27}$$

$$y_{(k)p\_\text{Mode4}} = 2D_{2(k)p} - D_{2(k)p}^2 - (\varphi_{s(k)p} - 1)^2. \tag{28}$$

Through the calculation of the duty cycles $D_{1(k)p}$ and $D_{2(k)p}$ for suppressing the transient dc bias current, it can not only ensure that the second half period operates in the optimal working modes but also enable the first half period meet the ZVS constraints, thereby reducing the turn-ON loss.

D. Control Strategy of Improved Modulation

The normalized average current of a vector within a switching period has been defined as y_i ($i = 12$) in Section II. In accordance with the analysis presented in Section VI-C, the input current during the first half period is defined as $y_{(k)p}$, while that in the second half period is defined as $y_{(k)}$. Both $y_{(k)p}$ and $y_{(k)}$ in an entire switching period determine the amplitude of the space vector y_i. Therefore, $y_{(k)}$ and $y_{(k)p}$ in a switching period must satisfy the constraint (29)

$$y_{(k)}\cdot\frac{T_s}{2} + y_{(k)p}\cdot\frac{T_s}{2} = y_i\cdot T_s \tag{29}$$

$$y_{(k)} = 2y_i - y_{(k)p}. \tag{30}$$

Based on the previous analysis, the phase shift angle and input current of the first and second halves of the switching period can be derived by solving (31), where functions f_1 and f_2 can be expressed as the formulas of $P/(v_{\text{in}}\cdot I_{\text{base}})$, which can be derived based on the same method shown in (3), (4), and (5). Since the expressions of $y_{(k)}$ and $y_{(k)p}$ in different working modes are also different, solving (31) requires taking into account the four working modes (shown in Fig. 7) of the first and second halves of the switching period, respectively, which will significantly increase the complexity of the calculation

$$\begin{cases} \varphi_{(k)p} = \frac{\varphi_{(k)}+\varphi_{(k-1)}}{2} \\ y_{(k)p} = f_1(\varphi_{(k)p}) \\ y_{(k)} = f_2(\varphi_{(k)}) \\ y_{(k)} + y_{(k)p} = 2y_i \end{cases}. \tag{31}$$

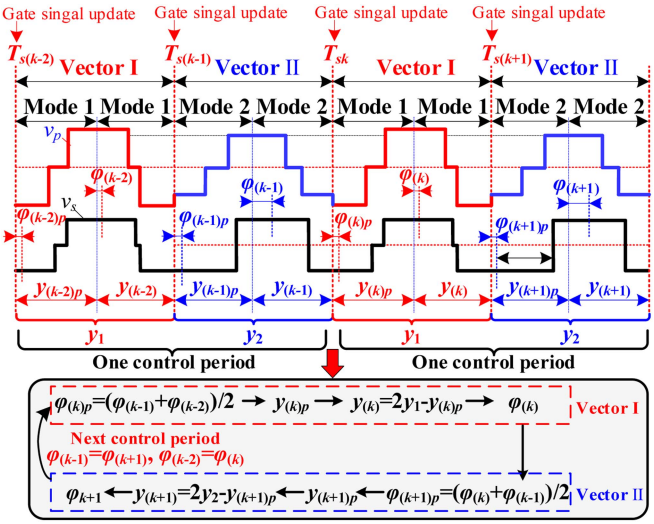


Fig. 20. Calculation flow of phase shift angle and current amplitude.

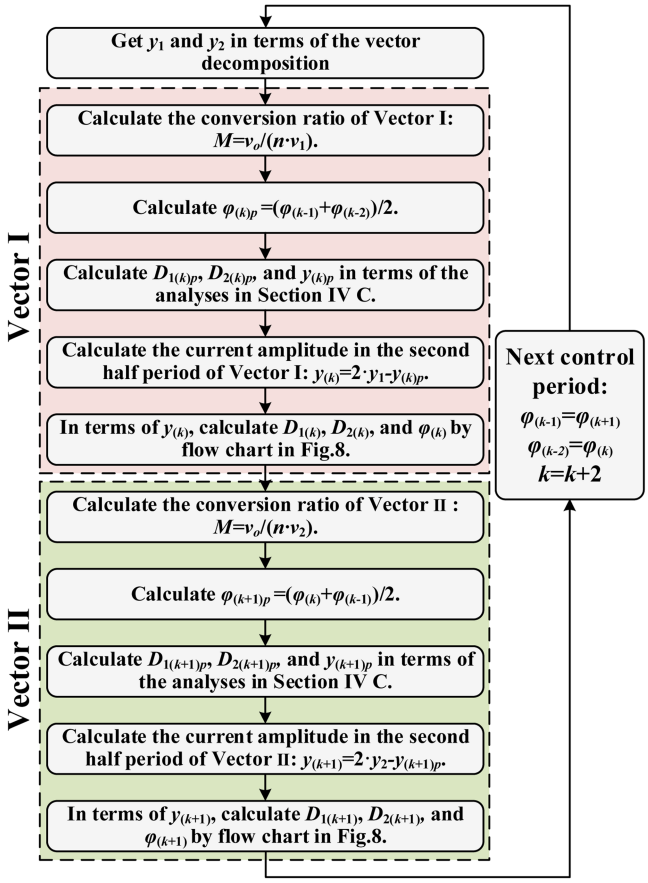


Fig. 21. Flowchart of the improved modulation scheme.

Because the switching frequency is sufficiently high, the vectors in kth and (k-2)th switching periods are approximately identical under steady-state conditions. $\varphi_{(k)}$ is approximately equal to $\varphi_{(k\text{-}2)}$. Therefore, $\varphi_{(k)p}$ in (31) can be revised to $(\varphi_{(k\text{-}1)}+\varphi_{(k\text{-}2)})/2$. The calculation process regarding the phase shift angle and current amplitude for kth and (k+1)th switching period is illustrated in Fig. 20. It should be noted that the control period is twice the switching period. In this algorithm, $\varphi_{(k)p}$ is determined by the phase shift angles in the previous two switching periods rather than the phase shift angles in the previous and current switching periods. This iteration algorithm serves to simplify the modulation scheme. The detailed flowchart of the improved modulation scheme is presented in Fig. 21. y_1 and y_2 represent the current amplitudes of Vector I and Vector II respectively. Within a control period, $\varphi_{(k)p}$ for Vector I is first calculated as $(\varphi_{(k\text{-}1)}+\varphi_{(k\text{-}2)})/2$. Based on $\varphi_{(k)p}$, the working modes during the first half period can be determined by the boundaries of the working mode shown in Table III. In terms of working mode determined by $\varphi_{(k)p}$, the current amplitude in the first half period of Vector I, i.e., $y_{(k)p}$, is calculated based on the analyses provided in Section IV-C. Then, $y_{(k)}$ is obtained from $2\cdot y_1$-$y_{(k)p}$. $D_{1(k)}$, $D_{2(k)}$, and $\varphi_{(k)}$ corresponding to the working mode of Vector I can be derived by following the flowchart shown in Fig. 8. That is, y_i in Fig. 8 is set as $y_{(k)}$. For Vector II, $\varphi_{(k+1)p}$ is calculated as $(\varphi_{(k)}+\varphi_{(k\text{-}1)})/2$, where $\varphi_{(k)}$ represents the phase shift angle of Vector I. The current amplitude in the first half period of Vector II, i.e., $y_{(k+1)p}$, is also calculated based on the analyses provided in Section IV-C. Then, $y_{(k+1)}$ is obtained from $2\cdot y_2$-$y_{(k+1)p}$. $D_{1(k+1)}$, $D_{2(k+1)}$, and $\varphi_{(k+1)}$ corresponding to the working mode of Vector II can be derived by following the flowchart shown in Fig. 8. That is, y_i in Fig. 8 is set as $y_{(k+1)}$. Within the current control period, the gate signals are generated based on the working mode of Vector I and Vector II. In the next control period, the same algorithm is implemented, and $\varphi_{(k)}$ and $\varphi_{(k+1)}$ will be used to calculate the phase shift angle during the first half period of Vector I and Vector II, respectively. Therefore, this algorithm can be regarded as an iteration algorithm. In the next control period, the index of the switching period is k+2. As depicted in the flowchart in Fig. 21, after the end of the flowchart, the process will return to the beginning of the flowchart for the next control period, where k is updated to k+2, $\varphi_{(k\text{-}1)}$ is assigned the value of $\varphi_{(k+1)}$, and $\varphi_{(k\text{-}2)}$ is assigned the value of $\varphi_{(k)}$. Based on the aforementioned iteration algorithm, the working modes can be derived in real-time without the need for the look-up table calculated offline. The iteration algorithm can reduce the complexity of the modulation scheme.

When the amplitude of Vector I and Vector II differ significantly, $y_{(k)}$ may be a negative value. For example, if $y_1 < y_{(k)p}/2$, $y_{(k)}$ will become negative. In this case, the phase shift angle $\varphi_{(k)}$ is less than 0 in the second half of the switching period, which corresponds to the reverse power flow of the DAB converter. Because of the symmetry of the forward and reverse power flows, the four working modes in reverse power flow can be symmetrical to the working mode depicted in Fig. 7, and they are designated as Mode -1, Mode -2, Mode -3, and Mode -4. In reverse power flow, the phase shift angle and the duty cycle of the working modes can be obtained similarly to the expression presented in Table III. The working modes and expressions in reverse power flow will not be elaborated on in detail in this article.

Fig. 22 shows the 3-D modulation surfaces of $y_{(k)p}$ and $y_{(k)}$ versus the normalized amplitude and angle of the input current

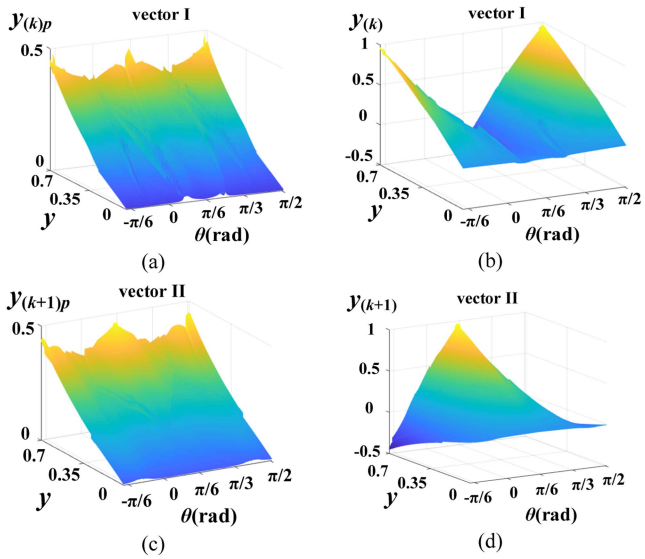


Fig. 22. Three-dimensional modulation surfaces of $y_{(k)p}$ and $y_{(k)}$ in vector I and $y_{(k+1)p}$ and $y_{(k+1)}$ in Vector II versus the phase angle θ and y. (a) $y_{(k)p}$ in Vector I. (b) $y_{(k)}$ in Vector I. (c) $y_{(k+1)p}$ in Vector II. (d) $y_{(k+1)}$ in Vector II.

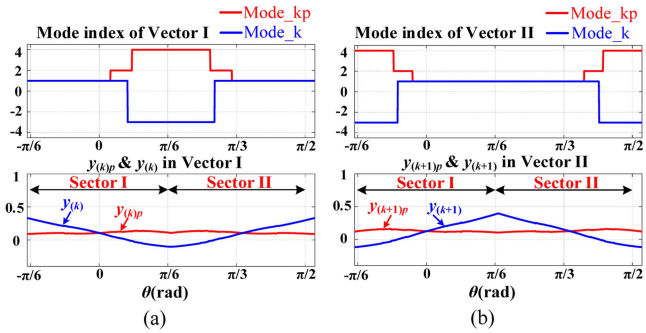


Fig. 23. Working modes, y_{kp} and y_k in Vector I and Vector II for 750 W load power ($y = 0.25$). (a) Vector I. (b) Vector II.

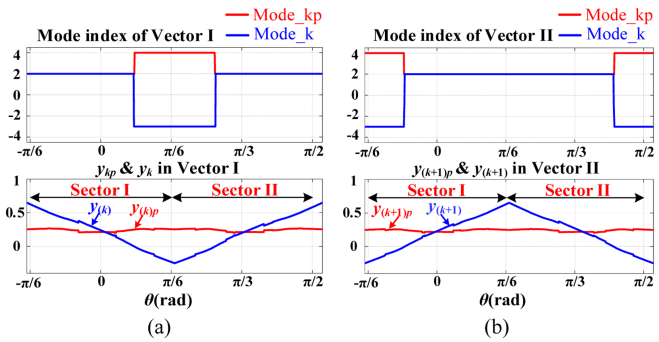


Fig. 24. Working modes, y_{kp} and y_k in Vector I and Vector II for 1500 W load power ($y = 0.5$). (a) Vector I. (b) Vector II.

vector from Sector I to Sector II, where the input line-to-line rms voltage is 200 V/50 Hz, $v_o = 200$ V, $L_r = 20\ \mu$H, $n = 0.98$, and $T_s = 20\ \mu$s. Fig. 23 shows the curves of the working modes, $y_{(k)p}$ and $y_{(k)}$ versus the angle of the input current vector from Sector I to Sector II, when the output power is 750 W (where $y = 0.25$). Fig. 24 shows the curves from Sector I to Sector II, when the load power is 1500 W (where $y = 0.5$). Because

TABLE IV
COMPARISONS OF STRATEGIES FOR THE THREE-PHASE SINGLE-STAGE MATRIX-TYPE ISOLATED AC–DC CONVERTERS

	Current mode	Solution of the strategy	Control strategy	Soft switching	Complexity
[17]	DCM+CCM	Offline Calculation	TPS	Global Soft Switching	High
[18]	CCM	Real-time	EPS	Not Global Soft Switching	Moderate
[19]	DCM	Real-time	TPS	Not Global Soft Switching	Low
[21]	DCM	Real-time	TPS	Not Global Soft Switching	Low
This work	CCM	Real-time	TPS	Global Soft Switching	Moderate

$\varphi_{(k)p}$ is determined by the average phase shift angle in the two previous second-half periods, $y_{(k)p}$ varies in a small range. In Sector I, $y_{(k)}$ in Vector I is decreasing, and $y_{(k+1)}$ in Vector II is increasing. In Sector II, $y_{(k)}$ in Vector I is increasing, and $y_{(k+1)}$ in Vector II is decreasing. The distribution of working modes in the other sectors follows a similar pattern.

Table IV shows the comparisons of the control strategies for three-phase single-stage matrix-type isolated ac–dc converters. In [17], the current mode constitutes a combination of DCM and continuous conduction mode (CCM). The modulation scheme in [17] relies on offline calculation. Offline calculation is based on numerical solutions, so a precise model of the converter should be built. The implementation for each input and output voltage should be designed individually. For a wide conversion ratio, a greater number of lookup tables need to be stored in the digital controller. It is less flexible for a wide conversion ratio. If the lookup table is extensive, a significant amount of time will be consumed in querying it. Therefore, the scheme presented in [17] is of greater complexity. In [19] and [21], the current in the series inductor operates in DCM, which leads to a large peak current for high-power applications. In [19] and [21], the current in the transformer exhibits a triangular or trapezoidal waveform. The duty cycle and phase shift angle are calculated in real-time, so the complexity of the control strategies is low. In [18], the control strategy is also based on the minimum peak current in the EPS control. However, the duty cycle of the secondary full bridge is fixed at 0.5, which does not represent the globally optimal working mode. The conduction loss is also large. The implementation is more complex compared to that of the triangular or trapezoidal waveform, but the complexity of the control strategy in [18] is moderate. In [18], [19], and [21], the full ZVS performance cannot be achieved, which gives rise to higher turn-ON losses of the switches. In contrast, the proposed control strategy in this article is capable of achieving ZVS for all the switches. Furthermore, the modulation scheme is implemented in real-time without the need for offline calculation. Therefore, the design and implementation of the control strategy are flexible. Among the aforementioned control strategies, dual control loops with the inner current loop are necessary. However, the proposed control strategy involves only a single voltage loop, thereby rendering the control structure simpler. The proposed

TABLE V
DETAILED SPECIFICATIONS

Items	Symbol	Parameter
RMS line-to-line AC voltage	v_{abc}	200V/50Hz
Output voltage	v_o	200V
Turns ratio of the transformer	n	0.98
Switching frequency	$f_s(T_s)$	50kHz (20μs)
Switches	$S_{1p\text{-}6n}$, $Q_{1\text{-}4}$	C3M0045065D
Series inductor	L_r	20μH
Output voltage regulator capacitance	C_o	470μF
Input filter capacitance	C_a, C_b, C_c	9.4μF

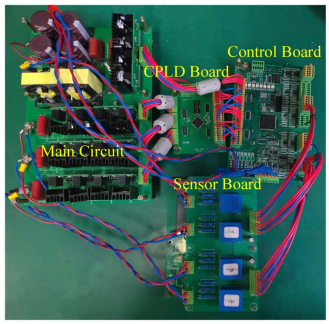


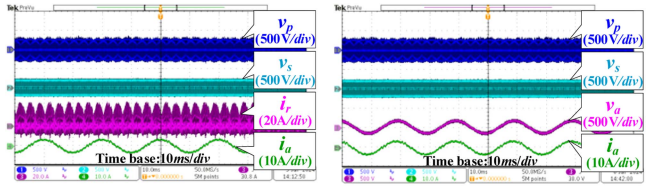
Fig. 25. Experimental prototype for test.

control strategy is based on the optimal working modes of the TPS control, so the implementation of the modulation scheme is more complex than that in [19] and [21]. Therefore, the complexity of the proposed control strategy is categorized as moderate. Although the proposed control strategy depicted in Fig. 21 appears to involve many steps, all the calculations are simple arithmetic operations. Furthermore, the calculation processes for Vector I and Vector II are identical. Therefore, they are readily implemented in the digital controller. The proposed control strategy can meet a wide conversion ratio and is easily implemented in practical applications.

V. EXPERIMENTAL VALIDATION

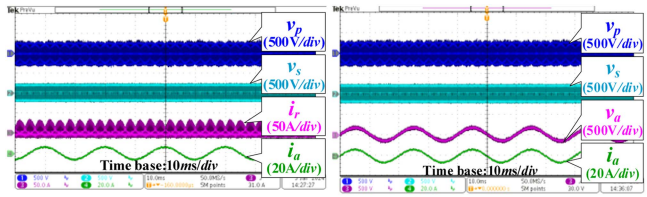
A prototype with a rated load power of 1.5 kW was built to verify the control strategy. The detailed specifications are presented in Table V. The control strategy and modulation strategy are implemented in a digital signal processor (DSP) TMS320F28377, and the signal output by the DSP is processed in a complex programmable logic device EPM240T100C5N to generate the gate signals for the ac–dc converter. The experimental prototype for the test is shown in Fig. 25. The switching frequency of the experiment is 50 kHz, and the control and sampling frequency is 25 kHz.

This section is partitioned into two parts. In the first part, the SVM based on the optimal working mode modulation strategy will be verified. In the second part, the improved strategy without a transient dc bias current will be validated.



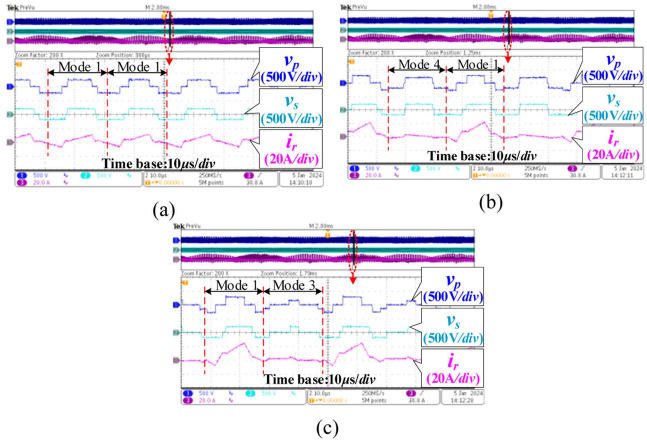
(a) (b)

Fig. 26. Waveforms in 800 W load power. (a) Full bridge voltages and transformer current. (b) Voltage and current of Phase A.



(a) (b)

Fig. 27. Waveforms in 1500 W load power. (a) Full bridge voltages and transformer current. (b) Voltage and current of Phase A.



(a) (b) (c)

Fig. 28. Zoomed-in waveforms in 800 W load power. (a) Mode 1/Mode 1. (b) Mode 1/Mode 4. (c) Mode 1/Mode 3.

A. Optimal Working Mode in TPS

Fig. 26 shows the waveforms under a load power of 800 W. Fig. 26(a) shows the full-bridge voltages and series inductor current. The envelope curve of the primary voltage v_p of the transformer coincides with the ac side input line voltage presented in Fig. 5. Fig. 26(b) presents the input voltage and current of phase A. It can be observed that the input voltage is in phase with the input current, which demonstrates the unity PF. Fig. 27 shows the waveforms under a power load of 1500 W. As the power increases, both the series inductor current and the grid current rise accordingly. The phases of voltage and current also demonstrate the unity PF.

Fig. 28 depicts the working modes of the two adjacent switching periods within a sector when the load power is 800 W. Fig. 29 shows the working modes of the two adjacent switching periods within a sector under a load power of 1500 W. As the load power increases, Mode 1, which is applicable under lower load power conditions, is gradually replaced by Mode 2.

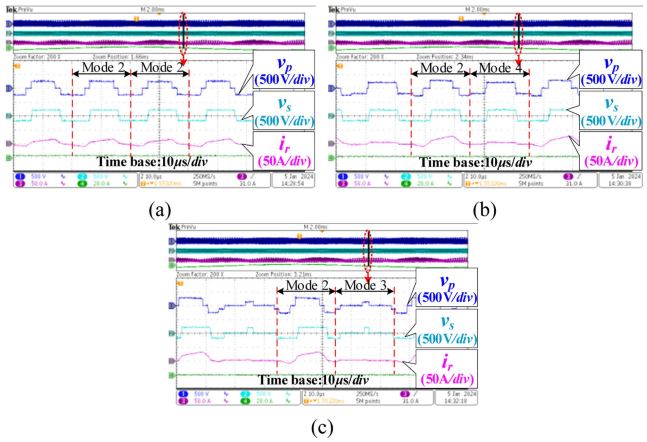


Fig. 29. Zoomed-in waveforms in 1500 W load power. (a) Mode 2/Mode 2. (b) Mode 2/Mode 4. (c) Mode 2/Mode 3.

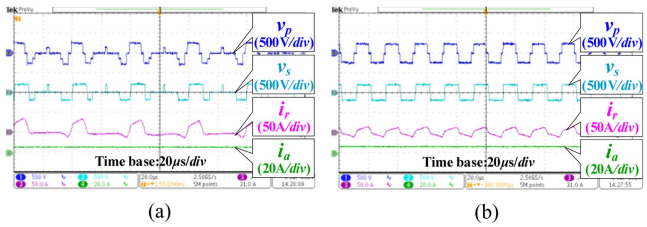


Fig. 30. Zoomed-in waveforms in 1500 W load power. (a) Waveforms at sector switching. (b) Waveforms in the middle of the sector.

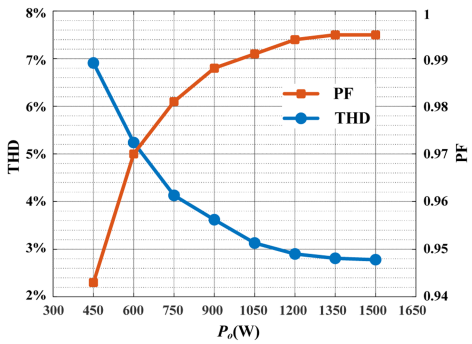


Fig. 31. PF and THD of the grid current.

Fig. 30(a) and (b) illustrates the zoomed-in waveforms during a sector switching and in the middle of a sector when the load power is 1500 W. During the sector-switching process, the amplitudes of the two vectors reach their maximum and zero values, respectively. When the vector amplitude is zero, the duty cycles and the transformer current tend to approach zero. Because of the presence of the transient dc bias current, the series inductor current becomes less than zero when the vector amplitude is zero. It will cause hard switching. When the grid current vector is located in the middle of the sector, the amplitudes of the two vectors are equal, and the duty cycles and phase shift angles of the two adjacent switching periods remain the same.

Fig. 31 shows the curves of THD of the grid current and power factor (PF) versus the load power. When the load power reaches 1500 W, the THD is 2.78% and the PF is 0.995. It demonstrates

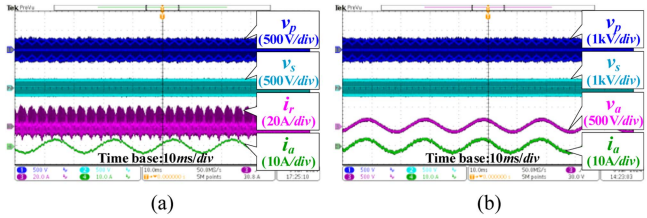


Fig. 32. Waveforms in 800 W load power without DC bias current. (a) Full bridge voltages and transformer current. (b) Voltage and current of Phase A.

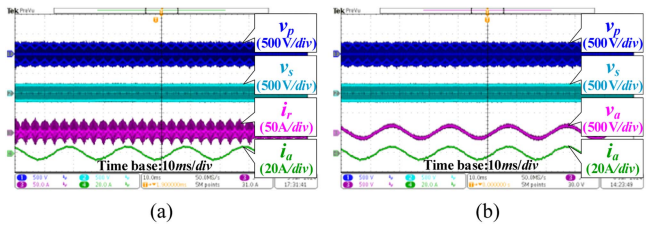


Fig. 33. Waveforms in 1500 W load power without DC bias current. (a) Full bridge voltages and transformer current. (b) Voltage and current of Phase A.

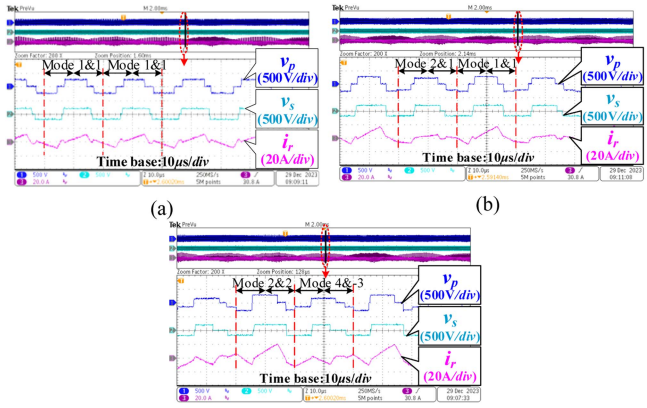


Fig. 34. Zoomed-in waveforms in 800 W load power without DC bias current. (a) (Mode 1, Mode 1)/(Mode 1, Mode 1). (b) (Mode 1, Mode 1)/(Mode 2, Mode 1). (c) (Mode 2, Mode 2)/(Mode 4, Mode -3).

that the proposed control strategy can achieve low THD and higher power factor without the inner current loop control.

B. Improved Strategy Without Transient DC Bias Current

Figs. 32 and 33 illustrate the waveforms in the absence of dc bias current under load powers of 800 W and 1500 W. In Fig. 32(b) and (b), the A-phase input voltage is in phase with the grid current, which further demonstrates the unity power factor.

Figs. 34 and 35 illustrate the zoomed-in waveforms of mode combinations in the absence of dc bias current within a sector under load powers of 800 W and 1500 W, respectively. The experimental results verify the mode distributions depicted in Fig. 23 and Fig. 24. During a switching period, the improved modulation scheme can reduce the transient dc bias current.

Fig. 36 illustrates the ZVS performance of the switch S_{1p} in a line frequency period. During the commutation, the current in the series inductor is larger than zero to discharge the junction

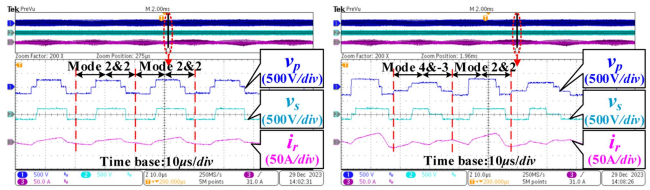


Fig. 35. Zoomed-in waveforms in 1500 W without DC bias current. (a) (Mode 2, Mode 2)/(Mode 2, Mode 2). (b) (Mode 4, Mode -3)/(Mode 2, Mode 2).

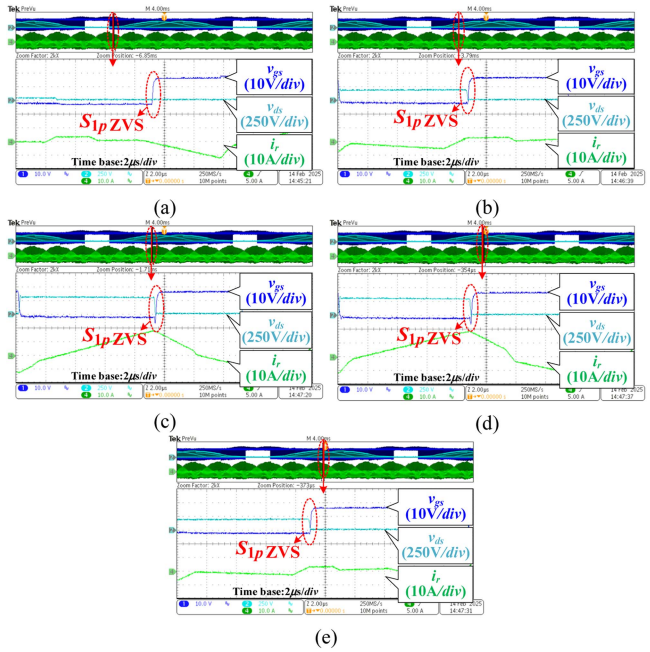


Fig. 36. (a)–(e) Gate signal and drain-source voltage of switch S_{1p} in different phase angles.

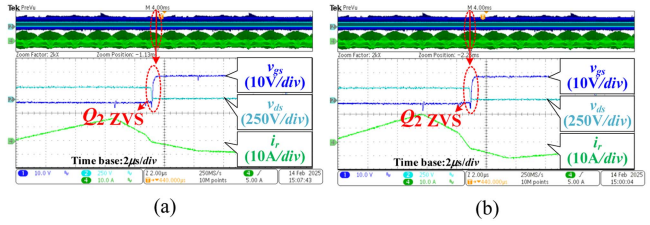


Fig. 37. (a) and (b) Gate signal and drain-source voltage of switch Q_2 in different phase angles.

capacitor of S_{p1}. The waveform of the gate signal and drain-source voltage indicates that S_{1p} can achieve ZVS throughout the entire line frequency period, thereby reducing the switching loss. Given that the working mode of the MC is periodic, the other switches in the MC also work in ZVS. Figs. 37 and 38 depict the ZVS performance of the switches Q_2 and Q_3 in the secondary H bridge during half of a line frequency period, which demonstrates the ZVS of the switches on the secondary side of the transformer. As seen in Figs. 37 and 38, the series inductor current is less than zero during the dead time, which also indicates that the junction capacitors of Q_2 and Q_3 are discharged for the ZVS.

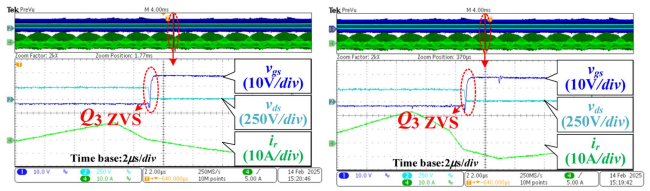


Fig. 38. (a) and (b) Gate signal and drain-source voltage of switch Q_3 in different phase angles.

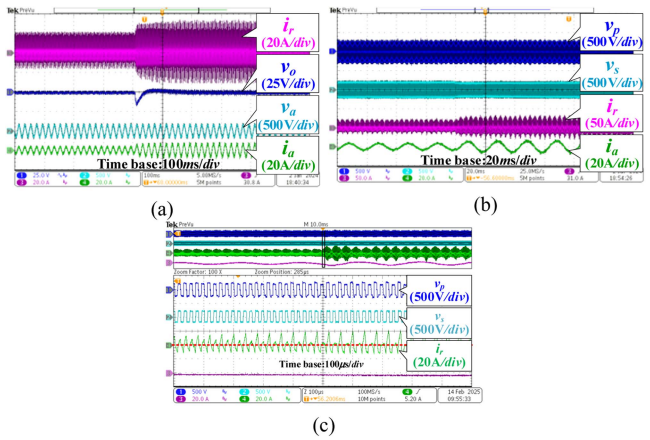


Fig. 39. Dynamic waveforms under the load step change from 800 W load power to 1500 W load power. (a) Output voltage. (b) Series inductor current and grid current. (c) Zoomed-in waveforms of Fig. 39(b).

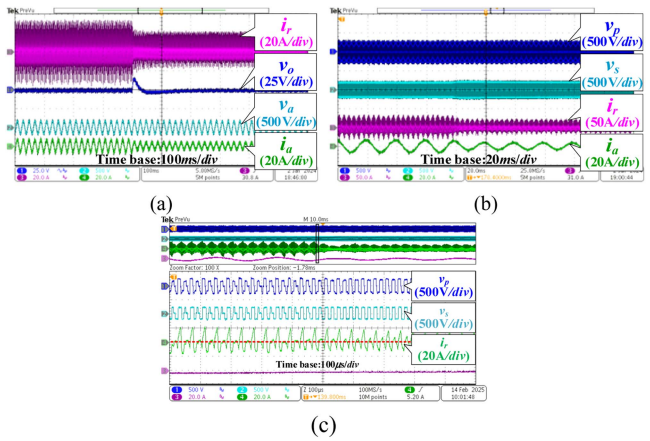


Fig. 40. Dynamic waveforms under the load step change from 1500 W load power to 800 W load power. (a) Output voltage. (b) Series inductor current and grid current. (c) Zoomed-in waveforms of Fig. 40(b).

Figs. 39 and 40 illustrate the dynamic waveforms under the load step change. For the load step change with different load powers, the transformer current undergoes a smooth transition, and the input side current maintains a sinusoidal waveform, which further demonstrates the effectiveness of the control strategy. Fig. 39(c) depicts the zoomed-in waveforms of Fig. 39(b), and Fig. 40(c) depicts the zoomed-in waveforms of Fig. 40(b). During the dynamic response, the dc bias current is also effectively suppressed. The experimental results demonstrate that the control strategy is effective in dynamic response.

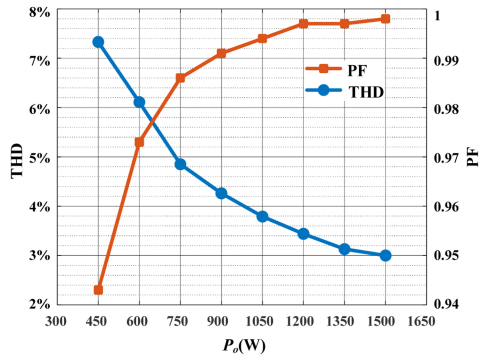


Fig. 41. PF and THD of the grid current with improved modulation.

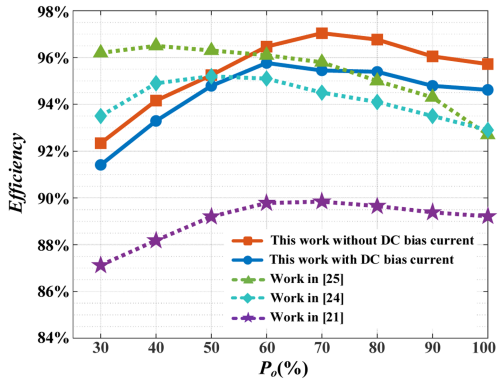


Fig. 42. Experimental efficiency curves.

Fig. 41 illustrates the curves of THD and PF versus the output power with the improved modulation scheme. When the load power is 1500 W, the THD is 3.0% and the PF is 0.998.

Fig. 42 shows the comparison of efficiency curves with and without dc bias current, and other different studies. When the converter works in the TPS control, the peak efficiency attains 95.77% at a load power of 900 W. At rated load power of 1500 W, the efficiency is 94.62%. Because of the hard switching caused by the dc bias current, the efficiency is degraded. When the converter operates without dc bias current, it reaches the peak efficiency of 97.04% at 1050 W. At 1500 W, the efficiency is 95.72%. ZVS performance contributes to the improvement of efficiency. For the works in [21], the current stress is taken into account for the efficiency improvement, but it is not the global minimum for the TPS control. Therefore, the conduction loss is still very large. Furthermore, the control strategies fail to account for the switching losses in the converter. Most of the switches work in hard switching, which causes large switching losses. Therefore, the efficiency curve is lower than the proposed control strategy. Although the converters in [24] and [25] achieve higher efficiency under light-load conditions, their efficiency decreases significantly under heavy load. The proposed method improves the efficiency by 3% at the rated load.

Fig. 43 illustrates the loss distribution diagram of the converter under 450, 1050, and 1500 W load power, respectively. As shown in the figure, the conduction loss of the switches accounts for the largest proportion in the converter, followed by the turn-OFF loss of the switches. The core loss and copper loss of the resonant inductors and transformer are relatively minor.

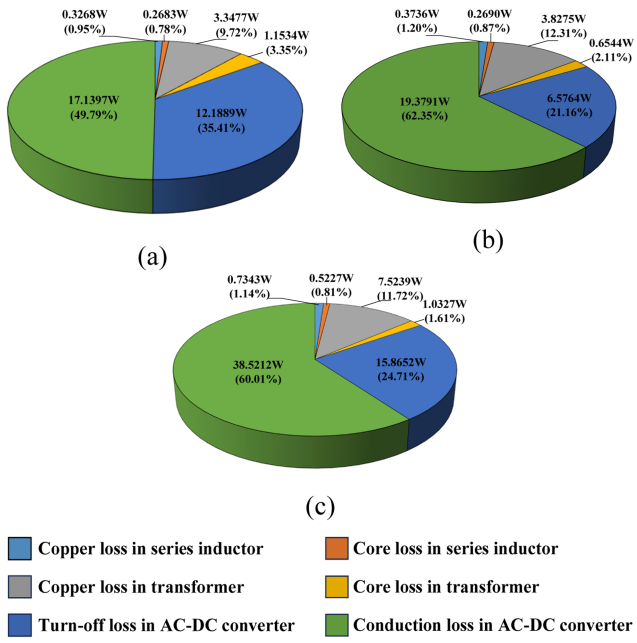


Fig. 43. Calculated power loss distribution. (a) Loss distribution for 450 W load power. (b) Loss distribution for 1050 W load power. (c) Loss distribution for 1500 W load power.

VI. Conclusion

In this article, a control strategy based on the optimal working mode with SVM is proposed for the three-phase single-stage matrix-type isolated ac–dc converter. By introducing four optimal working modes of DAB, the current stress of the matrix-type isolated ac–dc converter is reduced. The reason for the transient dc bias current during vector switching is analyzed, and an improved modulation strategy aiming at suppressing the dc bias current is proposed. The ZVS of all working modes is achieved in all working modes, and the turn-ON loss of the switches is reduced. Moreover, a single voltage loop control without current sampling is proposed, which is capable of achieving the unity power factor and simplifies the controller design. The experimental prototype was built, and the experimental results verified the control strategy based on the SVM optimal working mode. In comparison, the improved modulation strategy exhibits higher efficiency. The proposed control strategy enables the converter to possess a high power factor, high power quality, high efficiency, and fast dynamic response.

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