A Switched-LC Bidirectional DC–DC Converter With Quadratic Voltage Gain and High Gain Ratio for Film Capacitor Hybrid Energy Storage System

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***Abstract*—This article presents a quadratic high voltage gain and high gain ratio bidirectional dc–dc converter for film capacitor hybrid energy storage systems, which significantly widens the film capacitor operating voltage range (20–150 V) and effectively enhances the braking energy utilization of electric vehicles. The converter consists of a switched-quasi-Z-source cell and a switched-*LC* cell. The former realizes the bidirectional energy flow and ensures that the voltage stress on the three power switches is lower than the dc link voltage within the effective duty cycle range, which effectively reduces the system cost and improves the reliability of the proposed converter. The inductor and capacitor in the latter are controlled to work in series or in parallel. As a result, the voltage gain range of the proposed converter is extended to 2.56–31, with a gain ratio of 12.11 at nonextreme duty cycles. Additionally, the input and output of this converter share an absolute common ground, which reduces electromagnetic interference and enhances the reliability of the converter. A prototype experiment of 200 W verifies the feasibility and effectiveness of the proposed converter.**

***Index Terms*—Bidirectional dc–dc converter (BDC), film capacitor hybrid energy storage system, high gain ratio, quadratic voltage gain, switched-*LC* cell.**

I. Introduction

ELECTRIC vehicles (EVs) are one of the effective solutions to alleviate the energy crisis and environmental pollution. However, power batteries have several shortcomings, including low power density, poor low-temperature performance, and slow charging speed, which are the main obstacles to the further promotion of EVs. Hybrid energy storage systems (HESS) based on power battery (PB) and supercapacitor can not only improve the driving range and dynamic performance of EVs by utilizing braking energy, but also avoid the high current charging and discharging of PB and improve the service life and reliability of PB. It is an effective technical means to address the numerous shortcomings of current power batteries [1], [2], [3], [4].

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However, supercapacitors have disadvantages such as high equivalent series resistance (ESR) and a low maximum operating temperature ($\leq$70 °C), which leads to obvious deficiencies such as low efficiency and poor reliability in such HESS [5]. Film capacitors (FC) have an operating voltage of up to 1200 V, small ESR, and a maximum operating temperature of 125 °C. Therefore, the HESS based on FC has a simpler structure, higher reliability, and is more suitable for EVs with harsh operating environments and limited installation space. However, FC are large in size and high in cost, and the film capacitor hybrid energy storage systems (FCHESS) can only use small FC to absorb the braking energy of EVs. In order to improve the effect of braking energy utilization of EVs, the voltage of the FC should undergo large and rapid changes. Therefore, a bidirectional dc-dc converter with both high voltage gain ($\geq$20) and high gain ratio ($\geq$10) is necessary in FCHESS.

Cascading bidirectional dc–dc converter (BDC) is an easy way to realize high voltage gain. Multilevel techniques can also significantly improve the voltage gain of BDCs. However, they suffer from the disadvantages of low efficiency and low power density, which make it difficult to meet the narrow space installation requirements of HESS [6], [7], [8]. The incorporation of coupled inductors into traditional dc–dc converters enables the BDCs possessing high voltage gain and high-power density [9], [10]. However, the leakage inductance of the coupled inductors considerably augments the voltage stress on the power switches [11]. Even though buffer circuits can mitigate this issue, it nevertheless leads to a substantial diminution in the power density of these high gain BDCs.

Switched-capacitor cells or switched-inductor cells are often incorporated into a traditional BDC. In this way, the voltage gain of the BDCs can be increased while the voltage stress on the power switches can be effectively reduced [12], [13]. Nevertheless, although these converters based on switched-capacitor cells can proficiently suppress the voltage spikes on power switches, their potential for enhancing the voltage gain in wide-range applications is rather restricted. In study [14], the BDC with four power switches has a maximum voltage gain of only 10. In comparison, the BDCs based on switched-inductor cells can achieve a higher voltage gain. For instance, the BDC in study [15] can obtain a voltage gain of 19 times. However, the voltage stress of the power switches also rises significantly with the

increment of the converter's voltage gain. To reduce costs and enhance system reliability, reducing the voltage stress of power switches has become one of the crucial research directions in the field of BDC. In study [16], a symmetrical switched-inductor cell is used to suppress the voltage spikes of power switches, yet the two inductors must be strictly identical. In study [17], a structure of splitting capacitors on high voltage side is proposed to alleviate the voltage spikes of power switches, but this inevitably increases system cost and control complexity.

Different from the traditional BDC, the voltage gain of the BDC based on the switched-quasi-Z-source can be as high as nine times, which lays a good foundation for the further development of high voltage gain BDCs [18]. In study [19], a switched-quasi-Z source cell is combined with a switched-capacitor cell to obtain a maximum voltage gain of 14 times. Meanwhile, its voltage stress is less than half of the dc link voltage.

The converter in study [20] introduces both switched-inductor cell and switched-capacitor cell simultaneously, aiming to increase the voltage gain while reducing the voltage stress on the power switches. Although this BDC can only achieve unidirectional energy flow, it provides a new idea for high-gain BDCs. In [21], an H-bridge switched-inductor cell is used to achieve the bidirectional energy flow between the supercapacitor and the dc link, and the voltage stress of power switches is reduced through a symmetric switched-capacitor cell. In addition, this BDC has a 14 times voltage gain and zero current ripple on the low voltage side, which helps to improve the reliability and lifetime of batteries and supercapacitors. However, more active and passive devices are required for higher voltage gain.

In conclusion, the existing BDCs can meet the voltage gain requirements of the HESS based on supercapacitors. However, for the FCHESS, their voltage gain and gain ratio are unable to effectively deal with the problem of stabilizing the dc link voltage under the condition of large changes in the FC voltage. Besides, the parameters and efficiencies of these converters are only designed for a small range of duty cycle variations. Under the condition of large gain variations, the global performance of the key indexes of the BDC still needs to be optimized.

In this article, a novel BDC with high voltage gain and high gain ratio is proposed. The converter mainly consists of a switched-quasi-Z-source cell and a switched-*LC* cell. The switched-quasi-Z-source cell realizes the bidirectional energy flow between the FC and the high-voltage dc link, and at the same time effectively reduces the voltage stress on the power switches and capacitors. The switched-*LC* cell changes the energy flow path by switching the series–parallel connection of the inductor and the capacitor to further improve the voltage gain of the proposed BDC. The two cells mentioned above work together to endow the proposed converter with the characteristics of high voltage gain, high gain ratio and an absolute common ground, meeting the FCHESS operational requirements.

The rest of this article is organized as follows. Section II describes the configuration of the proposed BDC and its working principle. Section III gives the BDC's characteristics. Section IV compares the proposed BDC with the existing BDCs. Section V gives the experimental results and their analysis. Finally, Section VI concludes this article.

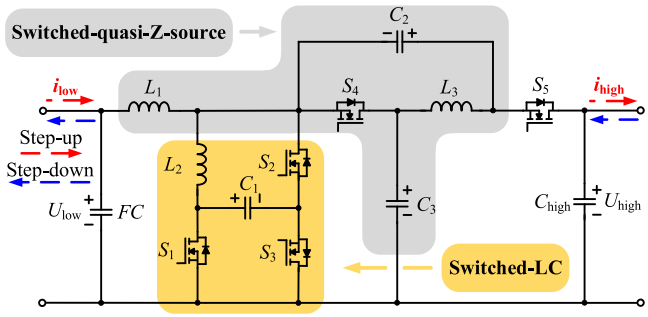

Fig. 1. Structure of the proposed converter.

II. Operating Principle of the Proposed Converter

A. Configuration of the Proposed Converter

As shown in Fig. 1, this article proposes a quadratic high voltage gain bidirectional dc–dc converter with a high gain ratio. The converter mainly consists of a switched-quasi-Z-source cell (L_1, L_3, C_2, C_3, and S_4) and a switched-LC cell (L_2, C_1, S_1, S_2, and S_3). FC and $C_{\rm high}$ denote the low voltage side (LVS) and the high voltage side (HVS) capacitor, respectively, and the corresponding voltages are denoted as $U_{\rm low}$ and $U_{\rm high}$, $i_{\rm low}$ and $i_{\rm high}$ denote the current of the LVS and the HVS, respectively. The voltage of capacitor C_i ($i = 1, 2, 3$) is denoted as $U_{{\rm C}i}$ and the current of inductor L_i ($i = 1, 2, 3$) is denoted as $i_{\rm Li}$. The proposed converter can operate in step-up mode and step-down mode according to the operating state of the EV and achieves the bidirectional power flow between the LVS and the HVS within the voltage variation range of 20 to 150V for the FC, thus effectively improving the utilization of braking energy of the EVs with FCHESS.

B. Operating Principle of the Proposed Converter

To simplify the analysis, it is assumed that the proposed converter operates in current continuous mode (CCM), all devices are ideal and the capacitor voltage remains stable within one switching cycle.

Step-up mode: In this mode, the energy is transferred from the FC on the LVS to the HVS. S_1 and S_2 have the same control signals, S_3–S_5 have the same control signals, and the drive signals of S_1–S_2 and S_3–S_5 are complementary. The power switches' drive signals and the key waveforms of proposed converter in step-up mode are shown in Fig. 2(a).

State I [t_0-t_1]: S_1 and S_2 are ON, S_3, S_4 and S_5 are OFF and the current flow path is shown in Fig. 3(a). L_2 and C_1 in the switched-*LC* cell are discharged in parallel, and there are two energy flow paths: one that L_2 in the switched-*LC* cell is connected in series with the FC to supply power to L_1, $i_{\rm L1}$ rises And $U_{\rm low}$ falls. The other is that C_1 in the switched-*LC* cell is connected in series with C_3 to charge L_3 and C_2, $i_{\rm L3}$ and $U_{\rm C2}$ rises and $U_{\rm C3}$ falls. Meanwhile, $C_{\rm high}$ fed energy to the load on the HVS and $U_{\rm high}$

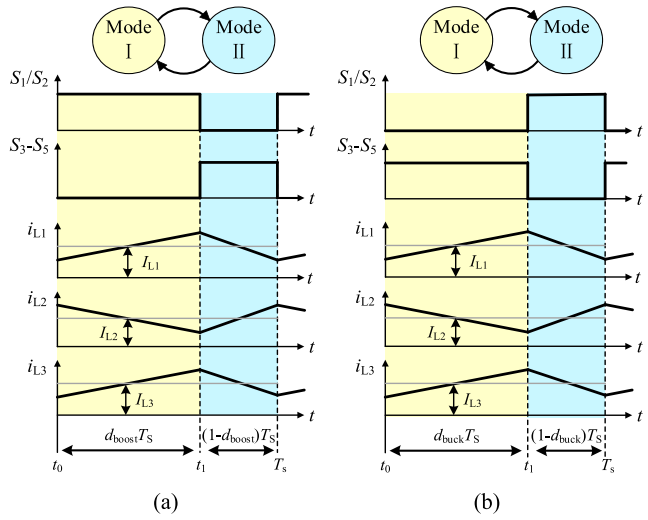

Fig. 2. Typical waveforms of the proposed converter. (a) Step-up mode. (b) Step-down mode.

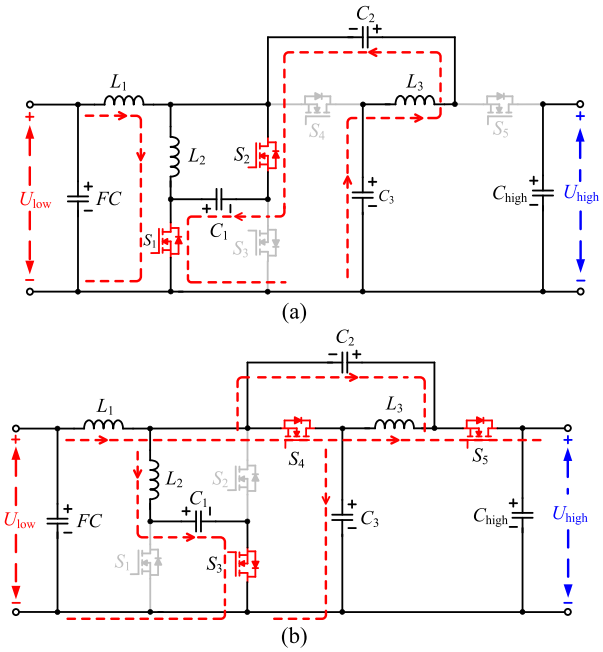

Fig. 3. Current flow path in step-up mode. (a) State I. (b) State II.

falls. The proposed BDC in this state has the voltage relationship

$$\begin{cases} U_{L1} = U_{low} + U_{C1} \\ U_{L2} = -U_{C1} \\ U_{L3} = U_{C1} + U_{C3} - U_{C2} \end{cases}. \tag{1}$$

State II [t_1-T_S]: S_1 and S_2 are OFF, S_3, S_4 and S_5 are ON, and the current flow path is shown in Fig. 3(b). The FC is connected in series with L_1. It charges L_2 and C_1 in the switched-LC cell through S_3, and simultaneously charges C_3 through S_4. As a result, i_{L1} decreases and U_{C3} increases. At the same time, C_2 and L_3 are discharged in parallel to the load, and U_{C2} and i_{L3} decrease. The proposed BDC in this state has the following

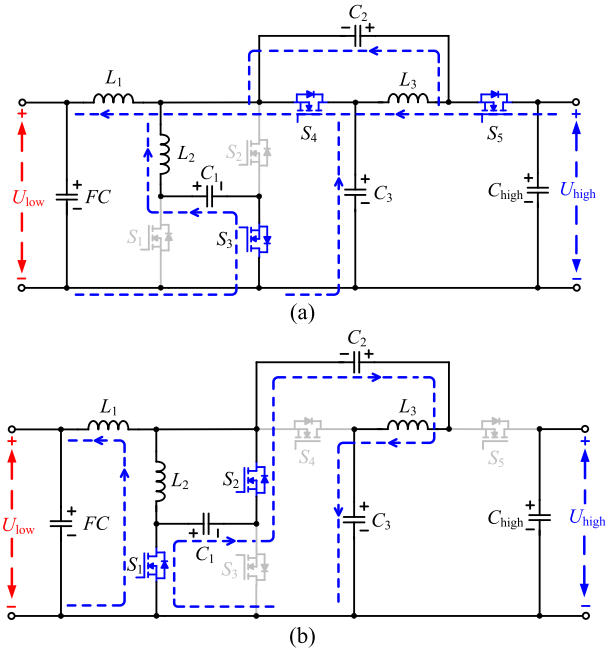

Fig. 4. Current flow path in step-down mode. (a) State I. (b) State II.

voltage relationship:

$$\begin{cases} U_{L1} = U_{low} - U_{C3} \\ U_{L2} = U_{C3} - U_{C1} \\ U_{L3} = -U_{C2} \end{cases}. \tag{2}$$

By applying the volt-second balance principle on L_1, L_2, and L_3, there exist

$$\begin{cases} (U_{low} + U_{C1}) \times d + (U_{low} - U_{C3}) \times (1-d) = 0 \\ -U_{C1} \times d + (U_{C3} - U_{C1}) \times (1-d) = 0 \\ (U_{C1} + U_{C3} - U_{C2}) \times d - U_{C2} \times (1-d) = 0 \end{cases}. \tag{3}$$

It can be concluded from (3) that the voltage gain M_{boost} of the proposed converter in step-up mode is as follows:

$$M_{boost} = \frac{1 + 2d - d^2}{(1-d)^2}. \tag{4}$$

Step-down mode: In this mode, the energy of the dc link capacitor on the HVS is transferred to the LVS. The drive signals of S_1–S_2 and S_3–S_5 are complementary, and the power switches' drive signals and the typical waveforms of proposed converter in step-down mode are shown in Fig. 2(b).

State I [t_0-t_1]: S_3, S_4 and S_5 are ON and S_1 and S_2 are OFF, and the current flow path is shown in Fig. 4(a). L_2 and C_1 in the switched-LC cell are connected in series. Three charging paths exist for L_1 and FC: L_2 and C_1 in the switched-LC cell are connected in series; C_3 passes through S_4; and C_{high} passes through the parallel branch of C_2 and L_3. In this mode, i_{L1}, i_{L3}, and U_{C2} rise and U_{C3} fall. The proposed BDC in this mode has

the following voltage relationship:

$$\begin{cases} U_{L1} = U_{C3} - U_{low} \\ U_{L2} = U_{C1} - U_{C3} \\ U_{L3} = U_{C2} \end{cases}. \tag{5}$$

State II [t_1-T_S]: S_1 and S_2 are ON and S_3, S_4, and S_5 are OFF, and the current flow path is shown in Fig. 4(b). L_2 and C_1 in the switched-LC cell are charged in parallel, and there are two energy flow paths: one is that L_1 discharges to the FC and L_2 in the switched-LC cell, and i_{L1} decreases. The other is that C_2 and L_3 in series discharge C_3 and C_1 in the switched-LC cell and U_{C3} rises while U_{C2} and i_{L3} decrease. The proposed BDC in this state has the following voltage relationship:

$$\begin{cases} U_{L1} = -U_{C1} - U_{low} \\ U_{L2} = U_{C1} \\ U_{L3} = U_{C2} - U_{C1} - U_{C3} \end{cases}. \tag{6}$$

By applying the volt-second balance principle on L_1, L_2, and L_3, there exist:

$$\begin{cases} (U_{C3} - U_{low}) \times d + (-U_{C1} - U_{low}) \times (1-d) = 0 \\ (U_{C1} - U_{C3}) \times d + U_{C1} \times (1-d) = 0 \\ U_{C2} \times d + (U_{C1} + U_{C2} - U_{C3}) \times (1-d) = 0 \end{cases}. \tag{7}$$

It can be concluded from (7) that the voltage gain M_{buck} of the proposed converter in step-down mode is as follows:

$$M_{buck} = \frac{d^2}{(2-d^2)}. \tag{8}$$

The duty cycles of all the power switches in the proposed converter are set at [0.25, 0.75] to avoid the reliability and efficiency degradation of the FCHESS due to extreme duty cycles. It can be obtained from (4) and (8) that the voltage gain range of proposed converter is from 2.55 to 31 with a gain ratio of 12.11 in step-up mode, and from 0.03 to 0.39 with a gain ratio of 12.11 in step-down mode.

III. Characteristics Analysis of the Proposed Converter

A. Gain Ratio

The voltage gain M is defined as the ratio of output voltage to input voltage, and the gain ratio G is the ratio of the highest to the lowest voltage gain within the given duty cycle range. When the proposed BDC operates in the step-up mode, M_{boost} and G_{boost} are expressed as follows:

$$M_{boost}(d) = \frac{U_{high}}{U_{low}} \tag{9}$$

$$G_{boost} = \frac{M_{boost}(d_{max})}{M_{boost}(d_{min})}. \tag{10}$$

In HESS, where U_{high} is fixed, substituting (9) into (10), G_{boost} is rewritten as follows:

$$G_{boost} = \frac{U_{low\_max}}{U_{low\_min}}. \tag{11}$$

Therefore, the energy storage of the capacitor is expressed as follows:

$$W = \frac{C}{2}\left({U_{low\_max}}^2 - {U_{low\_min}}^2\right) = \frac{C}{2}{U_{low\_min}}^2\left({G_{boost}}^2 - 1\right). \tag{12}$$

Equation (12) shows that a larger capacitor, a higher minimum voltage, and a larger G_{boost} can all increase the stored energy of the film capacitors. However, excessive capacitor is not reasonable due to cost and size. To enhance the energy release capability of the film capacitor, U_{low_min} should not be too large. Therefore, an increase in G_{boost} is a more reasonable approach.

B. Voltage Stresses on Power Switches and Capacitors

Step-up mode: The U_{C1}–U_{C3} are obtained from (3)

$$\begin{cases} U_{C1} = U_{high}(1-d)/(2-(1-d)^2) \\ U_{C2} = U_{high}d \times (2-d)/(2-(1-d)^2) \\ U_{C3} = U_{high}/(2-(1-d)^2) \end{cases}. \tag{13}$$

According to (13) and Fig. 3, the voltage stress of S_1–S_5 can be obtained based on Kirchhoff's voltage law

$$\begin{cases} U_{S1} = U_{S3} = U_{high}(1-d)/(2-(1-d)^2) \\ U_{S2} = U_{high}/(2-(1-d)^2) \\ U_{S4} = U_{S5} = U_{high}(2-d)/(2-(1-d)^2) \end{cases}. \tag{14}$$

Step-down mode: The U_{C1}–U_{C3} are obtained from (7)

$$\begin{cases} U_{C1} = U_{low}/d \\ U_{C2} = U_{low}(1-d^2)/d^2 \\ U_{C3} = U_{low}/d^2 \end{cases}. \tag{15}$$

According to (15) and Fig. 4, the voltage stress of S_1–S_5 can be obtained based on Kirchhoff's voltage law:

$$\begin{cases} U_{S1} = U_{S3} = U_{low}/d \\ U_{S2} = U_{low}/d^2 \\ U_{S4} = U_{S5} = U_{low}(1+d)/d^2 \end{cases}. \tag{16}$$

Equations (14) and (16) show that when the proposed converter operates in step-up or step-down mode, the voltage stresses of S_1–S_3 are less than $0.7U_{high}$, and the voltage stresses of S_4 and S_5 reach a maximum of $1.22U_{high}$ when $d = 0.25$, and then gradually decrease to $0.65U_{high}$ when $d = 0.75$. Therefore, the proposed BDC can use lower rated power switches to reduce costs and improve reliability and efficiency.

C. Current Stresses on Power Switches and Capacitors

Step-up mode: Based on the ampere-second balance on C_1–C_3, there exist

$$\begin{cases} (I_{L2} - I_{L1} - I_{L3}) \times d + I_{L2} \times (1-d) = 0 \\ I_{L3} \times d + (I_{L2} + I_{L3} - I_{L1} + I_{C1\_II}) \times (1-d) = 0 \\ -I_{L3} \times d + (I_{L1} - I_{L2} - I_{L3} + I_{C2\_II}) \times (1-d) = 0 \\ -I_{high} \times d + (I_{L3} - I_{C2\_II} - I_{high}) \times (1-d) = 0 \end{cases} \tag{17}$$

where $I_{\mathrm{L}i}$ ($i=1,2,3$) are the average current of L_1–L_3, $I_{\mathrm{C}i\_\mathrm{I}}$ and $I_{\mathrm{C}i\_\mathrm{II}}$ ($i=1,2,3$ and high) are the average currents of C_1–C_3 and C_{high} at state I or at state II.

The average current of L_1–L_3 can be obtained from (17)

$$\begin{cases} I_{\mathrm{L1}} = I_{\mathrm{high}} \times M_{\mathrm{boost}} \\ I_{\mathrm{L2}} = 2I_{\mathrm{high}} d/(1-d)^2 \\ I_{\mathrm{L3}} = I_{\mathrm{high}} \end{cases}. \tag{18}$$

According to (18) and Fig. 3, the current stress of S_1–S_5 is obtained based on Kirchhoff's current law

$$\begin{cases} I_{\mathrm{S1}} = 2I_{\mathrm{high}}/(1-d)^2 \\ I_{\mathrm{S2}} = I_{\mathrm{high}} d/(1-d)^2 \\ I_{\mathrm{S3}} = I_{\mathrm{high}}\,(2-d)\,/(1-d)^2 \\ I_{\mathrm{S4}} = I_{\mathrm{S5}} = I_{\mathrm{high}}/\,(1-d) \end{cases}. \tag{19}$$

Step-down mode: The average current of L_1–L_3 and the current stress of S_1–S_5 can be obtained from Fig. 4 according to the ampere-second balance principle on C_1–C_3

$$\begin{cases} I_{\mathrm{L1}} = I_{\mathrm{low}} \\ I_{\mathrm{L2}} = 2I_{\mathrm{low}}(1-d)/(2-d^2) \\ I_{\mathrm{L3}} = I_{\mathrm{low}} \times M_{\mathrm{buck}} \end{cases} \tag{20}$$

$$\begin{cases} I_{\mathrm{S1}} = 2I_{\mathrm{low}}/\left(2-d^2\right) \\ I_{\mathrm{S2}} = I_{\mathrm{low}}\,(1-d)\,/\left(2-d^2\right) \\ I_{\mathrm{S3}} = I_{\mathrm{low}}\,(1+d)\,/\left(2-d^2\right) \\ I_{\mathrm{S4}} = I_{\mathrm{S5}} = I_{\mathrm{low}} d/\left(2-d^2\right) \end{cases}. \tag{21}$$

It can be seen from (19) and (21) that, in step-up mode, S_1 has the maximum current stress of $32I_{\mathrm{high}}$ at $d=0.75$, and the current stress of other power switches is less than $20I_{\mathrm{high}}$. In step-down mode, S_1 has the maximum current stress of $1.39I_{\mathrm{low}}$ at $d=0.75$, and the current stress of other power switches is less than $1.22I_{\mathrm{low}}$.

D. Parameters Design of the Proposed Converter

1) Design of Inductors: The minimum allowable inductance of L_1–L_3 in step-up mode is obtained from the voltage–current relationship (VCR) of inductors and (18)

$$\begin{cases} L_1 \geq \left(d\,(2-d)\,U_{\mathrm{high}}\right)/\left((1-d)\,M_{\mathrm{boost}}^2 I_{\mathrm{high}} r_{\mathrm{L1}} f_s\right) \\ L_2 \geq \left((1-d)\,U_{\mathrm{high}}\right)/\left(2M_{\mathrm{boost}} I_{\mathrm{high}} r_{\mathrm{L2}} f_s\right) \\ L_3 \geq \left(d\,(2-d)\,U_{\mathrm{high}}\right)/\left((1-d)\,M_{\mathrm{boost}} I_{\mathrm{high}} r_{\mathrm{L3}} f_s\right) \end{cases}. \tag{22}$$

Similarly, the minimum allowable inductance of L_1–L_3 in step-down mode can be derived as follows:

$$\begin{cases} L_1 \geq ((1-d^2) M_{\mathrm{buck}}^2 U_{\mathrm{low}})/(d \times I_{\mathrm{low}} r_{\mathrm{L1}} f_s) \\ L_2 \geq (d \times M_{\mathrm{buck}} U_{\mathrm{low}})/(2 I_{\mathrm{low}} r_{\mathrm{L2}} f_s) \\ L_3 \geq ((1-d^2) M_{\mathrm{buck}} U_{\mathrm{low}})/(d \times I_{\mathrm{low}} r_{\mathrm{L3}} f_s) \end{cases} \tag{23}$$

where r_{L1}, r_{L2}, and r_{L3} denote current ripple rate of L_1–L_3, respectively, and f_s denotes the switching frequency.

Equations (22) and (23) show that I_{L1}, I_{L2} and I_{L3}, U_{high}, d, f_s, and $\mathrm{r_{L1}}$, r_{L2} and r_{L3} jointly determine the inductor value in the proposed converter. It is worth noting that the maximum values of r_{L1}, r_{L2} and r_{L3} are selected as 200% to ensure that the proposed converter operates in CCM.

2) Design of Capacitors: The minimum allowable capacitance of C_1–C_3 and C_{high} in step-up mode can be obtained from the VCR of capacitors and (13)

$$\begin{cases} C_1 \geq \left((2-d)\,M_{\mathrm{boost}} I_{\mathrm{high}}\right)/\left(U_{\mathrm{high}} r_{\mathrm{C1}} f_s\right) \\ C_2 \geq \left(\left(1-d\right)^2 M_{\mathrm{boost}} I_{\mathrm{high}}\right)/\left((2-d)\,U_{\mathrm{high}} r_{\mathrm{C2}} f_s\right) \\ C_3 \geq \left(d\left(1-d\right)^2 M_{\mathrm{boost}} I_{\mathrm{high}}\right)/\left(U_{\mathrm{high}} r_{\mathrm{C3}} f_s\right) \\ C_{\mathrm{high}} \geq \left((1-d)\,I_{\mathrm{high}}\right)/\left(U_{\mathrm{high}} r_{\mathrm{Chigh}} f_s\right) \end{cases}. \tag{24}$$

Similarly, the minimum allowable capacitance in step-down mode can be derived as follows:

$$\begin{cases} C_1 \geq ((1+d) I_{\mathrm{low}})/(M_{\mathrm{buck}} U_{\mathrm{low}} r_{\mathrm{C1}} f_s) \\ C_2 \geq (d^2 \times I_{\mathrm{low}})/((1+d) M_{\mathrm{buck}} U_{\mathrm{low}} r_{\mathrm{C2}} f_s) \\ C_3 \geq (d^2(1-d) I_{\mathrm{low}})/(M_{\mathrm{buck}} U_{\mathrm{low}} r_{\mathrm{C3}} f_s) \\ C_{\mathrm{low}} \geq (d \times I_{\mathrm{low}})/(U_{\mathrm{low}} r_{\mathrm{Clow}} f_s) \end{cases} \tag{25}$$

where r_{C1}, r_{C2}, r_{C3}, and r_{low} denote the capacitor voltage ripple rate, which, according to engineering datum, should be within $\pm\,0.5\%$ of the rated voltage.

3) Design of Power Switches: Power switches are selected according to voltage and current stress, which is shown in (14) and (16) and in (19) and (21) while allowing for some margin.

E. Power Loss

The power loss of the proposed BDC can be expressed as follows:

$$P_{\mathrm{loss}} = P_{\mathrm{S}} + P_{\mathrm{L}} + P_{\mathrm{C}} \tag{26}$$

where P_{S}, P_{L}, and P_{C} denote the losses incurred by power switches, inductors, and capacitors, respectively.

P_{S} mainly includes conduction losses P_{SC} and switching losses P_{SS}

$$P_{\mathrm{SC}} = \sum_{\mathrm{i}=1}^{5} I_{\mathrm{S}i\_\mathrm{RMS}} R_{\mathrm{S}i\_\mathrm{on}} \tag{27}$$

where $I_{\mathrm{S}i\_\mathrm{RMS}}$ ($i=1,2,3,4,5$) denotes the RMS current of S_i, and $R_{\mathrm{S}i\_\mathrm{on}}$ ($i=1,2,3,4,5$) denotes the ON-resistance of S_i

$$P_{\mathrm{SS}} = \frac{1}{2}\sum_{i=1}^{5}\left[V_{\mathrm{S}i} I_{\mathrm{S}i} f_{\mathrm{s}} (t_{\mathrm{rise}} + t_{\mathrm{fall}})\right] \tag{28}$$

where $V_{\mathrm{S}i}$ ($i=1,2,3,4,5$) denotes the reverse voltage when S_{i} is completely turned OFF, $I_{\mathrm{S}i}$ ($i=1,2,3,4,5$) denotes the current flowing when S_{i} is completely turned OFF, and t_{rise} and t_{fall} denote the ON-time and OFF-time of power switches.

P_{L} mainly include copper loss P_{Cu} and iron loss P_{Fe}. P_{Cu} is mainly generated by the ESRs of the inductor, and P_{Fe} is mainly generated by the hysteresis loss and eddy current loss generated by the core of the inductor

$$P_{\mathrm{Cu}} = \sum_{i=1}^{3} {I_{\mathrm{L}i\_\mathrm{RMS}}}^2 R_{\mathrm{L}i} \tag{29}$$

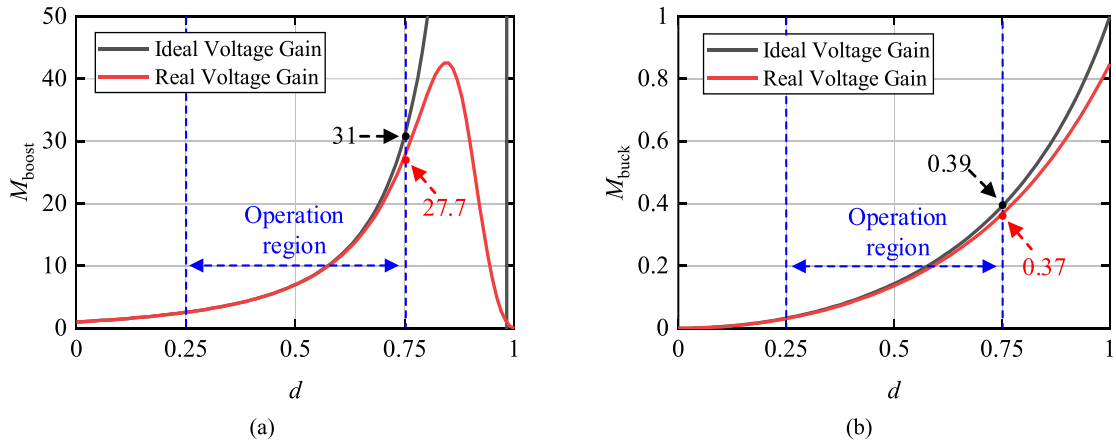

Fig. 5. Voltage gain curves. (a) Voltage gain in step-up mode. (b) Voltage gain in step-down mode.

TABLE I
PARASITIC PARAMETERS OF THE PROPOSED CONVERTER

Parameters	Values	Internal Resistances
$L_1/L_2/L_3$	1mH/1.5mH/4mH	15mΩ/22mΩ/125mΩ
$S_1/S_3/S_3$	IXTQ52N30P	48mΩ
S_4/S_5	SPW47N60C3	55mΩ
$C_1/C_2/C_3$	110uF/550V	5mΩ

where $I_{\mathrm{L}i\_\mathrm{RMS}}$ ($i = 1, 2, 3$) denotes the RMS current of L_i, and $R_{\mathrm{L}i}$ ($i = 1, 2, 3$) denotes the ESR of L_i

$$P_{\mathrm{Fe}} = \sum_{i=1}^{3} l_{\mathrm{L}i} A_{\mathrm{L}i} (a B_{\mathrm{acL}i}^{b} f_{\mathrm{s}}^{c}) \tag{30}$$

where $l_{\mathrm{L}i}$ ($i = 1, 2, 3$) and $A_{\mathrm{L}i}$ ($i = 1, 2, 3$) denote the magnetic flux path length and the cross-sectional area of the inductor core, respectively. $B_{\mathrm{acL}i}$ ($i = 1, 2, 3$) denotes the magnetic flux density of the inductor core. a, b and c are coefficients determined by the core material.

P_{C} is mainly caused by ESR

$$P_{\mathrm{C}} = \sum_{i=1}^{3} I_{\mathrm{C}i\_\mathrm{RMS}}^{2} R_{\mathrm{C}i} \tag{31}$$

where $R_{\mathrm{C}i}$ and $I_{\mathrm{C}i\_\mathrm{RMS}}$ are ESR and RMS current of C_i($i = 1$, 2, 3).

F. Real Voltage Gain

Table I indicates the parasitic parameters. The ESRs of the inductors, the $R_{\mathrm{DS(on)}}$ of the power switches, and the ESRs of the capacitors will affect the voltage gain, especially at high duty cycles. Since the ESR of FC is very small, they are neglected.

In the step-up mode, the real voltage gain is as follows:

$$M_{\mathrm{boost\_real}} = \frac{R_{\mathrm{high}}(1-d)^2(1+2d-d^2)}{A_1 d^4 + B_1 d^3 + C_1 d^2 + D_1 d + E_1} \tag{32}$$

where A_1, B_1, C_1, D_1, and E_1 are as follows:

$$\begin{cases} A_1 = R_{\mathrm{high}} + r_{\mathrm{L1}} + r_{\mathrm{L3}} \\ B_1 = -4R_{\mathrm{high}} - 4r_{\mathrm{L1}} - 4r_{\mathrm{L3}} - 2r_{\mathrm{S1}} + 4r_{\mathrm{S2}} + 2r_{\mathrm{S3}} + 4r_{\mathrm{S4}} \\ C_1 = 6R_{\mathrm{high}} + 2r_{\mathrm{L1}} + 4r_{\mathrm{L2}} + 6r_{\mathrm{L3}} - 4r_{\mathrm{S1}} - 5r_{\mathrm{S4}} - 3r_{\mathrm{S5}} \\ D_1 = -4R_{\mathrm{high}} + 4r_{\mathrm{L1}} - 4r_{\mathrm{L3}} + 2r_{\mathrm{S1}} + 2r_{\mathrm{S2}} + 4r_{\mathrm{S3}} + r_{\mathrm{S4}} + 3r_{\mathrm{S5}} \\ E_1 = R_{\mathrm{high}} + r_{\mathrm{L1}} + r_{\mathrm{L3}} + r_{\mathrm{S4}} - r_{\mathrm{S5}} \end{cases} . \tag{33}$$

Similarly, the real voltage gain in the step-down mode is as follows:

$$M_{\mathrm{buck\_real}} = \frac{R_{\mathrm{low}} d^2(2-d^2)}{A_2 d^4 + B_2 d^3 + C_2 d^2 + D_2 d + E_2} \tag{34}$$

where A_2, B_2, C_2, D_2, and E_2 are as follows:

$$\begin{cases} A_2 = R_{\mathrm{low}} + r_{\mathrm{L1}} + r_{\mathrm{L3}} \\ B_2 = -2r_{\mathrm{S2}} - 2r_{\mathrm{S3}} - r_{\mathrm{S4}} + r_{\mathrm{S5}} \\ C_2 = -4R_{\mathrm{low}} - 4r_{\mathrm{L1}} + 4r_{\mathrm{L2}} + 8r_{\mathrm{S2}} + 4r_{\mathrm{S4}} \\ D_2 = -8r_{\mathrm{L2}} - 4r_{\mathrm{S1}} - 10r_{\mathrm{S2}} + 2r_{\mathrm{S3}} \\ E_2 = 4R_{\mathrm{low}} + 4r_{\mathrm{L1}} + 4r_{\mathrm{L2}} + 4r_{\mathrm{S1}} + 4r_{\mathrm{S2}} \end{cases} . \tag{35}$$

Fig. 5(a) and (b) represents the ideal voltage gain curves and the real voltage gain curves in the step-up mode and the step-down mode, respectively. In the step-up mode, as d increases, there is a deviation between the ideal voltage gain curve and the real voltage gain curve. When d is 0.75, the ideal voltage gain M_{boost} is 31 times, while the real voltage gain M_{boost} is 27.2 times. The same situation occurs in the step-down mode, when d is 0.75, the ideal voltage gain M_{buck} is 0.39 times, while the real voltage gain M_{buck} is 0.37 times.

G. Comparisons With Other Converters

Table II compares the key parameters of the proposed BDC with some existing BDCs, and Fig. 6(a) and (b) show the voltage gain curves of all the BDCs in Table II. It shows that the maximum voltage gain of the BDCs proposed in studies [22], [23], and [24] is between 10 and 13. Although these converters can be used for supercapacitor HESS, their gain ratios G, including

TABLE II
COMPARISON WITH EXISTING BIDIRECTIONAL CONVERTERS

Topology	[22]	[23]	[24]	[25]	[26]	[27]	[28]	Proposed Converter
Number of Elements	4L/5C/4S	2L/5C/7S	3L/4C/4S	2L/3C/4S	3L/5C/5S	3L/5C/5S	2L/4C/5S	3L/5C/5S
Step-up Gain d_{boost}=0.25~0.75	$\frac{1+2d_{boost}}{1-d_{boost}}$ (2~10)	$\frac{3}{1-d_{boost}}$ (4-12)	$\frac{1+3d_{boost}}{1-d_{boost}}$ (2.33~13)	$\frac{1}{(1-d_{boost}^2)}$ (1.78~16)	$\frac{2-d_{boost}}{(1-d_{boost})^2}$ (3.11~20)	$\frac{d_{boost}^2-3d_{boost}+3}{(1-d_{boost})^2}$ (4.11~21)	$\frac{1+d_{boost}}{(1-d_{boost})^2}$ (2.22~28)	$\frac{2-(1-d_{boost})^2}{(1-d_{boost})^2}$ (2.56~31)
Step-down Gain d_{buck}=0.25~0.75	$\frac{d_{buck}}{3-2d_{buck}}$ (0.1~0.5)	$\frac{d_{buck}}{3}$ (0.08-0.25)	$\frac{d_{buck}}{4-3d_{buck}}$ (0.08~0.43)	d_{buck}^2 (0.06~0.56)	$\frac{d_{buck}^2}{1+d_{buck}}$ (0.05~0.32)	$\frac{d_{buck}^2}{d_{buck}^2+d_{buck}+1}$ (0.05~0.24)	$\frac{d_{buck}^2}{2-d_{buck}}$ (0.04~0.45)	$\frac{d_{buck}^2}{2-d_{buck}^2}$ (0.03~0.39)
Max Voltage Gain/Number of Elements	0.77	0.86	1.18	1.78	1.54	1.62	2.55	2.38
Max Gain Ratio	5	3	5.58	8.99	6.43	5.11	12.61	12.11
Max Voltage Stress on Power Switches	$\frac{2U_{high}}{1+2d_{boost}}$ ($1.33U_{high}$)	$\frac{U_{high}}{3}$ ($0.33U_{high}$)	$\frac{2U_{high}}{4-3d_{boost}}$ ($1.14U_{high}$)	$(2-d_{boost})U_{high}$ ($1.75U_{high}$)	$\frac{U_{high}}{2-d_{boost}}$ ($0.8U_{high}$)	$\frac{(2-d_{boost})U_{high}}{d_{boost}^2-3d_{boost}+3}$ ($0.95U_{high}$)	$\frac{2U_{high}}{1+d_{boost}}$ ($1.6U_{high}$)	$\frac{(2-d_{boost})U_{high}}{2-(1-d_{boost})^2}$ ($1.22U_{high}$)
Max Current Stress on Power Switches	$\frac{2I_{high}}{1-d_{boost}}$ ($8I_{high}$)	$\frac{4+d_{boost}}{2-2d_{boost}}I_{high}$ ($9.5I_{high}$)	$\frac{1+d_{boost}}{1-d_{boost}}I_{high}$ ($7I_{high}$)	$\frac{d_{boost}I_{high}}{(1-d_{boost})^2}$ ($12I_{high}$)	$\frac{I_{high}}{d_{boost}(1-d_{boost})^2}$ ($21.33I_{high}$)	$\frac{I_{high}}{d_{boost}(1-d_{boost})^2}$ ($21.33I_{high}$)	$\frac{2I_{high}}{(1-d_{boost})^2}$ ($32I_{high}$)	$\frac{2}{(1-d_{boost})^2}$ ($32I_{high}$)
Common Ground	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes
Rated Power /Frequency	200W /50kHz	500W /25kHz	300W /50kHz	200W /25Hz	1000W /50KHz	200W /50KHz	500W /50KHz	200W /50KHz
Maximum Efficiency	η_{boost}=94.9% η_{buck}=95.1%	η_{boost}=97.2% η_{buck}=96.41%	η_{boost}=94.10% η_{buck}=98.96%	η_{boost}=93.7% η_{buck}=95.3%	η_{boost}=95.09% η_{buck}=95.24%	η_{boost}=94.5% η_{buck}=95.5%	η_{boost}=96.8% η_{buck}=97.2%	η_{boost}=94.8% η_{buck}=95.0%
Current Ripple on LVS	Zero Ripple	Large	Large	Large	Zero Ripple	Zero Ripple	Large	Large
Minimum Inductance	10uH	60uH	297uH	500uH	75uH	389uH	400uH	1mH
Power Density (W/cm^3)	1.68	0.88	0.9	1.53	2.88	0.83	1.94	1.05
Cost ($)	31.63	97.75	50.78	52.09	106.82	51.78	77.28	56.13

that of [27], are lower than 6, and they are unable to fully utilize EVs braking energy with FCHESS.

Fig. 6(c) and (d) shows the curves of the maximum voltage stress and maximum current stress on the power switches. The converters in studies [25], [26], and [28] have relatively high voltage gains and gain ratios. However, the maximum voltage stress of the power switches in both studies [25] and [28] is $1.75U_{\rm high}$ and $1.6U_{\rm high}$, respectively, higher than $1.22U_{\rm high}$ of the proposed BDC. Study [26] has a high voltage gain with low voltage stress, which is relatively rare in nonisolated converters. However, its gain ratio is only 6.43. Whether the input and output of the converter are commonly grounded is another important indicator, which determines the reliability and EMI immunity of the FCHESS. In Table II, except for study [24], other converters have the advantage of absolute common ground.

As shown in Fig. 6(d), study [28] and the proposed BDC have the highest current stress on the power switches. This is because the voltage gains of different converters at the same duty cycle are not the same, resulting in different power. From Fig. 6(d), converters with higher voltage gains, such as those in studies [26], [27], and [28] and the proposed BDC, all have higher current stress. Compared with studies [22], [26], and [27] that adopt the zero current ripple technology, the proposed BDC reduces the current ripple on the LVS by using a larger inductor, resulting in decreased power density and increased cost.

In addition, it is necessary to compare the semiconductor utilization factor (SUF) of the proposed converter with existing high-gain converters. The SUF is defined as follows:

$$\mathrm{SUF} = \frac{P_{\rm o}}{\sum_{i=1}^{n} V_{Si} \cdot I_{Si}} \tag{36}$$

where $P_{\rm o}$ is the output power, $V_{{\rm S}i}$ and $I_{{\rm S}i}$ represent the voltage and current on the power switches, respectively, and n is the number of power switches.

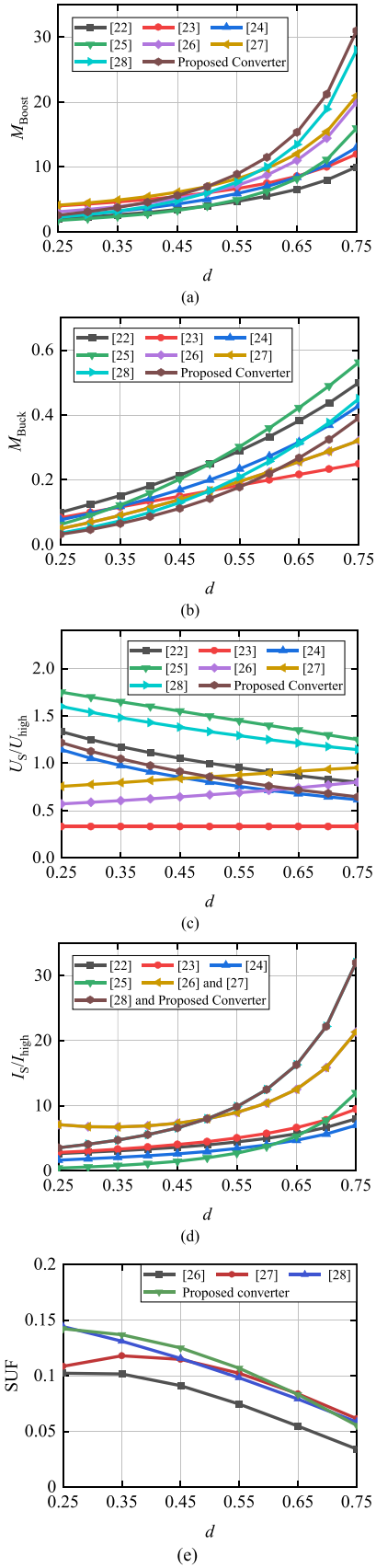

Fig. 6. Comparisons of key parameters. (a) Voltage gains in step-up mode. (b) Voltage gains in step-down mode. (c) Max voltage stress on power switches. (d) Max current stress on power switches. (e) SUF.

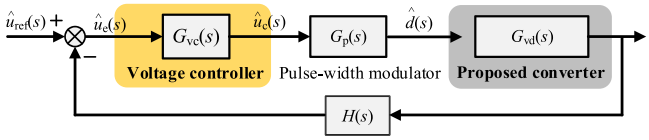

Fig. 7. Voltage loop control scheme of the proposed converter.

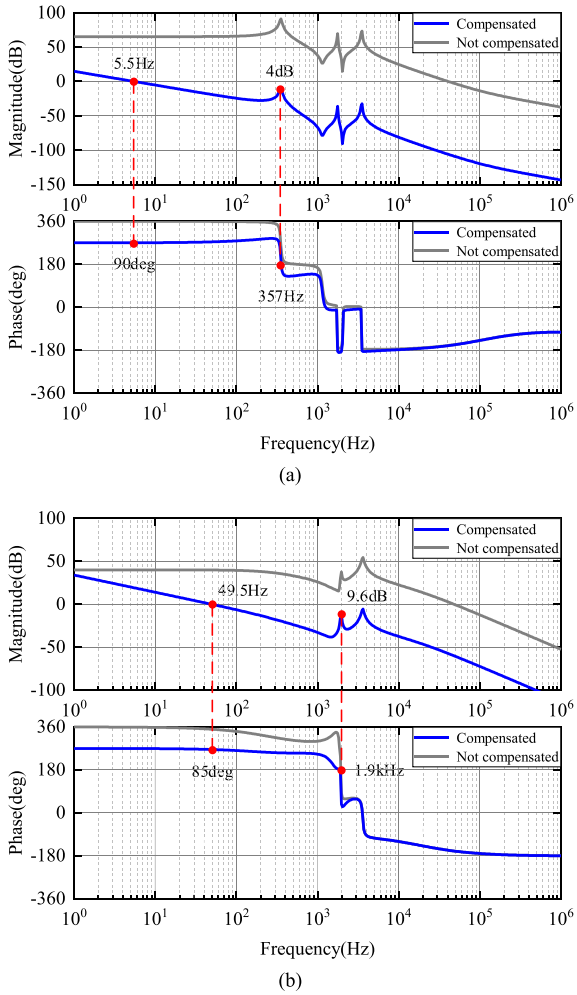

Fig. 8. Bode plots of the open-loop transfer functions before and after compensation. (a) Step-up mode. (b) Step-down mode.

According to (36), a higher SUF of the converter is more desirable. Fig. 6(e) shows the SUF comparison between the proposed converter and existing high-gain converters, such as studies [26], [27] and [28]. From Fig. 6(e), the proposed converter outperforms other high-gain converters with a slight advantage.

In conclusion, the proposed BDC has a maximum voltage gain of 31 times in the step-up mode and a minimum voltage gain of 0.03 times in the step-down mode, which is the highest among all BDCs in Table II. Although its gain ratio is only slightly lower than that of the converter in study [26], it has lower voltage stress on power switches. The latest converter has achieved a higher voltage-gain ratio through more power switches [29]. In addition, the proposed BDC can generate a voltage gain of 2.38

times per component, ranking second only to study [28]. So, the proposed converter shows outstanding advantages over other high-gain BDCs and can effectively reuse EVs braking energy through FCHESS.

H. Analysis of Small-Signal Models

In this section, the small-signal model is presented to demonstrate the dynamic performance of the proposed converter. Figs. 3(b) and 4(a) show that $u_{C2}(t)$, $u_{C3}(t)$, and $u_{Chigh}(t)$ are coupled, and there is an invalid state variable. To resolve it, an ESR r of C_2 is introduced into the state equation, $u_{C2}(t)$, $u_{C3}(t)$, and $u_{Chigh}(t)$ can be decoupled. The state-space averaging method is used to derive the small-signal equations of the proposed converter in both the step-up/step-down mode. The transfer function and characteristic matrix of this converter can be obtained, which are shown in (37)–(40).

To verify the dynamic performance of the proposed converter, a voltage loop controller is designed. The voltage loop control scheme is shown in Fig. 7. Here, $G_{vd}(s)$ represents the transfer function according to the small-signal modeling, as shown in (37) shown at the bottom of this page and (39) shown at the bottom of the next page, where $G_p(s)$ is the transfer function of the PWM, $H(s)$ is the feedback transfer function, and $G_{vc}(s)$ is the transfer function of the voltage controller. The transfer functions $G_p(s)$ and $H(s)$ are normalized. The transfer function of the voltage controller can be expressed as follows:

$$G_{vc}(s) = K_p + K_i \frac{1}{s}. \tag{41}$$

Among them, K_p is the proportional coefficient and K_i is the integral coefficient. By adjusting the PI parameters K_p and K_i of the voltage loop controller, the closed-loop system of the proposed converter can achieve better stability performance. When the converter operates in step-up mode, the PI controller parameters are set as $K_p = 0.0005$ and $K_i = 0.003$, and when the converter operates in step-down mode, the PI controller parameters are $K_p = 0.001$ and $K_i = 0.5$.

Based on (37)–(40) and voltage controller $G_{vc}(s)$, the Bode plots of the open-loop transfer functions before and after compensation in the step-up mode and step-down mode can be obtained, as shown in Fig. 8(a) and (b) respectively. It can be seen from the figures that when the proposed converter operates in the step-up mode, the crossover frequency is 5.5 Hz, the phase margin γ is 90° and the gain margin K_g is 4 dB, both of which are greater than 0. When the proposed converter operates in the step-down mode, the crossover frequency is 49.5 Hz, the phase margin γ is 85° and the gain margin K_g is 9.6 dB, both of which are also greater than 0. Therefore, the closed-loop system of the proposed converter with the voltage controller can operate stably.

$$\frac{d}{dt}\begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{i}_{L3}(t) \\ \hat{u}_{C1}(t) \\ \hat{u}_{C2}(t) \\ \hat{u}_{C3}(t) \\ \hat{u}_{Chigh}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & D/L_1 & 0 & (D-1)/L_1 & 0 \\ 0 & 0 & 0 & -1/L_2 & 0 & (1-D)/L_2 & 0 \\ 0 & 0 & -(r\cdot D)/L_3 & D/L_3 & -D/L_3 & 1/L_3 & -(1-D)/L_3 \\ -D/C_1 & 1/C_1 & -D/C_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & D/C_2 & 0 & (D-1)/(r\cdot C_2) & (D-1)/(r\cdot C_2) & (1-D)/(r\cdot C_2) \\ (1+D)/C_3 & -(1+D)/C_3 & -1/C_3 & 0 & -(1+D)/(r\cdot C_3) & -(1+D)/(r\cdot C_3) & (1+D)/(r\cdot C_3) \\ 0 & 0 & (1-D)/C_{high} & 0 & (1-D)/(r\cdot C_{high}) & (1-D)/(r\cdot C_{high}) & \frac{-R(1-D)-r}{rRC_{high}} \end{bmatrix}$$
$$\cdot \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{i}_{L3}(t) \\ \hat{u}_{C1}(t) \\ \hat{u}_{C2}(t) \\ \hat{u}_{C3}(t) \\ \hat{u}_{Chigh}(t) \end{bmatrix}$$
$$+ \begin{bmatrix} 0 & 0 & 0 & 1/L_1 & 0 & 1/L_1 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1/L_2 & 0 \\ 0 & 0 & -r/L_3 & 1/L_3 & -1/L_3 & 0 & 1/L_3 \\ -1/C_1 & 0 & -1/C_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1/C_2 & 0 & 1/(r\cdot C_2) & 1/(r\cdot C_2) & -1/(r\cdot C_2) \\ 1/C_3 & -1/C_3 & 0 & 0 & -1/(r\cdot C_3) & -1/(r\cdot C_3) & 1/(r\cdot C_3) \\ 0 & 0 & 1/C_{high} & 0 & -1/(r\cdot C_{high}) & -1/(r\cdot C_{high}) & 1/(r\cdot C_{high}) \end{bmatrix} \cdot \begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ U_{C1} \\ U_{C2} \\ U_{C3} \\ U_{Chigh} \end{bmatrix} \cdot \hat{d}(t) + \begin{bmatrix} 1/L_1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \cdot \hat{u}_{low}(t) \tag{37}$$

$$G_{uhighd}(s) = \frac{\widehat{u}_{high}(s)}{\widehat{d}(s)}$$
$$= \frac{1.1\times10^4 s^6 + 4.1\times10^{10}s^5 + 4.4\times10^{15}s^4 - 1.3\times10^{17}s^3 + 2.4\times10^{22}s^2 - 1.4\times10^{24}s + 2.4\times10^{28}}{1.2s^7 + 2.8\times10^6 s^6 + 8.3\times10^7 s^5 + 4.3\times10^{13}s^4 + 8.5\times10^{14}s^3 + 1.1\times10^{20}s^2 + 1.7\times10^{21}s + 1.3\times10^{25}} \tag{38}$$

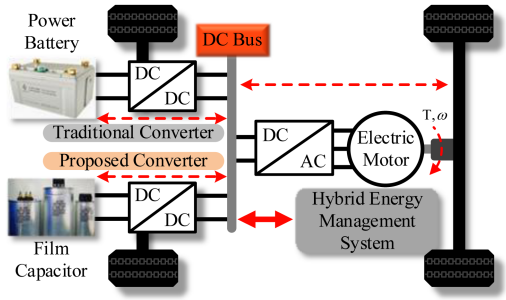

Fig. 9. Schematic diagram of the FCHESS.

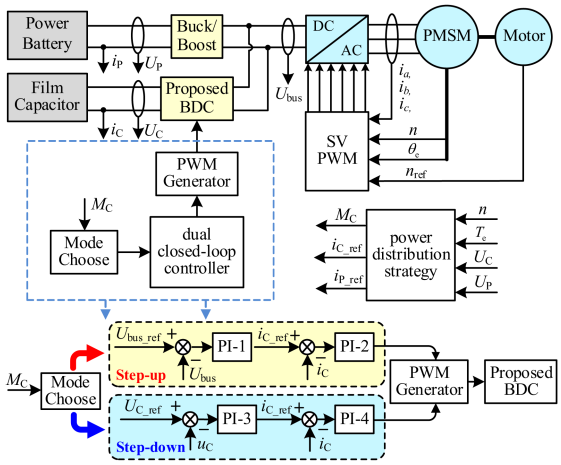

Fig. 10. Control block diagram of the FCHESS.

For the compensation of the current loop, the state-space average method can be used to derive the small-signal models $I_{\text{high}}(s)/d(s)$ and $I_{\text{low}}(s)/d(s)$ under step-up and step-down modes. It should also be noted that the cut-off frequency of the compensated current loop (voltage loop) should not exceed 1/5 to 1/10 of f_s (cut-off frequency of the current loop) to ensure the steady-state and dynamic performance of the proposed converter.

IV. Control System of the Proposed Converter

Fig. 9 shows the schematic diagram of the FCHESS, which mainly consists of a PB, a FC bank, a traditional BDC, the proposed BDC, a motor inverter, and a motor. When the FCHESS operates in a steady state, the PB provides energy to the motor through the traditional BDC. When the FCHESS operates in a transient state (e.g., acceleration and braking), the FC bank provides the additional energy to the motor through the proposed BDC or instantaneous energy is absorbed into the FC bank.

Fig. 10 shows the control block diagram of the FCHESS, where $U_{\text{bus\_ref}}$ is the dc link reference voltage, $U_{\text{C\_ref}}$ is the FC bank reference voltage, and $i_{\text{C\_ref}}$ is the FC reference current. Table III represents the control logic of the FCHESS. M_{C} represents the operating state of the EV, U_{L} is the voltage of the FC bank, $U_{\text{L\_min}}$ and $U_{\text{L\_max}}$ are the minimum and maximum

$$
\begin{aligned}
\frac{d}{dt}\begin{bmatrix}\hat{i}_{\text{L1}}(t)\\ \hat{i}_{\text{L2}}(t)\\ \hat{i}_{\text{L3}}(t)\\ \hat{u}_{\text{C1}}(t)\\ \hat{u}_{\text{C2}}(t)\\ \hat{u}_{\text{C3}}(t)\\ \hat{u}_{\text{Chigh}}(t)\end{bmatrix} &= \begin{bmatrix}0 & 0 & 0 & (D-1)/L_1 & 0 & D/L_1 & -1/L_1\\ 0 & 0 & 0 & 1/L_2 & 0 & -D/L_2 & 0\\ 0 & 0 & r\cdot(1-D)/L_3 & (D-1)/L_3 & (1-D)/L_3 & -1/L_3 & 0\\ (1-D)/C_1 & -1/C_1 & (1-D)/C_1 & 0 & 0 & 0 & 0\\ 0 & 0 & (D-1)/C_2 & 0 & -D/(r\cdot C_2) & -D/(r\cdot C_2) & 0\\ -D/C_3 & D/C_3 & 1/C_3 & 0 & -D/(r\cdot C_3) & -D/(r\cdot C_3) & 0\\ 1/C_{\text{low}} & 0 & 0 & 0 & 0 & 0 & -1/(R\cdot C_{\text{low}})\end{bmatrix}\\
&\cdot\begin{bmatrix}\hat{i}_{\text{L1}}(t)\\ \hat{i}_{\text{L2}}(t)\\ \hat{i}_{\text{L3}}(t)\\ \hat{u}_{\text{C1}}(t)\\ \hat{u}_{\text{C2}}(t)\\ \hat{u}_{\text{C3}}(t)\\ \hat{u}_{\text{Chigh}}(t)\end{bmatrix} + \begin{bmatrix}0 & 0 & 0 & 1/L_1 & 0 & 1/L_1 & 0\\ 0 & 0 & 0 & 0 & 0 & -1/L_2 & 0\\ 0 & 0 & -r/L_3 & 1/L_3 & -1/L_3 & 0 & 0\\ -1/C_1 & 0 & -1/C_1 & 0 & 0 & 0 & 0\\ 0 & 0 & 1/C_2 & 0 & -1/(r\cdot C_2) & -1/(r\cdot C_2) & 0\\ -1/C_3 & \frac{1}{C_3} & 0 & 0 & -1/(r\cdot C_3) & -1/(r\cdot C_3) & 0\\ 0 & 0 & 0 & 0 & 0 & 0 & 0\end{bmatrix}\cdot\begin{bmatrix}I_{\text{L1}}\\ I_{\text{L2}}\\ I_{\text{L3}}\\ U_{\text{C1}}\\ U_{\text{C2}}\\ U_{\text{C3}}\\ U_{\text{Clow}}\end{bmatrix}\cdot\hat{d}(t) + \begin{bmatrix}0\\ 0\\ D/L_3\\ 0\\ D/(r\cdot C_2)\\ D/(r\cdot C_3)\\ 0\end{bmatrix}\\
&\cdot\hat{u}_{\text{high}}(t) + \begin{bmatrix}0\\ 0\\ D/L_3\\ 0\\ 1/(r\cdot C_2)\\ 1/(r\cdot C_3)\\ 0\end{bmatrix}\cdot U_{\text{high}}\hat{d}(t)
\end{aligned}
\tag{39}
$$

$$
G_{\text{ulowd}}(s) = \frac{\hat{u}_{\text{low}}(s)}{\hat{d}(s)} = \frac{2.6\times10^{9}s^{5}+1.2\times10^{15}s^{4}+8\times10^{17}s^{3}+7.5\times10^{21}s^{2}+2.8\times10^{24}s+1.2\times10^{28}}{1.1s^{7}+5.1\times10^{5}s^{6}+9\times10^{9}s^{5}+1.3\times10^{13}s^{4}+1.5\times10^{17}s^{3}+7.5\times10^{19}s^{2}+4.4\times10^{23}s+1.2\times10^{26}}. \tag{40}
$$

TABLE III
CONTROL LOGIC OF THE PROPOSED FCHESS

	$M_C = -1$ (Deceleration)		$M_C = 1$ (Acceleration)	
	$U_L < U_{L\_max}$	$U_L \geq U_{L\_max}$	$U_L < U_{L\_min}$	$U_L \geq U_{L\_min}$
PB	IN ($SOC < SOC_{max}$)		OUT	OUT
FC	IN	×	×	OUT
R	×	IN ($SOC > SOC_{max}$)	×	×

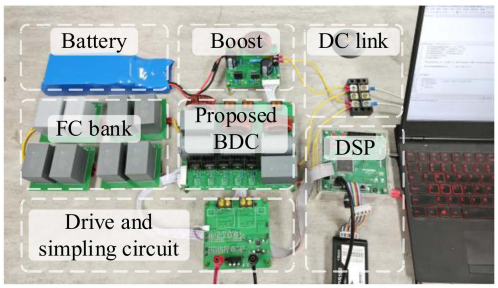

Fig. 11. Experimental prototype of FCHESS.

TABLE IV
EXPERIMENTAL PARAMETERS

Parameters	Values	Parameters	Values
P_n	200W	U_{high}	400V
C_{low}/C_{high}	110uF/550V	U_{low}	20-150V
C_1-C_3	110uF/550V	S_1-S_3	IXTQ52N30P
L_1-L_3	1/1.5/4mH	S_4-S_5	SPW47N60C3

voltages of the FC bank, SOC_{max} is the maximum state of charge of the PB, and R is the energy consumption resistor.

When M_C is 0, the EV operates in a steady state, and only the PB supplies energy to the EV. When M_C is 1, the EV operates in an accelerating state. When U_L is greater than U_{L_min}, both the PB and the FC bank supply energy to the EV. Otherwise, only the PB supplies energy to the EV. When the M_C is –1, the EV is in a decelerating state. When U_L is lower than U_{L_max}, the FC absorbs the energy of the motor's braking feedback. When the SOC is lower than the SOC_{max}, the PB absorbs the energy of the motor's braking feedback. If the SOC is greater than the SOC_{max} and U_L is greater than or equal to U_{L_max}, the excess energy is absorbed by the energy-consuming resistor.

V. EXPERIMENTAL RESULTS AND ANALYSIS

To verify the effectiveness of the proposed converter, an experimental platform is built as shown in Fig. 11 where the control signals of the power switches are generated by TMS320F28335 with a switching frequency of 50 kHz. The parameters used in the experimental circuit are shown in Table IV. L_1–L_3 are inductors with sendust cores. TC4452 are used to drive S_1–S_5. Voltage hall sensor and current hall sensor are used to accurately measure the voltage and current of key components All the circuit parameters are selected in accordance with the circuit parameter design guidelines given in Section III.

A. Experimental Results in the Step-Up Mode

Fig. 12 shows the key waveforms of the proposed converter in step-up mode, when $U_{low} = 20$ V and $d_{Boost} = 0.7$. Fig. 12(a) shows the U_{high} and the voltage across the capacitors in steady state, where $U_{high} = 398$ V, $U_{C1} = 68.3$ V, $U_{C2} = 188$ V, and $U_{C3} = 204$ V, which is in agreement with the theoretical calculations in (4) and (13), verifying the high voltage gain characteristics of the proposed converter. Fig. 12(b) and (c) show the voltage stresses on S_1–S_5, where $U_{S1} = 71.5$ V, $U_{S2} = 216$ V, $U_{S3} = 66.5$ V, $U_{S4} = 273$ V, and $U_{S5} = 275$ V. These waveforms show that the voltage stress on power switches is all less than U_{high}, and the voltage stresses on S_1 and S_3 are even lower than $U_{high}/4$, which are basically in agreement with theoretical calculations of (14) and verify the low voltage stress characteristic of the proposed converter. Fig. 12(d) shows that the inductor current waveforms, where the average values of i_{L1}, i_{L2} and i_{L3} are $I_{L1} = 10.7$ A, $I_{L2} = 7.48$ A, and $I_{L3} = 0.49$ A, respectively. These currents are consistent with theoretical calculation of (18). In this experiment, the efficiency is 91.2%.

B. Experimental Results in the Step-Down Mode

Fig. 13 shows the key waveforms of the proposed converter in step-down mode, when $U_{high} = 400$ V and $d_{Buck} = 0.3$. As in Fig. 13(a), $U_{low} = 19.5$ V, which verifies the voltage gain characteristics of the proposed converter in (8). In addition, Fig. 13(a) shows that $U_{C1} = 72.5$ V, $U_{C2} = 180$ V, and $U_{C3} = 212$ V, which verifies that (15) is correct. Figs. 13(b) and 12(c) show the voltage stresses on S_1–S_5, where $U_{S1} = 90.1$ V, $U_{S2} = 240$ V, $U_{S3} = 74.3$ V, $U_{S4} = 292$ V, and $U_{S5} = 280$ V. These voltages verify the correctness of (16). Moreover, it can be seen that the voltage stresses of all power switches are lower than $U_{high} = 400$ V, and voltage stresses on S_1 and S_3 are even lower than $U_{high}/4$. Therefore, the proposed BDC has the characteristic of low voltage stress on power switches. Fig. 13(d) shows the waveforms of the currents on L_1, L_2, and L_3, where $I_{L1} = 9.92$ A, $I_{L2} = 7.45$ A, and $I_{L3} = 0.53$ A, which are consistent with theoretical calculations of (20). In this experiment, the efficiency is 91.7%.

C. Dynamic Performance

In this experiment, a double closed-loop controller is adopted to control the dc link voltage and inductor current, while these two variables are collected by Hall sensors. Fig. 14(a) and (b) show the HVS voltage U_{high} of the proposed BDC with linear changes of the LVS voltage U_{low}. In Fig. 14(a), the proposed BDC operates in step-up mode: U_{low} is linearly increased from 20 to 150 V, and U_{high} remains steady at 400 V. In Fig. 14(b), the proposed BDC operates in step-down mode: When U_{high} is 400 V, U_{low} is linearly decreased from 150 to 20 V. This experiment proves that the proposed converter has a good performance of voltage tracking capability, wider voltage gain and higher gain ratio.

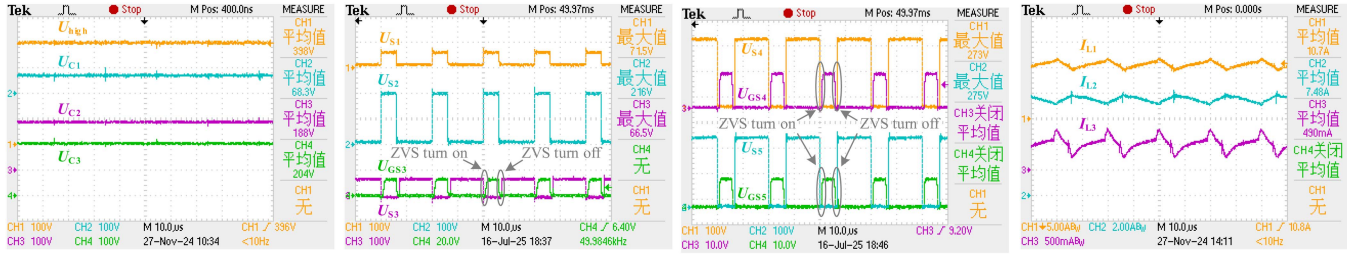

Fig. 12. Experimental waveforms in step-up mode. (a) U_{high}, U_{C1}, U_{C2}, and U_{C3}. (b) U_{S1}, U_{S2}, and U_{S3}. (c) U_{S4} and U_{S5}. (d) i_{L1}, i_{L2}, and i_{L3}.

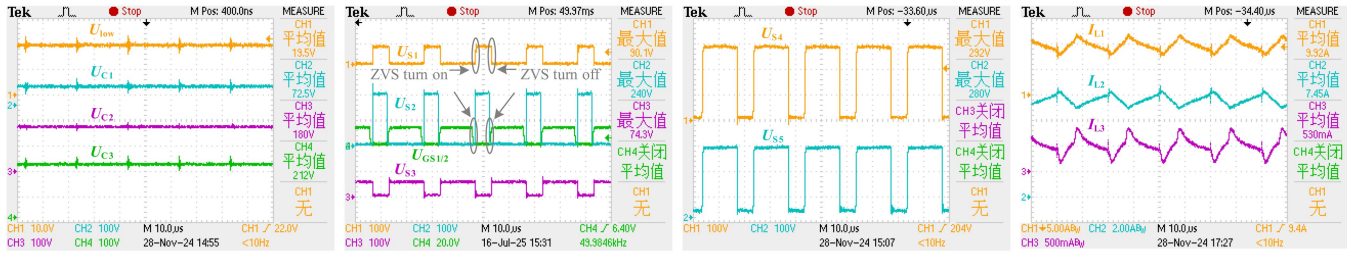

Fig. 13. Experimental waveforms in step-down mode. (a) U_{low}, U_{C1}, U_{C2}, and U_{C3}. (b) U_{S1}, U_{S2}, and U_{S3}. (c) U_{S4} and U_{S5}. (d) i_{L1}, i_{L2}, and i_{L3}.

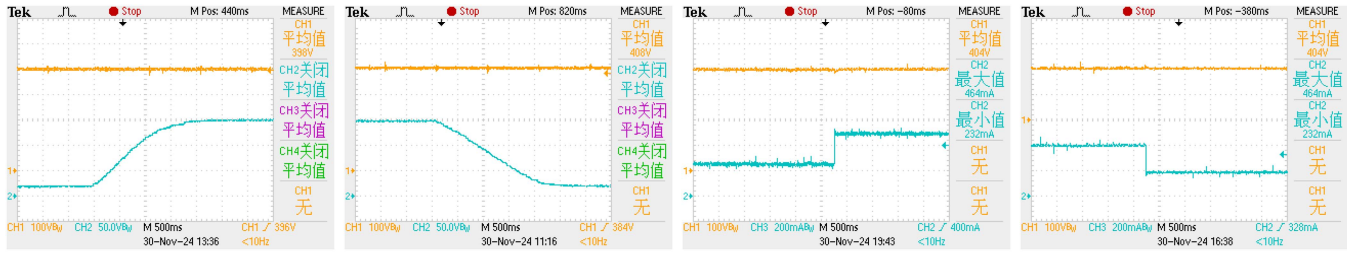

Fig. 14. Dynamic performance experimental waveforms. (a) Variable input in step-up mode. (b) Variable output in Step-down mode. (c) Step-up mode load variation. (d) Step-down mode load variation.

Fig. 14(c) and (d) show the output voltages of the proposed BDC when the output power varies from 100 to 200 W and from 200 to 100 W, respectively. In both cases, the output voltage remains almost unaffected by power variations, whether in step-up or step-down mode, which verifies that the proposed BDC has excellent dynamic performance during abrupt load power variations.

D. Thermal Performance

To verify the thermal stability performance, especially the maximum voltage stress on S_4 and S_5, thermal tests are conducted. The temperature rise ΔT is the difference between the junction temperature T_{j} and the ambient temperature T_{a}

$$\Delta T = T_{\mathrm{j}} - T_{\mathrm{a}} = P_{\mathrm{loss}} \times R_{\mathrm{th(j-a)}} \tag{42}$$

where P_{loss} represents the total power loss of the power switches, including switching loss and conduction loss, and $R_{\mathrm{th(j-a)}}$ represents the total thermal resistance from junction to ambient.

$R_{\mathrm{th(j-a)}}$ is the sum of the thermal resistances of all parts

$$R_{\mathrm{th(j-a)}} = R_{\mathrm{th(j-c)}} + R_{\mathrm{th(c-s)}} + R_{\mathrm{th(s-a)}} \tag{43}$$

where $R_{\mathrm{th(j-c)}}$ represents the thermal resistance from the junction to the case; $R_{\mathrm{th(c-s)}}$ represents the thermal resistance from the case to the heat sink; and $R_{\mathrm{th(s-a)}}$ represents the thermal resistance from the heat sink to the ambient.

Based on (42), (43), and Section III-E, the theoretical power loss and temperature rises of power switches under air cooling at the worst-case operating point ($U_{\mathrm{low}} = 20$ V, $U_{\mathrm{high}} = 400$ V, $P_{\mathrm{o}} = 200$ W) and the optimum operating point ($U_{\mathrm{low}} = 150$ V, $U_{\mathrm{high}} = 400$ V, $P_{\mathrm{o}} = 200$ W) can be obtained, as shown in Table V. The thermal image in Fig. 15 which was taken by HIKMICRO

TABLE V
THEORETICAL POWER LOSS AND TEMPERATURE RISE

Operating point	Worst-case operating point		Optimum operating point	
	ΔP	ΔT	ΔP	ΔT
S_1	5.16W	63.5°C	1.14W	14°C
S_2	2.63W	32.5°C	0.2W	2.5°C
S_3	1.91W	23.5°C	1.03W	12.7°C
S_4	1.03W	12.7°C	0.73W	9°C
S_5	1.03W	12.7°C	0.73W	9°C

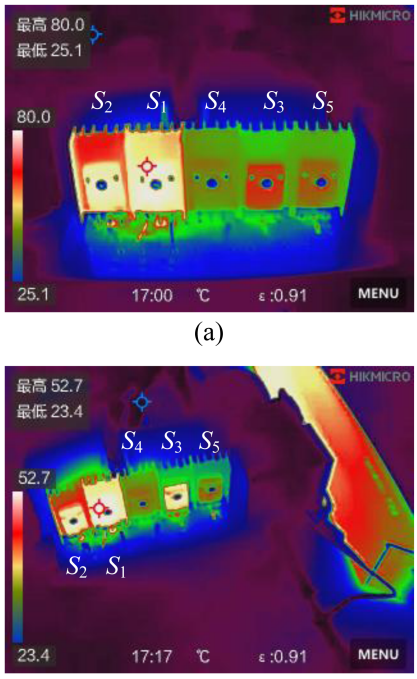

Fig. 15. Thermal image. (a) Worst-case operating point. (b) Optimum operating point.

K20 shows that S_4 and S_5, despite bearing the maximum voltage stress, do not suffer from thermal stability imbalance.

E. Converter Efficiency Analysis

Fig. 16 shows power loss distribution of the experimental prototype at $U_{\text{low}} = 20$ V, $U_{\text{high}} = 400$ V, and $P_{\text{n}} = 200$ W, and the experimental efficiency is measured by Yokogawa WT5000 power analyzer. The power loss distribution of the proposed converter in step-up mode is shown in Fig. 16(a), which has a total power loss of 18.83 W with an efficiency of 91.2%. The conduction loss of S_1–S_5 is 3.6 W, accounting for 19.12% of the total power loss. The switching loss of S_1–S_5 is 9.11 W, accounting for 48.38% of the total power loss. The copper loss of the inductor is 3.52 W, accounting for 18.69% of the total power loss. The core loss of the inductor is 1.53 W, accounting for 8.13% of the total power loss and the capacitor loss is 1.07W, accounting for 5.68% of the total power loss.

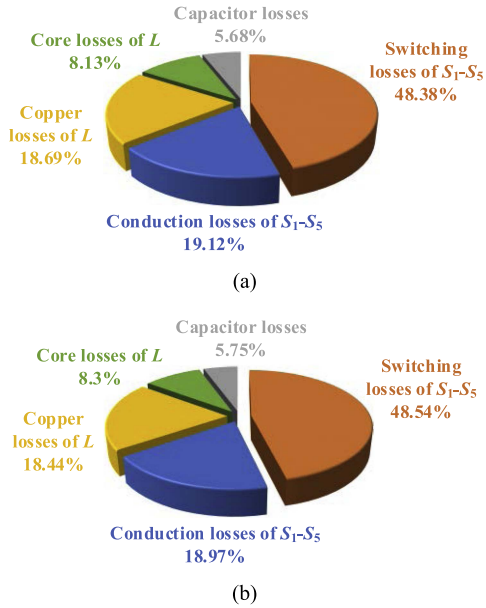

Fig. 16. Theoretical power loss distribution (a) Step-up mode. (b) Step-down mode.

The power loss distribution of the proposed converter in step-down mode is shown in Fig. 16(b), which has the total power loss of 18.56 W with an efficiency of 91.7%. The conduction loss of power switches S_1–S_5 is 3.34 W, accounting for 18.97% of the total power loss. The switching loss is 8.54 W, accounting for 48.54% of the total power loss. The copper loss of the inductor is 3.25 W, accounting for 18.44% of the total power loss. The core loss of the inductor is 1.46 W, accounting for 8.3% of the total power loss and the capacitor loss is 1.01 W, accounting for 5.75% of the total power loss. The above data show that the power loss of the proposed BDC is mainly attributed to the switching loss and conduction loss of the power switches, along with the copper loss of the inductors.

Fig. 17(a) shows the theoretical efficiency curve and the experimental efficiency curve of the proposed converter, where U_{low} is from 20 to 150 V, $U_{\text{high}} = 400$ V, and $P_{\text{n}} = 200$ W. Theoretical efficiency is calculated using the power loss formulas in Section III-E. The experimental efficiency of the proposed converter ranges from 91.7% ($U_{\text{low}} = 20$ V) to 94.8% ($U_{\text{low}} = 150$ V) in step-up mode, and 91.2% ($U_{\text{low}} = 20$ V) to 95% ($U_{\text{low}} = 150$ V) in step-down mode. These curves show that the converter efficiency gradually increases with increasing FC voltage at the same power level, since the input current decreases gradually in this case. Furthermore, Fig. 17(a) shows that the experimental efficiency of the converter is lower than the theoretical efficiency due to parasitic parameters and nonideal characteristics.

Fig. 17(b) shows the maximum efficiency curves at different powers in step-up and step-down modes. With the same voltage gain, the efficiency of the proposed BDC increases with an increase in load power and reaches its maximum at 200 W and then starts to decrease.

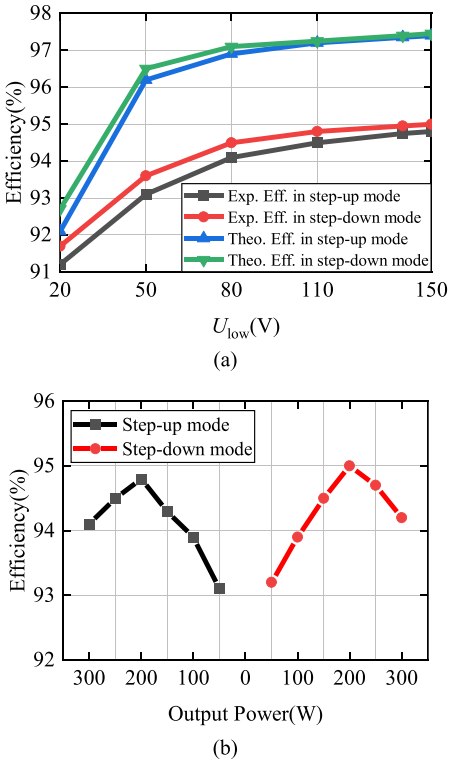

Fig. 17. Efficiencies curves. (a) Rated power. (b) Different power.

VI. Conclusion

In this article, a novel nonisolated bidirectional dc–dc converter for FCHESS is proposed, which has the advantages of wide voltage gain, high gain ratio, and absolute common ground. The experiment verifies the feasibility of the proposed converter. Under the step-up condition, the steady experiments show that the proposed converter has a high voltage gain, which can satisfy the energy transfer from the low voltage FC to the high voltage dc link. Meanwhile, the voltage stress of some power switches is less than U_{high}, and the average input current is 10 A, which effectively reduces the cost of the proposed converter, improves the efficiency of the FCHESS, and increases the energy utilization. The voltage of the FC is in the range of 20–150 V and the dc link voltage is stabilized at 400 V during the dynamic working condition, which effectively verifies the high gain ratio characteristic of the proposed converter. The proposed converter also shows excellent performance in step-down mode. All these advantages make the proposed converter a suitable solution for connecting FCHESS to dc link.

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