

A Peak-Current-Limit Soft Start Control Method With Short-Circuit Tolerance for CLLC Converter Based on Time-Domain Model

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Abstract—The CLLC converter has been widely adopted in electric vehicle chargers due to its advantages of high efficiency, high power density, and low electromagnetic interference. However, in outdoor applications, such as fast-charging stations, harsh environmental conditions pose significant challenges to the CLLC converter, particularly in the form of short-circuit faults. To address this issue, a short-circuit-tolerant soft start control method for the CLLC resonant converter is proposed in this article. Based on time-domain model, the minimum limit of the switching frequency is adaptively adjusted according to the voltage gain, enabling limitation of the peak resonant current. Finally, experimental results obtained from a 1-kW prototype demonstrate that the proposed control method effectively limits the startup current under various load conditions and exhibits short-circuit tolerance during both startup and steady-state operation. The startup time is reduced by 20%–72% compared to existing methods with the same hardware configuration and maximum resonant current.

Index Terms—CLLC resonant converter, peak resonant current, soft start, time-domain model.

NOMENCLATURE

C	Vector of constants in the general solution of v_{Cr2} .
C_2	Secondary bus capacitance.
C_{r1}	Primary resonant capacitance.
C_{r2}	Secondary resonant capacitance.
D	Vector of derivatives of v_{Cr2} .
D_0	Phase of stage switching.
I	Identity matrix.
I_1	Input current of the converter.
I_2	Output current of the converter.
L_m	Magnetizing inductance.
L_{r1}	Primary resonant inductance.
L_{r2}	Secondary resonant inductance.
R_L	Load resistance.
S	Vector of bridge arm voltages.
T_s	Switching cycle.
T_{s0}	Initial switching cycle of the startup process.

V_1	DC voltage of primary side.
V_2	DC voltage of secondary side.
V_{2_ref}	Reference dc voltage of secondary side.
f_n	Normalized switching frequency ($f_n = f_s/f_r$).
f_{n_min}	Minimal normalized switching frequency limit.
f_r	Resonant frequency.
f_s	Switching frequency.
i_{Lm}	Magnetizing current.
i_{Lr1}	Primary resonant current.
i_{Lr1_peak}	Peak value of the primary resonant current.
i_{Lr2}	Secondary resonant current.
m	Normalized voltage gain ($m = nV_2/V_1$).
n	Turn ratio of transformer.
$t_{a,b,c}$	Intervals of initial switching pattern.
v_{Cr1}	Primary resonant capacitor voltage.
v_{Cr2}	Secondary resonant capacitor voltage.
v_{ab}	H-bridge voltage of primary side.
v_{cd}	H-bridge voltage of secondary side.
x	Vector of state variables.

I. INTRODUCTION

WITH excellent soft-switching, power density and efficiency characteristics, CLLC converters are gradually becoming the most popular isolated bidirectional dc–dc converter topology and are realizing a wide range of applications in areas, such as dc microgrid, electric vehicle (EV), and space power supply [1], [2], [3], [4].

The CLLC resonant converter, as shown in Fig. 1, has been treated as the bidirectional version of the LLC resonant converter. Like the LLC converter, the CLLC converter adjusts the output voltage by varying the switching frequency, also known as pulse frequency modulation (PFM) [5], [6], [7], [8].

Modeling of resonant converters is important to achieve high performance operation. Operation mode analysis (OMA) is the most utilized time-domain modeling method, creates separate sets of transcendental equations for different operating mode to obtain the expression of state variables. However, the OMA method requires solving for at least five unknowns, which places high demands on the initial values used to iteratively solve the system of nonlinear equations, and unsuitable initial values may lead to solution failure [5], [6]. Therefore, an OMA model with fewer unknowns is more desirable.

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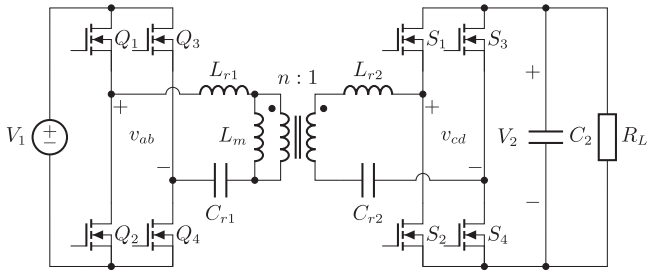


Fig. 1. Diagram of CLLC resonant converter.

In this article, an improved OMA model for CLLC converters is presented, where the number of unknowns is reduced to one as compared to the conventional OMA model [5], which ensures the speed and reliability of the time-domain model.

As EV charging systems typically operate in outdoor environments, the equipment is prone to aging due to exposure to environmental factors, such as water ingress, dust accumulation, and salt corrosion, ultimately leading to degradation of insulation performance [9], [10].

The failures of converters can be categorized as internal and external. Internal failures are mainly short-circuit fault and open-circuit fault of switches, where the short-circuit fault of switches are usually caused by switch breakdowns, and the open-circuit fault of switches generally occurs as a result of the gate drive circuit malfunctioning [11].

An internal failure of the converter usually means that the hardware function has changed and cannot be restored on its own. Recently, many solutions have been proposed to detect and fix failures of switches [11], [12], [13]. On the other hand, if the converter is protected, it can usually be recovered after external failures (mainly short-circuit of the outputs) [14].

During the startup phase of the converter, although the duration is relatively short, the output voltage rises rapidly. If the breakdown voltage of the external circuit has already decreased below the output voltage due to insulation degradation, a short-circuit fault may occur [15]. In steady-state operation, continuous current flow through conductors generates heat, causing thermal expansion of materials that may also lead to short circuits. In addition, external vibrations or accidental human contact may trigger such faults. Therefore, short-circuit faults can occur during both the startup and steady-state operating phases of the converter, necessitating effective short-circuit protection under both conditions [16].

The objective of short-circuit protection is to prevent damage to the switches in the event of a sudden drop in output voltage to zero. Existing protection strategies can be broadly categorized into two approaches: incorporating additional protection circuit [17] or employing trajectory control method [19]. Adding protection circuit [14] usually brings additional hardware and volume costs, and trajectory control method is based on high frequency sampling of the resonant currents, which requires high controller performance [18].

Resonant converters are subject to very high voltage and current stresses during startup, which usually result in overheating damage to the switches and overvoltage breakdown

of the resonant capacitors, making soft start essential [20], [21], [22]. Soft start techniques for CLLC converter are typically divided into fixed-frequency and variable-frequency types, as summarized in Table I, where more stars for speed indicate a faster startup speed, and more stars for complexity indicate a more difficult controller implementation. And the complexity metrics include the type of signals being sampled, the type of control variables and the number of computational operations in the controller.

In [15], a fixed frequency fixed duty cycle soft start approach is introduced, offering inherent short-circuit protection during startup. Nevertheless, the limited power transfer leads to prolonged startup time, and the method may fail to initiate properly under load conditions. An adaptive current-limit soft start method that iteratively computes the time-domain model during startup and change the duty cycle to regulate the resonant current is proposed in [20]. But the necessity of predefining the load resistance and output capacitance prior to the computation constrains the method's applicability.

Compared to fixed-frequency methods, variable-frequency approaches offer the advantage of a wider zero-voltage switching (ZVS) range and can maintain ZVS throughout the entire startup process. Since the output current under PFM control increases with the peak resonant current at the same voltage gain, the starting speed can be maximized by controlling the peak resonant current near the limiting value [23].

A variable-frequency soft-start method based on an artificial neural network is proposed in [21], which enables fast startup but imposes high demands on the controller performance and lacks short-circuit tolerance. Optimal trajectory control (OTC) can regulate the peak resonant current of LLC converter during startup to stabilize it under different load conditions, enabling fast startup without overcurrent [18]. And there are simplified OTC methods that do not require high-frequency sampling [19], [24], [25]. Unfortunately, these simplified OTC cannot be migrated due to the high circuit order of the CLLC converter.

In summary, an ideal soft start method for CLLC converter should exhibits the following characteristics.

- 1) Short-circuit tolerance.
- 2) Minimized startup time.
- 3) Low controller performance requirement.

In this article, a current-limit soft start method based on a m - f_{n_min} curve is proposed. The m - f_{n_min} curve is generated offline based on the proposed improved OMA model, enabling peak current limitation throughout the entire operating process. And this current constraint inherently provides the controller with soft start capability and short-circuit tolerance.

The rest of this article is organized as follows. Section II provides the derivation of the improved OMA model of CLLC converters. In Section III, the proposed soft start method is introduced. Experimental results are provided in Section IV. Finally, Section V concludes this article.

II. TIME DOMAIN MODEL

The CLLC converter can be divided into three parts: the inverter at the primary side, the resonant tank in the middle, and the rectifier at the secondary side. The equivalent circuit of

TABLE I
COMPARISON OF DIFFERENT STARTUP TECHNIQUES FOR LLC AND CLLC CONVERTERS

References	Method	Converter	Switching frequency	Sampling variables	Short-circuit tolerance	Startup speed	Complexity
[15]	Fixed frequency fixed duty cycle	LLC and CLLC	Fixed	V_1, V_2	Yes	*	*
[20]	Fixed frequency adaptive duty cycle	LLC and CLLC	Fixed	V_1, V_2	No	****	****
[21]	Artificial neural network control	LLC and CLLC	Variable	V_1, V_2, I_2	No	*****	*****
[19]	Simplified optimal trajectory control	LLC	Variable	V_1, V_2, I_2	Yes	*****	****
This article	Minimal switching frequency limit	LLC and CLLC	Variable	V_1, V_2	Yes	*****	***

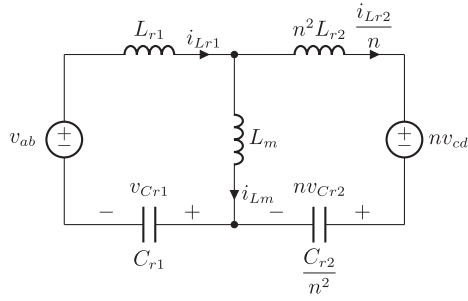


Fig. 2. Equivalent circuit of the CLLC resonant tank.

TABLE II
DIFFERENT OPERATING STAGES OF CLLC

Stage	P	N	O
Rectifier			
nv_{cd}	nV_2	$-nV_2$	$v_{Lm} - nv_{Cr2}$

the resonant tank is shown in Fig. 2, where the value of v_{ab} can be $-V_1$, 0, or V_1 depending on the inverter drive signal. And the value of v_{cd} depends on the conduction state of the rectifier.

As shown in Table II, according to the conduction state of the rectifier, the operation of CLLC converter can be categorized into three stages, P, N, O, which represent the forward conduction, reverse conduction, and turnoff of the rectifier, respectively. During the O stage, the nv_{cd} in Fig. 2 is open-circuited with its value equals to $v_{Lm} - nv_{Cr2}$.

According to the OMA model introduced in [5] and [6], the operation mode of the CLLC converter is determined by the sequence of stages occurring during half a switching cycle, of which the most common modes are PN, PO, PON, OPO exist when $f_n < 1$ and OPO, NOP, NP exist when $f_n > 1$, summarized in Table III.

During a frequency-decreasing soft start, f_n will gradually decrease from a large value (usually 1.5–2.5) while V_2 increases from 0. And the output current will be large in order to shorten the startup time. So, the CLLC converter will operate in NP mode

TABLE III
DIFFERENT OPERATING MODES OF CLLC

Frequency f_s	$< f_r$			f_r	$> f_r$			
	PN	PON	PO	OPO	P	OPO	NOP	NP
Mode	Buck/Boost		Boost		I	Buck		
Output current	Large \rightarrow Small			All	Small \rightarrow Large			

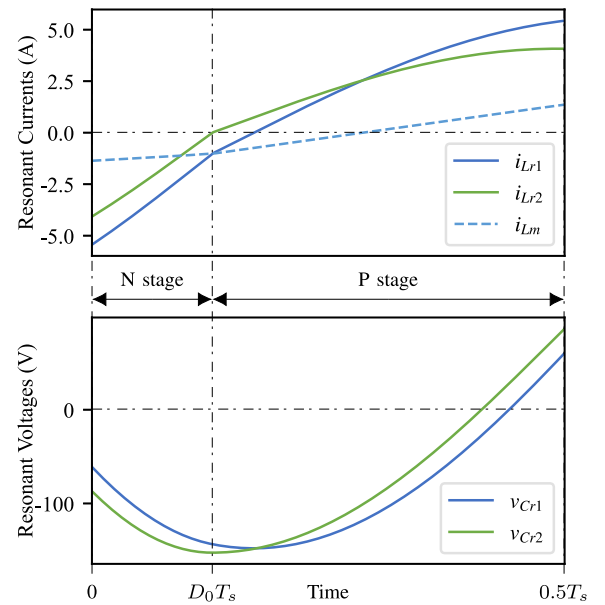


Fig. 3. Operation waveforms of NP mode.

during the startup process, as shown in Fig. 3. For the brevity, the analysis in this section will also focus on the NP mode.

Since the dc link capacitor C_2 is much larger than the resonant capacitors C_{r1} and C_{r2} , within a single stage V_2 can be considered constant. Then, v_{ab} and v_{cd} in the equivalent circuit can also be constant during single stage. In addition, there are four independent state variables as

$$\mathbf{x} = [i_{Lr1} \quad i_{Lr2}/n \quad v_{Cr1} \quad nv_{Cr2}]^T. \quad (1)$$

According to Kirchhoff's circuit laws, there is

$$\begin{cases} i_{Lr1} = i_{Cr1} \\ i_{Lr2} = i_{Cr2} \\ i_{Lm} = i_{Lr1} - i_{Lr2}/n \\ v_{Cr1} = v_{ab} - v_{Lr1} - v_{Lm} \\ nv_{Cr2} = v_{Lm} - nv_{Lr2} - nv_{cd} \end{cases} \quad (2)$$

and based on the differential equations for capacitors and inductors, there is

$$\begin{cases} v_{Lr1} = L_{r1}i'_{Lr1} \\ v_{Lr2} = L_{r2}i'_{Lr2} \\ v_{Lm} = L_m i'_{Lm} \\ i_{Cr1} = C_{r1}v'_{Cr1} \\ i_{Cr2} = C_{r2}v'_{Cr2}. \end{cases} \quad (3)$$

Combining (2) and (3) together and eliminating state variables other than nv_{Cr2} gives

$$anv_{Cr2}^{(4)} + bnv_{Cr2}'' + n(v_{Cr2} + v_{cd}) = 0 \quad (4)$$

where

$$\begin{cases} a = (n^2 L_{r1} L_{r2} + L_{r1} L_m + n^2 L_{r2} L_m) C_{r1} C_{r2} / n^2 \\ b = (L_{r1} + L_m) C_{r1} + (n^2 L_{r2} + L_m) C_{r2} / n^2. \end{cases} \quad (5)$$

The characteristic equation of (4) has two pairs of conjugate imaginary roots, denoted $\pm\omega_1 i$ and $\pm\omega_2 i$, respectively, where

$$\begin{cases} \omega_1 = \sqrt{\frac{b - \sqrt{b^2 - 4a}}{2a}} \\ \omega_2 = \sqrt{\frac{b + \sqrt{b^2 - 4a}}{2a}}. \end{cases} \quad (6)$$

Then, the generalized solution for $n(v_{Cr2} + v_{cd})$ and its derivatives can be obtained as

$$\mathbf{D}(t) = \mathbf{M}_C(t) \mathbf{C} \quad (7)$$

where

$$\mathbf{M}_C(t) =$$

$$\begin{bmatrix} \sin \omega_1 t & \cos \omega_1 t & \sin \omega_2 t & \cos \omega_2 t \\ \omega_1 \cos \omega_1 t & -\omega_1 \sin \omega_1 t & \omega_2 \cos \omega_2 t & -\omega_2 \sin \omega_2 t \\ -\omega_1^2 \sin \omega_1 t & -\omega_1^2 \cos \omega_1 t & -\omega_2^2 \sin \omega_2 t & -\omega_2^2 \cos \omega_2 t \\ -\omega_1^3 \cos \omega_1 t & \omega_1^3 \sin \omega_1 t & -\omega_2^3 \cos \omega_2 t & \omega_2^3 \sin \omega_2 t \end{bmatrix} \quad (8)$$

$$\mathbf{D}(t) = [n(v_{Cr2} + v_{cd}) \quad nv'_{Cr2} \quad nv''_{Cr2} \quad nv'''_{Cr2}]^T \quad (9)$$

and

$$\mathbf{C} = [c_1 \quad c_2 \quad c_3 \quad c_4]^T. \quad (10)$$

Based on (2) and (3), there also is

$$\mathbf{D}(t) = \mathbf{M}_V(\mathbf{x}(t) + \mathbf{S}) \quad (11)$$

where

$$\mathbf{M}_V =$$

$$\begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & \frac{n^2}{C_{r2}} & 0 & 0 \\ 0 & 0 & \frac{n^2 L_{r2}}{a/C_{r1}} & \frac{L_{r1} + n^2 L_{r2}}{a/C_{r1}} \\ -\frac{n^2 L_{r2}}{a} & -\frac{n^2 L_{r1} + n^4 L_{r2}}{a C_{r2}/C_{r1}} & 0 & 0 \end{bmatrix} \quad (12)$$

$$\mathbf{S} = [0 \quad 0 \quad -v_{ab} \quad nv_{cd}]^T. \quad (13)$$

Taking $t = 0$, from (11) and (7) there is

$$\mathbf{C} = \mathbf{M}_C(0)^{-1} \mathbf{D}(0) = \mathbf{M}_C(0)^{-1} \mathbf{M}_V(\mathbf{x}(0) + \mathbf{S}) \quad (14)$$

and

$$\begin{aligned} \mathbf{x}(t) &= \mathbf{M}_V^{-1} \mathbf{D}(t) - \mathbf{S} \\ &= \mathbf{M}_V^{-1} \mathbf{M}_C(t) \mathbf{C} - \mathbf{S} \\ &= \mathbf{M}_V^{-1} \mathbf{M}_C(t) \mathbf{M}_C(0)^{-1} \mathbf{M}_V(\mathbf{x}(0) + \mathbf{S}) - \mathbf{S}. \end{aligned} \quad (15)$$

Denote

$$\mathbf{A}(t) = \mathbf{M}_V^{-1} \mathbf{M}_C(t) \mathbf{M}_C(0)^{-1} \mathbf{M}_V \quad (16)$$

there is

$$\mathbf{x}(t) = \mathbf{A}(t)(\mathbf{x}(0) + \mathbf{S}) - \mathbf{S}. \quad (17)$$

Since $\mathbf{A}(t)$ is a function of t , the state variable $\mathbf{x}(t)$ within a single stage can be obtained from (17) provided that $\mathbf{x}(0)$ is known.

Let us go back to the NP mode waveforms shown in Fig. 3, the state variables at the start and end moments can be expressed according to (17) as (18), where \mathbf{S}_P and \mathbf{S}_N represent voltage sources in P stage and N stage equivalent circuits, respectively. In the first half of the switching cycle, $V_{ab} = V_1$, thus according to Table II and (13), there are

$$\mathbf{S}_P = [0 \quad 0 \quad -V_1 \quad nV_2]^T \quad (19)$$

$$\mathbf{S}_N = [0 \quad 0 \quad -V_1 \quad -nV_2]^T \quad (20)$$

Morphing (18) shown at the bottom of the next page, gives the expression of $\mathbf{x}(0)$ as (21). Unfortunately, for single active modulation, the D_0 is unknown, and its value depends on the moment when i_{Lr2} crosses zero, i.e.,

$$i_{Lr2}(D_0 T_s) = 0. \quad (22)$$

Since $i_{Lr2}(D_0 T_s)$ is a part of $\mathbf{x}(D_0 T_s)$, and $\mathbf{x}(D_0 T_s)$ can be computed from (15) with the $\mathbf{x}(0)$ calculated from (21), shown at the bottom of the next page.

Then, the D_0 is the only unknown in the calculation, but (22) is transcendental, which needs to be calculated by numerical methods.

Since there is only one unknown, the waveform solving will be more stable and effective. Based on Intel Core i5-1240P CPU with single-threaded condition and Newton's method, the proposed model takes only 400–500 ms to complete 10 000 calculations while the conventional OMA method with more unknowns in [5] takes 2000–2500 ms.

Once the solution of D_0 is obtained, $\mathbf{x}(0)$ can be calculated from (21), then $\mathbf{x}(t)$ at any moment in the switching cycle can be obtained from (15).

III. PROPOSED SOFT START METHOD

A. Control Method

The control block diagram of the proposed soft start method is shown in Fig. 4, and the main difference compared to the conventional closed-loop control with PFM modulation is the addition of a m - f_{n_min} curve. This m - f_{n_min} curve is calculated offline based on the proposed time-domain model, which can output the minimum normalized switching frequency f_{n_min} based on

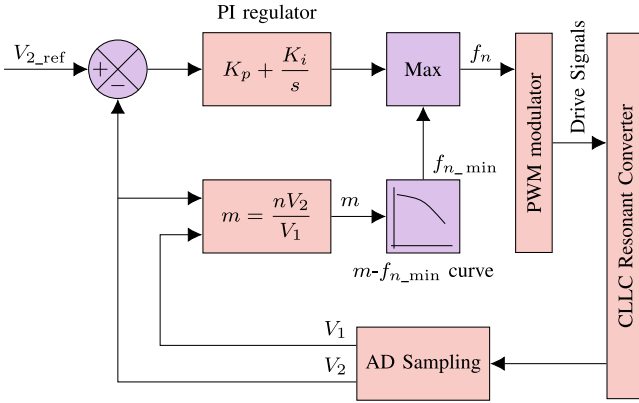


Fig. 4. Control block diagram with the proposed soft start method.

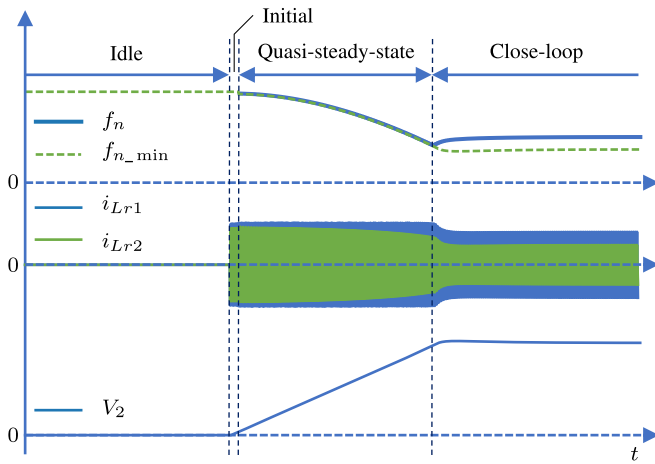
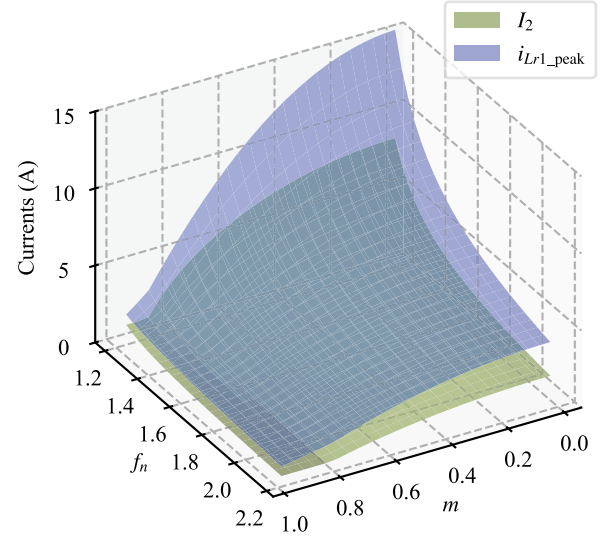


Fig. 5. Simulation waveforms of the proposed soft start method.

different normalized voltage gains m to achieve the limitation of the peak resonant current during the starting process.

The waveforms of the proposed soft start method are shown in Fig. 5, which can be categorized into the initial phase and the quasisteady-state phase. In the initial phase, the controller sends out drive signals according to the preset initial switching pattern to smooth the converter from the idle phase to the quasisteady-state phase.

During the quasisteady-state phase, the normalized switching frequency f_n outputted by the PI regulator remains clamped by f_{n_min} , which decreases as m increases. As the output voltage V_2 approaches its reference value V_{2_ref} , the output of PI regulator will fall slower than f_{n_min} , at which point the converter will smoothly transition to the closed-loop operation.

Fig. 6. Steady-state currents varying with normalized voltage gain m and normalized switching frequency f_n .

Since the output capacitor C_2 is much larger than the resonant capacitors, the difference in output voltage before and after a single switching cycle is very small, and it can be approximated that the waveforms of a single switching cycle are equal to the steady-state operating waveforms at the same voltage gain and switching frequency.

B. m - f_{n_min} Curve

Based on the time-domain model introduced in the previous section, the steady-state waveforms at $m < 1$ and $f_n > 1$ can be calculated and the corresponding peak resonant current i_{Lr1_peak} and average output current I_2 are obtained, as shown in Fig. 6.

Since I_2 is proportional to the rise speed of output voltage and increases with i_{Lr1_peak} . To make the startup process as fast as possible, i_{Lr1_peak} needs to be controlled close to its maximum limit.

The $m - f_n$ curves at different peak currents are shown in Fig. 7, where f_n decreases as m increases, and the smaller the peak current, the greater the switching frequency. In practice, the maximum peak current can be determined based on the specifications of the switches.

After selecting maximum peak current i_{Lr1_peak} , the m - f_{n_min} curve can be computed from the time domain model. In order to deposit the curve into the controller, curve fitting is required to reduce the amount of data. Polynomial fitting is performed using the curve_fit method of Scipy [26], which

$$\begin{aligned} -\mathbf{x}(0) &= \mathbf{x}(0.5T_s) = \mathbf{A}(0.5T_s - D_0T_s)(\mathbf{x}(D_0T_s) + \mathbf{S}_P) - \mathbf{S}_P \\ &= \mathbf{A}(0.5T_s - D_0T_s)(\mathbf{A}(D_0T_s)(\mathbf{x}(0) + \mathbf{S}_N) - \mathbf{S}_N + \mathbf{S}_P) - \mathbf{S}_P \end{aligned} \quad (18)$$

$$\mathbf{x}(0) = -(\mathbf{I} + \mathbf{A}(0.5T_s - D_0T_s)\mathbf{A}(D_0T_s))^{-1}(\mathbf{A}(0.5T_s - D_0T_s)(\mathbf{A}(D_0T_s)\mathbf{S}_N - \mathbf{S}_N + \mathbf{S}_P) - \mathbf{S}_P). \quad (21)$$

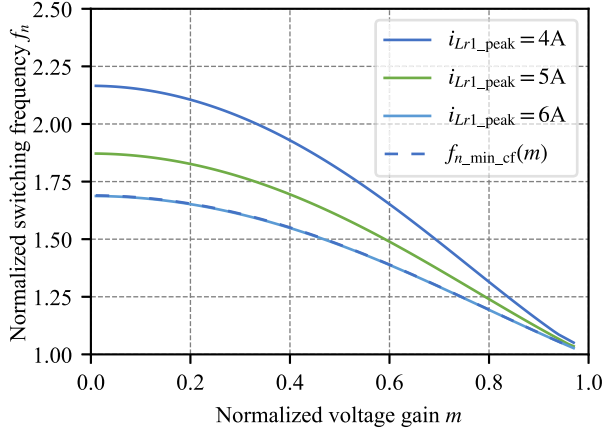


Fig. 7. Normalized switching frequency f_n varying with normalized voltage gain m at different peak resonant currents.

TABLE IV
PARAMETERS OF THE CLLC PROTOTYPE

Parameter	Values
Voltages	$V_1 = 400\text{V}$
	$V_2 = 250 - 400\text{V}$
Currents	$i_{Lr1_peak} \leq 6\text{A}$
	$I_1 = 0 - 2.5\text{A}, I_2 = 0 - 4\text{A}$
Resonant tank	$n = 1, L_m = 500\mu\text{H}$
	$L_{r1} = L_{r2} = 100\mu\text{H}, C_{r1} = C_{r2} = 44\text{nF}$
	$f_r = 75.9\text{kHz}$
Output capacitors	3D1U356KLMB0420450250EVT(35 μF , STE) NFC500V100M18*45 (100 μF , SAMYOUNG)

is based on a least squares method. The curve fitting result corresponding to the parameters in Table IV are obtained as follows:

$$f_{n_min_cf}(m) = 1.69 - 0.01m - 0.82m^2 - 0.2m^3 + 0.34m^4. \quad (23)$$

C. Initial Switching Pattern

As shown in Fig. 8, there are voltage and current overshoots at the startup moment, and these overshoots will significantly increase the current stress on the switches and the voltage stress on the resonant capacitors.

The waveforms of each switching cycle in the quasisteady-state phase should be approximately equal to the steady-state waveforms with the same switching frequency and voltage gain, so the waveforms of the first switching cycle in the quasisteady-state phase should be the same as the steady-state waveforms at $m = 0$, and their initial values should be the same as well. However, all state variables in the idle phase are 0, which differs from the initial values of the steady-state waveforms, resulting in an unsmooth switching process and overshoots. The role of the initial phase is to change the initial values of the quasisteady-state phase to match the steady-state waveform.

The waveforms in the initial phase are shown in Fig. 9. When $t = t_a + t_b + t_c$, the converter switch from the initial phase to

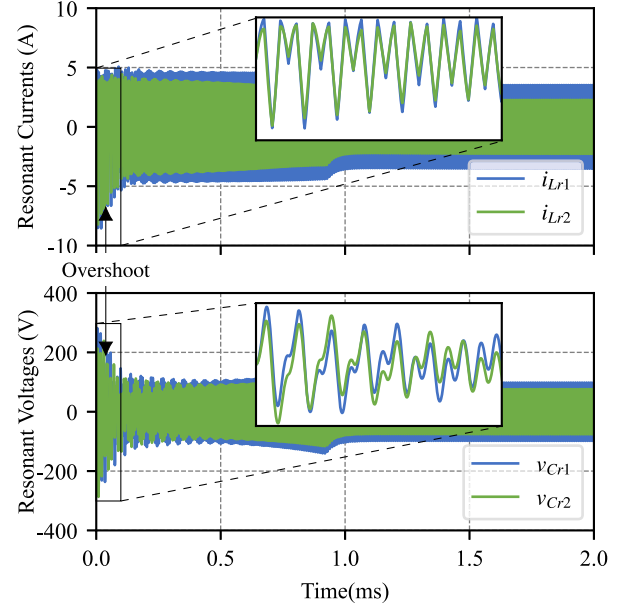


Fig. 8. Startup waveforms without initial phase.

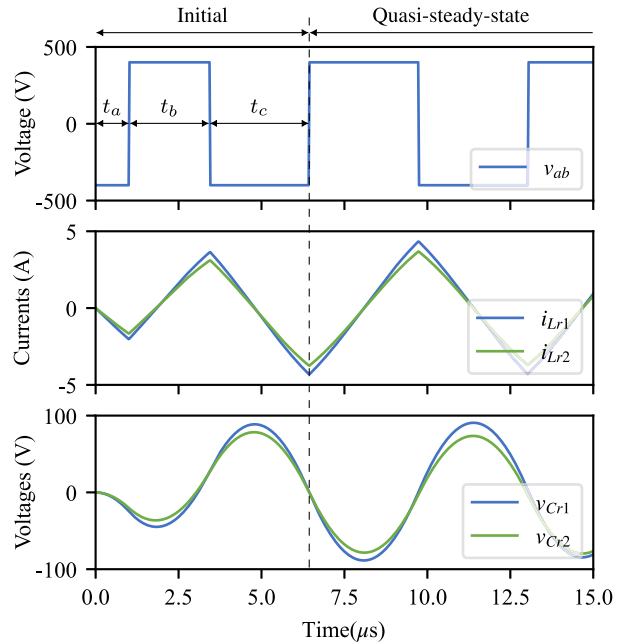


Fig. 9. Waveforms of initial phase.

the quasisteady-state phase. And t_a , t_b , and t_c are the three independent variables to control the waveforms of v_{ab} . Since $V_2 = 0$ at the beginning, based on (17), the state variables in the initial phase can be calculated as follows:

$$\mathbf{x}(t_a) = \mathbf{A}(t_a) \begin{bmatrix} 0 \\ 0 \\ -V_1 \\ 0 \end{bmatrix} - \begin{bmatrix} 0 \\ 0 \\ -V_1 \\ 0 \end{bmatrix} \quad (24)$$

TABLE V
CRITICAL COMPONENTS OF THE PROTOTYPE

Category	Manufacturer	Part
Controller	Altera	EP4CE10F17C8N
Switches	ROHM	SCT3060AL
Gate drivers	Infineon	1EDI60N12AF
Digital isolators	Chipanalog	CA-IS3740HW
Operational amplifiers	Texas Instruments	AMC1311DWVR
Analog-to-digital converters	Analog Devices, Inc.	AD7276AUJZ

$$\mathbf{x}(t_a + t_b) = \mathbf{A}(t_b) \left(\mathbf{x}(t_a) + \begin{bmatrix} 0 \\ 0 \\ V_1 \\ 0 \end{bmatrix} \right) - \begin{bmatrix} 0 \\ 0 \\ V_1 \\ 0 \end{bmatrix} \quad (25)$$

$$\mathbf{x}(t_a + t_b + t_c) = \mathbf{A}(t_c) \left(\mathbf{x}(t_b) + \begin{bmatrix} 0 \\ 0 \\ -V_1 \\ 0 \end{bmatrix} \right) - \begin{bmatrix} 0 \\ 0 \\ -V_1 \\ 0 \end{bmatrix}. \quad (26)$$

Since there are transcendental functions in the $\mathbf{A}(t)$, it is not possible to compute t_a , t_b , and t_c directly from $\mathbf{x}(t_a + t_b + t_c)$. Instead, the particle swarm optimization algorithm is required and the optimization objective is to minimize $\|\mathbf{x}(t_a + t_b + t_c) - \mathbf{x}_d\|$, where \mathbf{x}_d is the desired initial values. Since $V_2 = 0$ at the initial moment, hence $\mathbf{S}_P = \mathbf{S}_N$. From (21) gives

$$\mathbf{x}_d = \left(\mathbf{I} + \mathbf{A}\left(\frac{T_{s0}}{2}\right) \right)^{-1} \left(\begin{bmatrix} 0 \\ 0 \\ V_1 \\ 0 \end{bmatrix} - \mathbf{A}\left(\frac{T_{s0}}{2}\right) \begin{bmatrix} 0 \\ 0 \\ V_1 \\ 0 \end{bmatrix} \right) \quad (27)$$

where

$$T_{s0} = 1 / (f_{n_min_cf}(0)f_r). \quad (28)$$

Since the objective function is analytic, the computational process of the optimization algorithm will be very fast. With Intel Core i5-1240P CPU and single-threaded condition, 20 iterations can be completed in less than 10 s with 50 000 particles. Thus, the local minima problem can be mitigated by increasing the number of particles and the number of repeated computations.

The calculation process is independent of the output capacitance C_2 and load conditions, so the time parameters t_a , t_b , and t_c can be precomputed once the resonant tank parameters of the CLLC converter are determined. These values are then stored in the controller's memory for real-time implementation.

IV. EXPERIMENTS

A. Experiment Setup

A CLLC converter prototype with parameters in Table IV was built to verify the proposed control method, as shown in Fig. 10. The critical components of the prototype are listed in Table V, and a self-made board based on the Intel Cyclone IV EP4CE10 field programmable gate array is used as the controller.

The output capacitance comprises a metallized polypropylene film capacitor and multiple aluminum electrolytic capacitors.

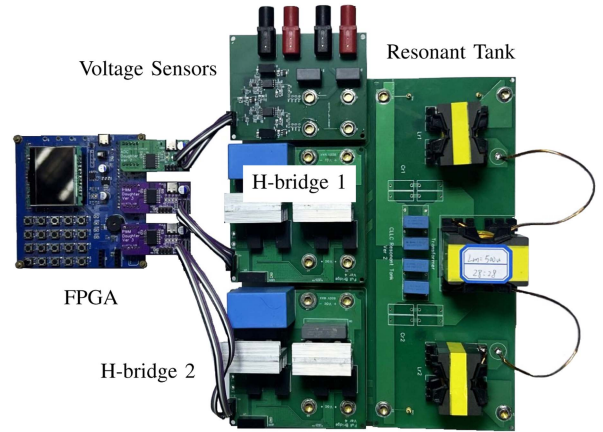


Fig. 10. CLLC prototype.

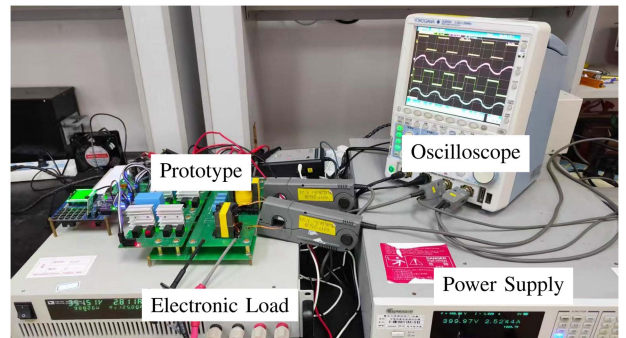


Fig. 11. Experimental test platform.

These electrolytic capacitors are mounted on a separate printed circuit board and connected in parallel with the output port V_2 to test the proposed soft start method with different output capacitance.

The corresponding experimental test platform is shown in Fig. 11, where the CLLC prototype operates at $p = 1$ kW and the four channels of the oscilloscope measure the bridge arm voltages and resonant currents, respectively.

The peak resonant current i_{Lr1_peak} is set to 6 A when calculating the m - f_{n_min} curve and initial switching pattern. The result of the m - f_{n_min} curve is saved as (23), with the timing parameters in the initial switching pattern optimized as $t_a = 1.31\mu\text{s}$, $t_b = 3.02\mu\text{s}$, and $t_c = 3.46\mu\text{s}$.

The program control flowchart is shown in Fig. 12, where the closed loop mode flag is false after initialization, and the flag is set to true after the initial pulse is issued to enter close-loop control. The value of f_{n_min} is updated in each interrupt according to m and (23).

B. Waveform Results

The waveforms at the startup moment are shown in Fig. 13, where the v_{cd} waveform approximates a straight line since the output voltage is very small at the beginning. The comparison of Fig. 13(a) and (b) shows that the converter enters the quasisteady-state phase quickly and smoothly with the initial

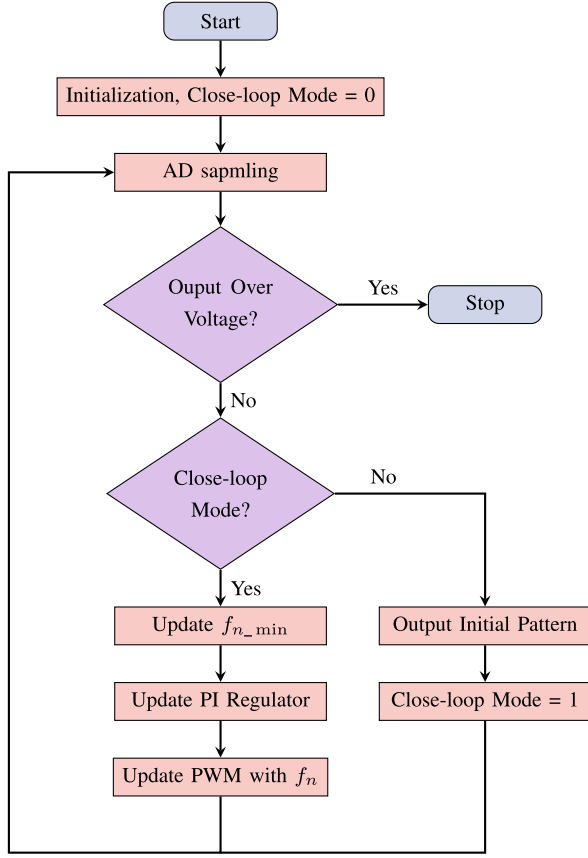


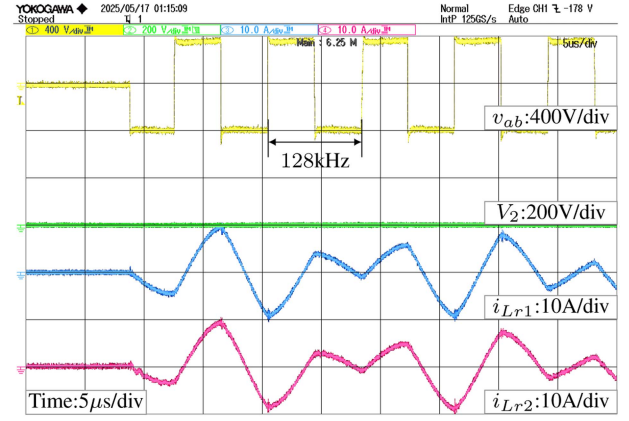
Fig. 12. Program control flowchart.

 TABLE VI
 SWITCHING FREQUENCIES AT DIFFERENT OPERATING CONDITIONS

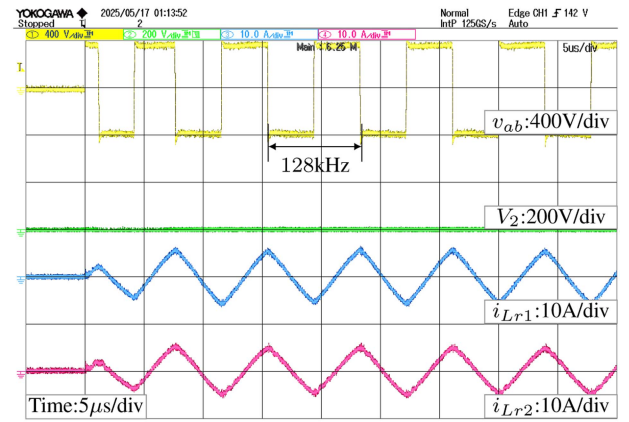
Load R_L	Reference output voltage V_{2_ref}	Output voltage V_2	Power	Switching frequency f_s
300 Ω	280 V	280 V	261 W	156.5 kHz
300 Ω	320 V	320 V	341 W	119.4 kHz
300 Ω	360 V	360 V	432 W	93 kHz
200 Ω	320 V	320 V	512 W	105.1 kHz
100 Ω	320 V	320 V	1024 W	91.5 kHz
0	320 V	0	0	128 kHz

phase, and there is no current overshoot. Since the output voltage is zero and essentially unchanged for several switching cycles, the switching frequency at the startup moment is around 128 kHz according to (23). All switching operations throughout the startup are ZVS except for the first one due to the absence of current at the beginning.

Figs. 14 to 16 are the startup waveforms with the proposed method under different load conditions, since the m - f_{n_min} curve and initial pattern are only related to the circuit parameters in resonant tank and the peak resonant current, the proposed soft start method can be considered load-independent and there is no need to regenerate the m - f_{n_min} curve or initial switching pattern when the test conditions change.



(a)



(b)

Fig. 13. Experimental waveforms with the proposed soft start method at the startup moment. (a) Without initial phase. (b) With initial phase.

The tested switching frequencies of Figs. 14 to 16 after entering steady-state are shown in Table VI, which excludes C_2 because it has no effect on the steady-state performance.

Fig. 14 illustrates the startup waveforms with different reference output voltage V_{2_ref} , and the rising slope of V_2 remains consistent, while the startup time increases with V_{2_ref} .

Fig. 15 illustrates the startup waveforms at different C_2 , and the rising slope of the V_2 decreases with increasing C_2 .

Fig. 16 illustrates the startup waveforms at different load resistance R_L , the rising slope of V_2 continues to drop during the startup process since the current flowing through R_L increases with V_2 , resulting in less current flowing through C_2 . And Fig. 16(c) shows that the proposed method keeps the peak resonant current stay fixed when the output is short-circuited.

Fig. 17 presents the comparison of measured and simulation results of soft start process when $V_1 = 400$ V, $V_{2_ref} = 320$ V, $C_2 = 35$ μ F, and $R_L = 300$ Ω , and the experimental results are generally consistent with the simulation.

During mass fabrication, there are deviations in the circuit parameters (L_{r1} , L_{r2} , L_m , C_{r1} , and C_{r2}) which in turn cause the operation waveforms to deviate from the offline-calculated results and ultimately leads to increased startup time or peak resonant currents.

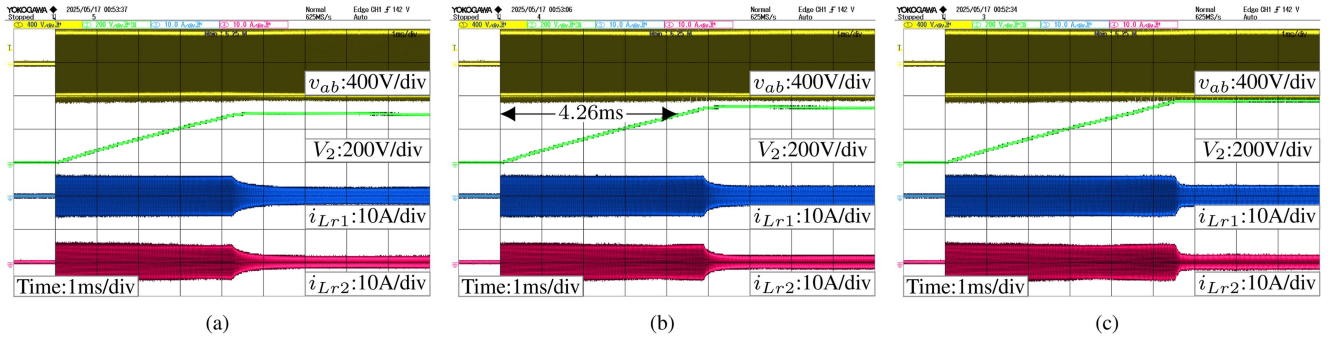


Fig. 14. Experimental waveforms with the proposed soft start method at different V_{2_ref} when $C_2 = 35 \mu\text{F}$ and $R_L = 300 \Omega$. (a) $V_{2_ref} = 280 \text{ V}$, $m = 0.7$. (b) $V_{2_ref} = 320 \text{ V}$, $m = 0.8$. (c) $V_{2_ref} = 360 \text{ V}$, $m = 0.9$.

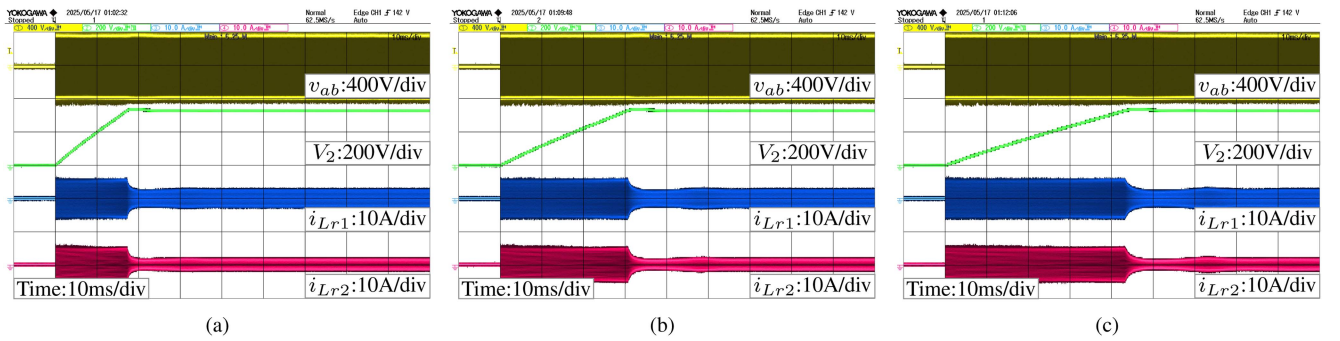


Fig. 15. Experimental waveforms with the proposed soft start method at different C_2 when $R_L = 300 \Omega$ and $V_{2_ref} = 320 \text{ V}$. (a) $C_2 = 135 \mu\text{F}$. (b) $C_2 = 235 \mu\text{F}$. (c) $C_2 = 335 \mu\text{F}$.

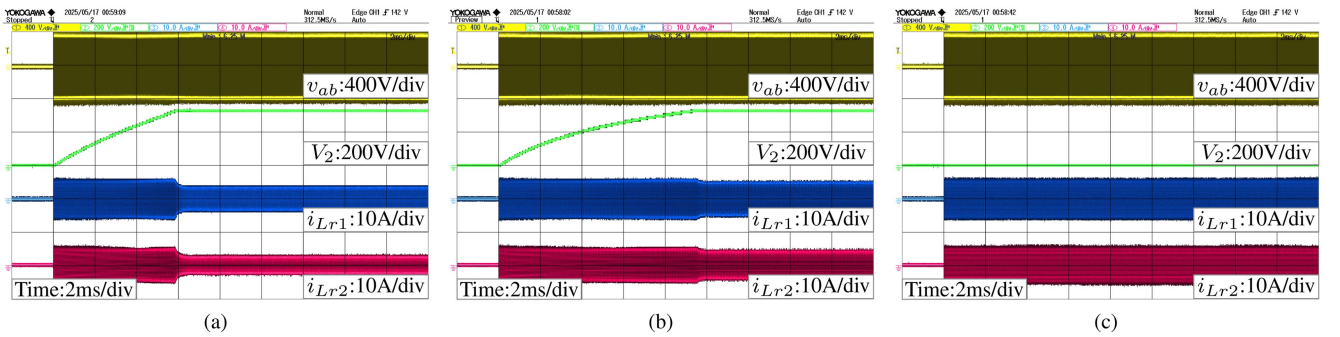


Fig. 16. Experimental waveforms with the proposed soft start method at different R_L when $C_2 = 35 \mu\text{F}$ and $V_{2_ref} = 320 \text{ V}$. (a) $R_L = 200 \Omega$. (b) $R_L = 100 \Omega$. (c) $R_L = 0$.

Taking the maximum deviation as 5%, the startup is slowest when the circuit parameters (L_{r1} , L_{r2} , L_m , C_{r1} , and C_{r2}) reach (95%, 105%, 105%, 95%, and 105%) of their design values, respectively. As shown in Fig. 18(a), the slowest startup time is 4.88 ms, which is a 15.4% increase over the startup time of 4.26 ms in Fig. 14(b) without parameter deviations.

In contrast, the peak resonant current is maximum when the circuit parameters (L_{r1} , L_{r2} , L_m , C_{r1} , and C_{r2}) reach (105%, 95%, 95%, 105%, and 95%) of their design values, respectively. As shown in Fig. 18(b), the startup time is 3.74 ms, which is 11.6% less than the startup time without parameter deviations.

However, the peak resonant current increased by 9.1%, from 6 to 6.55 A.

Due to the measurement range limitation of the output current probe, the input voltage V_1 is reduced to one-tenth of its nominal value during the following short-circuit experiments. An H-bridge identical to that in Fig. 10 was connected in parallel with the output port V_2 to emulate short-circuit. With contact resistance accounted for, the total short-circuit resistance measures approximately 0.5Ω . At $V_2 = 320 \text{ V}$ and $p = 1 \text{ kW}$, the equivalent output resistance is calculated as 102.4Ω . Consequently, the short-circuit current in this

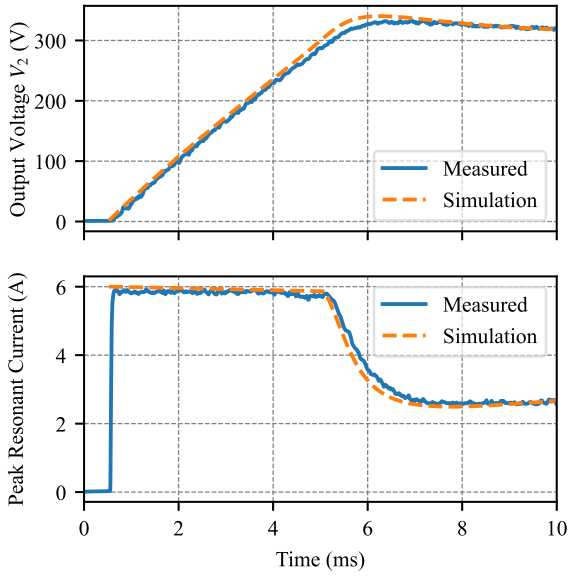
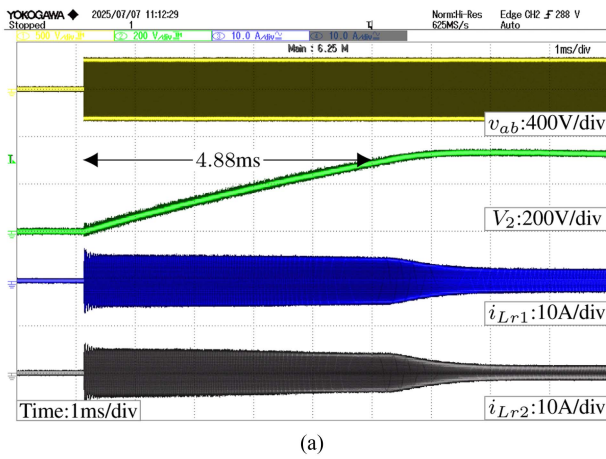
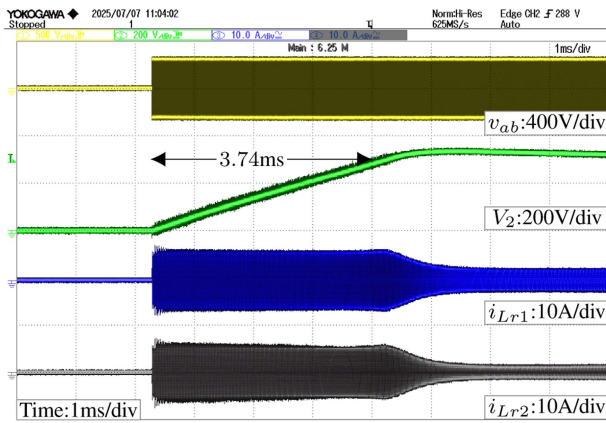


Fig. 17. Comparison of measured and simulation results of soft start process when $V_1 = 400$ V, $V_{2_ref} = 320$ V, $C_2 = 35$ μ F, and $R_L = 300$ Ω .

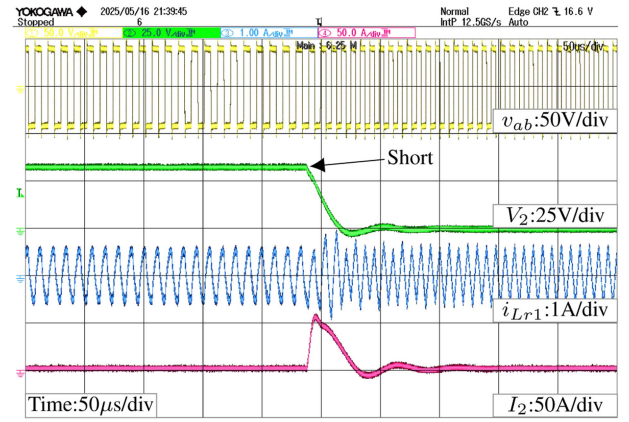


(a)

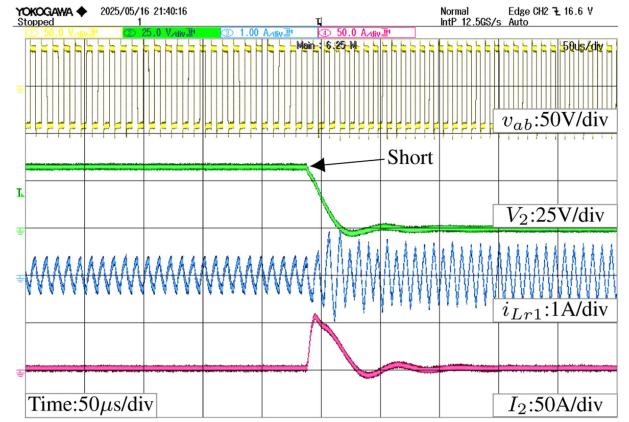


(b)

Fig. 18. Experimental waveforms with the proposed soft start method at worst circuit parameters deviations when $C_2 = 35$ μ F, $V_{2_ref} = 320$ V, and $R_L = 300$ Ω . (a) Worst startup time. (b) Worst peak resonant current.



(a)



(b)

Fig. 19. Short-circuit experimental waveforms with the proposed method during steady-state operation at $m = 0.8$. (a) $R_L = 100$ Ω . (b) $R_L = 200$ Ω .

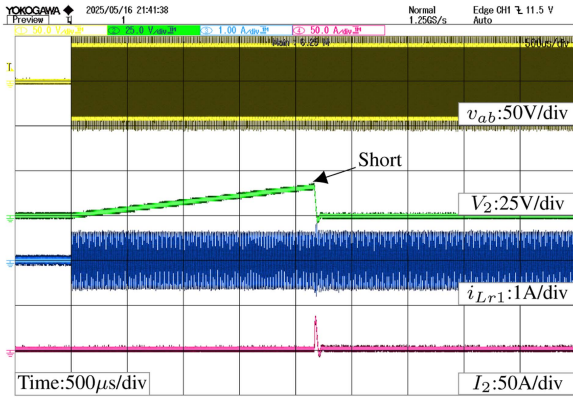
experiment reaches around 200 times the full-load output current.

Fig. 19 illustrates the short-circuit waveforms of the proposed method during steady-state operation. It can be observed that the peak resonant current is effectively confined within the predefined range after the short-circuit event, while an instantaneous overshoot (approximately 1.5 times the limit) occurs at the fault inception. This overshoot primarily stems from the digital sampling delay in the control loop, which diminishes within several switching cycles. Notably, the pulsed current rating of the switching devices typically exceeds twice their continuous current handling capability [27], [28]. Therefore, this transient overshoot imposes no adverse effects on the power switches.

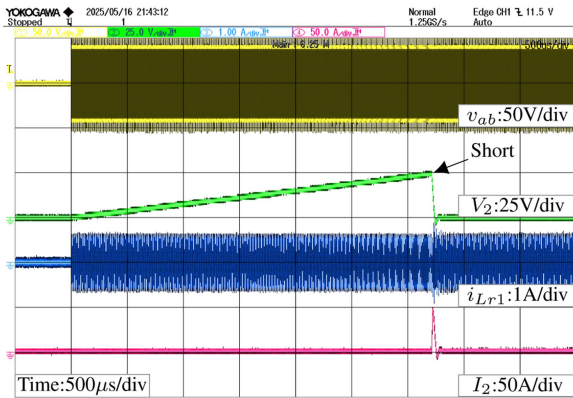
The waveforms of the short-circuit during the startup process are shown in Fig. 20, where the current peaks remain consistent before and after the short-circuit moment. Fig. 21 then shows that with the proposed method it is possible to seamlessly enter the soft start process after recovery from a short-circuit fault.

C. Comparison With Previous Soft Start Techniques

To validate the novelty of the proposed method, comparative experiments were conducted with the fixed frequency fixed



(a)



(b)

Fig. 20. Short-circuit experimental waveforms with the proposed soft start method during startup. (a) Short at $m = 0.4$. (b) Short at $m = 0.6$.

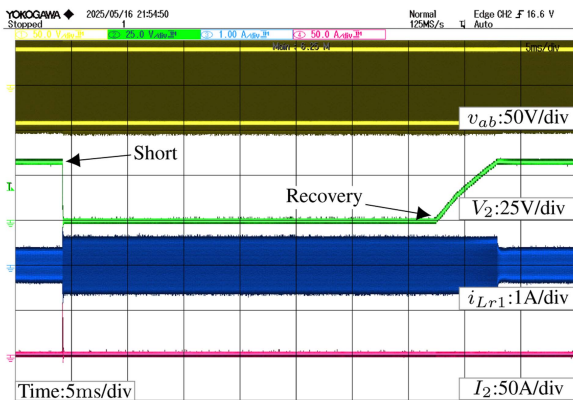
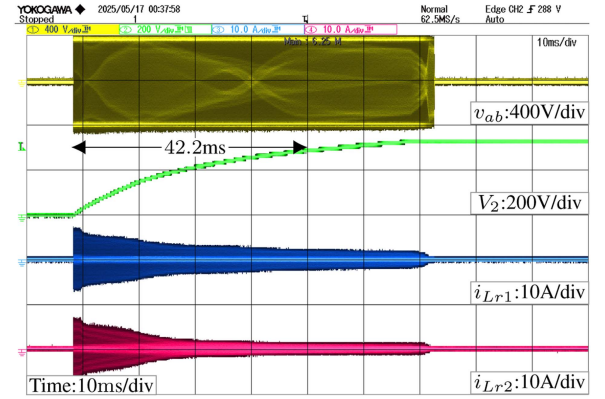


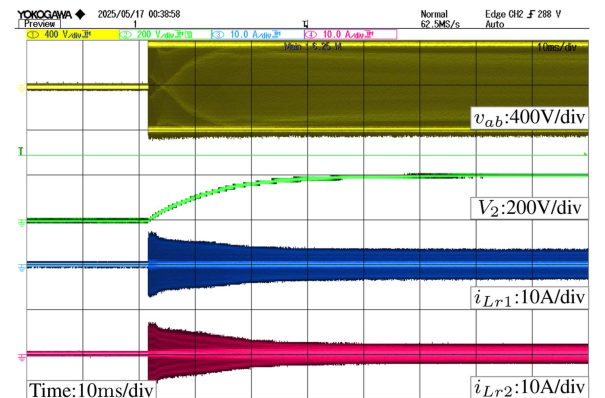
Fig. 21. Short-circuit and restart experimental waveforms with the proposed method during steady-state operation.

duty cycle method from [15] and the fixed frequency adaptive duty cycle method from [20], which are selected from Table I. These selection criteria are based on two key factors: 1) they are the latest advancements in this research domain, and 2) their implementations require the same sampling signals as the proposed approach.

For quantitative comparison of startup performance, the startup time is defined as the duration required for the output



(a)



(b)

Fig. 22. Experimental waveforms with the fixed frequency fixed duty cycle soft start method when $C_2 = 135 \mu\text{F}$ and $V_{2_ref} = 320 \text{ V}$. (a) $R_L = 0 \Omega$. (b) $R_L = 300 \Omega$.

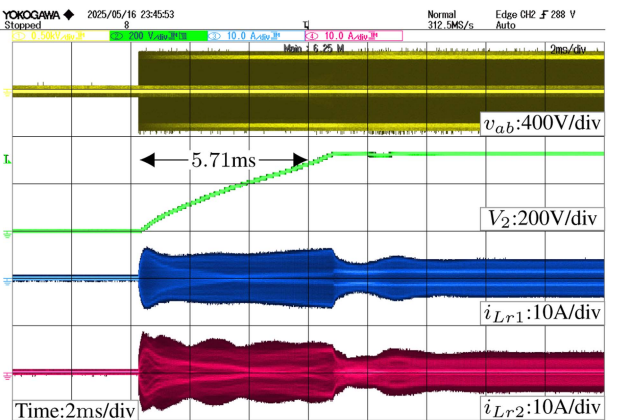


Fig. 23. Experimental waveforms with the fixed frequency adaptive duty cycle soft start method when $R_L = 300 \Omega$, $C_2 = 35 \mu\text{F}$, and $V_{2_ref} = 320 \text{ V}$.

voltage to reach 90% of its set value. The oscilloscope's trigger is configured to activate when V_2 reaches 288 V (90% of 320 V). This setup allows accurate measurement of the startup time, as shown in Figs. 22(a) and 23. To ensure fairness in testing the startup speed, the maximum resonant current limit for both methods is maintained consistent with the proposed method at 6 A.

TABLE VII
COMPARISON OF STARTUP TIME AT $V_{2_ref} = 320V$

Load R_L	Output C_2	Fixed frequency Fixed duty cycle	Fixed frequency Adaptive duty cycle	Proposed
∞	35 μF	13.2 ms	4.84 ms	3.75 ms
300 Ω	35 μF	N/A	5.71 ms	4.26 ms
200 Ω	35 μF	N/A	6.85 ms	5.06 ms
100 Ω	35 μF	N/A	12.2 ms	8.24 ms
∞	135 μF	42.2 ms	17.6 ms	14.1 ms
300 Ω	135 μF	N/A	18.8 ms	15 ms
200 Ω	135 μF	N/A	23.8 ms	17.3 ms
100 Ω	135 μF	N/A	32.7 ms	26.2 ms

The startup time measurements under various operating conditions are summarized in Table VII. Compared to fixed frequency adaptive duty cycle method (without short-circuit tolerance), the proposed approach achieves a 20%–26% reduction in startup time. More significantly, when benchmarked against fixed frequency fixed duty cycle method (with inherent short-circuit tolerance), the startup time is reduced by 66%–72%.

The slow startup speed of fixed frequency fixed duty cycle method primarily stems from its insufficient output current capability, which is sacrificed for the inherent short-circuit tolerance [15]. In scenarios where additional loads are connected to the output port, the load current increases as the output voltage rises during the startup process. This current-demand surge creates an operational deadlock—where the converter cannot simultaneously satisfy both the output capacitor charging requirement and the load current demand—as visually evidenced by the stalled startup waveform in Fig. 22(b).

In summary, the proposed method demonstrates two advantages over existing solutions:

- 1) Startup acceleration: Achieves a 20%–72% reduction in startup time compared to state-of-the-art methods with the same hardware configuration and maximum resonant current.
- 2) Comprehensive fault protection: Provides continuous short-circuit protection spanning both the startup and steady-state operation.

V. CONCLUSION

In this article, an improved OMA model for CLLC converters is introduced, which reduces the number of unknown variables in the solving process to a single variable. And based on the improved OMA model, a peak-current-limit soft start method with short-circuit tolerance for CLLC converters is proposed. With the aid of offline-calculated initial switching pattern and the m - f_{n_min} curve, the proposed method can keep the peak resonant current fixed to maximize the startup speed and provide continuous short-circuit protection spanning both the startup phase and steady-state operation without additional sensors. Finally, the comparative experiments conducted on the 1-kW prototype demonstrate that the proposed method exhibits a faster startup speed and more comprehensive short-circuit protection capabilities.

REFERENCES

- [1] C. Zhang, P. Li, Z. Kan, X. Chai, and X. Guo, "Integrated half-bridge CLLC bidirectional converter for energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3879–3889, May 2018.
- [2] T. Luo et al., "An optimal VF-TPS modulation scheme for clc converter with minimized RMS current," *IEEE Trans. Power Electron.*, vol. 40, no. 3, pp. 4170–4185, Mar. 2025.
- [3] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC-DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.
- [4] H. Li et al., "Bidirectional control with fitting model-based synchronous rectification and input ripple current feedforward for SiC bidirectional CLLC EV charger," *IEEE Trans. Ind. Electron.*, vol. 70, no. 9, pp. 9136–9146, Sep. 2023.
- [5] L. Zhao, Y. Pei, L. Wang, L. Pei, W. Cao, and Y. Gan, "Design methodology of bidirectional resonant CLLC charger for wide voltage range based on parameter equivalent and time domain model," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12041–12064, Oct. 2022.
- [6] R. Yu, G. K. Y. Ho, B. M. H. Pong, B. W.-K. Ling, and J. Lam, "Computer-aided design and optimization of high-efficiency LLC series resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3243–3256, Jul. 2012.
- [7] Y. Xuan, X. Yang, W. Chen, T. Liu, and X. Hao, "A novel three-level CLLC resonant DC-DC converter for bidirectional ev charger in DC microgrids," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 2334–2344, Mar. 2021.
- [8] T. Luo et al., "A full-iteration optimal design methodology of CLLC converter with minimized RMS current," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 11916–11930, Oct. 2024.
- [9] Y. Xu, X. Ge, R. Guo, and W. Shen, "Online soft short-circuit diagnosis of electric vehicle li-ion batteries based on constant voltage charging current," *IEEE Trans. Transport. Electrification*, vol. 9, no. 2, pp. 2618–2627, Jun. 2023.
- [10] K. Zia, W.-J. Lee, A. Papanani, and P.-E. Su, "Li-ion battery resistance study due to an external short circuit using a zero bouncing circuit and its comparison to cyclic ageing," *IEEE Trans. Ind. Appl.*, vol. 60, no. 2, pp. 2453–2461, Mar./Apr. 2024.
- [11] M. S. Karimzadeh, H. Goudarzhagh, M. S. Mahdavi, and G. B. Gharehpetian, "A novel open-circuit fault detection and localization method for the CLLC converter," *IEEE Trans. Power Electron.*, vol. 40, no. 7, pp. 9898–9907, Jul. 2025.
- [12] L. Costa, G. Buticchi, and M. Liserre, "A fault-tolerant series-resonant DC-DC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 900–905, Feb. 2017.
- [13] M. Yaghoubi, J. S. Moghani, N. Noroozi, and M. R. Zolghadri, "IGBT open-circuit fault diagnosis in a quasi-z-source inverter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2847–2856, Apr. 2019.
- [14] X. Xie, J. Zhang, C. Zhao, Z. Zhao, and Z. Qian, "Analysis and optimization of LLC resonant converter with a novel over-current protection circuit," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 435–443, Mar. 2007.
- [15] H. Chen, K. Zhang, L. Wang, K. Sun, and Y. Li, "A soft startup method with natural short-circuit tolerance features for CLLC converters," *IEEE Trans. Power Electron.*, vol. 40, no. 3, pp. 4008–4019, Mar. 2025.
- [16] F. Duan, M. Xu, X. Yang, and Y. Yao, "Canonical model and design methodology for LLC DC/DC converter with constant current operation capability under shorted load," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6870–6883, Oct. 2016.
- [17] W. Wang, Y. Liu, P. Zhang, Y. Yuan, J. Zhao, and P. C. Loh, "A fault-tolerant LLC converter with high reliability and low cost for two-stage converters," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9647–9659, Aug. 2023.
- [18] W. Feng and F. C. Lee, "Optimal trajectory control of LLC resonant converters for soft start-up," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1461–1468, Mar. 2014.
- [19] C. Fei, F. C. Lee, and Q. Li, "Digital implementation of soft start-up and short-circuit protection for high-frequency LLC converters with optimal trajectory control (OTC)," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 8008–8017, Oct. 2017.
- [20] L. Xiong, J. Song, and Y. Gao, "An adaptive current-limit soft start method for asymmetric CLLC resonant converter," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 6, no. 1, pp. 248–258, Jan. 2025.
- [21] Z. Xiao, X. Li, and Y. Tang, "A lightweight artificial neural network start-up controller for CLLC resonant converters," *IEEE Trans. Power Electron.*, vol. 39, no. 11, pp. 14775–14786, Nov. 2024.
- [22] T. Yu, G. Sicheng, and X. Shaojun, "Research on open-loop soft-start strategy of CLLC bi-directional resonant converter," in *Proc. 2018 IEEE Int. Power Electron. Appl. Conf. Expo.*, 2018, pp. 1–6.

- [23] J. Min and M. Ordonez, "Bidirectional resonant CLLC charger for wide battery voltage range: Asymmetric parameters methodology," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6662–6673, Jun. 2021.
- [24] Q. Li, B. Liu, R. Zheng, and S. Duan, "Constant resonant current limiting strategy for LLC converter without current sensing," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6756–6764, Sep. 2016.
- [25] A. Nabih, M. H. Ahmed, Q. Li, and F. C. Lee, "Transient control and soft start-up for 1-MHZ LLC converter with wide input voltage range using simplified optimal trajectory control," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 24–37, Feb. 2021.
- [26] O. Campesato, *Chapter 4: Work. with Sklearn and Scipy*, Berlin: Walter de Gruyter GmbH, 2022, pp. 133–160.
- [27] ROHM Semiconductor, N-channel SiC power MOSFET, SCT3060AL, rev.006, 2022. [Online] Available: <https://fscdn.rohm.com/en/products/databook/datasheet/discrete/sic/mosfet/sct3060al-e.pdf>
- [28] Wolfspeed, 1200V 40mohm Silicon Carbide Power MOSFET N-Channel Enhancement Mode, C3M0040120K, rev.03, 2024. [Online] Available: https://assets.wolfspeed.com/uploads/2023/08/Wolfspeed_C3M0040120K_data_sheet.pdf



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