A High-Speed Soft Startup Method With Full-Load Startup Capability for CLLC Converters

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***Abstract*—The *CLLC* converter is a high-frequency, high-efficiency isolated bidirectional dc/dc converter. For application scenarios like data center and battery energy storage (BES) systems, a high-speed soft startup with load is important for improving system dynamic response ability. In this article, an optimized variable duty cycle soft startup method with full-load startup capability is proposed for *CLLC* converters. Specifically, an optimal duty cycle variation law is derived accurately to maintain the maximum resonant current in the whole startup process. First, a special operation condition with energy limitation features is introduced ahead, where the core idea of the proposed method is emphasized. After that, the operation mode analysis method is used to analyze the detail working principle for different duty cycle, and the relationship among resonant current, duty cycle, and output voltage is illustrated. Second, detail application framework of proposed method is given, and corresponding duty cycle optimization process is introduced carefully. Moreover, an accurate mathematical model of the load starting capability of the proposed method is established, which proves that the proposed method can realize a full-load startup. Finally, a 900-W lab-level *CLLC* prototype is built for experiment verification: the accuracy of the theoretical mode analysis is verified first, then a high-speed no-load startup is realized in 9 ms for the proposed method, which is nearly nine times faster than the conventional varying frequency method, and a full-load startup is also achieved successfully in 14 ms.**

***Index Terms*— *CLLC* resonant converter, dc-dc power converters, mode analysis, soft startup.**

NOMENCLATURE

Definition of Important Variables

Variable	*Physical meaning*
f_r	Resonant frequency.
f_s	Switching frequency.
D	Duty cycle.
i_o	Equivalent output current.
i_{load}	Equivalent load current.
T	Period of a cycle.
k	Inductance ratio.
k_1	Scale factor of the eigen frequency in the P and N mode stages to f_r.
k_2	Scale factor of the eigen frequency in the Z mode stages to f_r.
P_1 to P_4	Undetermined coefficients of time domain expressions in the P mode.
N_1 to N_4	Undetermined coefficients of time domain expressions in the N mode.
Z_1 to Z_2	Undetermined coefficients of time domain expressions in the Z mode.
ϕ_P	Duration of the P mode stage.
ϕ_N	Duration of the N mode stage.
ϕ_Z	Duration of the Z mode stage.
M	Voltage gain.

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I. INTRODUCTION

THE*CLLC* converter is a high-frequency and high-efficiency isolated bidirectional dc/dc converter that has gained significant attention from academia and industry due to its excellent soft-switching characteristics [1]. Having a promising topology for bidirectional power transmission, the *CLLC* converter's application spans uninterrupted power supply systems, vehicle-to-grid systems, battery energy storage systems, electric aircraft, and data centers [2], [3], [4], [5], [6], [7]. Since the surge current at the startup moment of the converter will bring great harm to the switching devices and the resonant tank, efficient soft startup method is one of the research focuses of *CLLC* converters.

Surge current limitation is one of the main criterions for soft startup, published researches can be categorized into methods based on switching frequency variation [8], [9], [10], [11] and duty cycle variation [13], [14]. Specifically, Jia et al. [8] pointed out that a higher switching frequency can limit the surge current at the startup moment, while the change law is sometimes experiential and the initial frequency is always several times of the resonant frequency, which has strict requirements on the high-frequency working ability of switches and driving circuits, and will increase the cost. In order to enhance the accuracy of the frequency variation process, state trajectory is introduced to clarify the boundary frequency and detail variation law in

TABLE I
BRIEF COMPARISON OF DIFFERENT SOFT STARTUP METHODS MENTIONED ABOVE

Soft startup method	Application area	Control loop	Control parameters	Current suppression	Startup speed	Loading capability
[8], [9], [10] and [11]	*CLLC* converters	Close-loop	Frequency	▲▲▲	▲▲	/
[14]	*CLLC* converters	Close-loop	Duty cycle	▲▲▲	▲▲	/
[12], [13]	*CLLC* converters	Close-loop	Frequency and duty cycle	▲▲▲	▲	/
[15]	LLC converters	Close-loop	Duty cycle	▲▲▲	▲▲	▲▲▲
[19]	*CLLC* converters	Open-loop	Duty cycle	▲▲▲	▲▲▲	/
[20]	*CLLC* converters	Open-loop	Fixed duty cycle	▲▲▲	▲▲	/
[24], [25]	Buck/Boost converters	Close-loop	Duty cycle	▲▲▲	▲▲	▲▲▲
[26]	DAB converters	Close-loop	Phase shift	▲▲▲	▲▲	▲▲▲
[27]	LLC converters	Close-loop	Frequency	▲▲▲	▲▲	▲▲▲
Proposed method	*CLLC* converters	Close-loop	Duty cycle	▲▲▲	▲▲▲	▲▲▲

Note: The number of "▲" represents the quality of the corresponding performance.

[9], [10], and [11], and a current limitation is used to control the trajectory. To mitigate issues caused by high switching frequency, duty cycle control is engaged. The authors in [12] and [13] proposed a three-stage hybrid control by integrating duty cycle control to substitute the ultimate pursuit of high initial frequency. Furthermore, several pure duty cycle variation startup control methods were given in [14] by using different variation rules to achieve nonlinear rise and linear rise of the output voltage, respectively.

Speed is another key evaluation indicator of soft startup, which is increasingly valued for rapid power restoration in critical applications, such as data centers, EV charging, and emergency power supply [15], [16], [17]. Specifically, the startup speed depends on the resonant current, so that corresponding methods focus on the current control. Chen et al. [15] proposed a variable duty cycle soft startup strategy for *LLC* converters based on current-limiting curve, which may be suitable for *CLLC* converters since they have similar topology. Similarly, Xiong et al. [19] showed an adaptive current-limit soft startup method for asymmetric *CLLC* converters, which is an open-loop method with an offline duty cycle table.

Besides, the abovementioned soft startup methods mainly focus on equivalent voltage gain by using the first harmonic approximation method, which is a macro mathematic approximation and the essence of startup is neglected. Exactly, Chen et al. [20] gave a soft startup method with fixed duty cycle and fixed frequency, which introduces a four-mode operation condition for an energy limitation-based stable startup. Specifically, the mode analysis-based energy limitation feature is figured as the essence of a stable soft startup, which can provide an accurate illustration of the startup process. Although this method can realize a stable startup with a fixed duty cycle control, the energy transmitted per cycle will shrink along with the setup of the output voltage, resulting in a limited startup speed.

However, the conventional soft startup methods mainly concentrate on current limitation and are always used for no-load startup, lacking of research on load starting. Actually, the *CLLC* converter is expected with load starting capability in reality industrial applications, which can simplify the control loop and improve the dynamic response characteristics [21], [22], [23]. Due to the lack of load starting methods of *CLLC* converters, several load starting researches of other familiar converters are listed as follows.

The most original research on load starting is carried out around buck and boost converters. The authors in [24] and [25] proposed a series of load starting methods aiming at the classic working condition of constant power load, which are mainly based on the perspective of energy limitation and current control. Furthermore, Gao et al. [26] proposed a soft startup method for DAB converter working in DCX mode, which enables it to have full-load startup capability. In addition, the loading soft startup of resonant converter has also been gradually studied. The authors in [15] and [27] proposed some soft startup control methods of *LLC* converters to realize the soft startup under different load conditions, which are mainly based on the control of peak resonant current and the energy transmission. Table I shows a brief comparison of different soft startup methods mentioned above.

In this article, an optimized variable duty cycle soft startup method with full-load startup capability for *CLLC* converters is proposed, which is a close-loop strategy based on an optimal variation formula between the output voltage and the duty cycle. Specifically, the core idea of the proposed method is enlarging the resonant current to the boundary up limit with energy limitation features (fully discussed in [20]) along the whole startup process. To clearly analyze the detail working principle, the operation mode analysis method is used for basic time-domain illustration of the special energy limited operation condition during the whole startup process for the *CLLC* converter, especially considering the influence drawn by different duty cycle. Based on the mode analysis, the main improvement of the proposed method compared with the method in [20] and the actual application process of the proposed method is figured out. Furthermore, the detail duty cycle optimization process is introduced step by step. Besides, the loading capability of the proposed method is emphasized since the resonant current is maintained large enough. Meanwhile, the actual load current

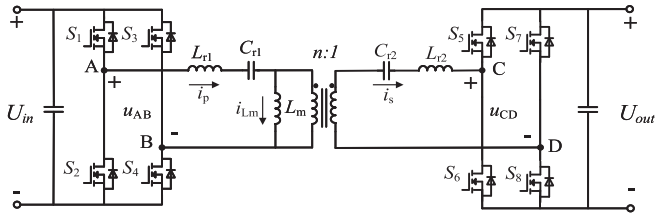

Fig. 1. Topology of a typical *CLLC* converter.

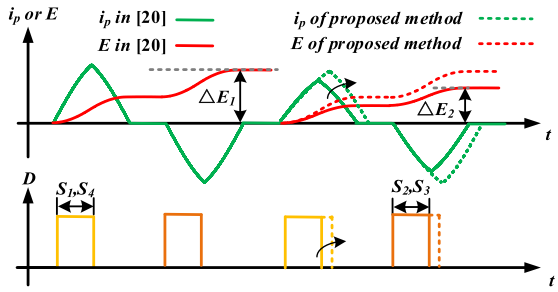

Fig. 2. Illustration of the operation condition with energy limitation features.

for pure resistance load is analyzed accurately and the full-load startup ability of the proposed method is demonstrated. Finally, verification experiments are conducted and experimental results proved a high-speed soft startup and the capability of full-load startup under the proposed method as well as the correctness of corresponding analysis.

The rest of this article is organized as follows: In Section II, the basic soft startup operation condition with energy limitation features is illustrated ahead. Then, a detailed operation mode analysis is provided to clarify the startup process of proposed soft startup control method, especially for the working principle corresponding with different output voltage and duty cycle. In Section III, the core idea of the proposed method is emphasized again and a step-by-step solving pattern of the optimal duty cycle is provided. Furthermore, the loading capability of proposed method is analyzed accurately based on the mode analysis. In Section IV, corresponding experimental validation results are provided to verify the proposed soft startup strategy, the accuracy of the mode analysis and the duty cycle variation is verified, and the startup speed comparison experimental results of different soft startup control methods are given. Moreover, several load starting experiments are given for different load conditions. Finally, Section V concludes this article. The comparison of duty cycle variation rule in different fitting forms is given in Appendix.

II. Basic Soft Startup Operation Condition and Its Mode Analysis for *CLLC* Converters

A. Basic Idea of the Proposed Soft Startup Driving Scheme

Fig. 1 illustrates the topology of a typical *CLLC* converter. S_1 to S_4 are the primary side switches, and S_5 to S_8 are the secondary side switches. The magnetizing current in primary side and secondary side are indicated by i_p, i_s, and i_{Lm}, respectively. The positive directions of voltage and current used in the analysis are also indicated, and the turn ratio of the transformer is denoted as n.

Different from classical varying frequency or varying duty cycle soft startup methods, which are mainly based on the equivalent voltage gain, Chen et al. [20] proposed an energy limitation-based method with a special operation condition, as shown in Fig. 2, where a suitable fixed duty cycle is required to conduct the switching tubes in the primary side with the switching frequency equals to the resonant frequency. Specifically, in every switching period, i_p will rise from zero when S_1 and S_4 are conducting and drop down to zero before the next on state. By this way, the amplitude of i_p is limited instead of increasing cycle by cycle so that the transmitted energy in a cycle is limited, which means ΔE in Fig. 2 is controllable.

However, since the abovementioned principle is conducted for a no-load startup and the duty cycle is fixed during the startup process, the maximum amplitude of i_p in a cycle will decrease along with the startup process, so that the energy transmitted per cycle will shrink ($\Delta E_2 < \Delta E_1$ in Fig. 2), which will limit the startup speed.

To deal with the speed limitations mentioned above, this article attempts to find out an optimal duty cycle variation law to maintain the energy transmitted per cycle limited and maximum, rather than shrinking with the establishment of U_{out}. Specifically, the imaginary improved varying duty cycle driving scheme is presented in Fig. 2 with several dashed lines, the core point is to increase duty cycle as the startup proceeds, keeping the energy transmitted per cycle at the controllable up limit. In this way, the resonant current is controlled as large as possible, so that the startup speed is improved and the loading capability is enlarged.

B. Operation Mode Analysis of the Driving Scheme

To identify the energy transfer law exactly, the time-domain operation mode analysis method is used, which consists of five main steps: 1) distinguish operation modes; 2) establish equivalent circuits; 3) derive time domain expressions; 4) illustrate boundary conditions; and 5) solve for required characteristics [28]. Actually, Chen et al. [20] provided a detailed mode analysis for the operation condition shown in Fig. 2 with a fixed duty cycle, while the proposed method uses a variable duty cycle driving scheme, resulting some different operation modes. The detail mode analysis of the proposed driving scheme is given as follows.

Distinguish Operation Modes: As shown in Fig. 3, the operating process under the proposed soft startup control method comprises three operation mode stages, they are named as the P mode stage, N mode stage, and Z mode stage. Specially, the Z mode stage consists of two types of operation conditions conducted by different directions of i_s. Since the operating processes in the positive and negative half cycles are symmetrical for the *CLLC* converters, the subsequent analysis focuses on the positive half cycle.

Establish Equivalent Circuits: The circuit working process of each mode is shown in Fig. 3, and the equivalent circuits of P mode stage, N mode stage, and Z mode stage employed in the operation mode analysis can be established, as illustrated in

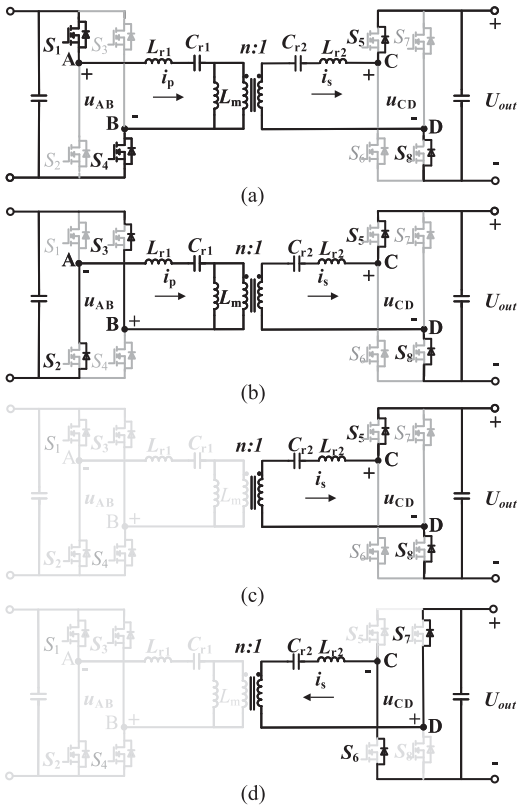

Fig. 3. Detail circuit operation condition of each mode. (a) *P* mode stage. (b) *N* mode stage. (c) *Z* mode stage of positive i_s. (d) *Z* mode stage of negative i_s.

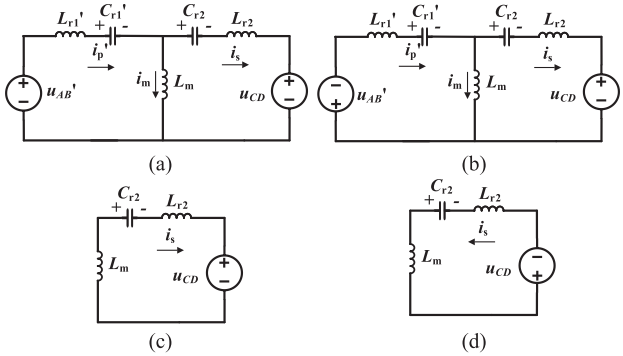

Fig. 4. Detail equivalent circuit of each mode. (a) *P* mode stage. (b) *N* mode stage. (c) *Z* mode stage of positive i_s. (d) *Z* mode stage of negative i_s.

Fig. 4, respectively. Corresponding state variables in the primary side are converted to the secondary side: $u'_{AB} = u_{AB}/n$, $i'_p = n \cdot i_p$, $C'_{r1} = n^2 \cdot C_{r1}$, and $L'_{r1} = L_{r1}/n^2$

In the *P* mode stage, the entire resonant tank participates in resonance, where $u_{AB} = U_{\text{in}}$and $u_{CD} = U_{\text{out}}$. In the *N* mode stage, the whole resonant tank participates in resonance, where $u_{AB} = -U_{\text{in}}$and $u_{CD} = U_{\text{out}}$. In the *Z* mode stage, only the secondary side of the resonant tank participates in resonance, where $u_{AB} = 0$ and $u_{CD} = U_{\text{out}}$for a positive i_s and $u_{CD} = -U_{\text{out}}$for a negative i_s.

Derive Time Domain Expressions: According to Fig. 4, equivalent circuits of *P* mode stage and *N* mode stage are both four-order resonance circuits, and equivalent circuit of *Z* mode stage is two-order resonance circuits. Therefore, time domain expressions of i_p, i_s, u_{cr1}, and u_{cr2} in *P* mode stage, *N* mode stage, and *Z* mode stage can be derived by solving the corresponding resonance circuits.

For simplicity, per-unit form time domain expressions are employed. The base values for the voltage, current, and impedance are defined as

$$Z_{\text{base}} = \sqrt{\frac{L_r}{C_r}}, u_{\text{base}} = U'_{\text{in}} = U_{\text{in}}/n, i_{\text{base}} = \frac{u_{\text{base}}}{z_{\text{base}}} \quad (1)$$

where $L_r = L_{r1} = L_{r2}$, $C_r = C_{r1} = C_{r2}$.

Then, the per-unit form time domain expressions of i_p, i_s, u_{cr1}, and u_{cr2} in the *P* mode stage, *N* mode stage, and *Z* mode stage can be expressed in Table II. Specifically, since the equivalent circuit of *Z* mode stage depends on the direction of i_s, corresponding time-domain state equations are distinguished by using different subscripts in the undetermined variables.

Specially, there exists a boundary condition for different working patterns in *Z* mode stage, which is $i_s = 0$, as shown in Fig. 5(a). Detailedly, four operation modes are required for a small duty cycle since $i_s > 0$ at the end of *N* mode stage [shown in Fig. 5(a)], while only three operation modes are required for a higher duty cycle if $i_s \leq 0$ at the end of *N* mode stage [shown in Fig. 5(b) and (c) without Z mode stage of positive i_s].

The abovementioned boundary criterion and boundary duty cycle is given in (2). When $0 < D < D_b$, four modes analysis should be used, otherwise three modes analysis is more appropriate. Furthermore, since the four modes analysis is presented comprehensively in [20], the following mode analysis focuses on the three modes operation condition:

$$\begin{cases} i_{s,N}(\phi_N) = 0 \\ D_b = 0.2 \end{cases} \quad (2)$$

where ϕ_N is the length of the *N* mode stage, and D_b is the boundary duty cycle.

Illustrate Boundary Conditions: Boundary conditions are included to solve undetermined variables so that the steady-state condition of *CLLC* converters can be described completely and accurately. Apart from P_1, P_2, P_3, P_4, N_1, N_2, N_3, N_4, Z_{n1}, and Z_{n2}, another four variables, ϕ_P, ϕ_N, and ϕ_Z are defined in Fig. 5. They are the durations of the *P* mode stage, *N* mode stage, and *Z* mode stage, respectively.

For the time domain continuity of the primary side current i_p, the secondary side current i_s, the voltage across the primary resonant capacitor u_{cr1}, and the voltage across the secondary side resonant capacitor u_{cr2}, the following boundary conditions

TABLE II
TIME-DOMAIN EQUATIONS OF i_p, i_s, u_{cr1}, AND u_{cr2} FOR EACH MODE

***P* mode stage**	***N* mode stage**
$\begin{cases} i_{p,P}(\phi) = P_1 cos\phi - P_2 sin\phi + k_1 P_4 \sin(k_1\phi) + P_3 \cos(k_1\phi) \\ i_{s,P}(\phi) = P_1 cos\phi - P_2 sin\phi - k_1 P_4 \sin(k_1\phi) - P_3 \cos(k_1\phi) \\ u_{cr1,P}(\phi) = P_1 sin\phi + P_2 cos\phi - P_4 \cos(k_1\phi) + \frac{P_3}{k_1}\sin(k_1\phi) + 1 \\ u_{cr2,P}(\phi) = P_1 sin\phi + P_2 cos\phi + P_4 \cos(k_1\phi) - \frac{P_3}{k_1}\sin(k_1\phi) - M \end{cases}$	$\begin{cases} i_{p,N}(\phi) = N_1 cos\phi - N_2 sin\phi + k_1 N_4 \sin(k_1\phi) + N_3 \cos(k_1\phi) \\ i_{s,N}(\phi) = N_1 cos\phi - N_2 sin\phi - k_1 N_4 \sin(k_1\phi) - N_3 \cos(k_1\phi) \\ u_{cr1,N}(\phi) = N_1 sin\phi + N_2 cos\phi - N_4 \cos(k_1\phi) + \frac{N_3}{k_1}\sin(k_1\phi) - 1 \\ u_{cr2,N}(\phi) = N_1 sin\phi + N_2 cos\phi + N_4 \cos(k_1\phi) - \frac{N_3}{k_1}\sin(k_1\phi) - M \end{cases}$
***Z* mode stage of positive i_s**	***Z* mode stage of negative i_s**
$\begin{cases} i_{p,Z}(\phi) = 0 \\ i_{s,Z}(\phi) = Z_{p1}\, cos(k_2\phi) - k_2 Z_{p2}\, sin(k_2\phi) \\ u_{cr1,Z}(\phi) = u_{cr1,Z0} \\ u_{cr2,Z}(\phi) = Z_{p2}\, cos(k_2\phi) + \frac{Z_{p1}}{k_2} sin(k_2\phi) - M \end{cases}$	$\begin{cases} i_{p,Z}(\phi) = 0 \\ i_{s,Z}(\phi) = Z_{n1}\, cos(k_2\phi) - k_2 Z_{n2}\, sin(k_2\phi) \\ u_{cr1,Z}(\phi) = u_{cr1,Z0} \\ u_{cr2,Z}(\phi) = Z_{n2}\, cos(k_2\phi) + \frac{Z_{n1}}{k_2} sin(k_2\phi) + M \end{cases}$
Note: P_1, P_2, P_3, P_4 denote undetermined variables in the *P* mode stage, N_1, N_2, N_3, N_4 represent undetermined variables in the *N* mode stage, Z_{p1}, Z_{p2}, Z_{n1}, Z_{n2} are undetermined variables in the *Z* mode stage. $M = nU_{out}/U_{in}$ is the voltage gain. Other variables are as follows: $\phi = 2\pi f_r t$, $f_r = 1/(2\pi\sqrt{L_{r1}C_{r1}}) = 1/(2\pi\sqrt{L_{r2}C_{r2}})$, $k = L_m/L_{r1}$, $k_1 = \sqrt{1/(1+2k)}$, $k_2 = \sqrt{1/(1+k)}$	

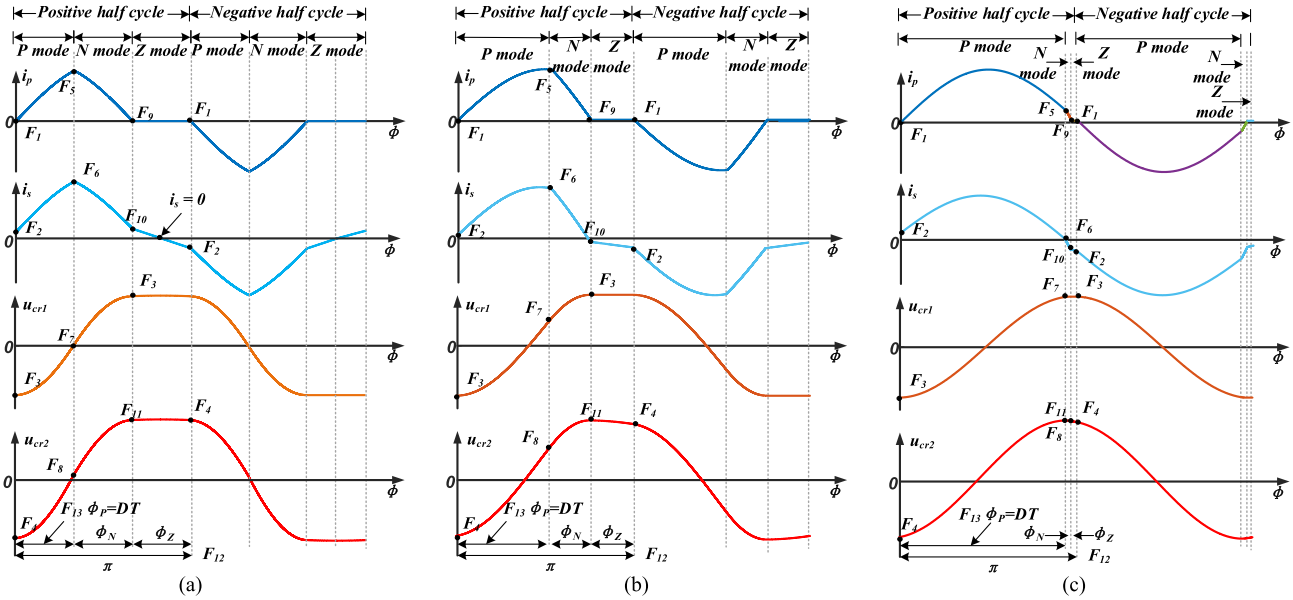

Fig. 5. Detail waveforms of i_p, i_s, u_{cr1}, and u_{cr2} under different *M* (different duty cycle) and the boundary conditions. (a) $M = 0$. (b) $M = 0.5$. (c) $M = 1$.

(F_1 to F_{11}) should be satisfied, as shown in Fig. 5:

$$\begin{cases} F_1 = i_{p,P}\ (0) = 0 \\ F_2 = i_{s,P}\ (0) + i_{s,z}\ (\phi_Z) = 0 \\ F_3 = u_{cr1,P}\ (0) + u_{cr1,z}\ (\phi_Z) = 0 \\ F_4 = u_{cr2,P}\ (0) + u_{cr2,z}\ (\phi_Z) = 0 \\ F_5 = i_{p,P}\ (\phi_P) - i_{p,N}\ (0) = 0 \\ F_6 = i_{s,P}\ (\phi_P) - i_{s,N}\ (0) = 0 \\ F_7 = u_{cr1,P}\ (\phi_P) - u_{cr1,N}\ (0) = 0 \\ F_8 = u_{cr2,P}\ (\phi_P) - u_{cr2,N}\ (0) = 0 \\ F_9 = i_{p,N}\ (\phi_N) = 0 \\ F_{10} = i_{s,N}\ (\phi_N) - i_{s,z}\ (0) = 0 \\ F_{11} = u_{cr2,N}\ (\phi_N) - u_{cr2,z}\ (0) = 0 \end{cases} \tag{3}$$

where the subscript *P*, *N*, and *Z* means corresponding variables use the expressions of *P* mode stage, *N* mode stage, and *Z* mode stage, respectively. ϕ_P, ϕ_N, and ϕ_Z are the lengths of the *P* mode stage, *N* mode stage, and *Z* mode stage, respectively. They are all undetermined variables too.

There are now 11 boundary equations (F_1 to F_{11}) and 13 undetermined variables (P_1, P_2, P_3, P_4, N_1, N_2, N_3, N_4, Z_{n1}, Z_{n2}, ϕ_P, ϕ_N, ϕ_Z) in (3) which means two additional constraint equations are needed to solve these undetermined variables.

It can be found from Fig. 5 that the total duration of the four modes is half a cycle, and the duration of the first *P* mode stage corresponds to the conduction time of the switch tube, so F_{12} and F_{13} can be illustrated as follows:

$$\begin{cases} F_{12} = \phi_P + \phi_N + \phi_Z = \frac{T}{2} \\ F_{13} = \phi_P = DT \end{cases} \tag{4}$$

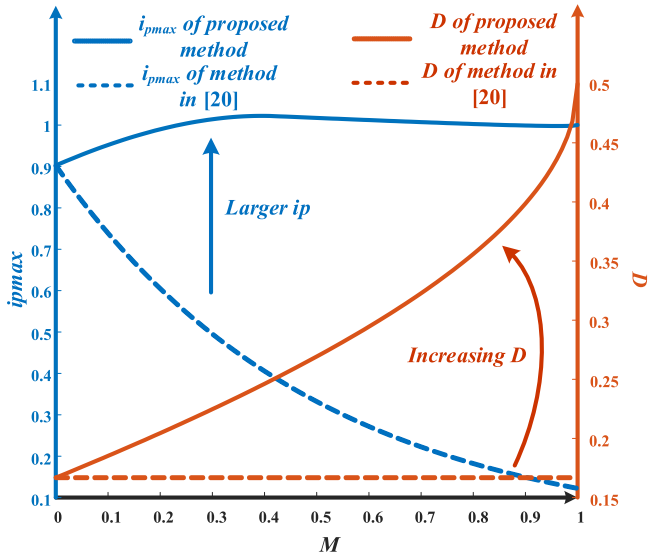

Fig. 6. Ideal relationship among the maximum i_p, voltage gain M, and the duty cycle D of the proposed method and the energy limited method in [20].

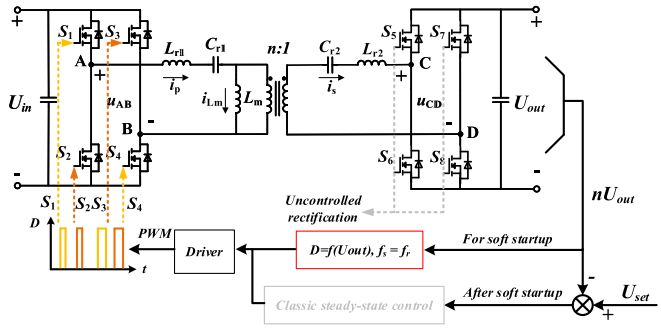

Fig. 7. Schematic diagram of the core idea of the proposed soft startup method.

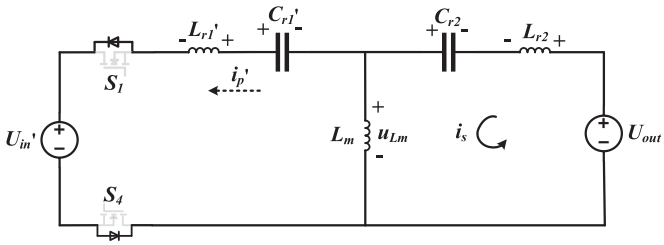

Fig. 8. Schematic diagram of the critical condition for four mode operation.

Solve for Required Characteristics: Solving for the required characteristics involves combining (3) and (4) to determine the undetermined variables. Specifically, the ideal relationship among the maximum i_p (figured as ipmax), the voltage gain M, and the duty cycle D of the proposed method and method in [20] are both given in Fig. 6, which shows that the proposed method uses a varying duty cycle driving scheme to achieve a safe and larger resonant current compared with the fixed duty cycle driving scheme used in the method mentioned in [20].

III. Proposed Soft Startup Method and Its Load Starting Capability Analysis

A. Proposed High-Speed Soft Startup Method

The core idea of the proposed soft startup method is varying the duty cycle with the output voltage to realize the resonant current i_p as large as possible, rather than decreases along with the startup process just like the results in Fig. 6. In this way, an optimal duty cycle variation law is required, with a stable energy limitation feature and fastest speed. Detailed illustration of the differences between the proposed method and the method in [20] is given in Fig. 6, which shows that the proposed method controls the duty cycle varying with the output voltage to maintain ipmax, while the ipmax of the method in [20] will shrink due to the fixed duty cycle.

Come back to the practical control method, the proposed method is a varying duty cycle-based close-loop control, which is illustrated in Fig. 7. Specifically, the switching frequency of the switching tubes in the primary side is set as the resonant frequency, while the duty cycle is varying followed by the output voltage, and the secondary side is working in uncontrolled rectification mode.

Furthermore, the duty cycle variation law ($D = f(U_{\text{out}})$) is a detail function expression obtained by offline calculation. Combine the mode equations shown in Table II and the boundary conditions given in (3), the duty cycle is directly corresponded with the output voltage (or the voltage gain M). Therefore, the optimal duty cycle D matched with a given output voltage U_{out} can be calculated and the variation law can be easily derived. Detail derivation of the optimal duty cycle and the corresponding variation law is given as follows.

B. Optimal Duty Cycle of the Proposed Method

The key point of the mode analysis used above is that i_p will be fixed to zero after the first reduction to zero, which is also the key of natural energy limitation. Assume $i_p = 0$ after the N mode stage. Fig. 8 shows the critical condition of the Z mode stage; if the sum of u_{cr1} and u_{Lm} is larger than U_{in}, then the body diodes of S_1 and S_4 will turn ON, and i_p will rise as a negative value, which contradicts the assumptions above ($i_p = 0$). Therefore, a criterion to ensure $i_p = 0$ can be derived as follows:

$$u_{cr1} + (u_{cr2} - U_{\text{out}}) \cdot \frac{k}{1+k} \le U_{\text{in}}/n \tag{5}$$

where $k = L_m/L_r$, u_{cr1} and u_{cr2} can be solved by the operation mode analysis, U_{in} is the input voltage, and U_{out} is the output voltage.

Specifically, both u_{cr1} and u_{cr2} depend on the duty cycle refered to in Table II, which means the boundary duty cycle $D_{\max}$ corresponding to a given U_{out} can be easily gotten by (5). Subsequently, by iteratively solving a simple optimization problem [as shown in formula (6)] with the startup speed as the optimization objective, the optimal duty cycle D_{op} matched

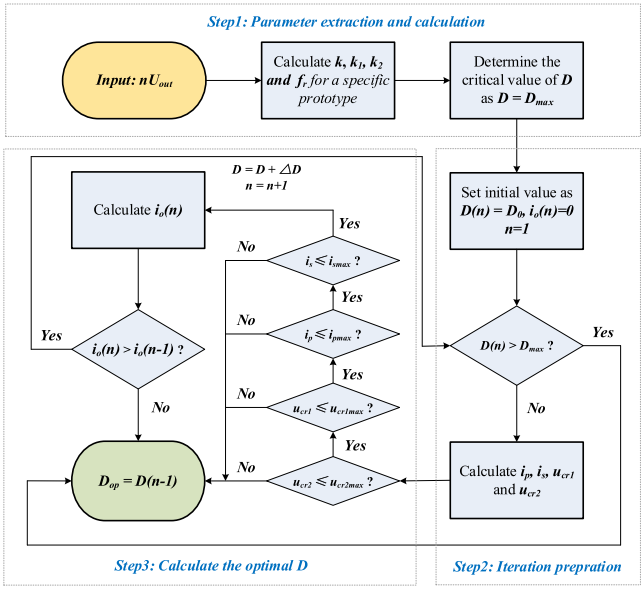

Fig. 9. Solution flow chart of optimal duty cycle under given U_{out}.

with a given U_{out} for the fastest startup can be computed as

$$\begin{cases} \max & i_o = f(D) \\ s.t. & D < D_{\max} \\ & i_s \le i_{s\max} \\ & i_p \le i_{p\max} \\ & u_{cr1} \le u_{cr1\max} \\ & u_{cr2} \le u_{cr2\max} \end{cases} \tag{6}$$

where the output current i_o is introduced to measure the startup speed, which is calculated by (7); $D_{\max}$ is the boundary duty cycle for an energy-limited operation; and $i_{s\max}$, $i_{p\max}$, $u_{cr1\max}$, and $u_{cr2\max}$ are the upper limit of the devices

$$i_o = \frac{1}{T}\int i_s dt. \tag{7}$$

The abovementioned duty cycle optimization process can be illustrated by Fig. 9, in which three core steps are mentioned as follows.

Step1: Variable Extraction and Calculation: The state equations used in operation mode analysis contain several coefficients (such as k_1, k_2, and f_r) depending on the specific parameters of the *CLLC* converter. Subsequently, the boundary duty cycle $D_{\max}$ can be determined by (5).

Stpe2: Iteration Preparation: In order to evaluate the startup speed, the average output current i_o is engaged. The core content is calculating corresponding resonance parameters according to the operation mode analysis.

Step3: Calculate the Optimal D: The optimal *D* can achieve the fastest startup within the safe range.

Moreover, Fig. 10 presents the relationship between the voltage gain *M* and the duty cycle gotten by the iteration given in Fig. 9, where the varying law of *D* can be fitted as follows:

$$D = a \cdot e^{b \cdot M} + c \cdot e^{d \cdot M} \tag{8}$$

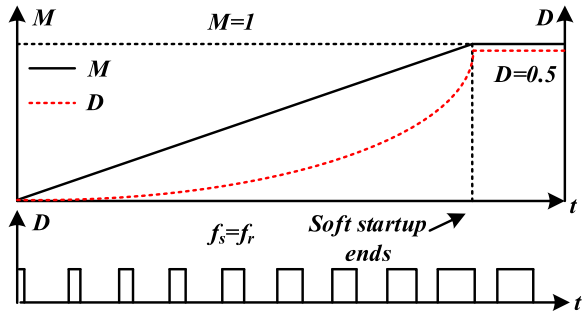

Fig. 10. Schematic diagram of duty cycle variation during soft startup.

where *a*, *b*, *c*, and *d* are the fitting coefficients and $M = nU_{\text{out}}/U_{\text{in}}$.

Besides, considering the computing time of normal DSP, the natural logarithm operation used in (8) usually takes more time, which will undoubtedly affect the response speed of the whole closed-loop control. Therefore, simpler polynomial fitting is usually more practical, which can be expressed as follows:

$$D = a1 + b1 \cdot M + c1 \cdot M^2 + d1 \cdot M^3 \tag{9}$$

where $a1$, $b1$, $c1$, and $d1$ are the fitting coefficients.

Details about the computing time and the fitting accuracy of these two formulas are given in APPEDIX A.

C. Load Starting Capability Analysis of Proposed Method

Conventional soft startup methods of *CLLC* converters mainly focus on the no-load startup, since the largest surge current always occurs at no-load startup condition. However, in the common applications of *CLLC* converters, the load capability is very critical. If the loading soft startup can be realized, the control process can be simplified and the system response speed can be improved.

Actually, the loading capability of a *CLLC* converter depends on the operation conditions, the following analysis is given for $n = 1$. Chen et al. [3] indicated the relationship between the length of *P* mode stage and the output current i_o, and the desired full loading capability of a *CLLC* converter can be achieved with a pure *P* mode stage working condition, where the corresponding $i_{o\max}$ can be expressed as follows:

$$i_{o\max} = \frac{2}{\pi} f_n \tag{10}$$

where $f_n = f_s/f_r$ and $i_{o\max}$ is in per-unit form, which means that appropriate resonant parameters should be designed to match different requirements of the rated power.

Since the proposed method is committed to achieving the maximum resonant current under the boundary of energy limited operation, rather than blindly pursuing the suppression of current, it has a certain load starting ability. Specifically, the average output current of the proposed method can be derived by (11) for a given U_{out}. Furthermore, a more detailed expression of i_o can be derived based on the abovementioned operation mode

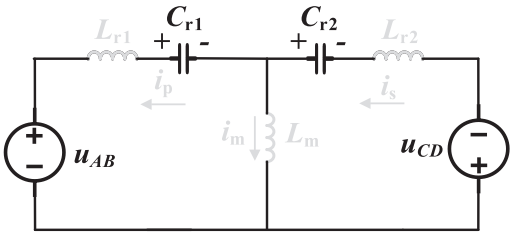

Fig. 11. Equivalent circuit at the end of the positive half cycle.

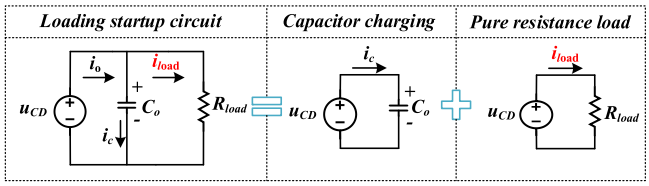

Fig. 12. Relationship between i_o and i_{load}.

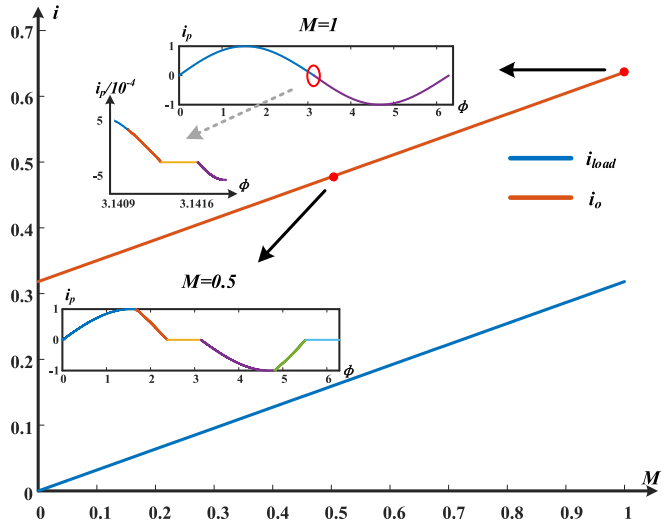

Fig. 13. Loading capability of proposed startup method.

analysis

$$i_o = \frac{1}{T}\left(\int_0^{\phi_P} i_{s,P} + \int_{\phi_P}^{\phi_P+\phi_N} i_{s,N} + \int_{\phi_P+\phi_N}^{T} i_{s,Z}\right) \quad (11)$$

Take the P mode stage as an example, the integration of $i_{s,P}$ can be expressed by variation of $u_{cr2,P}$ as in (12) and (13). Similarly, the integration in (11) of the other two modes can be simplified in (14) and (15)

$$\int_0^{\phi_P} i_{s,P} = -P_2 + P_4\cos(k_1\pi) - \frac{P_3}{k_1}\sin(k_1\pi) - P_2 - P_4 \quad (12)$$

$$\int_0^{\phi_P} i_{s,P} = u_{cr2,P}(\phi_P) - u_{cr2,P}(0) \quad (13)$$

$$\int_{\phi_P}^{\phi_P+\phi_N} i_{s,N} = u_{cr2,N}(\phi_P+\phi_N) - u_{cr2,N}(\phi_P) \quad (14)$$

$$\int_{\phi_P+\phi_N}^{T} i_{s,Z} = u_{cr2,Z}(T) - u_{cr2,Z}(\phi_P+\phi_N). \quad (15)$$

Consider the continuity of $u_{cr2,P}$, $u_{cr2,N}$, and $u_{cr2,Z}$, i_o can be simplified by combining (12)–(15). Besides, since the operation mode of the *CLLC* converter in the negative cycle is symmetrical with the positive cycle, the end of the *Z* mode stage is the same with the next *P* mode stage, which means (16) can be simplified further to (17)

$$i_o = \frac{1}{T}\left(u_{cr2,Z}(T) - u_{cr2,P}(0)\right) \quad (16)$$

$$i_o = \frac{2}{T}\left|u_{cr2,Z}(T)\right| = \frac{2}{T}\left|u_{cr2,P}(0)\right| \quad (17)$$

Furthermore, Fig. 11 shows the equivalent circuit at the end of the positive half cycle, since $i_p = 0$ during the *Z* mode stage and $C_{r1} = C_{r2}$, $u_{cr2,Z}(T)$ can be simplified as shown in (18), and (17) can be expressed by (19), which shows the relationship

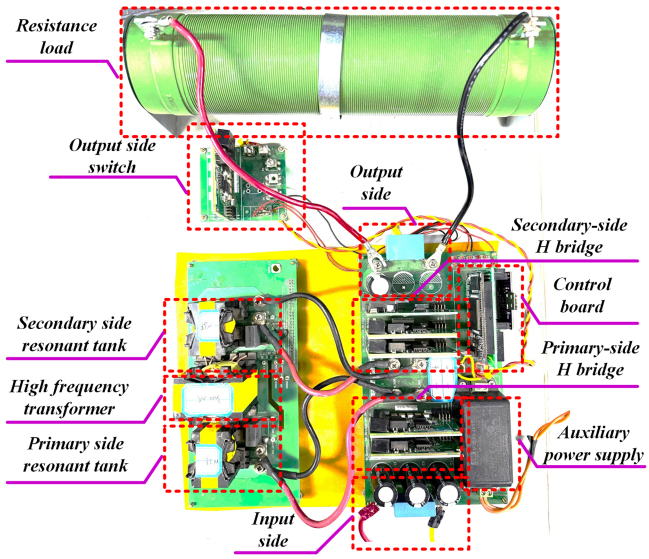

Fig. 14. Picture of lab-level *CLLC* prototype.

between i_o and U_{out} during the startup process

$$u_{cr2,Z}(T) = \left(\frac{U_{\text{in}} + U_{\text{out}}}{2}\right) \quad (18)$$

$$i_o = \frac{2}{T}\left(\frac{U_{\text{in}} + U_{\text{out}}}{2}\right) \quad (19)$$

Significantly, i_o expressed by (19) is not the actual load current for a pure resistance load due to there being an output side capacitor; the relationship between i_o and the actual load current i_{load} during the startup process is illustrated in Fig. 12, and the corresponding formula can be written as (20). Specifically, the capacitor charging circuit used in Fig. 12 is equivalent to the circuit at the beginning of the load starting ($U_{\text{out}} = 0$), which means the i_c mentioned in (20) can be replaced by i_o at $U_{\text{out}} = 0$. Therefore, the actual load current i_{laod} under a pure

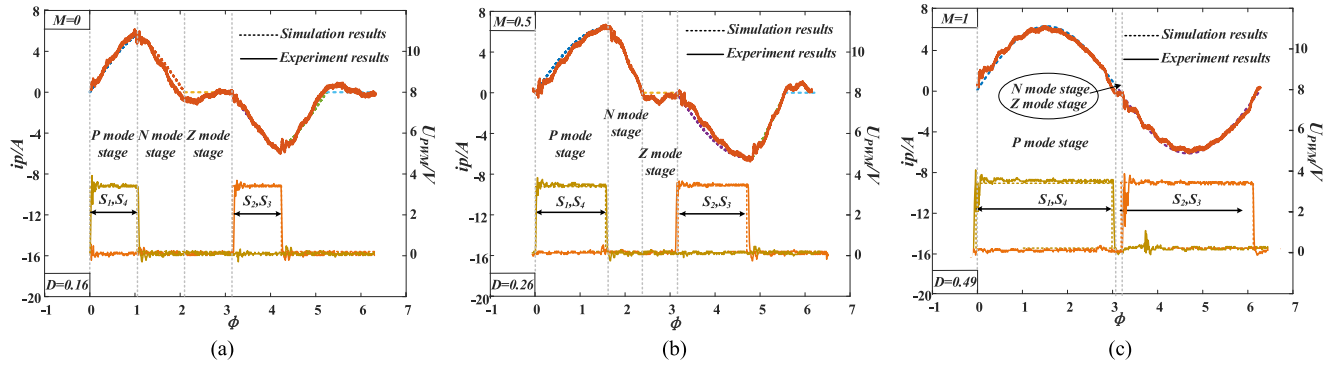

Fig. 15. Comparison of the simulation results and the experiment results for the detail operation mode under different *M*. (a) Comparison results with $\boldsymbol{M} = 0$, where $\boldsymbol{D} = 0.16$. (b) Comparison results with $\boldsymbol{M} = 0.5$, where $\boldsymbol{D} = 0.26$. (c) Comparison results with $\boldsymbol{M} = 1$, where $\boldsymbol{D} = 0.49$.

TABLE III
PARAMETER TABLE OF THE EXPERIMENTAL PROTOTYPE

Resonant tank			
Turns ratio	n	L_m	386uH
L_{r1}/L_{r2}	35uH	C_{r1}/C_{r2}	34nF
C_o	100uF	R_{load}	0~200Ω
Rated power		900W (300V/3A)	
Resonant frequency		145.9kHz	
Switching tubes (SiC MOSFET)		C3M0120090J	

resistance load is shown in (21)

$$i_{\text{laod}} = i_o - i_c \tag{20}$$

$$i_{\text{laod}} = \frac{2}{T}\left(\frac{U_{\text{in}} + U_{\text{out}}}{2}\right) - \frac{2}{T}\left(\frac{U_{\text{in}}}{2}\right) = \frac{U_{\text{out}}}{T}. \tag{21}$$

The loading capability of the proposed startup method can be calculated by (21), and the relationship between $i_o$and i_{laod} is illustrated in Fig. 13. Specifically, the operation condition when $M = 1$ is nearly a pure *P* mode stage due to the duty cycle being close to 0.5. Meanwhile, the operation principle of a higher duty cycle ($D > D_b = 0.2$) is strict three modes, where $M = 0.5$ is given as an example in Fig. 13

$$\begin{cases} i_{o\_\max} = \frac{2}{\pi} \\ i_{\text{load\_max}} = \frac{1}{\pi} \end{cases} \tag{22}$$

Since the duty cycle increases along with the startup progress, the maximum loading capability of the proposed startup method in per-unit form calculated by (19) and (21) and can be given as shown in (22), which is equal to the full-load capability of a *CLLC* converter [see (10) with $f_n = f_s/f_r = 1$].

IV. EXPERIMENTAL VERIFICATION

A lab-level prototype is constructed to validate the proposed soft startup control method and corresponding analysis. The figure of the prototype is illustrated in Fig. 14. Parameters of the prototype are shown in Table III.

For this prototype, the optimal duty cycle variation law is given in (23), which is calculated following the iteration steps given in Fig. 9, and the soft startup is realized. Detail experiment results are as follows:

$$D = 0.3243M^3 - 0.2918M^2 + 0.2688M + 0.1611. \tag{23}$$

First, the accuracy of the operation mode analysis is verified and the duty cycle variation rule is examined. Specifically, three working points are chosen as example, which are the moment of $M = 0$, $M = 0.5$, and $M = 1$, respectively. The turns ratio is set as $n = 1$, and the input voltage $U_{in} = 300\ V$. Fig. 15 shows the detail comparison results, on the one hand the experiment results of i_p are highly anastomotic with the simulation results given by the operation mode analysis, where the three-mode working pattern (consists of the *P* mode stage, *N* mode stage, and *Z* mode stage) is clear for $D > D_b = 0.2$. On the other hand, the real duty cycle during the experiment of each M is consistent with the expected value calculated by formula (23), which means the close-loop control is perfectly working and the soft startup to $M = 1$ is achieved. Meanwhile, soft switching is achieved, as shown in Fig. 15, which is also important for the converter [29].

Second, the advantages of the proposed method in the startup speed are verified. To show the startup speed clearly, the key startup performance of different startup methods is summarized in Table IV, which proves the proposed method can highly improve the startup speed for a same peak current working condition. Particularly, bidirectional startup is realized in the operation condition of 240–48 V (by replacing the transformer's turns ratio), further verifying the proposed method is effective under different voltage conversion ratios. Specifically, Fig. 16 illustrates the no-load soft startup performance of different operation conditions and different methods. Since the startup effect is similar for different working pattern, only take the 300—300 V operation condition as an example for a detailed analysis as follows.

In the 300—300 V transfer condition, the proposed method can realize soft startup in 9 ms and the peak i_p is 6.9 A. Meanwhile, the soft startup experiment results of the typical linear duty cycle variation method (as in [14]) shows the startup time is about 24 ms for the same peak i_p. In addition, the soft startup experiment of the fixed frequency and fixed duty cycle method is done with $U_{\text{in}} = 300\ V$ (rather than $U_{\text{in}} = 100\ V$ in [20]), corresponding results show a 42-ms soft startup. Moreover,

Fig. 16. Comparison of the startup speed between the proposed method and the conventional soft startup methods.

TABLE IV
BRIEF COMPARISON OF DIFFERENT STARTUP METHOD

Operation Condition	**300V-300V**		**240V-48V**		**48V-240V**	
Soft startup method	Startup time	Peak i_p	Startup time	Peak i_p	Startup time	Peak i_p
Proposed method	**9ms**	6.9A	**3.2ms**	1.63A	**160ms**	4.11A
Linear duty cycle variation method in [14]	24ms	6.9A	7.6ms	1.63A	300ms	4.11A
Fixed frequency and fixed duty cycle method in [20]	42ms	6.9A	12.2ms	1.63A	350ms	4.11A
Varying frequency method in [8], [9], [10] and [11]	83ms	6.9A	50ms	1.63A	800ms	4.11A

The first line is bolded to highlight different experimental conditions, and the third line is bolded to highlight the startup speed of the method proposed in the paper.

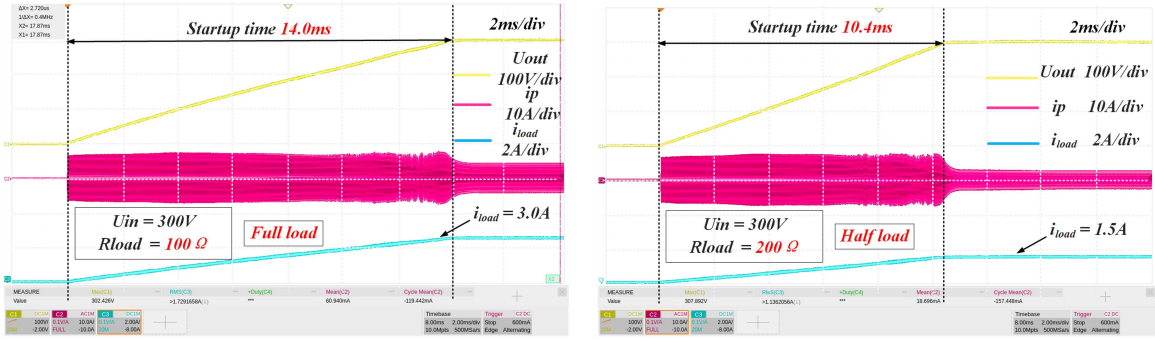

Fig. 17. Load starting experiment results of the proposed method. (a) Full load startup for $U_{in} = 300$ V. (b) Half load startup for $U_{\text{in}} = 300$ V.

the soft startup experiment of the most commonly used varying frequency method is also redone in the same prototype, the results show that 83 ms is required to achieve the same startup target for a frequency variation rule mentioned in [8], [9], [10], [11].

The experiment results of the bidirectional startup of 240–48 V illustrate a similar conclusion, the core indexes are listed in Table IV for quick comparison. Obviously, the proposed method highly improves the soft startup speed for nearly nine times faster than the varying frequency methods. Besides, the optimized duty cycle variation rule shows its excellent performance in the startup speed, no matter compared with the simple linear variation rule or the fixed duty cycle rule. Furthermore, the proposed method is suitable for different operation conditions, including different input voltage levels and bidirectional operation patterns.

Finally, the loading capability of the proposed method is verified. The corresponding theoretical maximum loading current for a pure resistance load of the prototype can be calculated by (1) and (22), and the results are given in (24) considering the detail parameters of the prototype

$$i_{\text{load\_max}} = 0.01U_{\text{in}} \tag{24}$$

Moreover, the corresponding load starting experiment verification results are given in Fig. 17, including the full-load startup, half-load startup results under the rated $U_{\text{in}} = 300\ V$ for a pure resistance load.

Specifically, the full-load startup experiment results are shown in Fig. 17(a), where a $100\ \Omega$ pure resistance is used. On the one hand, the theoretical maximum load current of $U_{\text{in}} = 300$ V is $i_{\text{load\_max}} = 3$ A [see (24)], on the other hand, Fig. 17(a) verifies a successful startup in 14 ms with a 3-A actual load current, which proves the accuracy and the full-load (900 W in Table III) startup capability of the proposed method. Furthermore, the half-load soft startup experiment results are provided in Fig. 17(b) with a $200\ \Omega$ pure resistance load, where the startup time is 10.4 ms and the load current is 1.5 A. By the way, the heavier the load, the longer the startup time, but the overall starting speed has little change, and also shows outstanding speed.

V. Conclusion

In this article, a high-speed soft startup method with full-load startup capability is proposed for *CLLC* converters. Following the energy limitation principles, an optimal duty cycle variation rule is derived to realize such a fast startup, which can also handle different operation conditions. The main contributions of this article can be summarized as follows.

1) The operation mode of an energy limitation-based startup is given detailed ly for different duty cycle, which derives the boundary duty cycle $D = 0.2$ for four-mode and three-mode operation conditions.
2) An optimal duty cycle variation law is figured out to achieve a fast soft startup, which is effective under different input voltage levels and different voltage conversion ratios. The experiment verifies that a 9-ms soft startup can be achieved at $U_{\text{in}} = U_{\text{out}} = 300\ V$, which is nearly nine times faster than the classic varying frequency methods.
3) The load starting capability of the *CLLC* converter is analyzed detailedly, which proves a maximum loading threshold $i_{\text{load}} = 1/\pi$ (or $i_o = 2/\pi$) of the proposed method, and corresponding full-load soft startup is achieved in a 900-W *CLLC* prototype.

The soft startup method proposed in this article achieves high-speed startup with full-load startup capability. The next step is trying to establish a control paradigm suitable for fast soft startup of resonant converters.

Appendix

This section is a brief comparison of different duty cycle variation fitting types of the proposed method. Fig. 10 illustrates the initial relationship between the duty cycle and the output voltage, which can be fitted as shown in (8) and (9).

The fitting accuracy and the computational complexity are the two main indicators to measure the fitting results. Specifically, the higher the fitting accuracy and the less the amount of computation required, the better the fitting results. In order to present the fitting effect, the parameters of the *CLLC* prototype used in the experiment verification section are used to derive the different duty cycle fitting formulas [which are given by (A1) and (A2)], and some corresponding comparison results are listed

TABLE V
COMPARISON RESULTS FOR DIFFERENT FITTING FORMULAS

Fitting formular	R^2	Computation time
Equation (A-1)	0.9996	1643 clock cycles
Equation (A-2)	0.9961	284 clock cycles
Hint: The computation time is measured by clock cycles needed for DSP 28335, where 1 clock cycle equals to 0.67ns.		

in Table V

$$D = 0.1683e^{0.9233M} + 2.72 \times 10^{-11} e^{21.62M} \quad \text{(A1)}$$

$$D = 0.3243M^3 - 0.2918M^2 + 0.2688M + 0.1611. \quad \text{(A2)}$$

In conclusion, the fitting accuracy of these two formulas is similar, but the compute complexity of third-order polynomial fitting (A2) is significantly less than that of second-order exponential fitting (A1). Therefore, the third-order polynomial fitting shown in (9) is selected in the actual experiment.

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