A Compensation-Based 3D-SVPWM Strategy Employing Positive and Negative DC-Link Voltages Sampling for Three-Phase Four-Wire Three-Level Converters

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***Abstract*—Three-phase four-wire three-level (3P4W-3L) converters demonstrate broad application prospects in off-grid systems, while facing complex and variable operating conditions. Under asymmetrical loads, their dc-link neutral-point potential (NPP) exhibits fundamental-frequency oscillation proportional to the load unbalance factor. The adoption of traditional three-dimensional space vector modulation (3D-SVPWM) based on the assumption of balanced positive and negative dc-link voltages leads to substantial output errors during large-amplitude NPP oscillation, ultimately causing three-phase voltage unbalance and elevated total harmonic distortion (THD). Further theoretical analysis confirms that such errors introduce third-harmonic components in the output voltages. A compensation-based 3D-SVPWM strategy employing positive and negative dc-link voltages sampling is proposed in this article, which constructs the 3D space vector diagram based on the real-time sampling values of positive and negative dc-link voltages. Using the real-time positions of basic vectors, subsectors in the vector diagram are optimally redivided and the vector dwell times are calculated accordingly. This strategy effectively suppresses third-harmonic components in the output voltages, ensuring that the system can still output high-quality voltage waveforms even when the NPP oscillates greatly. Finally, the effectiveness of the proposed strategy is verified through comparative experiments, showing a high balance degree and low THD of the output voltages.**

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***Index Terms*—Neutral-point potential (NPP) oscillation, power quality, three-dimensional space vector modulation (3D-SVPWM), three-phase four-wire three-level (3P4W-3L) converters.**

I. Introduction

In order to reduce the impact of the volatility of new energy generation and ensure the reliability of independent power supply, three-phase converters have become an essential device in new energy power generation systems [1]. Compared with the two-level, a 3L topology has become a significant solution for high-frequency power conversion applications due to its reduced voltage stress on power devices and enhanced output power quality [2]. However, dc-link NPP oscillation is an inherent issue of 3L systems, and the oscillation becomes more severe especially when small-capacity film capacitors are used instead of electrolytic capacitors on the dc-link to extend the system's service life [3]. Moreover, when a 3P4W topology with zero-sequence output circuit is operated under asymmetrical loads, the zero-sequence current is injected directly into the dc-link NPP through the neutral line, further aggravating the oscillation [4]. At this time, if the modulation calculation is still based on the assumption that the positive and negative dc-link voltages are equal, there will be a large error between the output vector and the reference vector, eventually leading to three-phase output voltage unbalance and causing serious damage to the normal operation of the load.

To address this issue, two primary research approaches exist: the first aims to achieve NPP balancing, while the second relocates the basic vector position based on the actual values of positive and negative dc-link voltages. NPP balancing can be implemented through hardware modifications – for instance, the 3P4W four-leg topology connects the zero-sequence current path to a fourth leg, enabling active zero-sequence current control to prevent its reflux into the NPP [5], [6]. However, this approach not only increases hardware costs and power losses but also significantly elevates control and modulation complexity. Alternatively, the three-leg split-capacitor 3P4W topology (where the zero-sequence path directly connects to the NPP) can reduce NPP fluctuations by enlarging dc-link capacitors—a

conceptually straightforward solution at the expense of substantially increased hardware volume [7]. Consequently, software-based methods for NPP balancing have gained extensive research focus in three-leg 3P4W systems [8], [9], [10], [11], [12]. Although [8] proposes a carrier-based zero-level decomposition method providing quantitative NPP fluctuation compensation, it demonstrates significant effectiveness only under low load imbalance conditions. [9] introduces an NPP balancing method by reconstructing O-state dwell times, integrating simplified 3D-SVPWM with NPP control to achieve desired balancing, but incurs elevated output voltage harmonics. Yu et al. [10] use SPWM decomposition into dual modulation waves for simple neutral-point balancing, but only tests at tens of volts. While [12] employs continuous control set model predictive control for independent phase regulation in 3P4W systems with dc offset injection to balance NPP, it exhibits high hardware-parameter dependency. A fundamental limitation common to these algorithms is their compromised performance during severe dc-link oscillation, as forcibly suppressing such oscillation may exacerbate output distortion and compromise system stability.

The SVPWM of real-time location of basic vector position is mainly applied to 3P3W, and only a few literatures have been studied based on 3P4W topology. In [13], an optimization of the symmetrical SVPWM is proposed to deal with the output vector distortion caused by unbalanced and oscillated NPP in 3P3W topology. It is proved in [14] that the VSVPWM can work well with the unbalanced positive and negative voltages, though it has high switching losses and current ripples. Based on the 3P3W model of NPP oscillation caused by the failure of a single bridge arm, Ge et al. [15] and Zhang et al. [16] compensate the basic voltage vector to eliminate the three-phase output voltage unbalance. These modulation strategies for real-time basic vector positioning or compensation in 3P3W topology operate exclusively in the two-dimensional (2D) plane, where vectors possess only $\alpha\beta$-axis components without zero-sequence components (also termed γ-components). Consequently, they are not applicable to 3P4W systems requiring zero-sequence component control [17]. Although [18] presents an optimized compensated SVPWM for an eight-switch 3P4W topology under single-phase leg fault conditions, its space vector model degenerates to a 2D plane due to the phase switch fault. Conversely, for normally loaded 3P4W systems, presence of a zero-sequence current path necessitates SVPWM research in 3D coordinates [3], [17], [19], [20], [21], [22]. Therefore, a Compensation-Based 3D-SVPWM for 3P4W three-leg topology is proposed in this article, and the basic vector position is repositioned to ensure that the output voltages still maintain three-phase balance under the condition of NPP oscillation.

This journal paper extends its conference version with more thorough theoretical analysis of fluctuation-induced output errors and additional experimental results under multiple operating conditions [23].

The rest of this article is organized as follows. Section II investigates the NPP oscillation mechanism, quantitatively analyzing its effect on the output voltages under the traditional 3D-SVPWM and demonstrating that it introduces third-harmonic distortions in the three-phase outputs. Then, a compensation-based 3D-SVPWM is proposed in Section III, which obtains

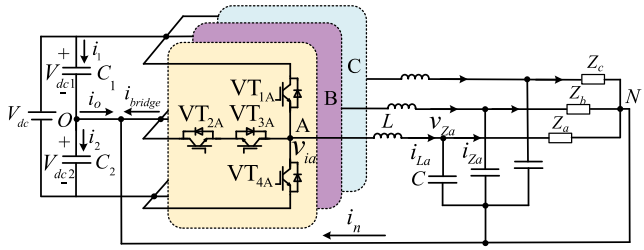

Fig. 1. Topology of 3P4W-3L converters.

calculation and vector synthesis by relocating the position of the basic vector under the NPP oscillation based on the real-time sampling values of positive and negative dc-link voltages. It can reduce the error between the output vector and the reference vector to achieve the effect of reducing the output voltage unbalance and improving the power quality. The experimental verifications are presented in IV. Finally, Section V concludes this article.

II. Problems of the Traditional 3D-SVPWM

The topology of converters investigated in this article is shown in Fig. 1, where the load neutral-point is connected to the dc-link neutral-point via a neutral line. It should be noted that three-phase load unbalance represents a typical operational scenario in practical applications.

A. Principle of NPP Oscillation

In the converter topology shown in Fig. 1, the presence of the neutral line ensures that the voltage drop between the load neutral point (NP) and the dc-link NP is 0, enhancing the ability to carry asymmetrical loads. But, this provides a loop for the unbalanced current, and the NPP is more likely to oscillate.

As shown in Fig. 1, $V_{\rm dc1}$ and $V_{\rm dc2}$ are regarded as positive and negative dc-link voltages, and $\Delta V_{\rm dc}$ is the voltage difference between the positive and negative buses. i_1 and i_2 are the currents on the positive and negative dc capacitors respectively; i_o is the current flowing out of the dc-link NPP; i_n is the current through the neutral line; $i_{\rm bridge}$ is the sum of the currents of the three bridge arms. By establishing the voltage and current equations for the positive and negative dc links, the principle of NPP oscillation can be analyzed, yielding the following relations:

$$\begin{cases} \Delta V_{\rm dc} = V_{\rm dc1} - V_{\rm dc2} = \left(\frac{V_{\rm dc}}{2} + \frac{1}{C_1}\int i_1 dt\right) - \left(\frac{V_{\rm dc}}{2} + \frac{1}{C_2}\int i_2 dt\right) \\ i_o = i_1 - i_2 = -i_{\rm bridge} - i_n \\ i_n = i_{La} + i_{Lb} + i_{Lc} = \frac{v_{za}}{Z_a} + \frac{v_{zb}}{Z_b} + \frac{v_{zc}}{Z_c} \end{cases}. \tag{1}$$

Neglecting the effect of device parameter variations and assuming that the positive and negative dc capacitances are the same, $C_1 = C_2 = C_{\rm dc}$, it can be obtained as

$$\Delta V_{\rm dc} = -\frac{1}{C_{\rm dc}}\int (i_{\rm bridge} + i_n) dt. \tag{2}$$

Ignoring the influence of high-frequency harmonics, it can be seen from (2) that when the load is balanced, the current i_n on the neutral line is 0. The NPP is only affected by the $i_{\rm bridge}$ and

TABLE I
THREE-PHASE OUTPUT LEVEL

Three-phase output level	Three-level magnitude	Symbol of representation	Conducted switching tube
v_{ix} (x=a、b、c)	$\frac{(1+0.5k)V_{dc}}{2}$	P	VT_{1x}、VT_{2x}
	0	O	VT_{2x}、VT_{3x}
	$-\frac{(1-0.5k)V_{dc}}{2}$	N	VT_{3x}、VT_{4x}

lead to the fundamental-frequency unbalanced current flowing through the neutral line, and then a fundamental-frequency voltage oscillation will be superimposed on the dc-link NPP, the amplitude of which is related to the unbalanced current and the size of the dc capacitance [24]. The smaller the dc capacitance, the larger the unbalanced current and the larger the resulting oscillation in the NPP.

B. Performance of the Traditional 3D-SVPWM Under NPP Oscillation

The variable k related to the oscillation of the NPP is defined, which is called the bus unbalancing degree, and its expression is:

$$k = \frac{\Delta V_{\rm dc}}{V_{\rm dc}/2} = K_1\cos(\omega t+\varphi_1) + K_3\cos(3\omega t+\varphi_3)$$
$$-2 \le k \le 2. \tag{3}$$

The oscillation of the NPP leads to the unbalance of positive and negative dc-link voltages. The magnitudes of the three-level signals that can be actually output by each phase are given in Table I. A total of 27 switching combinations can be output by three phases.

Performing Clarke transformation on the 27 switching combinations using (4), and then the coordinates of 27 basic vectors in the $\alpha\beta\gamma$ coordinate system are obtained, as given in Table II [17]. A 3D space vector diagram is created, as shown in Fig. 2. The traditional 3D-SVPWM assumes that the output voltage levels of each phase are $V_{\rm dc}/2$, 0, and $-V_{\rm dc}/2$, respectively, corresponding to $k = 0$, as shown in Fig. 2(a), where the basic vectors are symmetrically distributed around the center. However, the actual basic vectors vary in both magnitude and phase due to the oscillation of the NPP. Fig. 2(b) is the space vector diagram when $k > 0$, and the same can be obtained when $k < 0$

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_\gamma \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}. \tag{4}$$

The basic principle of the 3D-SVPWM is described below. According to the distribution of the vectors projected on the $\alpha\beta$ plane, four basic vectors with the closest positions to the reference vector are selected for synthesis. According to the volt-second equilibrium principle, the dwell times of each basic vector are calculated. According to the seven-stage time

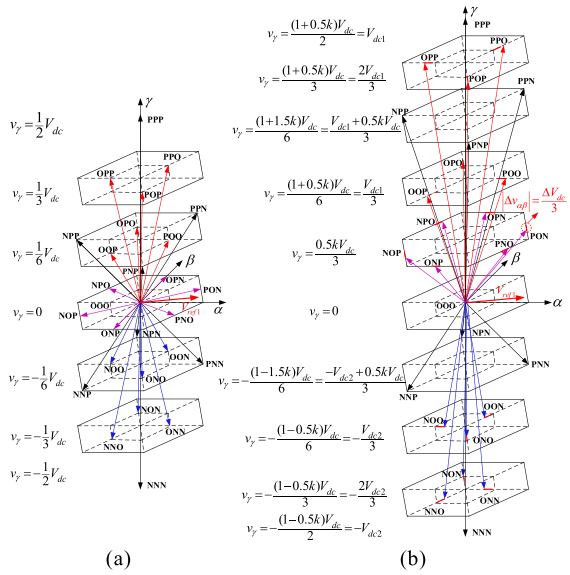

Fig. 2. Space vector diagram in the $\alpha\beta\gamma$ coordinate system. (a) $k = 0$. (b) $k > 0$.

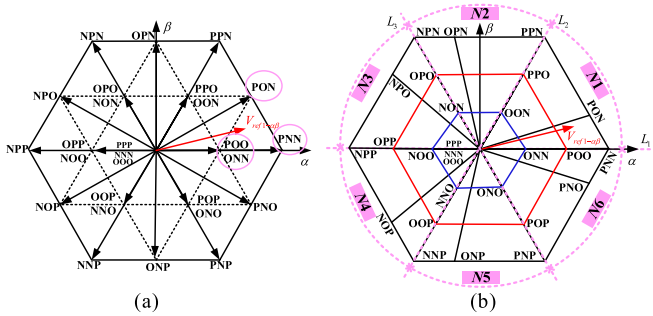

Fig. 3. Projections of space vectors on the $\alpha\beta$ plane. (a) $k = 0$ (b) $k > 0$.

allocation principle, the basic vectors are arranged and compared with the carrier to generate PWM waves [22].

Taking the synthesis of reference vector $V_{\rm ref1}$ as an example, the output error of the traditional 3D-SVPWM is illustrated. First, only the distribution of vectors on the $\alpha\beta$ plane is considered, as shown in Fig. 3(a), and the four basic vectors V_1, V_2, V_3 and V_4 selected for the synthesis of $V_{\rm ref}$ are successively V_{POO}, V_{ONN}, V_{PNN}, and V_{PON}. Their coordinates ($k = 0$) can be obtained from Table II as ($V_{\rm dc}/3$, 0, $-V_{\rm dc}/3$), ($2V_{\rm dc}/3$, 0, $-V_{\rm dc}/6$), ($V_{\rm dc}/2$, $\sqrt{3}V_{\rm dc}/6$, 0), ($V_{\rm dc}/3$, 0, $V_{\rm dc}/6$), respectively.

Then, according to the volt-second equilibrium principle, the dwell times t_1, t_2, t_3, t_4 of the four vectors should meet the following conditions:

$$V_1t_1 + V_2t_2 + V_3t_3 + V_4t_4 = V_{\rm ref}T_S \tag{5}$$
$$t_1 + t_2 + t_3 + t_4 = T_S. \tag{6}$$

The dwell time of each basic vector can be obtained by substituting their coordinates into (5) and (6), as shown in (7). $V_{\rm ref1\text{-}\alpha}$, $V_{\rm ref1\text{-}\beta}$ and $V_{\rm ref1\text{-}\gamma}$ are the components of the reference

TABLE II
BASIC VECTOR COORDINATES IN THE $\alpha\beta\gamma$ COORDINATE SYSTEM

Basic vector	Coordinate	Basic vector	Coordinate	Basic vector	Coordinate
V_{PNN}	$(\frac{2V_{dc}}{3},0,-\frac{(1-1.5k)V_{dc}}{6})$	V_{PON}	$(\frac{(3+0.5k)V_{dc}}{6},\frac{\sqrt{3}(1-0.5k)V_{dc}}{6},\frac{kV_{dc}}{6})$	V_{ONN}	$(\frac{(1-0.5k)V_{dc}}{3},0,-\frac{(1-0.5k)V_{dc}}{3})$
V_{PPN}	$(\frac{V_{dc}}{3},\frac{\sqrt{3}V_{dc}}{3},\frac{(1+1.5k)V_{dc}}{6})$	V_{OPN}	$(-\frac{kV_{dc}}{6},\frac{\sqrt{3}V_{dc}}{3},\frac{kV_{dc}}{6})$	V_{OON}	$(\frac{(1-0.5k)V_{dc}}{6},\frac{\sqrt{3}(1-0.5k)V_{dc}}{6},-\frac{(1-0.5k)V_{dc}}{6})$
V_{NPN}	$(-\frac{V_{dc}}{3},\frac{\sqrt{3}V_{dc}}{3},-\frac{(1-1.5k)V_{dc}}{6})$	V_{NPO}	$(-\frac{(3-0.5k)V_{dc}}{6},\frac{\sqrt{3}(1+0.5k)V_{dc}}{6},\frac{kV_{dc}}{6})$	V_{NON}	$(\frac{-(1-0.5k)V_{dc}}{6},\frac{\sqrt{3}(1-0.5k)V_{dc}}{6},\frac{-(1-0.5k)V_{dc}}{3})$
V_{NPP}	$(-\frac{2V_{dc}}{3},0,\frac{(1+1.5k)V_{dc}}{6})$	V_{NOP}	$(-\frac{(3-0.5k)V_{dc}}{6},-\frac{\sqrt{3}(1+0.5k)V_{dc}}{6},\frac{kV_{dc}}{6})$	V_{NOO}	$(-\frac{(1-0.5k)V_{dc}}{3},0,-\frac{(1-0.5k)V_{dc}}{6})$
V_{NNP}	$(\frac{-V_{dc}}{3},\frac{-\sqrt{3}V_{dc}}{3},\frac{-(1-1.5k)V_{dc}}{6})$	V_{ONP}	$(-\frac{kV_{dc}}{6},-\frac{\sqrt{3}V_{dc}}{3},\frac{kV_{dc}}{6})$	V_{NNO}	$(\frac{-(1-0.5k)V_{dc}}{6},\frac{-\sqrt{3}(1-0.5k)V_{dc}}{6},\frac{-(1-0.5k)V_{dc}}{3})$
V_{PNP}	$(\frac{V_{dc}}{3},-\frac{\sqrt{3}V_{dc}}{3},\frac{(1+1.5k)V_{dc}}{6})$	V_{PNO}	$(\frac{(3+0.5k)V_{dc}}{6},-\frac{\sqrt{3}(1-0.5k)V_{dc}}{6},\frac{kV_{dc}}{6})$	V_{ONO}	$(\frac{(1-0.5k)V_{dc}}{6},\frac{-\sqrt{3}(1-0.5k)V_{dc}}{6},\frac{-(1-0.5k)V_{dc}}{6})$
V_{PPP}	$(0,0,\frac{(1+0.5k)V_{dc}}{2})$	V_{POO}	$(\frac{(1+0.5k)V_{dc}}{3},0,\frac{(1+0.5k)V_{dc}}{6})$	V_{OPP}	$(-\frac{(1+0.5k)V_{dc}}{3},0,\frac{(1+0.5k)V_{dc}}{3})$
V_{NNN}	$(0,0,-\frac{(1-0.5k)V_{dc}}{2})$	V_{PPO}	$(\frac{(1+0.5k)V_{dc}}{6},\frac{\sqrt{3}(1+0.5k)V_{dc}}{6},\frac{(1+0.5k)V_{dc}}{3})$	V_{OOP}	$(\frac{-(1+0.5k)V_{dc}}{6},\frac{-\sqrt{3}(1+0.5k)V_{dc}}{6},\frac{(1+0.5k)V_{dc}}{6})$
V_{OOO}	$(0,0,0)$	V_{OPO}	$(\frac{-(1+0.5k)V_{dc}}{6},\frac{\sqrt{3}(1+0.5k)V_{dc}}{6},\frac{(1+0.5k)V_{dc}}{6})$	V_{POP}	$(\frac{(1+0.5k)V_{dc}}{6},\frac{-\sqrt{3}(1+0.5k)V_{dc}}{6},\frac{(1+0.5k)V_{dc}}{3})$

vector on each axis in the $\alpha\beta\gamma$ coordinate system

$$\begin{cases} t_{\text{ref1}-1} = T_S - (2V_{\text{ref1}-\alpha} + 2V_{\text{ref1}-\gamma}) * T_S/V_{\text{dc}} \\ t_{\text{ref1}-2} = (3V_{\text{ref1}-\alpha} - \sqrt{3}V_{\text{ref1}-\beta}) * T_S/V_{\text{dc}} - T_S \\ t_{\text{ref1}-3} = 2\sqrt{3}V_{\text{ref1}-\beta} * T_S/V_{\text{dc}} \\ t_{\text{ref1}-4} = T_S - (V_{ref1-\alpha} + \sqrt{3}V_{\text{ref1}-\beta} - 2V_{\text{ref1}-\gamma}) * T_S/V_{\text{dc}} \end{cases}. \tag{7}$$

When a large NPP oscillation occurs, there is a large difference between positive and negative dc-link voltages, resulting in a significant change in the actual position of the basic vectors compared with the model established in the traditional 3D-SVPWM. If the dwell times are still calculated and output based on the symmetric space vector diagram [see Fig. 2(a)], there will eventually be a large error between the actual output vector and the reference vector.

Considering the influence of the NPP oscillation, it can be seen from Table II that the actual coordinates of the four basic vectors selected in the above example are as follows:

$$\begin{cases} V_{ONN}((1-0.5k)V_{\text{dc}}/3, 0, -(1-0.5k)V_{\text{dc}}/3) \\ V_{PNN}(2V_{\text{dc}}/3, 0, -(1-1.5k)V_{\text{dc}}/6) \\ V_{PON}((3+0.5k)V_{\text{dc}}/6, \sqrt{3}(1-0.5k)V_{\text{dc}}/6, kV_{\text{dc}}/6) \\ V_{POO}((1+0.5k)V_{\text{dc}}/3, 0, (1+0.5k)V_{\text{dc}}/6) \end{cases}. \tag{8}$$

Combining (7) and (8) for calculation, the actual output voltage vector V_{out1} is obtained as

$$V_{\text{out1}} = \frac{1}{6}((6+k)V_{\text{ref1}-\alpha} + 4kV_{\text{ref1}-\gamma}, (6-3k)V_{\text{ref1}-\beta} \\ 2kV_{\text{ref1}-\alpha} + (6-k)V_{\text{ref1}-\gamma}). \tag{9}$$

TABLE III
OUTPUT VECTOR

Region	V'	V_{out}
$-\frac{\pi}{6} \le \theta < \frac{\pi}{6}$	$(V_{ref-\alpha} + 4V_{ref-\gamma}, -3V_{ref-\beta}, 2V_{ref-\alpha} - V_{ref-\gamma})$	$V_{out} = V_{ref} + \frac{k}{6}V'$
$\frac{\pi}{6} \le \theta < \frac{\pi}{2}$	$(2V_{ref-\alpha} - \sqrt{3}V_{ref-\beta} + 2V_{ref-\gamma}, -\sqrt{3}V_{ref-\alpha} + 2\sqrt{3}V_{ref-\gamma}, V_{ref-\alpha} + \sqrt{3}V_{ref-\beta} + V_{ref-\gamma})$	
$\frac{\pi}{2} \le \theta < \frac{5\pi}{6}$	$-(2V_{ref-\alpha} + \sqrt{3}kV_{ref-\beta} + 2V_{ref-\gamma}, \sqrt{3}V_{ref-\alpha} - 2\sqrt{3}V_{ref-\gamma}, V_{ref-\alpha} - \sqrt{3}V_{ref-\beta} - V_{ref-\gamma})$	
$\frac{5\pi}{6} \le \theta < \frac{7\pi}{6}$	$-(V_{ref-\alpha} + 4V_{ref-\gamma}, -3V_{ref-\beta}, 2V_{ref-\alpha} - V_{ref-\gamma})$	
$\frac{7\pi}{6} \le \theta < \frac{3\pi}{2}$	$-(2V_{ref-\alpha} - \sqrt{3}V_{ref-\beta} + 2V_{ref-\gamma}, -\sqrt{3}V_{ref-\alpha} + 2\sqrt{3}V_{ref-\gamma}, V_{ref-\alpha} + \sqrt{3}V_{ref-\beta} + V_{ref-\gamma})$	
$\frac{3\pi}{2} \le \theta < \frac{11\pi}{6}$	$(2V_{ref-\alpha} + \sqrt{3}kV_{ref-\beta} + 2V_{ref-\gamma}, \sqrt{3}V_{ref-\alpha} - 2\sqrt{3}V_{ref-\gamma}, V_{ref-\alpha} - \sqrt{3}V_{ref-\beta} - V_{ref-\gamma})$	

It can be observed from (9) that there are errors between the axis components of the actual output vector and the reference vector, and the magnitude of the error is proportional to the bus unbalancing degree. As k increases, the output performance of the traditional 3D-SVPWM worsens.

Considering only the influence of NPP oscillation, the output of the reference vector V_{ref} at different positions under the traditional modulation strategy is given in Table III. θ is the angle between the projection of V_{ref} on the $\alpha\beta$ plane and the α-axis.

The output vectors in the above table are converted to the *abc* coordinate system, and the output voltage expressions of each phase are shown in (10). $v_{\text{ref}-x}$ represents the three-phase reference voltage components. The output voltage of each phase is only related to the reference voltage of that phase and the

TABLE IV
DIVIDING LINE

The dividing line of the main sectors	The dividing line of the subsectors
$L_1 = 0$	$l_1 = (-\sqrt{3}V'_{ref-\alpha} + \frac{\sqrt{3}(2-k)V_{dc}}{6})$
$L_2 = \sqrt{3}V_{ref-\alpha}$	$l_2 = \frac{\sqrt{3}(2-k)}{(2+3k)} * (V'_{ref-\alpha} - \frac{(2-k)V_{dc}}{6})$
$L_3 = -\sqrt{3}V_{ref-\alpha}$	$l_3 = \sqrt{3}(2-k)V_{dc}/12$
	$l_4 = \sqrt{3}(V'_{ref-\alpha} - 2V'_{ref-\gamma})/3$

value of k, and there is no coupling relationship with the other two phases

$$v_{\text{out}-x} = \left[1 + \text{sign}(v_{\text{ref}-x}) * \frac{k}{2}\right] * v_{\text{ref}-x} \quad (x = a, b, c). \quad (10)$$

Suppose the reference voltage $v_{\text{ref-}x} = |v_m| * \cos(\omega t + \theta_0)$, where $|v_m|$ is the amplitude and θ_0 is the initial phase angle. By combining the expression of k in (3) and substituting them into (10), the output voltages are obtained as

$$\begin{aligned} v_{\text{out}-x} = {} & |v_m| * \cos(\omega t + \theta_0) + \frac{|v_m|}{3\pi}[3K_1 \cos(\omega t + \varphi_1) \\ & + K_1 \cos(\omega t - \varphi_1 + 2\theta_0) + K_3 \cos(\omega t + \varphi_3 - 2\theta_0)] \\ & + \frac{|v_m|}{3\pi}[K_1 \cos(3\omega t + \varphi_1 + 2\theta_0) \\ & + 3K_3 \cos(3\omega t + \varphi_3)] \end{aligned} \quad (11)$$

where in addition to the reference voltage component, additional fundamental and third-harmonic components induced by oscillation are also superimposed.

III. Proposed 3D-SVPWM Based On Positive and Negative DC-Link Voltages Sampling

Based on the above analysis, it is known that when there is a large NPP oscillation, the output error of the traditional 3D-SVPWM is relatively large. Therefore, it is particularly important to relocate the position of the basic vectors through the real-time sampling values of positive and negative dc-link voltages for subsequent modulation calculations based on the 3D space vector diagram shown in Fig. 2(b).

A. Sector Division

In 3D-SVPWM, main sector division is performed using the projections of the basic space vectors onto the $\alpha\beta$-plane (denoted as V_α and V_β). Based on the dividing lines $L_1 - L_3$ specified in Table IV, the space vector diagram is partitioned into six main sectors on the $\alpha\beta$-plane, with the resulting division illustrated in Fig. 3(b). The main sector number N containing the reference vector is determined by the flowchart depicted in Fig. 4(a).

After determining the main sector number containing the reference vector, if it resides in main sectors $N2-N6$, its new coordinates after rotation to the first main sector are obtained according to (12). Furthermore, for reference vectors located

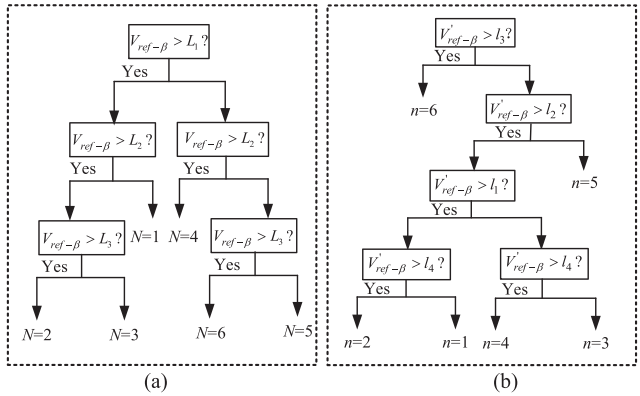

Fig. 4. Flowchart of sector division. (a) Flowchart of the main sector division. (b) Flowchart of the subsector division.

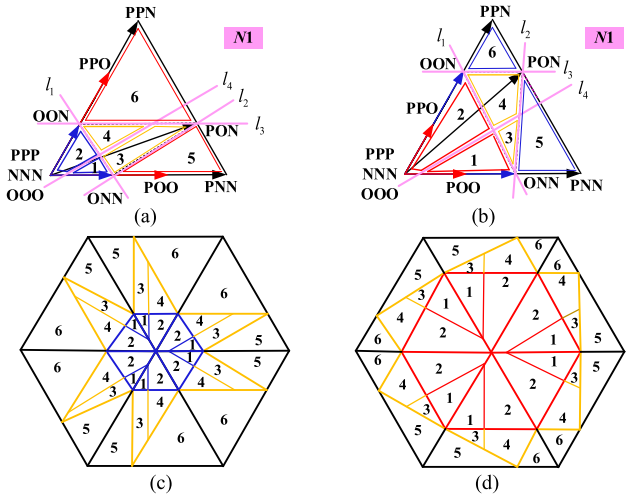

Fig. 5. Schematic diagram of subsectors division. (a) Main sector $N1$ with $k > 0$. (b) Main sector $N1$ with $k<0$. (c) Six main sectors with $k > 0$. (d) Six main sectors with $k<0$.

in even-numbered main sectors, a mirror transformation is additionally applied using (13) to obtain the final transformed coordinates

$$\begin{bmatrix} V'_{\text{ref}-\alpha} \\ V'_{\text{ref}-\beta} \end{bmatrix} = \begin{bmatrix} \cos(\frac{(N-1)\pi/3}{3}) & \sin(\frac{(N-1)\pi}{3}) \\ -\sin(\frac{(N-1)\pi}{3}) & \cos(\frac{(N-1)\pi}{3}) \end{bmatrix} \begin{bmatrix} V_{\text{ref}-\alpha} \\ V_{\text{ref}-\beta} \end{bmatrix} \quad (12)$$

$$\begin{bmatrix} V'_{\text{ref}-\alpha} \\ V'_{\text{ref}-\beta} \end{bmatrix} = \begin{bmatrix} 1/2 & \sqrt{3}/2 \\ -\sqrt{3}/2 & 1/2 \end{bmatrix} \begin{bmatrix} V'_{\text{ref}-\alpha} \\ V'_{\text{ref}-\beta} \end{bmatrix}. \quad (13)$$

Subsector division is performed based on the actual positions of the basic vectors rather than their ideally symmetric distribution ($k = 0$), which is illustrated using the first main sector as an example [25]. Initially, the first main sector is partitioned into four regions using auxiliary lines: line l_1 connecting the two negative small vectors, and lines l_2-l_3 connecting the negative small vectors to the medium vector V_{PON}, as shown in Fig. 5(a) and (b). Within the blue and yellow regions of Fig. 5(a) and (b), a further subdivision is implemented using line l_4, driven by the γ-axis component control requirement. (Note that l_4

TABLE V
BASIC VECTOR SELECTION IN THE FIRST MAIN SECTOR

Subsector number n	Basic vectors (V_1; V_2; V_3; V_4) in main sector $N1$	dwell time (t_1; t_2; t_3; t_4)
1	(V_{ONN}; V_{OON}; V_{OOO}; V_{POO})	(T_1; T_2; T_S-T_3-T_5; T_3+T_5-T_1-T_2)
2	(V_{OON}; V_{OOO}; V_{POO}; V_{PPO})	(T_3; T_S-T_3-T_5; T_4; T_5-T_4)
3	(V_{ONN}; V_{OON}; V_{PON}; V_{POO})	(T_1; T_S-T_1-T_5; -T_S+T_3+T_5; T_S-T_3)
4	(V_{OON}; V_{PON}; V_{POO}; V_{PPO})	(T_S-T_5; -T_S+T_1+T_5; T_S+T_1-T_3; T_3-2T_1)
5	(V_{ONN}; V_{PNN}; V_{PON}; V_{POO})	(T_S-T_5; T_S-T_1-T_5; T_2; -T_S+2T_5+T_1-T_2)
6	(V_{OON}; V_{PON}; V_{PPN}; V_{PPO})	(T_S-T_5; T_4; -T_S-T_1+T_3; T_S+T_5+T_1-T_3-T_4)

$$T_1=\frac{(V^{*}_{ref-\alpha}-\sqrt{3}V^{*}_{ref-\beta}-2V^{*}_{ref-\gamma})*T_S}{(1-0.5k)V_{dc}};T_3=\frac{(V^{*}_{ref-\alpha}+\sqrt{3}V^{*}_{ref-\beta}-2V^{*}_{ref-\gamma})*T_S}{(1-0.5k)V_{dc}}$$

$$T_2=\frac{2\sqrt{3}V^{*}_{ref-\beta}*T_S}{(1-0.5k)V_{dc}};T_4=\frac{(3V^{*}_{ref-\alpha}-\sqrt{3}V^{*}_{ref-\beta})*T_S}{(1+0.5k)V_{dc}};T_5=\frac{2(V^{*}_{ref-\alpha}+V^{*}_{ref-\gamma})*T_S}{(1+0.5k)V_{dc}}$$

is derived from time T_1 in Table V to prevent negative time calculation and avoid overmodulation.) Based on the rotated (and mirrored) coordinates of the reference vector, the subsector number containing its position is determined by the flowchart depicted in Fig. 4(b).

Subsector division in the other main sectors follows a similar approach. The schematic diagrams of all subsector divisions are provided in Fig. 5(c) and (d). When $k=0$ in Table IV, the subsector division of the proposed 3D-SVPWM is the same as that of the traditional 3D-SVPWM. In other words, the traditional 3D-SVPWM is a special case of the proposed 3D-SVPWM when the positive and negative dc-link voltages are equal.

B. Vector Selection and Time Calculation

Following the determination of the main and subsector numbers for the reference vector position, basic vectors are selected for application based on the nearest vector principle. The vector selection criteria and switching sequence for the first main sector are detailed in Table V. In 3D-SVPWM, the reference vector is synthesized using four basic vectors. Throughout the entire switching cycle, vector actions begin with a negative small vector, transitions to a positive small vector in the middle, and concludes with the same negative small vector. During each basic vector transition, only one phase changes its switching state. A seven-segment modulation scheme is adopted, wherein each phase changes its switching state twice per cycle, following either the O→P→O or N→O→N sequence.

The time calculation equations given in Table V are derived according to the exact magnitude and phase relationship of the basic vectors, and the dwell time of each basic vector can be calculated by bringing each axis component of the V_{ref}^{*} obtained after the transformation into the corresponding equations. The vector selection principle and time calculation formulas for the other main sectors are identical to those of the first main sector and are therefore omitted for brevity. The synthesis of V_{ref1} by the proposed 3D-SVPWM is taken as an example. The four basic vectors selected are the same as in Section II-B. The actual coordinates (8) of the four basic vectors are used to calculate the dwell time according to (5) and (6), and the result is shown as (14). The four basic vectors are output according to the times

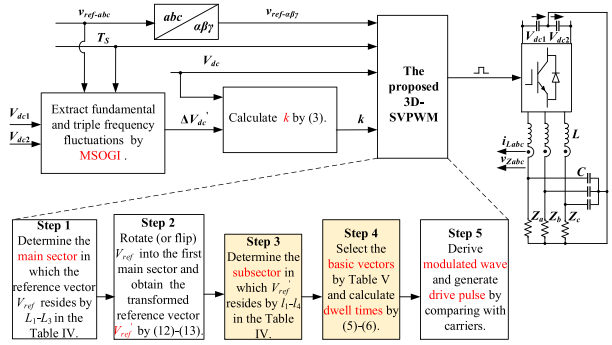

Fig. 6. Schematic diagram of the proposed 3D-SVPWM.

of (14), and thus the error caused by the NPP oscillation between the output vector and the reference vector is eliminated as

$$\begin{cases} t'_{\mathrm{ref1-1}}=t_{\mathrm{ref1-1}}+\frac{k(V_{\mathrm{ref1-\alpha}}+V_{\mathrm{ref1-\gamma}})*T_S}{(1+0.5k)*V_{\mathrm{dc}}} \\ t'_{\mathrm{ref1-2}}=t_{\mathrm{ref1-2}}+\frac{kT_S}{V_{\mathrm{dc}}}* \\ \left(\frac{(V_{\mathrm{ref1-\alpha}}-\sqrt{3}V_{\mathrm{ref1-\beta}}-2V_{\mathrm{ref1-\gamma}})}{2(1-0.5k)}-\frac{(V_{\mathrm{ref1-\alpha}}+V_{\mathrm{ref1-\gamma}})}{(1+0.5k)}\right) \\ t'_{\mathrm{ref1-3}}=t_{\mathrm{ref1-3}}+\frac{\sqrt{3}kV_{\mathrm{ref1-\beta}}*T_S}{(1-0.5k)V_{\mathrm{dc}}} \\ t'_{\mathrm{ref1-4}}=t_{\mathrm{ref1-4}}-\frac{0.5k(V_{\mathrm{ref1-\alpha}}+\sqrt{3}V_{\mathrm{ref1-\beta}}-2V_{\mathrm{ref1-\gamma}})*T_S}{(1-0.5k)V_{\mathrm{dc}}} \end{cases} . \quad (14)$$

The proposed 3D-SVPWM adaptively adjusts sector division and vector dwell time calculation based on real-time NPP feedback, compensating for voltage distortion caused by its oscillation. This results in more accurate output voltages and improved power quality.

C. NPP Oscillation Extraction and the Overall Schematic Diagram of the Proposed 3D-SVPWM

Fig. 6 shows the overall schematic diagram of the proposed 3D-SVPWM, and subsequent experiments were conducted based on it. $v_{\mathrm{ref}\text{-}abc}$ is the directly given reference voltage signal. To eliminate the influence of high-order harmonic components and the dc component caused by the unbalance of the capacitance parameters of the positive and negative buses, the ΔV_{dc} is processed by MSOGI to extract the fundamental and third-frequency components, which are then involved in the modulation process of the proposed 3D-SVPWM.

D. Comparison of Output Vectors Under the Two Strategies

In practical engineering, control delay also affects the output performance. Specifically, the V_{ref} applied for output at the current time is calculated using dc-link voltages sampled in the previous switching cycle, which introduces the error V_{error} between V_{out} and V_{ref} under the proposed 3D-SVPWM. Equation (15) shown at the bottom of the next page, provides the error expressions, denoted as V_t and V_p, for the traditional and proposed strategies, respectively. V_t is derived from Table III, where the variable k is defined as the bus unbalancing degree given in (3). The term k' in V_p is obtained from the difference of k over two adjacent switching cycles. Compared to k, each

TABLE VI
KEY PARAMETERS OF THE MAIN CIRCUIT

Parameters	Value
DC-link voltage V_{dc} /V	680
Positive and negative DC capacitance C_{dc} /μF	470
Switching frequency f_s /kHz	20
Fundamental frequency f /Hz	50
Filter inductance L /mH	1.28
Filter capacitance C /μF	20

component in k' exhibits a magnitude attenuation of ω/f_s (f_s is the switching frequency) and a phase advance of 90°. In other words, the compensation-based 3D-SVPWM strategy employing positive and negative dc-link voltages sampling is equivalent to changing the bus unbalancing degree from k to k' (though the actual circuit imbalance remains unchanged)

A concrete example of an output vector that considers both NPP oscillation and control delay is given below. Assume the following prerequisites: $V_{\text{ref}} = 311*(\cos(100\pi t); \sin(100\pi t), 0)$; and $k = 0.13\cos(100\pi t+\pi/2) + 0.013\cos(300\pi t+3\pi/4)$, as shown in Fig. 7(a) and (d); and f_s is 20 kHz. At this time, the amplitude and each axis component of the output vector V_{out} under the traditional and proposed strategies are shown in Fig. 7(b) and (c). Under the traditional 3D-SVPWM, the amplitude and the component of the γ axis of V_{out} have obvious fluctuations and deviate from the reference value. As shown in Fig. 7(e) and (f), the error V_{error} under the traditional modulation strategy is much larger than that under the proposed 3D-SVPWM, where all errors are solely attributed to control delay.

IV. EXPERIMENTAL RESULTS

A. Experimental Platform

In this article, a 5 kVA 3P4W-3L T-type converter prototype is built for experimental verification as shown in Fig. 8, whose parameters are given in Table VI. A 5 kW programmable dc power supply is connected to the dc side bus of the inverter, and a three-phase *LC* filter is connected to the ac side, with its NPP connected to the NPP of the dc-link. According to the experimental requirements, filter capacitors of each phase are connected in parallel with the load or left unloaded.

B. Analysis of Steady-State Experimental Results

Under the first operating condition, a purely resistive load of 34 Ω is connected to phase A while phases B and C remain unloaded ($Z_a = 34\ \Omega$, $Z_b = Z_c = +\infty$). Fig. 9 shows the waveforms of the positive and negative dc-link voltages, A-phase output voltage and inductor current when the reference voltage amplitude increases from 68 to 311 V and stabilizes (with the modulation index gradually rising from 0.2 to 0.915). Throughout the modulation index variation process, both modulation strategies sustain stable system operation without instability. When the reference voltage remains constant at 311 V, the peak value of ΔV_{dc} measures 45.5 V, with its fundamental component leading the A-phase voltage by 90° as shown in Fig. 9(b).

Fig. 10 shows the waveforms of output voltages v_{Zabc} and neutral-line current i_n under the traditional and proposed 3D-SVPWM when the reference voltage amplitude remains at 311V. By comparing voltage waveforms, it can be found that the three-phase unbalance factor of the output voltages under the traditional strategy is relatively high and the distortion is severe. The three-phase output voltages of the proposed strategy are more symmetrical and have a better sinusoidal degree.

As shown in Fig. 11, spectral analysis of three-phase output voltages reveals that the proposed 3D-SVPWM achieves over 75% third-harmonic reduction and up to 46% THD reduction (e.g., the THD of A-phase voltage is reduced from 3.11% to 1.77%). However, due to the open-loop control configuration, affected by the control delay described in Section III-D, voltage division across filter inductors, and voltage drops of switching devices, the output voltage amplitude of the loaded phase A is lower than the reference value; while the unloaded phases B and C have slightly elevated output voltages due to the capacitance rise effect. This results in the maximum amplitude difference between phase voltages being reduced from 27.1 V under the traditional strategy to only 18.2 V under the proposed strategy, instead of 0 V. Although perfect three-phase voltage balance is not achieved, both voltage unbalance and harmonic distortion are significantly lower than those of the traditional strategy, consistent with theoretical analysis.

Under the second operating condition, symmetric purely resistive loads are connected to phases A and B with phase C unloaded ($Z_a = Z_b = 34\ \Omega, Z_c = +\infty$). As observed in Fig. 12(a), ΔV_{dc} peaks at 58.4 V, with its fundamental component leading the A-phase voltage by 30°. Comparisons of output voltage waveforms in Fig. 12(b) and (c) confirm that under this operating condition, the proposed strategy improves three-phase power quality compared with the traditional strategy, where the sinusoidal degree of B-phase voltage is significantly better and the amplitude difference between phase voltages is reduced.

Under the third operating condition, a resistive-inductive (*RL*) load is connected to phase A ($Z_a = 36+j15.5\ \Omega$) with phases B and C unloaded (see Fig. 13). It has a measured power factor of 0.92, output power of about 1100 W, and an approximate 25.60° phase lead of A-phase voltage over current. Compared with the traditional strategy, the proposed strategy reduces the THD of A-phase current from 3.28% to 1.93%, and its three-phase voltage balance is superior to that of the traditional strategy.

$$\begin{cases} V_{\text{error\_}t} = \frac{k}{6}V' & k = K_1\cos(\omega t+\varphi_1) + K_3\cos(3\omega t+\varphi_1) \\ V_{\text{error\_}p} = \frac{k'}{6}V' & k' = k(t) - k(t-1) \approx -\frac{\omega}{f_s}[K_1\cos(\omega t+\varphi_1-\frac{\pi}{2}) + \\ & +3K_3\cos(3\omega t+\varphi_3-\frac{\pi}{2})] \end{cases} \quad (15)$$

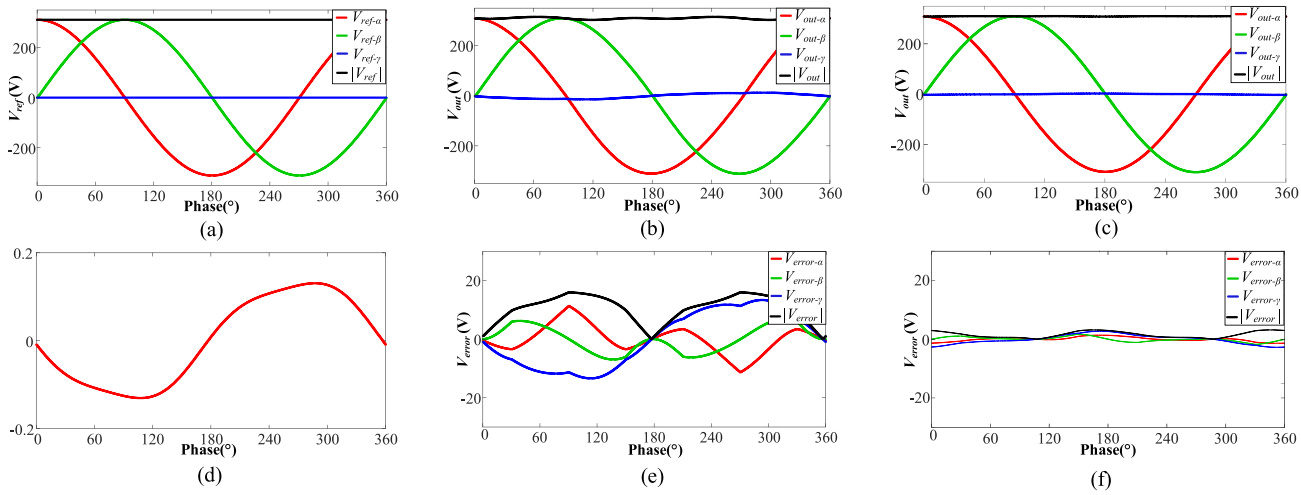

Fig. 7. Comparison of the output effects under the two modulation strategies. (a) V_{ref}. (b) V_{out} (the traditional 3D-SVPWM). (c) V_{out} (the proposed 3D-SVPWM). (d) k. (e) V_{error} (the traditional 3D-SVPWM). (f) V_{error} (the proposed 3D-SVPWM).

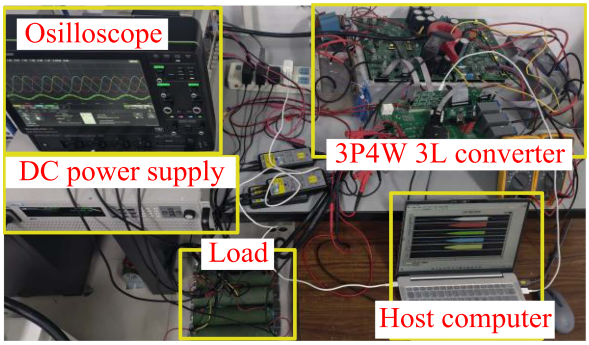

Fig. 8. Experimental setup of a 5kVA 3P4W-3L converter.

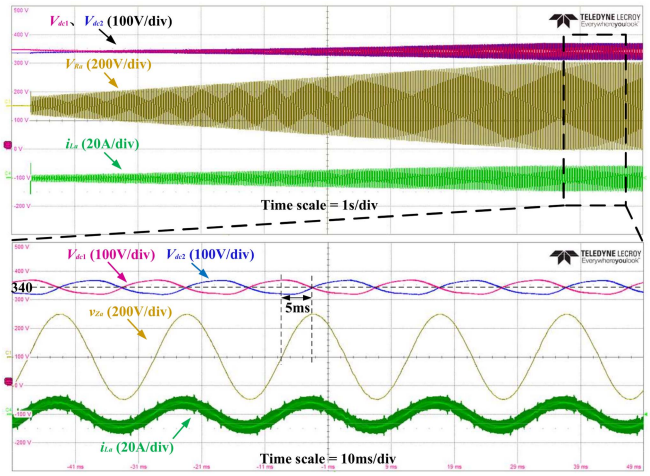

Fig. 9. Oscillation of positive and negative DC-link voltages.

Qualitative waveform improvements are evident above. Quantitative spectral analysis results under three operating conditions (see Table VII) demonstrate that compared to the traditional strategy, the proposed 3D-SVPWM.

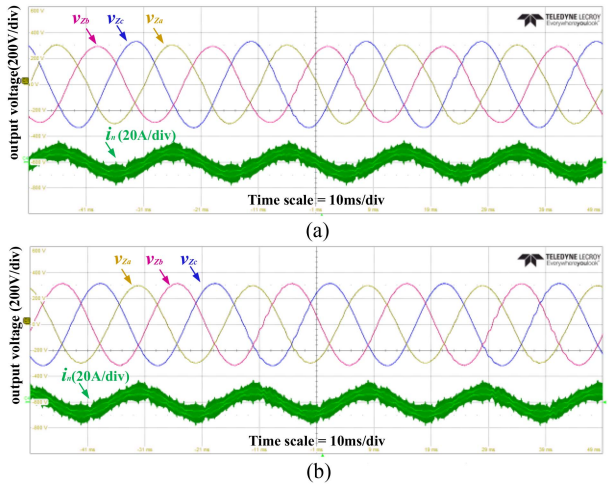

Fig. 10. Under a single-phase purely resistive load. (a) Three-phase output voltages under the traditional 3D-SVPWM. (b) Three-phase output voltages under the proposed 3D-SVPWM.

1) Significantly enhances voltage balance with 32.8%, 52.4%, and 34.9% reductions in maximum amplitude difference between phase voltages under three operating conditions respectively.
2) Achieves over 70% suppression of third-harmonic content, nearly reducing its amplitude from 5–7 V to almost below 2 V.
3) Substantially reduces harmonic content (46.5% decrease in A-Phase THD under purely resistive load, 48.8% THD reduction on phase B under two-phase resistive load, 35.7% THD reduction on phase A under a *RL* load).

C. Analysis of Dynamic Experimental Results

v_{Zabc} and i_n under the two strategies of the system operating from no-load to only phase A with a purely resistive load of 34 Ω are shown in Fig. 14. Under the traditional 3D-SVPWM,

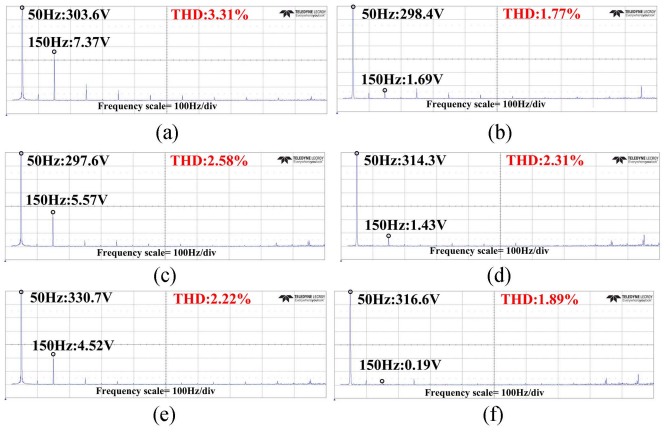

Fig. 11. Frequency spectrums comparison of output voltages. (a) Phase A (the traditional SVPWM). (b) Phase A (the proposed SVPWM). (c) Phase B (the traditional SVPWM). (d) Phase B (the proposed SVPWM). (e) Phase C (the traditional SVPWM). (f) Phase C (the proposed SVPWM).

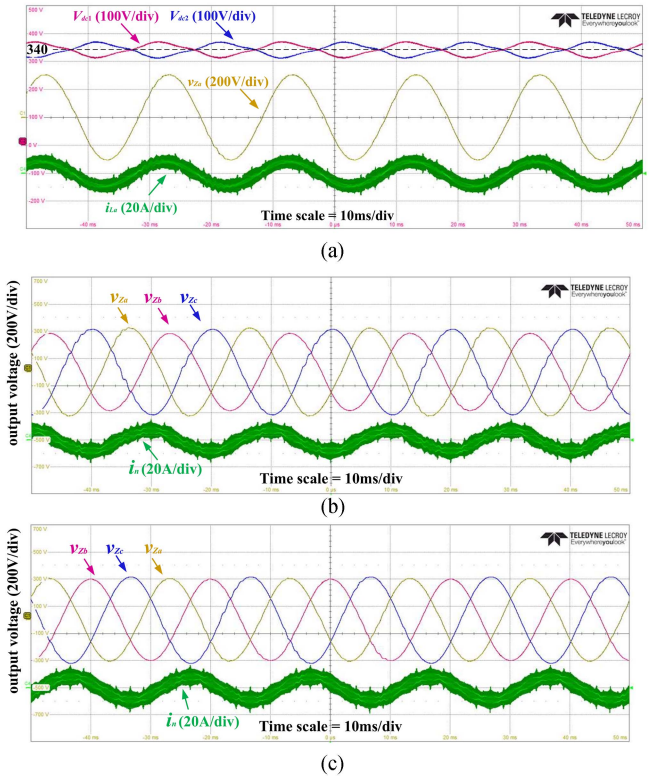

Fig. 12. Under symmetrical purely resistive loads on two phases. (a) Oscillation of positive and negative DC-link voltages. (b) Three-phase output voltages under the traditional 3D-SVPWM. (c) Three-phase output voltages under the proposed 3D-SVPWM.

when a single-phase load is added, the output voltages are severely asymmetrical and the sinusoidal degree is poor. Using the proposed strategy, the output voltage waveforms change less before and after the load change. The settling time to reach the new steady state is 0.05 s, consistent with the traditional strategy. In the new steady state, only the amplitude of A-phase voltage has dropped due to reasons, such as voltage division.

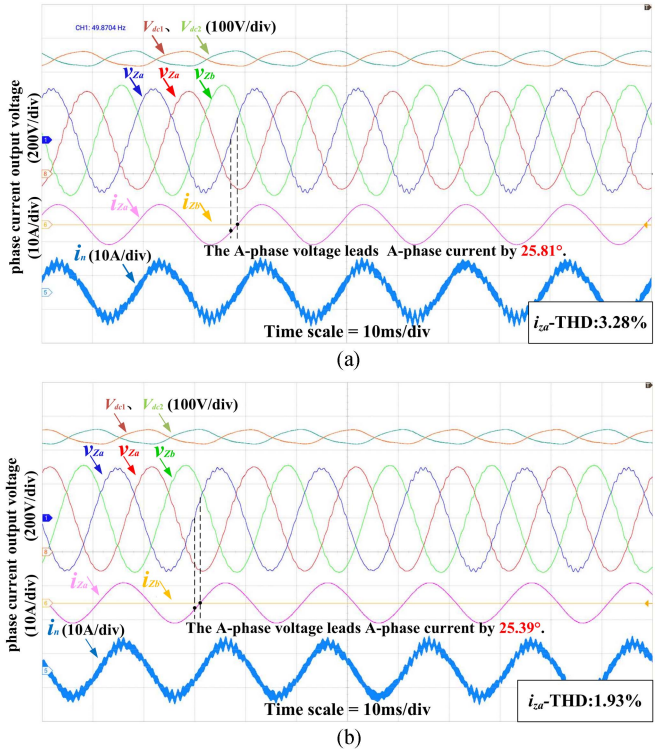

Fig. 13. Under a single-phase *RL* load. (a) Voltage and current waveforms under the traditional 3D-SVPWM. (b) Voltage and current waveforms under the proposed 3D-SVPWM.

TABLE VII
OUTPUT VOLTAGE COMPARISON UNDER TWO STRATEGIES

Operating condition	Measurement index	Modulation strategy	Phase A	Phase B	Phase C
Z_a=34Ω Z_b=Z_c=+∞	Amplitude of the fundamental voltage /V	traditional	303.6	297.6	330.7
		proposed	298.4	314.3	316.6
	Amplitude of the third-harmonic voltage /V	traditional	7.37	5.57	4.52
		proposed	1.69	1.43	0.19
	THD	traditional	3.31%	2.58%	2.22%
		proposed	1.77%	2.31%	1.89%
Z_a=Z_b=34Ω Z_c=+∞	Amplitude of the fundamental voltage /V	traditional	321.3	287.8	316.1
		proposed	304.9	301.4	317.5
	Amplitude of the third-harmonic voltage /V	traditional	7.84	7.12	5.74
		proposed	3.76	1.78	1.63
	THD	traditional	3.17%	3.24%	3.02%
		proposed	2.44%	1.66%	2.14%
Z_a=36+*j*15.5 Ω Z_b=Z_c=+∞	Amplitude of the fundamental voltage /V	traditional	303.8	296.1	325.3
		proposed	301.7	312.3	315.5
	Amplitude of the third-harmonic voltage /V	traditional	6.39	5.51	5.15
		proposed	1.35	0.51	0.59
	THD	traditional	3.47%	2.38%	2.66%
		proposed	2.25%	2.02%	1.90%

v_{Zabc} and i_n of the system under two modulation strategies, from operating with three-phase symmetrical loads (all three phases are purely resistive loads of 34 Ω) to removing the A-phase load, are shown in Fig. 15. Using the proposed modulation strategy, the output voltage waveforms also exhibit smaller changes before and after the load change, which is

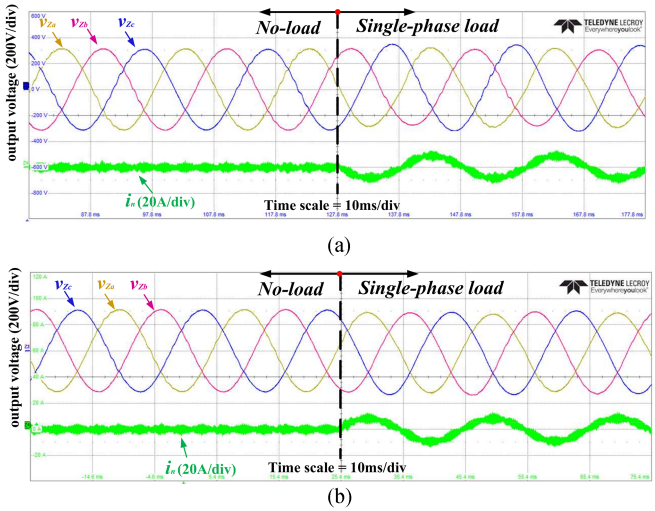

Fig. 14. Transition from three-phase no-load to only A-phase load. (a) Three-phase output voltages under the traditional 3D-SVPWM. (b) Three-phase output voltages under the proposed 3D-SVPWM.

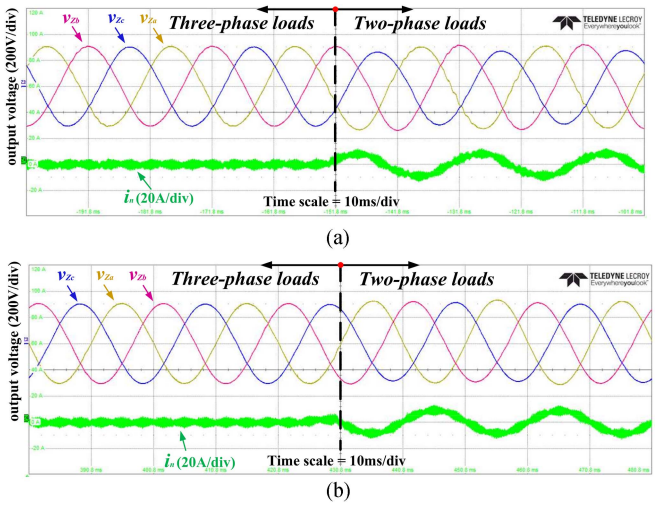

Fig. 15. Transition from three-phase symmetrical loads to no-load on phase A. (a) Three-phase output voltages under the traditional 3D-SVPWM. (b) Three-phase output voltages under the proposed 3D-SVPWM.

significantly better than the traditional strategy. The dynamic response time measures approximately 0.03 s. Compared to the traditional 3D-SVPWM, the proposed strategy reduces the maximum amplitude difference between phase voltages during transients from over 40 V to approximately 20 V under the above two operating conditions. Upon reaching the new steady state, only the A-phase voltage amplitude exhibits an increase.

D. Efficiency and Computation Time Comparison

System efficiency under both modulation strategies was measured using a ZIMMER LMG571 power analyzer. As given in Table VIII, under both single-phase resistive and *RL* loads, the efficiency difference between traditional and proposed 3D-SVPWM is less than 0.1% (peak delta: 0.06%). Synchronous variations in input and output power confirm consistent loss distribution characteristics, with the proposed algorithm introducing no additional power losses to the system.

TABLE VIII
SYSTEM EFFICIENCY COMPARISON UNDER TWO STRATEGIES

Operating condition	Modulation strategy	Input power /W	Output power /W	Efficiency
Single-phase purely resistive load ($Z_a = 40\ \Omega$)	traditional	1265.25	1215.93	96.10%
	proposed	1208.31	1161.66	96.14%
Single-phase *RL* load ($Z_a = 36 + j15.5\ \Omega$)	traditional	1127.21	1081.43	95.94%
	proposed	1156.62	1110.36	96.00%

The CPU execution times of both strategies were measured using the HPMicro-HPM6754 chip. The I/O port is set to logic-high at the beginning of the algorithm and to logic-low at the end. As depicted in Fig. 6, the computational stages of the proposed strategy comprise reference signal generation, bus voltage fluctuation extraction, and modulation calculation, whereas the traditional strategy excludes the fluctuation extraction stage. The average execution times for the proposed and traditional strategies measure 8.68 and 6.15 μs, respectively. Although the computational burden of the proposed method is higher than that of the traditional strategy, it remains substantially below 50 μs (a switching cycle) with sufficient computational resources available.

V. CONCLUSION

This article proposes a compensation-based 3D-SVPWM strategy to address the issue of poor modulation performance in 3P4W-3L converters under asymmetrical loads, caused by NPP oscillation. Compared to modulation strategies that reposition vector locations in the 2D plane for 3P3W topologies, this strategy constructs a 3D space vector diagram through real-time sampling of positive and negative dc-link voltages. Its subsector division and vector dwell-time calculations fully account for NPP oscillation characteristics. The following conclusions are drawn from experiments:

First, compared with the traditional strategy, the proposed 3D-SVPWM significantly improves voltage balancing performance under severely asymmetrical load conditions, achieves 41.4% average reduction in maximum amplitude difference between phase voltages, substantially reduces third-harmonic components (with 76.6% average reduction) and effectively lowers THD (29.4% average decrease), thereby enhancing power quality and ensuring reliable operation of connected loads. Moreover, the system under the proposed 3D-SVPWM exhibits excellent dynamic performance, as the three-phase output voltages exhibit less distortion with settling times of 0.03–0.05 s during abrupt load changes, highlighting its robustness. Finally, system efficiencies remain comparable between the two strategies. Although computational overhead increases under the proposed strategy, the execution time remains well below the control period duration. However, it ensures effective performance only when positive and negative dc-link voltages exceed the reference amplitude, which reflects its limitation and renders it unsuitable for scenarios with excessively small dc-link capacitances.

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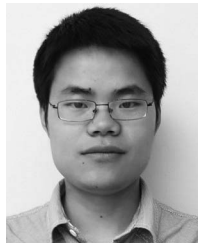

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