Ultralocal Model-Free Pulse-Frequency-Modulation of a Bidirectional Resonant DC-DC Converter for V2G System

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***Abstract*—CLLLC-type dc–dc converter (abbreviated as CLLLC converter) has drawn significant attention due to its capability to step-up and step-down voltage in both forward and reverse operation directions, while maintaining consistent operating characteristics, soft-switching across the full-load range, and high efficiency. Conventional control methods, such as proportional-integral regulator, are widely used due to their simple structure and straightforward principles. However, these approaches heavily depend on the model accuracy, which may lead to suboptimal performance in the presence of parameter mismatches and disturbances. To overcome this limitation, this article proposes a comprehensive control framework for voltage closed-loop regulation and introduces an ultralocal model-free pulse-frequency modulation (UMF-PFM) approach. In this framework, the frequency and output voltage are used as variables in frequency modulation. This enables the identification of the unknown nonlinear term of the system, which encapsulates all relevant structural information. By adjusting the frequency, the controller's performance remains robust, reducing its dependence on model accuracy. Simulation and experimental results demonstrate that, the UMF-PFM shows better stability against parameter mismatches and perturbations on the primary side of the dc–dc converter compared to existing PFM and PSM methods, which are affected by less than 1 V of the output voltage under the same conditions.**

***Index Terms*—Bidirectional CLLLC resonant converter, bidirectional dc–dc converter, pulse frequency modulation, ultralocal model-free control.**

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I. Introduction

VEHICLE-TO-GRID (V2G) technology plays a pivotal role as a core component by realizing bidirectional transmission and efficient configuration of energy, and its applications widely cover many fields such as electric vehicles, renewable energy systems, and power electronic transformers [1], [2], [3], [4], [5]. The applications in electric vehicles are shown in Fig. 1. Among the isolated bidirectional dc–dc converters, the CLLLC converter has received more and more attention because of its natural soft switching, large voltage regulation range, and simple control strategy [6]. This converter can realize bidirectional power transfer, and its symmetrical circuit structure not only ensures the consistency of bidirectional operation, but also maintains the same soft-switching characteristics as that of the *LLC* resonant converter in both forward and reverse operation [7], [8], [9], [10]. The CLLLC converter is well-suited for on-board charging and discharging dc–dc modules. However, in various practical scenarios, such as high temperature conditions or component aging, the system parameters may vary, leading to deviations in the actual mathematical model. In these cases, traditional control strategies, which heavily rely on precise models, tend to perform poorly when the model undergoes changes. As a result, minimizing the dependence of control systems on accurate models has become a crucial area of current research.

Recently, model-free-control (MFC) has gained increasing attention in the fields of power electronics and diversified motor drive systems. These methods are centered around the fundamental principle of reducing or eliminating the reliance on the system model, or at least mitigating its influence during the prediction process. Existing MFC techniques can be categorized into three primary groups based on the extent to which they are model-free, providing a deeper understanding and enabling a more thorough analysis of their applicability and performance [11].

The first category are predictive corrections. Predictive corrections are methods that exclusively use an ideal system model. It consists of two methods. Method one compensates the prediction by estimating some correction factors by utilizing the

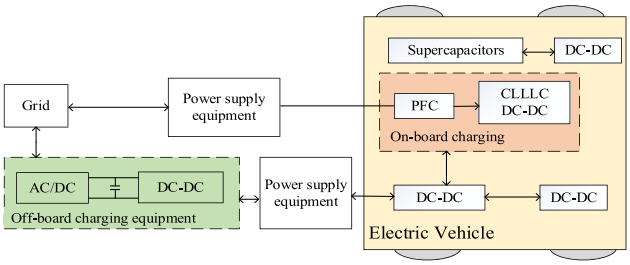

Fig. 1. Structure of V2G.

inputs, outputs, and previous prediction data of the system [12]. The correction can be done by modifying the ideal prediction model using a nominal reference ideal model. In study [13], the stator current, rotor speed, rotor position, and mechanical torque of a variable-speed wind turbine system were estimated by employing an extended Kalman filter. Another method is to compensate for the control inputs that will be applied to the control device in future sampling cycles. In study [14], inductor robustness to the divergence caused by stator inductor mismatch was enhanced by employing an extended state observer (ESO). In studies [15] and [16], an improved sliding-mode scheme based on differential beatless predictive current control (DPCC) was proposed by designing a unified higher order sliding mode observer for estimating perturbations and uncertainties in the speed and current loops. In [17], a static error DPCC using a second-order sliding-mode disturbance observer was proposed. In study [18], a combined observer based on a sliding-mode observer and Lemberger observer was designed to simultaneously observe the next compensation voltage and current predictions.

The second category is hyper-local model-free control, which is essentially an extension of traditional MFC through hyper-local modeling. Its lies in constructing a model framework that includes one or more unknown parameters, which are then determined through iterative optimization of system input/output. These parameters are eventually applied to the predictive aspect of the control system to optimize control performance, as shown in study [19]. It is worth noting that such methods skillfully circumvent the limitations of traditional methods relying on lookup tables, especially the problem of lagging update of lookup tables, and thus improve the real-time response capability and prediction accuracy of the system. In study [20], an continuous voltage vector model-free predictive current controller for surface mount permanent magnet synchronous motor (PMSM) was proposed. On the other hand, an improved model-free predictive current control based on an extended state observer, which did not require a priori knowledge of the motor parameters, was proposed in study [21]. In study [22], to achieve sinusoidal grid currents and a constant active power even under an unbalanced and distorted grid, a robust predictive current control for a pulsewidth modulation (PWM) rectifier was proposed. Additionally, in study [23], a robust predictive current control scheme based on the ultralocal model for *LCL*-filtered PWM rectifiers was proposed.

The third classification pertains to model-free predictive control, wherein the predictive process eschews dependence on system models and instead directly leverages historical input and output data of the system. For instance, in study [24], the historical data are systematically cataloged within a look-up table (LUT), serving as the fundamental cornerstone for prediction. In study [25], the duration of each voltage vector and the voltage prediction are calculated based on the updated voltage differences, so as to remove the impact of parameter variation on duration and prediction calculation, enabling their robustness. In study [26], a novel model-free predictive current control method, which centers on tracking and recording the current changes associated with the feedback voltage vector in real time and storing this dynamic information in the LUT, was contributed. By efficiently retrieving the LUT entries matching the current voltage vector, accurate prediction of future current states was realized. In study [27], a new model-free predictive current control which was insensitive to parameter variations of the electric machines, was proposed to drive the PMSM aiming at six-phase current error reduction within 0.36 A. In study [28], a transfer methodology via a delicately designed duty ratio mapping was proposed for a dc–dc buck converter. Then, a detailed sim-to-real process was presented to enable the implementation of a model-free deep reinforcement learning controller. In study [29], a novel data-driven model-free disturbance rejection control architecture was proposed for the output voltage regulation of dc–dc converters without model priori information. In study [30], a novel hybrid parallel-cascade ESO was proposed for dc–dc boost converter, which has better measurement noise suppression than conventional linear ESO.

As a traditional control strategy, pulse frequency modulation (PFM) relies heavily on precise mathematical models, and its performance deteriorates when there are model mismatches. Moreover, under the low output voltage and light load condition, the PFM control may fail because of the parasitic effect under high-frequency operation. Furthermore, existing research has not specifically targeted the CLLLC converter [27], [31], [32], [33]. To overcome the limitations of traditional control methods, which perform poorly under parameter mismatches and external disturbances, an ultralocal model-free pulse-frequency-modulation (UMF-PFM) approach is proposed. In short, the main contributions of this study are summarized as follows.

1) The working principle of CLLLC converter is analyzed, additionally, the advantages and disadvantages of PFM are discussed.
2) A UMF-PFM strategy is proposed. This strategy utilizes variable frequency and output voltage as modulation variables, enabling wide range voltage transmission. By adjusting the operation frequency, the unknown nonlinear terms of the system are addressed, improving the system robustness. Different with existing methods, this approach significantly reduces the reliance on precise modeling, enhancing system flexibility.
3) Experimental comparison results are presented, demonstrating that the UMF-PFM outperforms existing PFM and PSM methods in terms of parameter mismatch, load variations and perturbations.

The structure of this article is arranged as follows. In Section I, an overview of the research background of the CLLLC converter

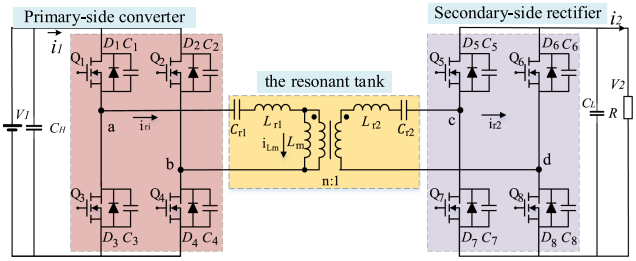

Fig. 2. Topology of a CLLLC converter.

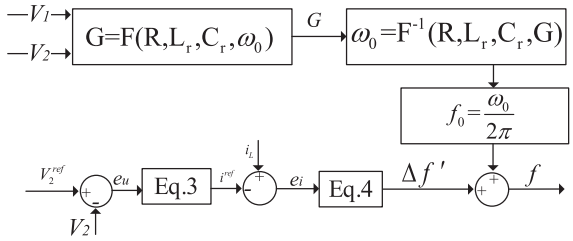

Fig. 3. Control block diagram of PFM.

and its research significance are discussed. Section II introduces the basic working principle. In Section III, an ultralocal model-free control (UMF-PFM) based on inverter modulation is proposed. The control system for the bidirectional dc–dc converter is designed. Then, in Section IV, the proposed theory is validated by constructing a simulation model, and results are highly consistent with the theoretical analysis. In Section V, it is verified in the hardware setup of a 6.6-kW CLLLC converter, and the verification results are consistent with the simulation results and the theoretical analysis. Finally, Section VI concludes this article.

II. Working Principle and PFM Modulation of the CLLLC DC–DC Converter

A. Power Circuit and Operation Mode of CLLLC Converter

Fig. 2 illustrates the topology of a CLLLC converter, which comprises three main components: the inverter full bridge, the resonant network, and the rectifier full bridge. Based on the switching frequency characteristics of the topology, the operating modes can be precisely classified into four distinct categories.

Mode I: Low-frequency mode ($f_s < f_m$), f_s has a switching frequency below the frequency threshold f_m of the primary-side inductance L_{r1}, capacitance C_{r1} and excitation inductance resonance L_m, $f_m = \frac{1}{2\pi\sqrt{(L_{r1}+L_m)C_{r1}}}$. In this mode, the CLLLC converter exhibits dominant capacitive characteristics, resulting in hysteresis between the inductor voltage and inductor current. Specifically, when the power transistor is driven by the excitation voltage, zero voltage switching (ZVS) cannot be achieved due to the nonzero voltage present on both sides of the diode. This limitation restricts the suitability of this mode for soft-starting.

Mode II: Under-resonant mode ($f_m < f_s < f_r$), $f_r = \frac{1}{2\pi\sqrt{L_{r1}C_{r1}}}$, in which the CLLLC converter exhibits inductive. Diametrically opposite to mode I, the inductor voltage exceeds the inductor current. During the conduction state of the power transistor, the diode is already preconducted, clamping the voltage of the switching transistor at zero potential, thus realizing zero-voltage turn-ON (ZVS). Furthermore, when the circuit containing the excitation inductor reaches a resonant state, the excitation inductor voltage is fixed, $i_{Lm} = i_{r1}$, the energy transfer is terminated from the primary to the secondary side, and the diode current gradually decays to zero, realizing a zero-current turn-OFF (ZCS). Considering the realization of ZVS and zero-current-switching (ZCS) in this mode, it is often chosen as the preferred operation mode.

Mode III: The critical resonant mode ($f_m < f_s = f_r$), which is characterized by a normalized frequency of exactly 1, when the equivalent impedance of the resonant loop is zero. In this condition, the input voltage is directly applied across the transformer terminals, minimizing power losses and causing the operating frequency to reach its peak. At this point, the voltage gain is fixed at 1, and the quality factor has no influence on the voltage gain, indicating that the converter is operating at its ideal efficiency state.

Mode IV: Over-resonance mode ($f_m < f_r < f_s$), the resonant circuit in this mode shows inductive impedance characteristics, although its operating state shares similarities with the under-resonance mode, the high switching frequency limits the resonance to the initial stage. As a result, the excitation inductor does not participate in the resonance, leading to a mismatch between the resonant inductance and the excitation inductance currents. Consequently, the energy transfer on both sides of the transformer cannot be effectively interrupted, preventing the rectifier from achieving zero-current turn-OFF. Instead, the diode itself achieves zero-current shutdown.

Through the above analysis among the four working modes., the under- and the critical-resonant states are the most ideal working states, and the converter needs to work in these two states to maintain a high efficiency. The common control method for traditional CLLLC converter is frequency-modulation, i.e., the duty cycle of the switching trigger pulse is 50%, and the output voltage of the converter is adjusted by the switching frequency.

B. Pulse-Frequency-Modulation and Its Limitations

Pulse-frequency modulation (PFM) is employed to maintain a constant pulsewidth of the drive signal while dynamically adjusting the pulse frequency. This strategy is referred to as "fixed-width frequency modulation." Specifically, when the output voltage fluctuates, the system built-in feedback loop intervenes promptly to precisely adjust the pulse frequency. It is important to note that PFM can be further classified into two methods: one that focuses on adjusting the duration of the high-level portion of the drive signal, and another that focuses on the duration of the low-level portion. Each method has its distinct emphasis, together contributing to the diversity of PFM modulation.

Fig. 3 shows the PFM control block diagram, where f is the controlled switching frequency, V_1 and V_2 represents the input

and output voltage of the CLLLC converter, G is the voltage gain and i_{L} is the load current. V_2^{ref} is the reference of the output voltage. $i_{2\mathrm{ref}}$ is the current reference. The feedforward frequency f_0 is calculated by using the gain inversion. f_0 is not applied sufficiently to offset the static error between the measured dc-bus voltage and its reference due to the assumption of parameter simplification. The PI controller with output Δf will be added to f_0 until the static voltage error tolerance of the dc bus voltage is acceptable.

The simplified model is obtained by analyzing the fundamental wave, which leads to $R_{\mathrm{eq}} = n^2\ R$, $C'_{r2} = \frac{C_{r2}}{N^2}$, $L'_{r2} = n^2\ L_{r2}$. n is the transformer ratio. ω is the angular frequency of the current i_{r1}. Thus, the impedance Z_1, Z_2, and Z_m can be derived as follows:

$$\begin{cases} Z_1 = L_{r1}\omega j + 1/\left(C_{r1}\omega j\right) \\ Z_m = L_m \omega j \\ Z_2 = L_{r2}{}'\omega j + 1/\left(C_{r2}{}'\omega j\right) \end{cases}. \tag{1}$$

The voltage gain G is derived as follows:

$$G = \frac{Z_m || \left(Z_2 + R_{\mathrm{eq}}\right)}{n(Z_1 + Z_m || \left(Z_2 + R_{\mathrm{eq}}\right))} \frac{R_{\mathrm{eq}}}{Z_2 + R_{\mathrm{eq}}}. \tag{2}$$

The equation of the PI controller for output voltage regulation is shown as follows:

$$e = K_{Pu}{}' e_u + K_{Iu}{}' \int e_u dt. \tag{3}$$

The PI controller for current regulation is shown as follows:

$$\Delta f\prime = K_{Pi}\prime e_i + K_{Ii}\prime \int e_i dt \tag{4}$$

where $K_{Pu}\prime$ and $K_{Iu}\prime$ are the parameters of the voltage controller. $K_{Pi}\prime$ and $K_{Ii}\prime$ are the parameters of the current controller.

C. Limitation Analysis of PFM

In dc–dc conversion architectures that involve mode switching, PFM is particularly prevalent due to its significant advantages in terms of superior efficiency and excellent frequency response under light load. Compared to PWM with the same peripheral configuration, PFM achieves notably better efficiency, particularly up to the peak efficiency point, which constitutes PFM's core advantage under certain operating conditions. However, as the load increases, the efficiency advantage of PFM gradually diminishes and may even become significantly lower than that of PWM. This is primarily due to the dispersion and irregularity of the output ripple spectrum in PFM mode, which complicates the filter circuit design. The irregular ripple characteristics necessitate the adoption of more sophisticated strategies to manage ripple effectively.

While PFM mode, with its unique fixed-width frequency modulation mechanism, offers substantial benefits in light-load efficiency and frequency response, it presents limitations in heavy-load conditions and filtering design. These factors must be carefully considered in practice. Additionally, as a traditional control strategy, PFM requires precise mathematical models of the converter, and its performance may degrade significantly if model mismatches occur in CLLLC converter.

III. UMF-PFM Controller for CLLLC Converter

A. Preliminaries of UMF-PFM Controller

Given the high likelihood that modern systems are highly nonlinear or time-varying, UMF-PFM does not rely on any modeling procedure. The advantages of the UMF-PFM approach are more pronounced compared to traditional methods. In this approach, a novel ultralocal model is employed to decompose the system into its linear part, which is represented by the system's state variables, and the unknown nonlinear term. The input–output behavior of the system is governed by a finite-dimensional ordinary differential equation, which, in its operating range, is often nonlinear. This relationship can be expressed as follows:

$$E(t, y, y', \ldots, y^{(a)}, u, u', \ldots, u^{(k)}) = 0 \tag{5}$$

where E is a sufficiently smooth function of its argument. Suppose that for some integer n, $0 < n \leq$ a, $\frac{\partial E}{\partial y^{(n)}} \not\equiv 0$. y is the measured dc bus voltage. The implicit function theorem then arises locally. u is the control input and y is the system output. This complex nonlinear system can be replaced in a very short time interval by the following hyperlocal model:

$$y^{(v)}(t) = L + \alpha u(t). \tag{6}$$

This equation is based on the description of a SISO system, where $y^{(v)}$ is the derivative of y of order v, where v is the relative degree of the system. $v = 1$ contains all the structural information, which depends on the other variables of the system (including perturbations and nonlinearities). $\alpha \in \mathrm{R}$ is a nonphysical constant parameter chosen by the engineer in the same way as L and α magnitude, and L is determined due to the knowledge of the estimated u, α, and $y^{(v)}$.

B. Design and Implementation of UMF-PFM Controller

The system discussed can be written as follows:

$$u(t) = \frac{1}{\alpha}\left[y^{*(v)}(t) - \tilde{L} + R(e(t))\right] \tag{7}$$

where $y^*$is the reference, $y^{*(v)}$ is the v-order derivative of the reference trajectory, R is a classical PI regulator, $\tilde{L}$ is the instantaneous estimated L of the hyperlocal model, and e is the frequency tracking error. The voltage outer-loop PI control equation is shown as follows:

$$e = V_2{}^* - V_2 \tag{8}$$

$$R(e(t)) = K_{Pu} e(t) + K_{Iu} \int e(t) dt \tag{9}$$

where $V_2{}^*$ represents the reference trajectory of the output voltage. The complex nonlinear CLLLC system can then be simplified by taking $v = 1$, with the equations as follows:

$$\dot{V}_2 = L + \alpha f(t) \tag{10}$$

where $\dot{V}_2$ is the first-order derivative of V_2 and $f(t)$ is the operation frequency. Therefore, the instantaneous estimation of

the coefficient $L(t)$ can be obtained from (7) as follows:

$$\tilde{L} = [\dot{V}_2]_e + \alpha f(t-h) \tag{11}$$

where $f(t-h) = u(t) + \mathrm{R(e(t))}$, $\tilde{L}$ is the instantaneous estimated value of L, and $[\dot{V}_2]_e$ can be obtained using the Euler derivative of the first-order approximation (h is the step-size)

$$[\dot{V}_2]_e = \frac{V_2(t) - V_2(t-h)}{h}. \tag{12}$$

At this point, the controlled object $f(t)$ is divided into two parts from (10)

$$f(t) = \underbrace{-\frac{\hat{L}}{\alpha}}_{\text{Robustness insured}} + \underbrace{\frac{1}{\alpha}\left(\dot{V}_2^* + K_{pu}e(t) + K_{Iu}\int e(t)\,dt\right)}_{\text{Closed-loop tracking}}. \tag{13}$$

In (13), $e(t) = V_2^* - V_2$, the first term aims at removing the effects of nonlinearities and disturbances, and the second term aims at tracking the reference in the closed loop. In the reference trajectory y^*.The transfer function based on the most ideal state simulated under PFM modulation is calculated from the hardware parameters. It can be obtained from (13) as follows:

$$f(t) = \frac{1}{\alpha}\left[\begin{array}{l}\frac{V_2^*(t)-V_2^*(t-h)}{h} - \frac{V_2(t)-V_2(t-h)}{h} \\ +\alpha f(t-h) + K_{Pu}e + K_{Iu}\int e(t)\,dt\end{array}\right]. \tag{14}$$

After sorting, the derivative result of (14) is obtained as follows:

$$h\dot{f}(t) = \frac{1}{\alpha}(\dot{e}(t) + K_{Pu}e(t) + K_{Iu}\int e(t)dt). \tag{15}$$

After performing Laplace transform, we have

$$hsF(s) = \frac{1}{\alpha}\left(sE(s) + K_{Pu}E(s) + K_{Iu}\frac{E(s)}{s}\right) \tag{16}$$

where F(s) and E(s) are the operation frequency and the tracking error of the output volage in s-domain. Thus, the transfer function between E(s) and F(s) is:

$$\frac{E(s)}{F(s)} = \frac{\alpha h s^2}{s^2 + K_{Pu}s + K_{Iu}}. \tag{17}$$

By using (17), the optimal damping ratio is considered, and the appropriate parameters of K_{Pu} and K_{Iu} are ultimately selected. At the optimal damping ratio, the system's response is neither too slow nor too fast, enabling it to quickly reach the steady-state value without excessive oscillation. At the optimal damping ratio, the overshoot is small, meaning that the system does not significantly exceed the reference during the response, thereby reducing unnecessary fluctuations and energy loss. The optimal damping ratio ensures the system stability and prevents unstable phenomena when subjected to external disturbances. The closed-loop poles of the system are located at appropriate positions in the s-plane, giving the system good dynamic and steady-state performance.

At the optimal damping ratio, the settling time is relatively short, meaning that the system can reach the steady state in a shorter period, improving the response efficiency. The optimal damping ratio can effectively weaken the oscillation characteristics of the system, making the system response more stable. This is particularly important for applications that require precise control, as it can improve the control accuracy and system reliability. This transfer function does not contain any model parameter values and is not affected by any model parameters and theoretically has better performance under parameter mismatch and perturbations.

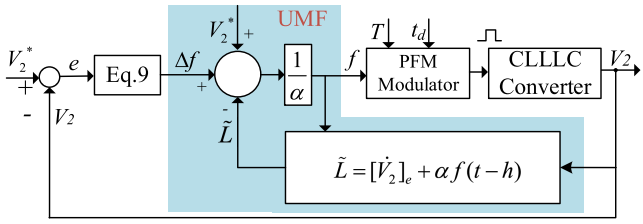

Fig. 4. Block diagram of the CLLLC converter with UMF-PFM controller.

In summary, the implementation of UMF-PFM controller is explained as follows:

1) Sample V_2 and V_2^* according to the voltage reference at instant, then calculate the setpoint in the closed loop.
2) The unknown term $\tilde{L}$ was estimated by using the new ultralocal model. The novel predicted converter frequency was calculated according to (13). The power transistors are controlled using frequency variations to achieve precise secondary-side voltage tracking.

C. Proposed UMF-PFM Scheme

Since there are multiple resonant capacitors and inductors in the CLLLC converter, the dynamic response is slower compared to the traditional *LLC* converter, so this paper adopts an equivalent closed-loop control method combining output voltage feedback, and the control block diagram is shown in Fig. 4. Where V_2 is the output voltage, V_2^* is the reference trajectory of the output voltage, and $[\dot{V}_2]_e$ is the derivative of the reference trajectory of the output voltage.

By applying PFM to the CLLLC converter, the controlled frequency generated by the UMF can be determined using the secondary-side voltage, secondary-side reference current, and secondary-side current. This allows the input deviation to be reflected through the frequency over time, enabling quicker and more efficient compensation of output deviations. As a result, the system exhibits a faster dynamic response and simplified control complexity. The proposed UMF-PFM enhances secondary-side voltage tracking and improves robustness against parameter variations and disturbances.

D. Parameter Design of the UMF-PFM Controller

1) Parameter Design of G, Q, *and* k*:* The initial step to preset the primary-side voltage ranging from 400 to 600 V, and the desired output voltage ranging from 300 to 450 V, a turns ratio of 1.33 is chosen to achieve appropriate voltage match. This selection ensures that the system can effectively handle the fluctuations in input voltage while delivering the required output range.

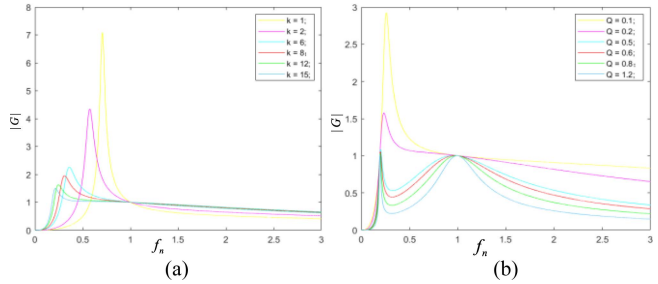

Fig. 5. Gain G vs. normalized frequency f_{n} for different k and Q. (a) $Q = 0.2$. (b) $k = 13$.

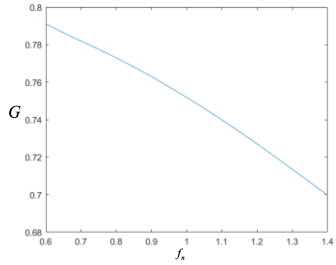

Fig. 6. Normalized frequency-gain plot.

To ensure ZVS operation of the primary-side power transistors, it is essential to guarantee that the energy stored in the resonant tank exceeds the energy stored in the MOSFET output capacitors. In this design, the desired switching frequency of the converter is 500 kHz. Parameters such as the dead-time (t_d) and the output capacitance (C_{oss}) of the selected SiC-MOSFET can be obtained from the device datasheet. Based on (18), the magnetizing inductance (L_m) must be limited to less than 48 μH. Additionally, beyond the energy contributions considered in the previous calculations, it is important to consider the interwinding capacitance present in a real transformer. This capacitance must also be discharged by the resonant tank current during operation. Therefore, $L_m = 25$ μH was selected to ensure ZVS across the full operating range

$$L_m \leq \frac{T \cdot t_d}{16 \cdot C_{oss}}. \tag{18}$$

According to (2), G can be derived as follows:

$$G = \frac{1}{\sqrt{\left(1+\frac{1}{k}-\frac{1}{kf_n^2}\right)^2+\left(\frac{Q}{k}\right)^2\left((2k+1)f_n-\frac{2k+2}{f_n}+\frac{1}{f_n^3}\right)^2}} \tag{19}$$

where $k = \frac{L_m}{L_{r1}}$, $Q = \frac{1}{R_{\mathrm{eq}}}\sqrt{\frac{L_{r1}}{C_{r1}}}$, $f_n = \frac{f_s}{f_r}$
where Q is the quality factor. To ensure soft-switching over the entire load range, further analysis is required. Starting from the input impedance Z_{in}, it is first necessary to ensure that the resonant converter operates in the inductive region

$$Z_{\mathrm{in}} = Z_r + Z_{\mathrm{in}} // \left(Z_r + R_{\mathrm{eq}}\right). \tag{20}$$

Fig. 5 shows the voltage gain G versus normalized frequency f_n for $Q = 0.2$ and $k = 13$. Fig. 5(a) shows that, as the inductance ratio k decreases, the peak voltage gain of the converter increases, and the switching frequency range required for the same output voltage is smaller, making the design of the magnetic components easier. However, the reduced excitation inductance leads to an increase in the resonant current, which in turn affects the efficiency. However, when k is too large, the peak voltage gain will be reduced and the voltage gain range will be reduced.

Fig. 5(b) shows that with small Q, lower switching frequency can obtain higher gain, and the gain at the resonant frequency point is 1, which decreases slightly as the switching frequency increases. As Q increases, the maximum gain tends to decrease, and the gain varies greatly as the switching frequency increases, but G at the resonance frequency point can still be guaranteed to be 1.

2) Influence of k *and* Q *on* G*:* k is chosen to ensure that the voltage gain in the resonant tank remains sufficient throughout the operating range. In combination with the need to maintain k at a sufficiently high value, serves to reduce the overall inductor size. The larger the k is, the smoother the voltage gain around the resonance point. would be. Moreover, if the inductance ratio k is too large, there will be a significant difference between the rate of change of the resonant current and the excitation current. This will also cause the resonant current to easily change direction during the dead-time, which means that the resonant current cannot completely release the charge in the parasitic capacitance of the switch transistors. This will result in being unable to achieve ZVS.

When Q is too large and exceeds a certain range, the switching frequency will decrease and the voltage gain will decrease, affecting the voltage output. But when Q is too small, it will extend the passband of the circuit and be easily affected by external interference, resulting in unstable output voltage. The final synthesis selects a suitable k and Q to ensures the ZVS/ZCS.

After selecting the appropriate k and Q, the normalized frequency-gain graph can be plotted in Fig. 6. The primary side of the CLLLC converter is often connected to a PFC, with a predicted voltage ripple of 10%, and with 600 V as an example, the primary side end may be at 570–630 V, for which the gain needed from the resonant tank will vary from 0.79 to 0.71. It is found that at a frequency of about 300–700 kHz can satisfy the required gain, so the operating frequency can be in the range of 300–700 kHz, but if it is necessary to guarantee the need to ensure that the ZCS, the operating frequency can only be lower than 500 kHz.

E. Stability Analysis

To analyze the stability of the CLLLC converter with the proposed scheme, substituting (1) into (2) gives the transfer function of the voltage gain G at the switching frequency as follows:

$$\begin{aligned} G(j\omega_s) = \omega L_m R_{eq} / \Bigg[& \left(\omega_s L_{r1} - \frac{1}{\omega C_{r1}} + \omega_s L_m\right) R_{eq} \\ & + j\left(\omega_s{}^2 L_{r1} L_m + \omega_s{}^2 L_{r2} L_m + \omega_s{}^2 L_{r1} L_{r2} - \frac{L_m}{C_{r1}}\right. \\ & \left. - \frac{L_m}{C_{r2}} - \frac{L_{r2}}{C_{r1}} - \frac{L_{r1}}{C_{r2}} + \frac{1}{\omega_s{}^2 C_{r1} C_{r2}}\right) \end{aligned} \tag{21}$$

where ω_s is the angular switching frequency. To simplify (21), we define

$$k=\frac{L_m}{L_{r1}},\ h=\frac{L_{r2}}{L_{r1}},\ g=\frac{C_{r2}}{C_{r1}},\ \omega_1=\frac{1}{\sqrt{L_{r1}C_{r1}}},$$
$$\omega_2=\frac{1}{\sqrt{L_{r2}C_{r2}}}=\frac{\omega_1}{\sqrt{hg}}.$$

Substituting *k, h, g*, ω_1 into (21) and dividing both the numerator and denominator by C_{r1}/L_{r1}, the voltage gain G can be simplified as follows:

$$G(j\omega_s)=k\omega C_{r1}R_{\text{eq}}\Big/ \begin{bmatrix} \omega_s C_{r1}-\frac{1}{\omega_s L_{r1}}+k\omega_s C_{r1})R_{\text{eq}} \\ +j\left(k\frac{{\omega_s}^2}{{\omega_1}^2}+kh\frac{{\omega_s}^2}{{\omega_1}^2}+h\frac{{\omega_s}^2}{{\omega_1}^2}-\frac{L_m}{C_{r1}}-k\right) \\ -\frac{k}{g}-h-\frac{1}{g}+\frac{1}{g}\frac{{\omega_1}^2}{{\omega_s}^2} \end{bmatrix}. \quad (22)$$

The imaginary part of the transfer function is zero when resonance occurs, and at this time the resonant frequency of the fundamental equivalent circuit is ω_r, which is obtained as follows:

$$(k+kh+h)\omega_r^4-\left(k+\frac{k}{g}+h+\frac{1}{g}\right)\omega_1^2\omega_r^2+\frac{1}{g}\omega_1^4=0. \quad (23)$$

Define$a=k+kh+h$,$b=k+\frac{k}{g}+h+\frac{1}{g}$,$c=\frac{1}{g}$, (23) can be updated as follows:

$$a\omega_r^4-b\omega_1^2\omega_r^2+c\omega_1^4=0. \quad (24)$$

Solving (24) gives the ω_r expressed as follows:

$$\omega_r^2=\frac{b\pm\sqrt{b^2-4ac}}{2a}\omega_1^2. \quad (25)$$

Since L_{m} is far greater than L_1, thus the series resonant frequency should be greater than the parallel resonant frequency, thus (26) should be positive for its solution. Thus, the series resonant frequency should be

$$\omega_r=\sqrt{\frac{b+\sqrt{b^2-4ac}}{2a}}\cdot\omega_1. \quad (26)$$

At this moment, *H*(*s*) at ω_r can be written as follows:

$$G(j\omega_r)=\frac{k}{1+k-\frac{1}{\omega_r^2 L_1 C_1}}. \quad (27)$$

From (26) and (27), because of the series resonant frequency, the system could not be linearized and expressed as a standard form of a transfer function or a state-space equation using small-signal modeling at an equilibrium point. Thus, it cannot be analyzed by exiting stability criteria. But the system would be stable at the resonance frequency. Simulation and experimental results of system stability under disturbance, input volage variation, load changes are provided in the followed sections, which can demonstrate its stability.

TABLE I
PARAMETER SPECIFICATION

Name	Symbol	Value
Primary-side Voltage	V_1	600 V
Rated Power	P	6.6 kw
Transformer turns ratio	n	1.33
Specified constant parameter	α	50
Excitation inductance	L_m	25 μH
Primary-side resonant inductance	L_{r1}	1.923 μH
Secondary resonant inductance	L_{r2}	1.3μH
Primary resonant capacitance	C_{r1}	57.4 nF
Secondary resonant capacitance	C_{r2}	82 nF
Load	R	13.63 Ω
Proportional parameter	K_{Pu}	0.05
Integral parameter	K_{Iu}	1e-3

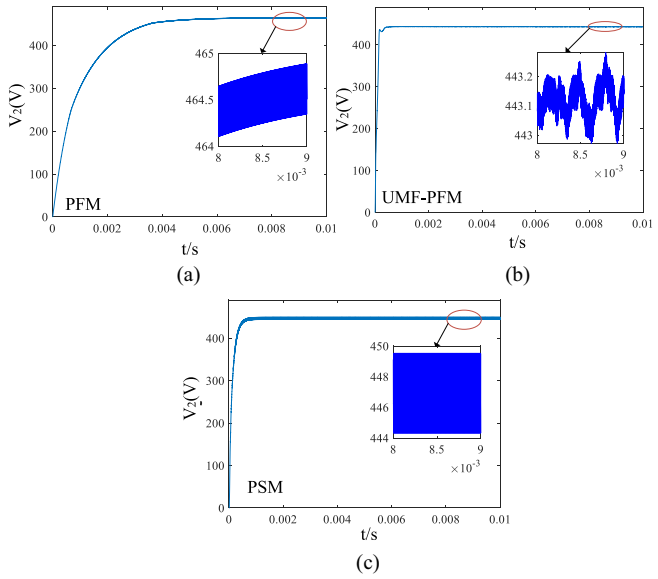

Fig. 7. Tracking error of the output voltage with different methods. (a) PFM. (b) UMF-PFM. (c) PSM.

IV. SIMULATION RESULT

A. Simulation Setup

Simulations of the CLLLC converter and its control strategy were performed using MATLAB/Simulink. To validate the advantages of UMF-PFM under steady-state conditions with parameter mismatches and perturbed performance, a comparison was made with PFM and PSM under identical conditions. The variations in parameters across different operating conditions were considered, with the specific changes outlined in the corresponding sections Table I presents the default parameter settings.

B. Results and Analysis

1) Tracking Performance of the Output Voltage: The reference output voltage V_2 is 450 V. Fig. 7 shows the tracking error of the output voltage with different methods. Specifically, although the PFM control strategy can operate effectively, there is a significant gap of about 14.5 V between its steady-state voltage and the rated voltage, about 464.5 V. In contrast, both the PSM and UMF-PFM demonstrate high voltage tracking accuracy,

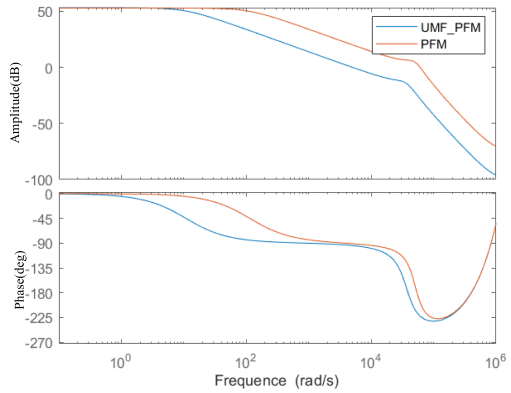

Fig. 8. Bode plots with different methods.

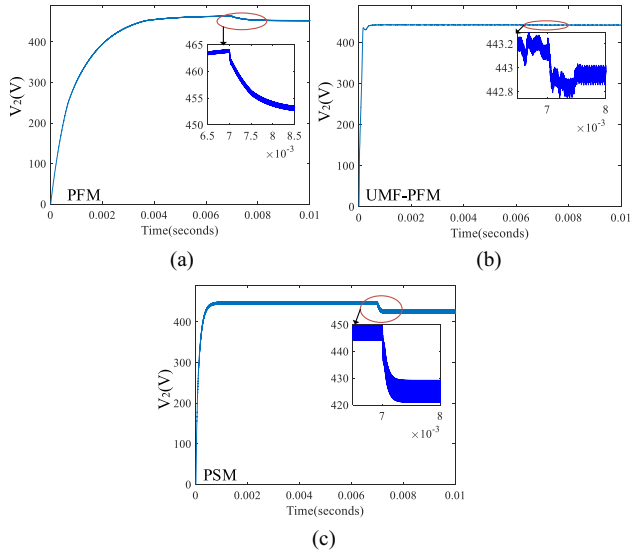

Fig. 9. Comparison of different control methods under parameter mismatch. (a) PFM. (b) UMF-PFM. (c) PSM.

with the maximum voltage tracking error of the PSM being about 3 V, about 447 V awhile the UMF-PFM further reduces this error to 6.9 V (although numerically slightly larger than the PSM, it needs to be comprehensively evaluated in the context of subsequent analyses), about 443.1 V. Something interest is that the UMF-PFM control shows an overwhelming advantage in voltage steady-state fluctuation, with the fluctuation difference between the PFM strategy of about 1 V and the PSM strategy of about 3.6 V, while the fluctuation difference of the UMF-PFM strategy is only 0.3 V.

Fig. 8 illustrates the Bode diagram comparison between PFM and UMF-PFM. The amplitude margin of UMF-PFM is 15.4 dB and the phase margin is 85.6°. It has a significant improvement compared to PFM. The Bode plot shows that the UMF-PFM can reduce the steady-state error, system overshoot, improve the dynamic performance, and improve the system stability compared to the PFM. It can be observed that both amplitude margin and phase margin are improved.

The results not only highlight the exceptional ability of UMF-PFM in enhancing system stability and reducing voltage fluctuations, but also provides a solid foundation for its application in systems that require high-precision voltage control. It offers strong support for its use in scenarios where precise voltage regulation is essential.

2) Comparison of Different Methods Under Parameter Mismatch: When analyzing the impact of different control methods on the output voltage stability under the extreme parameter mismatch, the excitation inductance L_{m} drops to 12 μH due to the transformer damage.

First, Fig. 9(c) shows the PSM control results, the output voltage experiences a significant shift in its steady-state value following a sudden decrease in the excitation inductance, dropping from 447 to 425 V. This highlights the limitations of the PSM strategy in handling system parameter mismatches. Next, Fig. 9(a) illustrates the performance of the PFM strategy, where the output voltage decreases from 464.5 to 454.5 V, indicating that while the PFM performs better than PSM, its ability to cope with such parameter mismatches still requires improvement. In contrast, the UMF-PFM control strategy, shown in Fig. 9(b), demonstrates exceptional robustness under the same parameter mismatch. Its steady-state voltage is almost unaffected, with a minimal difference of only about 0.2 V from the normal state, decreasing from 443.1 to 442.9 V.

This result verifies the effectiveness of the improved design based on inverter modulation. Further analysis reveals that although all control strategies maintain relatively stable fluctuations after the voltage reaches steady state, the UMF-PFM strategy stands out in preserving the steady state. Its superior performance in this regard provides strong support for its application in complex operating conditions.

3) Comparison of Different Control Methods Under Primary-Side Voltage Disturbances: In exploring the response characteristics of different control methods under external perturbation conditions, this paper designs an experiment in which the perturbation is introduced in the form of a parameter-specific sinusoidal signal, which is manifested as a periodic fluctuation with an amplitude of 50 V and a frequency of 500 kHz, and is applied to the primary-side voltage V_1 at 7 ms. It is shown in Fig. 10(d).

Fig. 10 demonstrates the performance of the three typical control methods under disturbances. It is particularly noteworthy that UMF-PFM demonstrates exceptional voltage maintenance capability under external disturbances, as clearly shown in Fig. 10. Specifically, both the PFM and PSM methods exhibit significant voltage fluctuations when influenced by disturbances, highlighting their limitations in handling sudden disturbances. The PFM's voltage increases from 464.5 to 475 V, while the PSM's voltage rises from 447 to 458 V. In contrast, the UMF-PFM efficiently tracks and controls the dynamic trajectory of the system, thanks to its built-in mechanism for accurate estimation of the parameter L within the MFC control law. This feature enables the UMF-PFM to maintain a high level of voltage stability in disturbed environments, with the voltage deviation effectively limited to a very low level of approximately 0.5 V, rising from 443.1 to 443.6 V. This result fully validates its outstanding robustness and control accuracy.

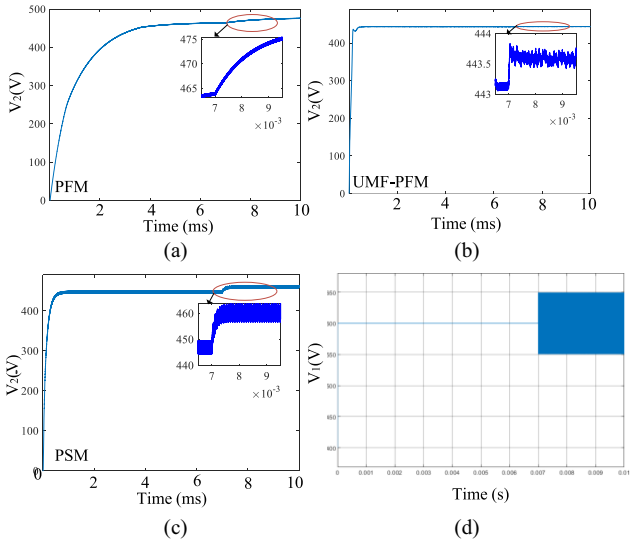

Fig. 10. Comparison of different control methods with perturbations. (a) PFM. (b) UMF-PFM. (c) PSM. (d) Primary-side voltage.

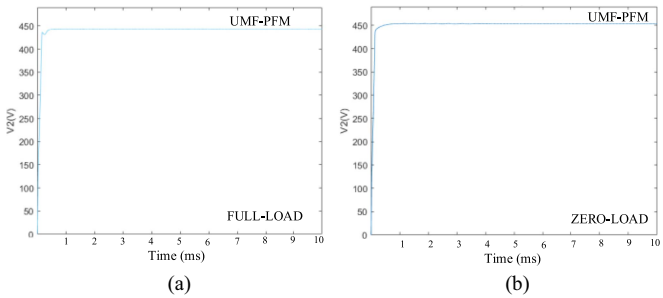

Fig. 11. Tracking performance of the output voltage with UMF-PFM with different load. (a) Full load. (b) Zero load.

Further analysis reveals that traditional control methods, such as PFM and PSM, often rely directly on instantaneous feedback of the secondary voltage output for adjustment. This approach proves to be fragile under complex and variable operating conditions, making it challenging to effectively mitigate the impact of external disturbances (e.g., load variations). In contrast, the UMF-PFM not only improves the system's dynamic response speed but also significantly enhances its adaptability to environmental changes. This advancement effectively addresses the shortcomings of traditional methods.

4) Tracking Performance of the Output Voltage Under Zero and Full Load: Fig. 11 shows the output waveforms under different loads. Under full load, the voltage output is about 442 V or so, and at zero load the voltage output is about 453 V. Indicating that the proposed UMF-PFM control the output voltage smoothly and quickly, whether it is started at full load or zero load.

5) Tracking Performance Under Disturbance of the Voltage Reference V_2^*: A comparative analysis is conducted between the UMF-PFM, PFM, and PSM techniques, with a focus on the evolution of the secondary-side voltage reference profiles in

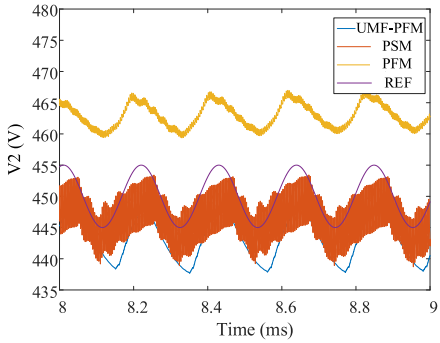

Fig. 12. Tracking performance with different methods.

TABLE II
COMPARISON OF DIFFERENT CONTROL METHODS

	PFM	UMF-PFM	PSM
Complexity	Medium	Low	High
Efficiency	94.5%	96.8%	94%
Dynamic response	Low	High	High
Voltage ripple	Medium	Low	High
Anti-interference	Medium	High	Low
Cost	Medium	Medium	Medium
Experimental feasibility	Easy	Medium	Easy

achieving the final secondary-side voltage. Specifically, a sinusoidal disturbance with an amplitude of 10 V and a frequency of 50 kHz is introduced to the V_2^* at 7 ms. Following this, the PFM and PSM methods cause deviations in the secondary-side voltage reference trajectory, as shown in Fig. 12. The superiority of the UMF-PFM control law lies in its use of the estimated parameter F, which enables precise control over the evolving dc bus trajectory and ensures accurate trajectory tracking. In contrast, the PFM and PSM rely directly on fluctuations in the secondary-side voltage, leading to inferior voltage tracking performance.

A comparative table summarizing is presented in Table II. PSM requires phase synchronization and soft-switching optimization, hence the high complexity of PSM. PFM requires dynamic frequency adjustment and stability control, hence PFM medium complexity. UMF-PFM only requires dynamic frequency adjustment. The efficiency will vary depending on the load, the efficiency shown in the table is at a load with 13.63 Ω.

V. EXPERIMENTAL RESULT

A. Hardware Setup

Experimental verifications were performed to validate the effectiveness of the proposed method further. A 6.6 kW CLLLC-type dc–dc platform was established in the laboratory, and the specific parameters are the same as the above simulation experiments. Fig. 13 shows the platform. The core of the control strategy is implemented in TMS320F280049 digital controller to achieve the full bridge of the eight power transistors (C3M0030090K TO-247-4 four-pin package SiC-MOSFET) are used. And its maximum drain-source voltage up to 900 V, ON-resistance of 30 mΩ, switching loss is small, very suitable

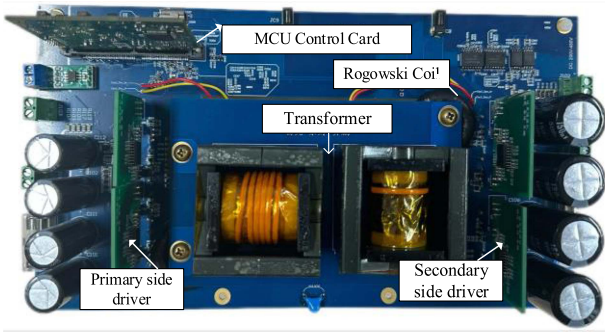

Fig. 13. Hardware setup of the CLLLC-type DC–DC converter.

for use in high-frequency scenarios. The implementation of soft switching techniques, specifically ZVS on the primary side and the combination of ZCS with ZVS on the secondary side, facilitates enhanced operational efficiency. Additionally, the incorporation of Rogowski coil sensors contributes to further augmenting this efficiency.

To facilitate the tuning of control loops with greater ease, the utilization of a software frequency response analyzer along with a compensation designer is proposed. Furthermore, software support tailored for the TMS320F28004x device, equipped with the control law accelerator, enables the integration of an on-board controller design that encompasses both ac–dc and dc–dc conversions, controlled seamlessly by a solitary C2000 Microcontroller Unit.

B. Results and Analysis

1) Comparison of Different Control Methods Under Parameter Mismatch: In this case, when L_m drops from 25 to 12 μH, Fig. 14 shows the local voltage waveforms of the three representative control methods under parameter mismatch conditions in turn. Fig. 13 shows that PFM decreases by about 10 V, the UMF-PFM decreases by about 0.3 V, and the PSM decreases by about 20 V. The experimental results are basically consistent with the simulation waveforms, which show the superior performance of the UMF-PFM under the parameter mismatch.

2) Comparison of Different Control Methods in the Presence of Disturbances in the Primary Side Voltage: At 7 ms, a periodic sinusoidal fluctuation with an amplitude of 50 V and a frequency of 500 kHz is introduced as a perturbation to the primary-side voltage. Fig. 15 presents the localized amplified waveforms of the secondary-side voltage under perturbation. The voltage increases by 12 V with PFM, 0.3 V with UMF-PFM, and 12 V with PSM. Notably, UMF-PFM demonstrates excellent voltage stability when the system is subjected to external disturbances. This observation is in line with the simulation and theoretical results, further confirming the superiority of the UMF-PFM approach.

3) Tracking Performance of the Output Voltage Under Light and Full Load: Fig. 16 presents the experimental waveforms obtained under different loads. At full load, the output voltage is approximately 442 V, while at zero load, it is around 453 V. These results demonstrate that the proposed UMF-PFM method

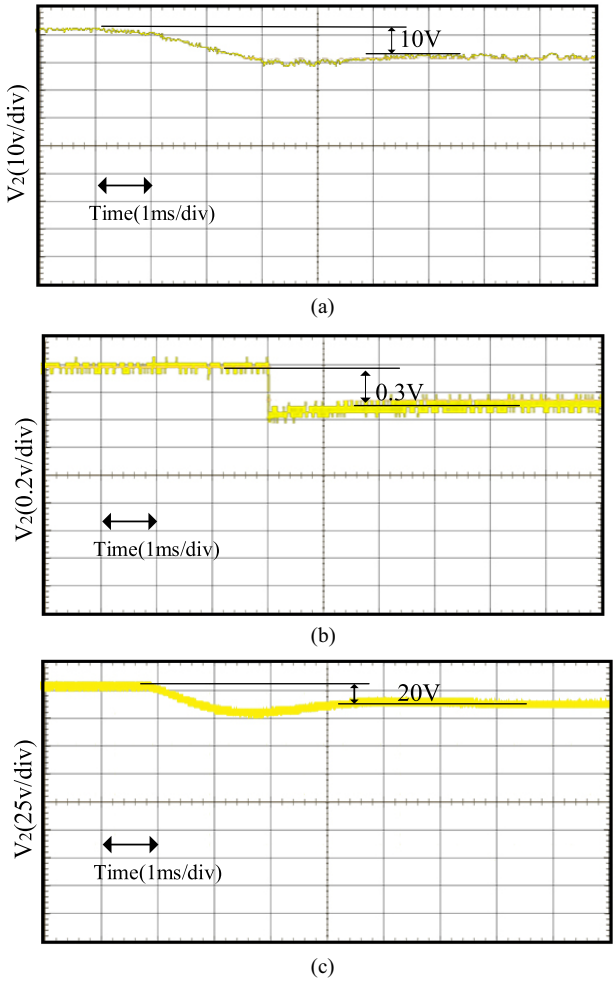

Fig. 14. Comparison of different control methods under parameter mismatch. (a) PFM. (b) UMF-PFM. (c) PSM.

enables a smooth and rapid tracking of the output voltage, regardless of whether the system is initiated under full load or no load. Furthermore, the experimental findings align well with the simulation results, confirming the effectiveness of the proposed method in achieving stable voltage regulation under load variations.

4) Steady-State Tracking Performance With Different Methods: Fig. 17 presents the output voltage for different control methods, clearly illustrating the performance of each strategy in regulating the output voltage during steady-state operation. The stabilized voltage of the UMF-PFM is approximately 443 V, exhibiting the smallest fluctuation of less than 1 V. In comparison, the stabilized voltage of the PSM is around 443 V, while the PFM stabilizes at approximately 463 V. These results are consistent with the simulation and theoretical expectations, further validating the superiority of the UMF-PFM.

It is needed to note that, in experiment, physical switching devices have ON/OFF delays and jitter in the clock source may destroy the phase synchronization accuracy of the PSM, leading to phase error accumulation. This may deteriorate the steady-state error with PSM. The UMF-PFM was slightly off in the

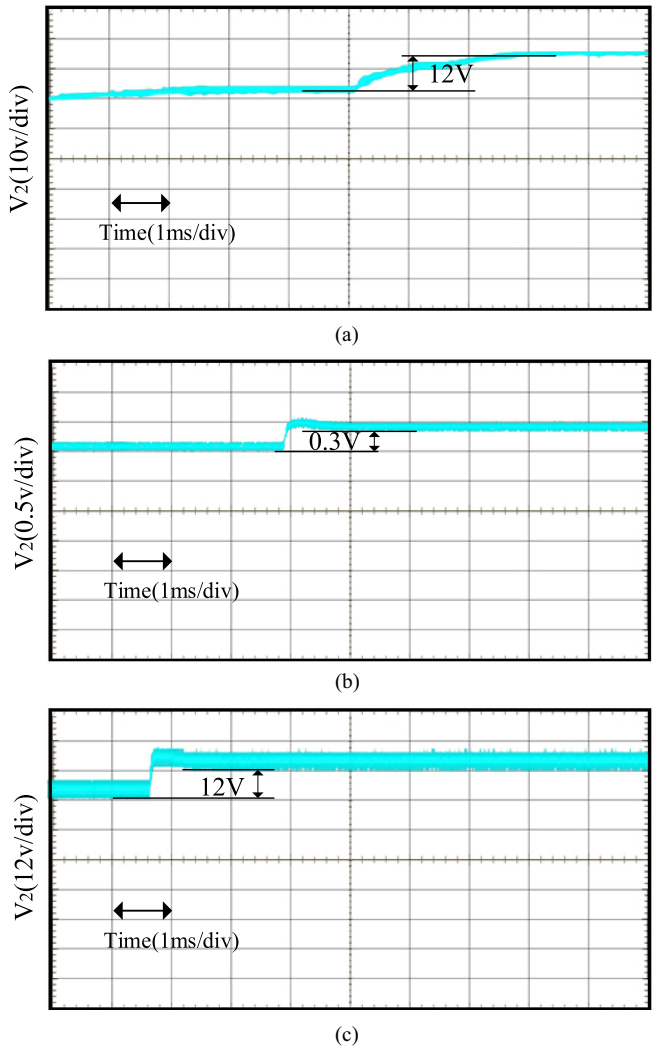

Fig. 15. Comparison of different control methods with perturbations. (a) PFM. (b) UMF-PFM. (c) PSM.

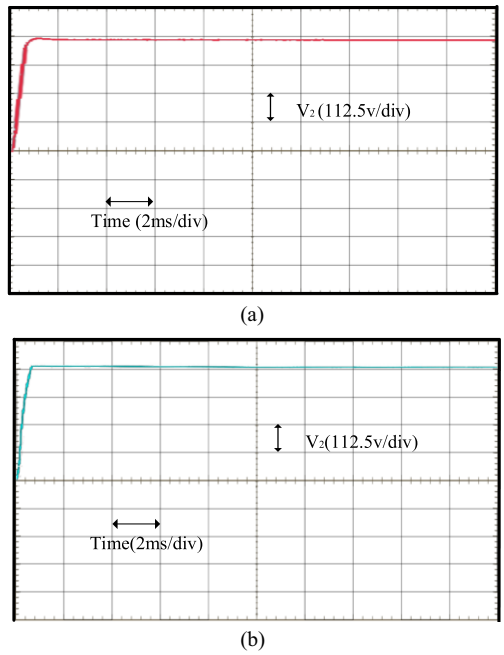

Fig. 16. Voltage tracking with UMF-PFM with different load. (a) Full load. (b) Zero load.

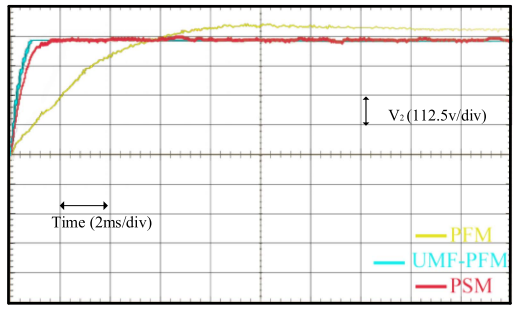

Fig. 17. Comparison of different control methods in steady state.

TABLE III
EFFICIENCY COMPARISON WITH DIFFERENT CONTROL METHODS

	PFM	PSM	UMF-PFM
Light Load (54.4 Ω)	83. 93%	66.33%	95.84%
Rated Load (27.3 Ω)	66.97%	68.54%	97.94%
Heavy Load (6.8 Ω)	65.4%	76.76%	96.75%
Heavy Load (13.6 Ω)	71.23%	85.61%	96.4%

last round of experiments, and is largely consistent with the simulation results.

5) Efficiency Analysis With Different Control Methods: To compare the efficiency of the CLLLC converter with different control methods, the experimental results with different loads (including rated load $R = 27.3\ \Omega$, heavy load $R = 6.8$ and $3.6\ \Omega$, and light load $R = 54.4\ \Omega$.) are provided and shown in Table III. The efficiency test results show that the proposed UMF-PFM method has very high efficiency at rated load (about 97.94%), with the increase of the load ($R = 54.4$ and $13.6\ \Omega$), the system efficiency decrease to 95.84% and 96.4%. Additionally, with the decrease of the load value (e.g., 6.8 Ω), the system efficiency is about 96.75%. In general, the system efficiency with UMF-PFM controller is remains higher than existing PFM and PSM controllers. This also demonstrate the advantage of the proposed scheme.

6) Verification of the Estimation Model of the Nonlinear Term: To verify the estimation model of the nonlinear terms by the hyperlocal model, both simulation and experimental results are given. Fig. 18(a) shows the estimation results of the unknown term $\tilde{L}$, and Fig. 18(b) shows the experimental results of the unknown term, which is output by the analog output port of the DSP, the results indicate that the experimental results are in accordance with the simulation results. This verifies the correctness of the proposed estimation scheme.

C. Summary

From the above experimental results, we may know that the proposed UMF-PFM outperforms existing methods under a variety of complex operating conditions. These conditions

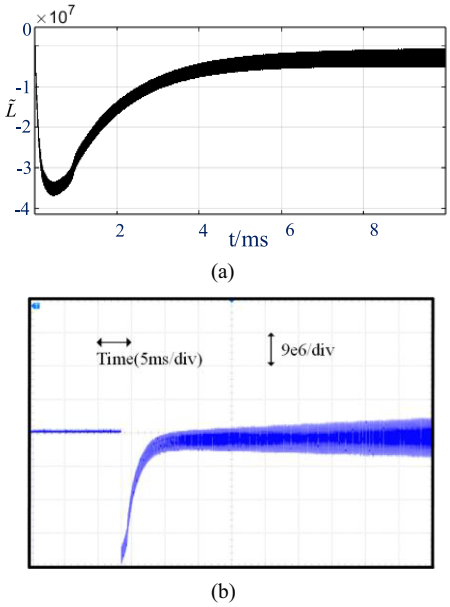

Fig. 18. Estimation verification of the nonlinear term in UMF-PFM controller. (a) Simulation results. (b) Experimental results.

include, but are not limited to, parameter mismatches and sudden fluctuations in input voltage. Notably, the proposed method ensures that the output voltage tracking control is consistently achieved across the entire range of full load. These findings underscore the promising potential of UMF-PFM for further research and practical applications in voltage regulation systems.

VI. Conclusion

This article investigates a UMF-PFM solution to enhance the control performance of a bidirectional CLLLC converter under parameter variations and perturbation. The proposed UMF-PFM utilize an ultralocal model to decompose the system into its linear term and the unknown nonlinear term, where unknown term is accurately estimated, which enables precise control over the evolving dc bus trajectory and ensures accurate trajectory tracking. The results demonstrate that UMF-PFM significantly improves control performance, exhibiting excellent voltage tracking capability and minimizing the impact of disturbances, such as changes in model parameters and input-side voltage fluctuations. A comparative study is conducted between the newly proposed UMF-PFM strategy and the conventional control methods, PFM and PSM. Future work includes the development of adaptive control designs for CLLLC converters and exploration of global model-free control approaches. UMF-PFM has a promising research prospect, and the future research may comprehensively consider the incorporation of ultralocal model-free control in different hybrid modulations.

References

[1] N. Hou, Y. Zhang, Y. Li, L. Ding, and Y. Li, "Topologies and operations of hybrid-type DC-DC converters interfacing DC-current bus and DC-voltage bus," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 4, pp. 4212–4221, Aug. 2023, doi: 10.1109/JESTPE.2022.3187074.

[2] S. Kumar, S. Jammeh, R. Samb, and A. Singh, "Efficient DC-DC power converters for fuel-cell electric vehicle: A qualitative assessment," *IET Power Electron.*, vol. 17, no. 16, pp. 3166–3204, Nov. 2024, doi: 10.1049/pel2.12819.

[3] H. Heydari-doostabad and T. O'Donnell, "A wide-range high-voltage-gain bidirectional DC-DC converter for V2G and G2V hybrid EV charger," *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 4718–4729, May 2022, doi: 10.1109/TIE.2021.3084181.

[4] A. Sharma and S. Sharma, "Review of power electronics in vehicle-to-grid systems," *J. Energy Storage*, vol. 21, pp. 337–361, Feb. 2019, doi: 10.1016/j.est.2018.11.022.

[5] R. P. Upputuri and B. Subudhi, "A comprehensive review and performance evaluation of bidirectional charger topologies for V2G/G2V operations in EV applications," *IEEE Trans. Transp. Electrific.*, vol. 10, no. 1, pp. 583–595, Mar. 2024, doi: 10.1109/TTE.2023.3289965.

[6] R. Wei, L. Ding, R. Liu, and Y. Li, "An intuitive and noniterative design methodology for CLLC chargers employing simplified operation modes model," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7771–7784, Jun. 2023, doi: 10.1109/TPEL.2023.3251284.

[7] N. Z. Jin, Y. Feng, Z. Y. Chen, and X. G. Wu, "Bidirectional CLLLC resonant converter based on frequency-conversion and phase-shift hybrid control," *Electronics*, vol. 12, no. 7, Apr. 2023, Art. no. 1605, doi: 10.3390/electronics12071605.

[8] X. Li, J. Huang, Y. Ma, X. Wang, J. Yang, and X. Wu, "Unified modeling, analysis, and design of isolated bidirectional CLLC resonant DC–DC converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 2, pp. 2305–2318, Apr. 2022, doi: 10.1109/JESTPE.2022.3145817.

[9] H. Li et al., "Bidirectional control with fitting model-based synchronous rectification and input ripple current feedforward for SiC bidirectional CLLC EV charger," *IEEE Trans. Ind. Electron.*, vol. 70, no. 9, pp. 9136–9146, Sep. 2023, doi: 10.1109/TIE.2022.3212382.

[10] S. Zou, A. Mallik, J. Lu, and A. Khaligh, "Sliding mode control scheme for a CLLC resonant converter," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12274–12284, Dec. 2019, doi: 10.1109/TPEL.2019.2904456.

[11] F. Bento, I. Jlassi, and A. J. M. Cardoso, "Model-free predictive control of interleaved DC-DC converters, based on ultra-local model, with constant switching frequency," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 2022–2028.

[12] X. Yuan, S. Zhang, C. N. Zhang, M. Degano, G. Buticchi, and A. Galassini, "Improved finite-state model predictive current control with zero-sequence current suppression for OEW-SPMSM drives," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4996–5006, May 2020, doi: 10.1109/TPEL.2019.2942156.

[13] M. Abdelrahem, C. M. Hackl, Z. B. Zhang, and R. Kennel, "Robust predictive control for direct-driven surface-mounted permanent-magnet synchronous generators without mechanical sensors," *IEEE Trans. Energy Convers.*, vol. 33, no. 1, pp. 179–189, Mar. 2018, doi: 10.1109/TEC.2017.2744980.

[14] M. Yang, X. Lang, J. Long, and D. Xu, "Flux immunity robust predictive current control with incremental model and extended state observer for PMSM drive," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9267–9279, Dec. 2017, doi: 10.1109/TPEL.2017.2654540.

[15] X. Zhang, B. Hou, and Y. Mei, "Deadbeat predictive current control of permanent-magnet synchronous motors with stator current and disturbance observer," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3818–3834, May 2017, doi: 10.1109/TPEL.2016.2592534.

[16] Y. J. Jiang, W. Xu, C. Mu, and Y. Liu, "Improved deadbeat predictive current control combined sliding mode strategy for PMSM drive system," *IEEE Trans. Veh. Technol.*, vol. 67, no. 1, pp. 251–263, Jan. 2018, doi: 10.1109/TVT.2017.2752778.

[17] B. Wang, Z. Dong, Y. Yu, G. Wang, and D. Xu, "Static-errorless deadbeat predictive current control using second-order sliding-mode disturbance observer for induction machine drives," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2395–2403, Mar. 2018, doi: 10.1109/TPEL.2017.2694019.

[18] C. Zhang et al., "Robust fault-tolerant predictive current control for permanent magnet synchronous motors considering demagnetization fault," *IEEE Trans. Ind. Electron.*, vol. 65, no. 7, pp. 5324–5334, Jul. 2018, doi: 10.1109/TIE.2017.2774758.

[19] Y. Zhou, H. Li, R. Liu, and J. Mao, "Continuous voltage vector model-free predictive current control of surface mounted permanent magnet synchronous motor," *IEEE Trans. Energy Convers.*, vol. 34, no. 2, pp. 899–908, Jun. 2019, doi: 10.1109/TEC.2018.2867218.

[20] Y. Zhang, J. Jin, and L. Huang, "Model-free predictive current control of PMSM drives based on extended state observer using ultralocal model," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 993–1003, Feb. 2021, doi: 10.1109/TIE.2020.2970660.
[21] Y. C. Zhang, X. Liu, B. Y. Li, and J. Liu, "Robust predictive current control of PWM rectifier under unbalanced and distorted network," *IET Power Electron.*, vol. 14, no. 4, pp. 797–806, Mar. 2021, doi: 10.1049/pel2.12065.
[22] M. Khalilzadeh, S. Vaez-Zadeh, and M. S. Eslahi, "Parameter-free predictive control of IPM motor drives with direct selection of optimum inverter voltage vectors," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 327–334, Feb. 2021, doi: 10.1109/JESTPE.2019.2949222.
[23] X. Liu, Y. C. Zhang, H. T. Yang, and J. Rodriguez, "Robust predictive current control of PWM rectifiers with LCL filters under unbalanced and distorted network conditions," *IET Power Electron.*, vol. 15, no. 3, pp. 226–236, Feb. 2022, doi: 10.1049/pel2.12223.
[24] C. Hu et al., "A novel modulated model-free predictive control for LC-filtered grid-forming inverters with double-difference updating," *IEEE Trans. Ind. Electron.*, vol. 71, no. 9, pp. 10806–10817, Sep. 2024, doi: 10.1109/TIE.2023.3335463.
[25] H. Yang, Y. Zhang, and W. Shen, "Predictive current control and field-weakening operation of SPMSM drives without motor parameters and DC voltage," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5635–5646, Oct. 2022, doi: 10.1109/JESTPE.2022.3167273.
[26] D. Da Rù, M. Polato, and S. Bolognani, "Model-free predictive current control for a SynRM drive based on an effective update of measured current responses," in *Proc. IEEE Int. Symp. Predictive Control Elect. Drives Power Electron.*, 2017, pp. 119–124.
[27] H. C. Yu, H. C. Chuang, Z. M. Wang, and C. K. Lin, "Simplified model-free predictive current control for dual air-gap transverse-flux six-phase permanent magnet electric machines," *Adv. Mech. Eng.*, vol. 9, no. 11, Nov. 2017, Art. no. 1687814017735291, doi: 10.1177/1687814017735291.
[28] C. Cui, T. Yang, Y. Dai, C. Zhang, and Q. Xu, "Implementation of transferring reinforcement learning for DC–DC buck converter control via duty ratio mapping," *IEEE Trans. Ind. Electron.*, vol. 70, no. 6, pp. 6141–6150, Jun. 2023, doi: 10.1109/TIE.2022.3192676.
[29] J. Yue, Z. Liu, and H. Su, "Data-driven adaptive extended state observer-based model-free disturbance rejection control for DC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 71, no. 7, pp. 7745–7755, Jul. 2024, doi: 10.1109/TIE.2023.3317860.
[30] O. Babayomi, Z. Zhang, and Z. Li, "Model-free predictive control of DC–DC boost converters: Sensor noise suppression with hybrid extended state observers," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 245–259, Jan. 2024.
[31] T. Zhu, F. Zhuo, F. Zhao, F. Wang, H. Yi, and T. Zhao, "Optimization of extended phase-shift control for full-bridge CLLC resonant converter with improved light-load efficiency," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 11129–11142, Oct. 2020, doi: 10.1109/TPEL.2020.2978419.
[32] C. Y. Tang, C. W. Wang, and H. C. Chien, "A dynamic smooth transition control integrated with hybrid modulation for wide output voltage range bidirectional CLLC resonant converters," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 13587–13593, Nov. 2023, doi: 10.1109/TPEL.2023.3305297.
[33] C. Zhang, P. Li, Z. Kan, X. Chai, and X. Guo, "Integrated half-bridge CLLC bidirectional converter for energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3879–3889, May 2018, doi: 10.1109/TIE.2017.2758741.

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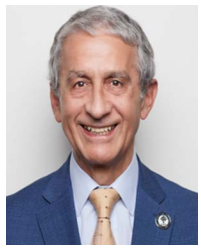

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