Ultra-Fast Dynamic Response and Current Harmonic Reduction in PFC Applications

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***Abstract*—This article introduces a digital zero crossing voltage control (ZCVC) strategy designed for general power factor correction (PFC) applications. The ZCVC approach performs voltage control calculations and updates the current reference precisely at input voltage zero-crossings. This timing ensures that the control output remains constant for each half-grid cycle, resulting in a pure sinusoidal ac current waveform. This method effectively eliminates second harmonic distortions in the bus voltage without requiring a notch filter (NF), thereby reducing even harmonics from the RMS filter. ZCVC offers a significantly faster dynamic response, achieving stability within 1.5 grid cycles during load changes, input voltage fluctuations, or step changes in output voltage reference. This preserves a power factor close to unity and results in very low total harmonic distortion. Furthermore, the proposed ZCVC considerably reduces the computational burden on the microcontroller by minimizing the execution of the digital voltage loop controller per grid cycle, thereby eliminating the need for NFs. The mathematical average model of the ZCVC is derived for general PFC applications. Various scenarios are simulated to validate the effectiveness of this method compared to prior approaches. The implementation of ZCVC on a 7.2 kW GaN-based interleaved totem pole PFC confirms the claimed improvements, demonstrating four times faster dynamic response and very low harmonic distortion. Additionally, the ZCVC reduces voltage sampling and control computations from a typical range of 200 times per grid cycle to only two times, achieved by eliminating the need for notch and low-pass filters.**

***Index Terms*—Control systems, digital control, harmonic distortion, power factor correction (PFC), voltage control, wide-bandgap devices.**

I. Introduction

POWER factor correction (PFC) is a critical requirement in modern power electronics, driven by the need to meet stringent regulatory standards and improve the overall efficiency of power conversion systems. Dual-loop controllers are commonly employed, consisting of an inner loop for shaping a sinusoidal current and an outer loop for regulating the dc-bus voltage to achieve efficient PFC [1]. The sinusoidal nature of the input voltage and current introduces double-line frequency power fluctuations in the dc-bus voltage. Additionally, fast ac RMS voltage estimation is essential for effectively addressing input voltage changes in PFC applications, such as uninterruptible power supplies (UPS) and bidirectional modes. Fig. 1 shows a simplified single-phase boost PFC. Conventional methods for maintaining dc-bus voltage and reducing ac filter ripple can result in current distortion and unwanted harmonics. Common solutions include increasing dc bus capacitance, reducing the bandwidth (BW) of the voltage loop controller, and lowering the BW of the ac RMS filter to prevent input current distortions. However, large dc-bus capacitors hinder power density, increasing the size, weight, cost, and overall footprint [2], [3]. Therefore, the outer loop BW in PFC converters must balance dynamic response requirements, stability, input current distortion, and overall system performance, often resulting in low BW and slow dynamics [4].

Various linear control techniques aimed at improving dynamic response have been proposed [5], [6]. These methods primarily address capacitor voltage ripple by either filtering or canceling it using estimated values. In [6], the critical mode (CrM) approach is utilized that is based on zero current detection (ZCD) to ensure CrM under PFC system states variations. While these approaches enhance voltage loop dynamics, they require several line-frequency cycles for the output voltage to stabilize after sudden load changes. A bus voltage control method offering zero distortion and high BW for the voltage control loop using FIR filtering is presented in [7] and [8]. Although this method effectively removes double-line frequency ripple from the dc-bus voltage in steady states, it may introduce stability issues in the presence of disturbances and is sensitive to grid frequency changes. The stability of a PFC converter with reduced dc-bus capacitance using both linear time-invariant (LTI) and linear time-periodic (LTP) models is examined in [9]. The LTI model assumes constant system behavior over time, making it simpler and computationally efficient. However, the LTI model may not be suitable for PFC converters with reduced dc-bus capacitance, where system behavior significantly changes over time. Although the LTP model provides accurate stability analysis, its increased computational complexity is a disadvantage.

Load disturbance compensation through load current feedforward algorithms has been widely studied [10], [11]. While this approach offers the fastest response to output voltage changes caused by load variations, it requires additional current sensor circuitry with corresponding sampling and feedforward loop

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implementation [12]. However, feedforward current loops cannot address ac RMS voltage variations.

To maintain unity power factor (PF) and minimize THD, PFC circuits must respond rapidly to input voltage changes, necessitating a higher BW. Voltage feedforward compensation is widely used to counteract the effects of input voltage variations. This method involves sensing the input voltage and feeding it forward into the voltage control loop to pre-emptively adjust the reference current of the current control loop. Advancements in digital control techniques have enabled more precise and adaptive control of PFC circuits.

Digital controllers offer the flexibility to implement advanced phase-locked loop algorithms that can dynamically respond to changes in load and input conditions, improving the performance and reliability of PFC systems [13]. However, these methods often involve complex control algorithms and require sophisticated filtering techniques, such as notch filters (NFs), to mitigate odd harmonics distortion in the input current introduced by RMS ac filter and output voltage.

While variable frequency control methods like CrM and triangle control mode offer certain advantages, this design employs a continuous conduction controller (CCM), like conventional totem-pole PFC topologies. Unlike CrM/TM-based totem-pole PFCs, CCM operation inherently avoids negative current distortion, as the inductor current remains positive throughout each switching cycle. This eliminates the complexity associated with controlling negative current distortion and removes the requirement for current zero-crossing detection circuits or zero voltage switching control loops, simplifying the overall control implementation and enhancing robustness [14], [15], [16], [17], [18].

The motivation for this research stems from the increasing demand for improved PFC techniques that can balance dynamic response, stability, and harmonic distortion, particularly in high-power density applications. Conventional methods often struggle to achieve this balance, leading to compromises in THD, PF or dynamic response performance. Our ZCVC strategy offers a unique solution by leveraging the zero-crossing points of the input voltage to achieve precise control of the output voltage with fast dynamic response to any disturbances while keeping low THD, and high PF.

This article builds upon our previous work presented in [14], which introduced a high-power density interleaved 6.6 kW PFC design for ac/dc stage of a two-stage isolated bidirectional onboard charger. While focused on the hardware implementation and power density achievements, this manuscript significantly extends that work by introducing a novel zero crossing voltage control (ZCVC) strategy. The ZCVC approach offers substantial improvements in dynamic response, harmonic reduction, and computational efficiency compared to conventional PFC control methods. This approach simplifies the control algorithm and significantly reduces the computational burden on the microcontroller unit (MCU), as the control loop is executed only twice per grid cycle, compared to conventional methods that require, on average, a hundred times more executions. This article provides a comprehensive mathematical analysis, extensive simulations, and experimental validation of the ZCVC strategy, demonstrating its improved performance in maintaining dc voltage stability and unity PF across a wide range of operating conditions.

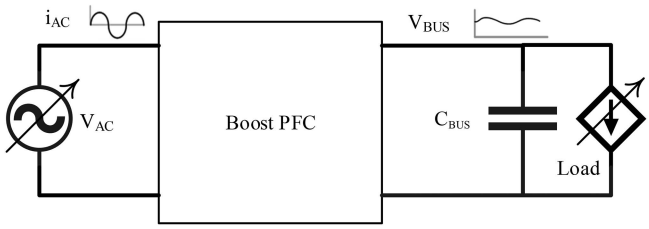

Fig. 1. Simplified single-phase boost PFC.

The primary contributions of this article are as follows:

1) Ensuring pure sinusoidal ac current during each half grid cycle and eliminating second harmonic distortion without the need for notch or comb filters.
2) Achieving high-BW input ac RMS filtering for feedforward voltage control without compromising total harmonic distortion (THD).
3) Providing a comprehensive framework for analyzing and designing PFC systems by deriving a mathematical steady-state average model.
4) Validating the proposed method through extensive simulations and practical implementation on a compact GaN-based interleaved totem pole PFC.

The remainder of this article is organized as follows: Section II presents a detailed overview of the proposed digital ZCVC methodology, including theoretical foundations and mathematical modeling. Section III describes the simulation setup and results, highlighting the effectiveness of the proposed methods under various operating conditions. Section IV gives the MCU implementation with corresponding block diagrams and state machine for safe operation of interleaved TTPPFC. Section V details the experimental validation on a GaN-based PFC prototype, comparing performance metrics with conventional PFC techniques. Finally, Section VI concludes the article.

II. PFC System and Control Approaches

A popular topology for high-power PFC applications is the interleaved totem pole topology, known for its ability to maximize efficiency, power density, and bidirectional power delivery. The bridgeless interleaved totem pole topology is selected as one of the most complex and practical PFC topologies. The proposed voltage loop controller is topology-agnostic and can be simply applied to other PFC topologies across a wide range of power ratings.

Fig. 2 illustrates the bridgeless interleaved totem pole PFC and its simplified sensing circuitry. S_1 and S_2, as well as S_3 and S_4, are complementary high-frequency GaN switches with a set dead-time to avoid shoot-through during switching transients. S_5 and S_6 are complementary grid frequency Si switches that are kept OFF during the grid voltage zero-voltage crossing detection (ZVCD) period. The minimum required measurements to ensure the controllability of the PFC system include inductor currents, output voltage, and input voltage.

The EMI filter is specifically designed to attenuate high frequency switching harmonics. However, grid frequency current

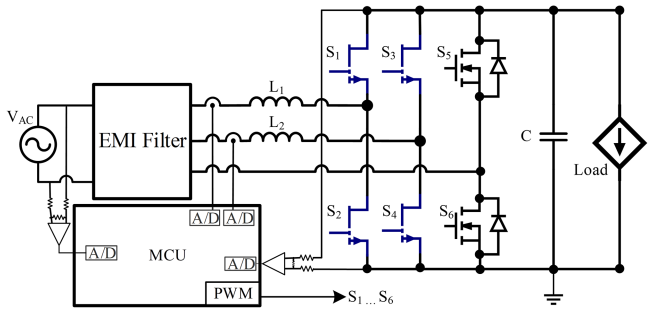

Fig. 2. Bridgeless interleaved Totem-Pole PFC and control block.

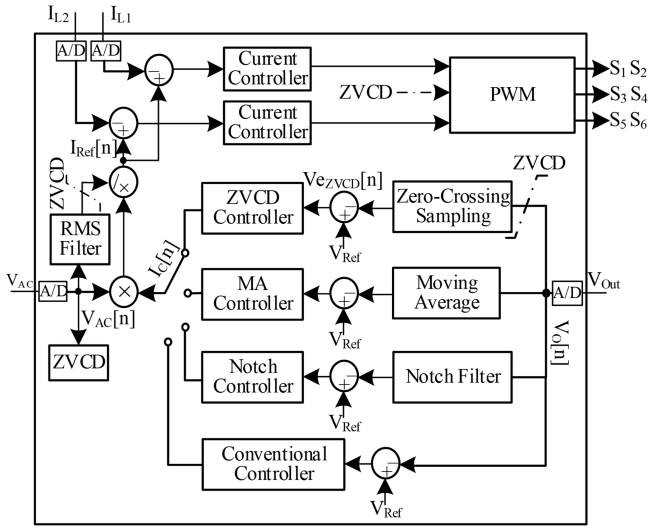

Fig. 3. MCU controller for proposed ZCVC and prior approaches.

harmonics cannot be effectively filtered by EMI filters. Consequently, it is critical to design an effective voltage loop controller that mitigates both input and output voltage measurement harmonics without compromising the system's dynamic response or increasing THD.

A. Voltage Loop Dynamic Model

The steady-state dynamic model of the interleaved PFC system is developed, considering various control strategies, including the conventional compensator, a controller with notch/comb filter, moving average (MA) controller, and the proposed ZCVC strategy, as illustrated in Fig. 3. These control approaches are implemented in both simulation tools and the MCU, allowing for comparative studies by switching between them. Steady-state conditions for the voltage loop compensator are defined by constant output current/power and fixed input RMS voltage.

Under steady state, the grid current is approximated by the controller reference current as follows:

$$I_{ref}(t) = \frac{I_C(t)\ V_{AC}(t)}{V_{RMS}(t)} \tag{1}$$

$$I_C(t) = \bar{I}_C + \tilde{I}_C(t) \tag{2}$$

$$V_{\text{RMS}}(t) = \bar{V}_{\text{RMS}} + \tilde{V}_{\text{RMS}}(t) \tag{3}$$

where I_C is the output of voltage controller loop. The filtered RMS voltage and compensated control signal exhibit second-order harmonics as their ac components:

$$\tilde{I}_C(t) = |H_c(j2\omega_g)| \times i_C \sin(2\omega_g t). \tag{4}$$

As the RMS value is derived from the absolute sampled values of $V_{AC}(t)$, the Fourier series will only contain cosine terms:

$$\tilde{V}_{\text{RMS}}(t) = \sum_{k=1}^{N} |H_{\text{RMS}}(j2k\omega_g)| \times v_{\text{RMS}}^{2k} \cos(2k\omega_g t). \tag{5}$$

Therefore, the reference current can be expanded as:

$$I_{\text{ref}}(t) = \frac{\left(\bar{I}_C + |H_c(j2\omega_g)| \times i_C \sin(2\omega_g t)\right) \times V_{\text{AC}}^{pk} \sin(\omega_g t)}{\bar{V}_{\text{RMS}} + \sum_{k=1}^{N} |H_{\text{RMS}}(j2k\omega_g)| \times v_{\text{RMS}}^{2k} \cos(2k\omega_g t)}. \tag{6}$$

The calculated steady-state reference current has an even component multiplied by $V_{\text{AC}}(t)$ resulting in only odd harmonics in the reference current.

THD of the injected grid current can be estimated from the reference current harmonics as follows:

$$\text{THD}_{\text{I}} = \frac{\sqrt{\sum_{m=2}^{\infty} I_m}}{\text{I}_1}. \tag{7}$$

where I_m is the mth harmonic of the reference current in (6). THD and reference current harmonics can be calculated through numerical analysis.

B. Digital Filters and Compensators

RMS filter block is simply defined as a first-order low-pass digital filter:

$$H_{\text{RMS}}(z) = \frac{1.11 \times \alpha}{1-(1-\alpha)z^{-1}} \tag{8}$$

where α is the filter coefficient, determining the cutoff frequency and response of the filter. A relatively high-BW ac input voltage RMS estimation in real-time is essential to ensure fast feed-forward compensation in the voltage loop when ac input voltage changes occur.

The implementation of a second-order digital NF is expressed as

$$H_{\text{Notch}}(z) = \frac{d_0 + d_1 z^{-1} + d_2 z^{-2}}{1 - c_1 z^{-1} - c_2 z^{-2}}. \tag{9}$$

Although the NF effectively reduces the second-order harmonic of the bus voltage from entering the voltage controller, it can affect the stability of the overall system during transients and startup. Therefore, a careful design process is required to achieve optimal performance.

A general form of a first-order digital compensator is employed for both current and voltage controllers

$$H(z) = \frac{b_0 + b_1 z^{-1}}{1 - a_1 z^{-1}}. \tag{10}$$

C. Proposed ZCVC Approach

The ZCVC executes the voltage compensator loop at each zero-crossing detection to provide a reference current for the current controller loops. Fig. 4 illustrates the sampling and

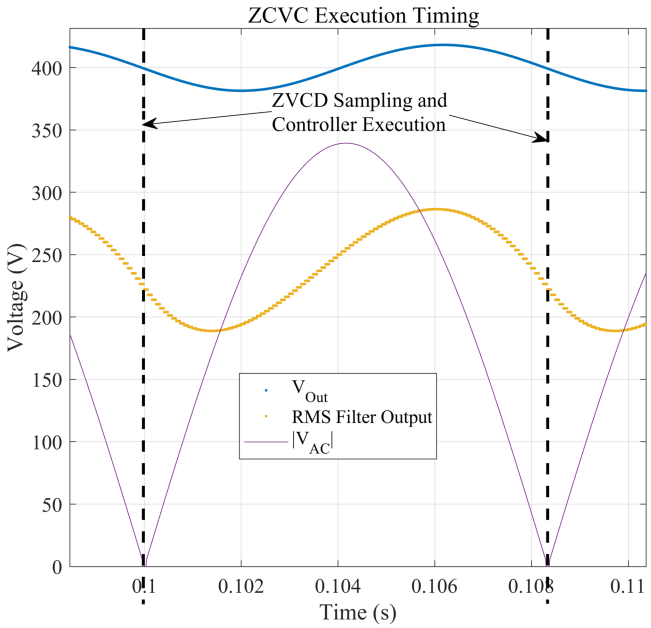

Fig. 4. Voltage Sampling and Controller Execution Timing in ZCVC.

execution timing. The reference current remains constant in each half grid cycle, resulting in a purely sinusoidal waveform.

By sampling at zero voltage crossing detection (ZVCD), as illustrated in Fig. 4, and mathematically derived in the Appendix section, we can show that the proposed ZCVC autonomously captures the average output voltage and average input RMS voltage without the need to reduce the compensator's BW for higher-order harmonic reductions.

The ZCVC approach results in $|H_c(j2\omega_g)|= 0$ and $|H_{\text{RMS}}(j2k\omega_g)|= 0$ for all grid frequency harmonics, theoretically eliminating all harmonics in the reference current. This significantly improves THD while maintaining a high-BW dynamic response.

D. Alternative Controller Approaches

In addition to the conventional voltage control, alternative approaches, such as MA and notch/comb filter methods have been proposed in the literature. The block diagram of these controllers is shown in conjunction with the proposed ZCVC method in Fig. 3. The notch/comb filter approach includes an additional calculation process, denoted as $H_{Notch}(z)$ compared to the conventional compensator controller.

While the NF effectively eliminates second harmonic oscillations in the output voltage, it compromises dynamic response to output voltage changes and increases memory and CPU usage. The MA controller includes an MA filter block that averages the output voltage at a reduced sampling frequency to mitigate the second harmonic before executing the MA voltage control.

The MA method employs a simple FIR filter with an order of N_{MA} as follows:

$$H_{\text{MA}}(z) = \frac{1}{N_{\text{MA}}} \sum_{k=0}^{N_{\text{MA}}-1} z^{-k}. \tag{11}$$

TABLE I
PFC System and Circuit Parameters

Input AC Voltage	240 V (85 – 265 V), 60 Hz (45 – 65) Hz
Output Voltage	355 – 425 V
Max Power	7200 W (3600 W per phase)
Switching Frequency	120 kHz CCM
Inductors	$2 \times 100\ \mu$H Interleaved
Capacitors	$3 \times 470\ \mu$F
RMS filter	$\alpha = 0.02$ (cut-off frequency ≅ 380Hz) $k_1 = 1.63$, $k_2 = 14.1$ for α<0.05
Notch filter	Notch frequency = 120 Hz, Bandwidth = 10 Hz, Sampling freq. = 12 kHz ($d_0 = 0.9999$, $d_1 = -1.9997$, $d_2 = 0.9999$, $c_1 = -1.9997$, and $c_2 = 0.9997$)
Current controller	Bandwidth = 10kHz, phase margin = 50 ° Sampling freq. = 120 kHz ($b_0 = 0.01$, $b_1 = 0.005$, $a_1 = 1$)
Voltage controller Conventional and Notch/Comb	Bandwidth = 12Hz, phase margin = 50 ° Sampling freq. = 12 kHz ($b_0 = 0.0024$, $b_1 = 0.0012$, $a_1 = 0.995$)
Voltage controller Moving Average	Bandwidth = 12Hz, phase margin = 50 ° Sampling freq. = N_{MA}×120Hz ($b_0 = 0.24/N_{MA}$, $b_1 = 0.12/N_{MA}$, $a_1 = 0.995$, $N_{MA} \geq 4$)
Voltage controller (Proposed ZCD)	Bandwidth = 48Hz, phase margin = 50 ° Sampling freq. = 120Hz ($b_0 = 0.24$, $b_1 = 0.12$, $a_1 = 0.995$)

The MA voltage controller can significantly reduce computational costs compared to conventional and NF approaches. The number of voltage controller executions in each grid cycle is determined by $N_{\text{MA}} \geq 4$. However, it is recommended in the literature to choose $N_{\text{MA}} \geq 16$ to reduce current waveform deformation during transients.

III. Simulation Results

A. PFC System Design Parameters

Table I gives the specifications of the studied PFC system, including its circuit parameters and the designed controllers and filters for different control approaches.

In digital PFC, we typically need to multiply the sinusoidal ac voltage by the output of the voltage loop compensator to generate a near-sinusoidal reference current for the current loops. The resolution of ac voltage samples directly impacts the accuracy of the generated reference current, which is crucial for reducing THD in digital controllers. A higher sampling rate allows for more precise tracking of the ac waveform, enabling better PFC and lower THD. The choice of approximately 200 samples per grid cycle represents a balance between accuracy and computational efficiency for many digital PFC applications.

The desirable performance of a stable PFC controller can be assessed by the following factors as the main motivation of the proposed ZCVC:

1) Fast response to ac voltage and load changes.
2) Short settling time (high BW).

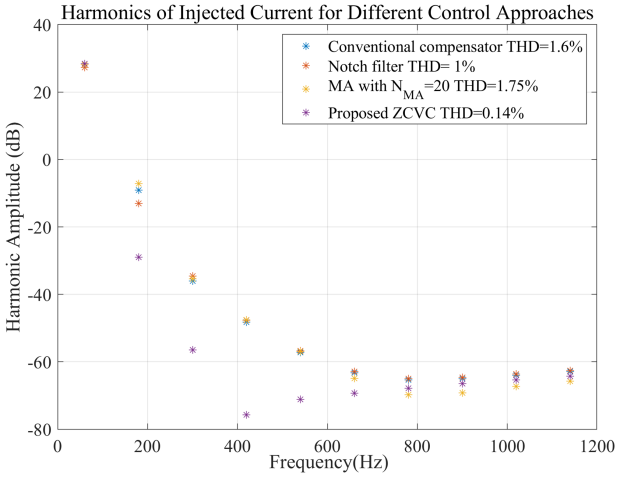

Fig. 5. Theoretical current harmonics of the proposed ZCVC compared to prior methods (α= 0.002).

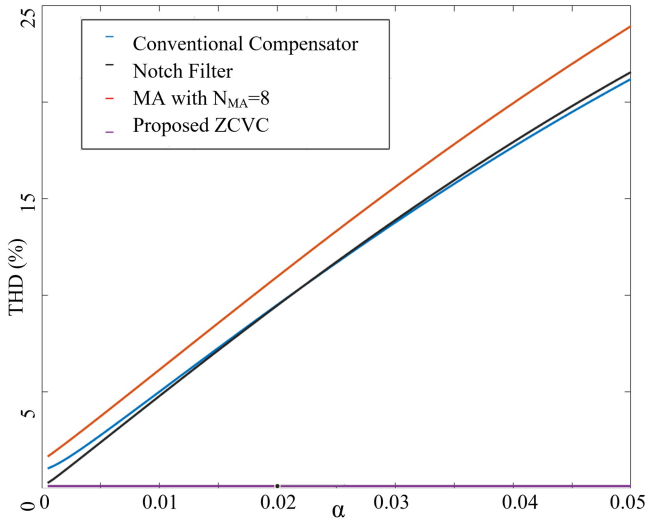

Fig. 6. Theoretical THD simulation results comparison versus α value.

3) High PF.
4) Low voltage drift.
5) Simple control.
6) Low THD.

All these factors are investigated and compared for the proposed ZCVC approach.

B. RMS Filter Versus Current Harmonics

Fig. 5 compares the reference current harmonics and THD of the studied voltage control approaches, based on the PFC system design parameters given in Table I, with $\alpha = 0.002$ (RMS filter cut-off frequency $\approx$ 38Hz). All approaches, except the proposed ZCVC, fail to reduce the higher-order harmonics introduced by the RMS filter in the voltage loop. This result in approximately 10% reference current THD when the RMS filter BW increases to 380 Hz, which is crucial for achieving a relatively fast dynamic response to input voltage changes, especially in islanded mode detection and UPS applications.

On the other hand, the proposed ZCVC method consistently maintains a reference current THD of less than 0.15% even with a high BW RMS filter, as shown in Fig. 6. In contrast, THD increases with higher RMS filter BW for the MA, NF, and conventional approaches. The ZCVC approach effectively keeps THD below 0.15% across the entire range of the α coefficient. The NF approach, however, is less effective at higher α values as it struggles to filter out the higher harmonics introduced by the RMS filter into the voltage loop.

C. PFC Response to Step Load Change

Fig. 7 presents the simulated waveforms of the interleaved PFC system using the NF controller. The NF controller demonstrates stability up to a 40% step load change.

Beyond this threshold, the transient voltage drop can approach the grid ac voltage, potentially leading to fault conditions.

The settling time for the NF approach is approximately four grid cycles, which closely aligns with the 12 Hz BW of the

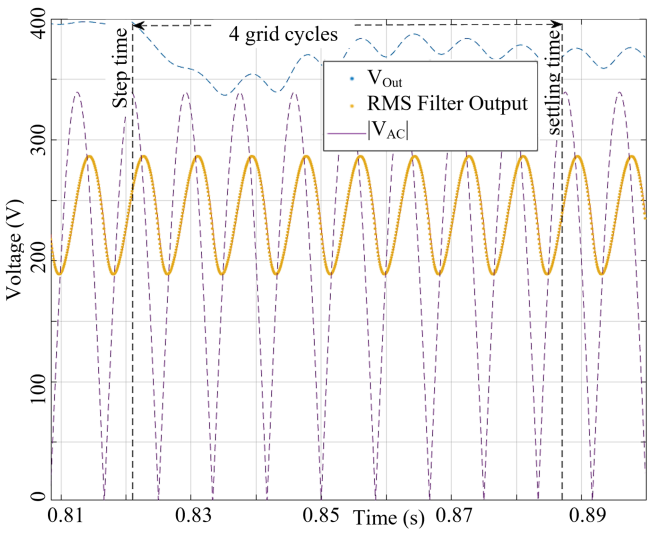

Fig. 7. Voltage response of NF method to 40% step-load.

designed controller as specified in Table I. Fig. 8 displays the average current waveforms of the phase inductor current and interleaved current, along with their corresponding ripple areas for the NF approach. Notable deformation in the current waveform is observed, where it deviates from a symmetric shape in each half cycle. This deformation results in a lower power factor (PF) and higher THD.

To mitigate current waveform deformation, one could reduce the RMS filter BW. However, this reduction is generally undesirable in most PFC applications due to its impact on system performance.

Fig. 9 illustrates the state transitions of the PFC system—interleaved current and output voltage—using eight-shape trajectories for the NF approach. A significant downside of conventional approaches is the noticeable voltage drift, which reduces the stability region of the PFC system, especially under high

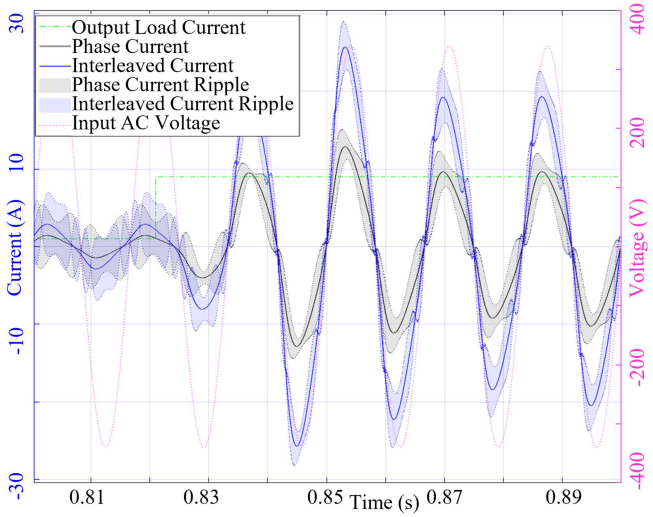

Fig. 8. Interleaved current waveforms of NF method.

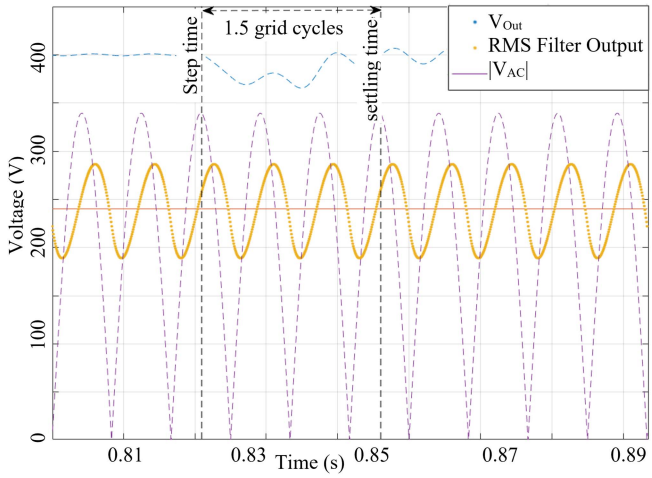

Fig. 10. Voltage response of proposed ZCVC to 40% step-load.

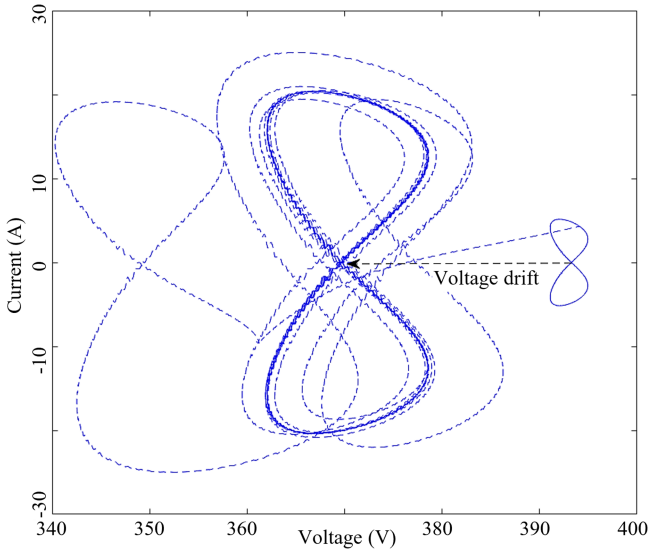

Fig. 9. 8-shape trajectories of NF method in response to 40% step-load.

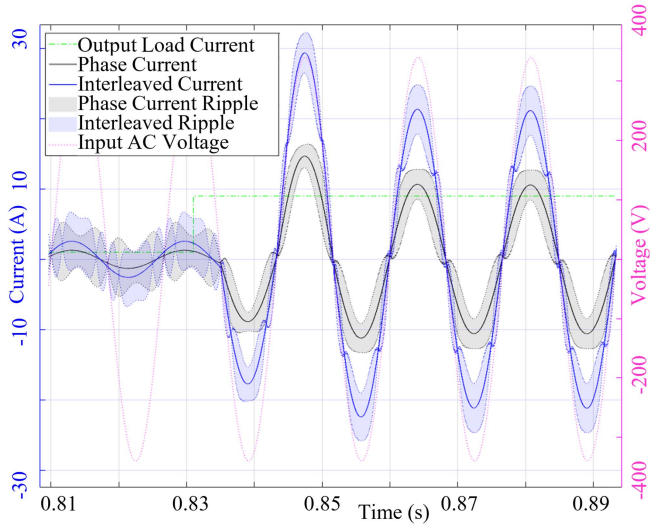

Fig. 11. Interleaved current waveforms of proposed ZCVC approach.

load conditions. To address voltage drift, several solutions are typically considered.

1) *Adding More Output Capacitors:* This approach reduces power density and increases cost.
2) *Increasing Voltage Loop Compensator Bandwidth:* While this may reduce voltage drift, it also increases THD, lowers PF, and reduces phase margin, which is generally undesirable.
3) *Employing a Higher Order Voltage Compensator:* Add complexity and demands more CPU and memory resources, requiring careful design and optimization.

For a fair comparison, all approaches are evaluated under the same conditions to highlight the advantages of the proposed ZCVC. The same simulation conditions applied to the proposed ZCVC controller reveal substantial improvements in performance, as shown in Figs. 10 and 11. The settling time for the ZCVC approach is notably reduced to approximately 1.5 grid cycles—around three times faster—compared to conventional methods. This improvement is achieved with no overshoot, minimal transient voltage drops, less than 1 V voltage drift, and an increased step load change capability of up to 90%, as illustrated in Fig. 12.

The key advantage of the ZCVC approach lies in its sampling at the input ac voltage zero crossing. This technique effectively filters out all harmonics introduced by the high BW RMS filter and output voltage, enhancing overall system performance.

Fig. 13 compares the steady-state PF across the entire output current range of the interleaved PFC under different control strategies. The ZCVC approach demonstrates a unity PF for loads above half capacity and significantly better PF performance compared to alternative approaches under light load conditions.

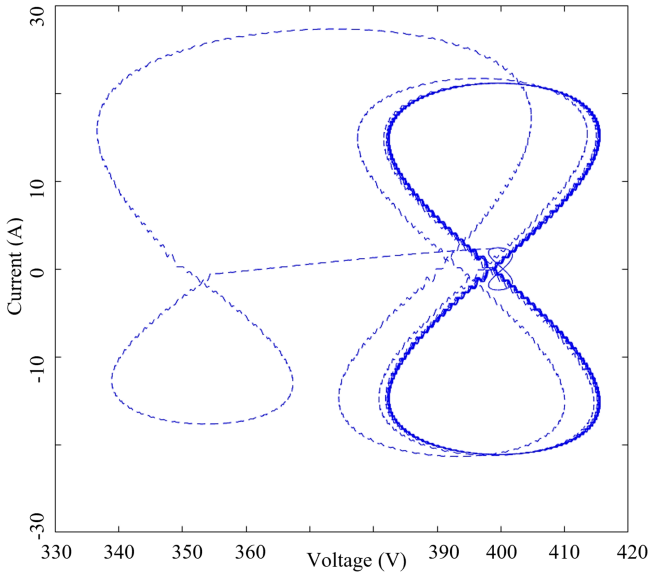

Fig. 12. Eight-shape trajectories of ZCVC in response to 90% step-load.

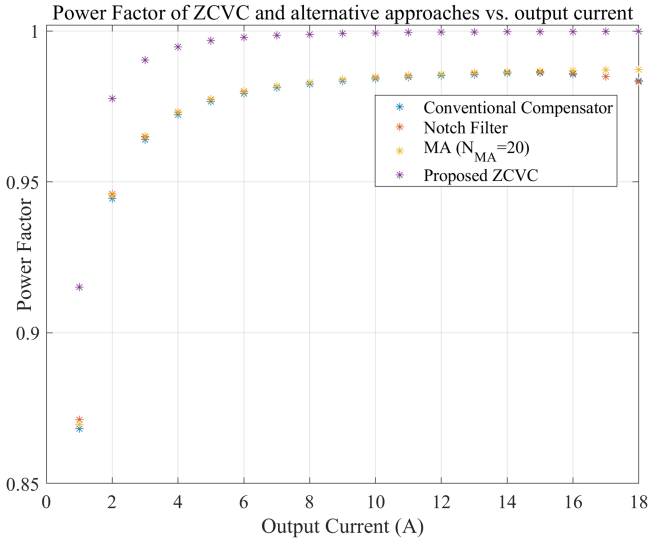

Fig. 13. Power factor of ZCVC compared to prior methods ($\alpha = 0.02$).

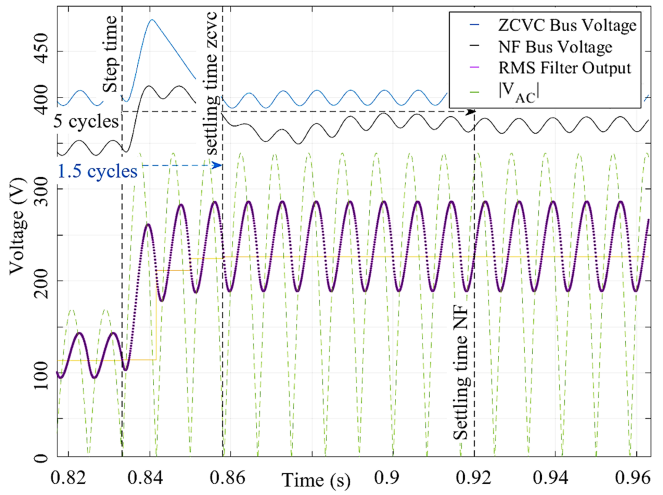

Fig. 14. Proposed ZCVC vs. NF voltage response to 100% AC voltage step up.

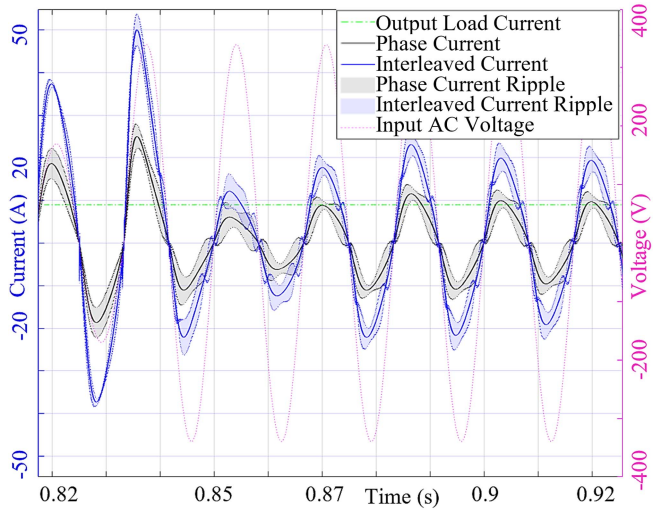

Fig. 15. Interleaved current waveforms of NF method in response to 100% AC voltage step up.

D. PFC Response to Step AC Voltage Change

The proposed ZCVC approach introduces a maximum delay of half a cycle in response to changes in the ac input voltage.

To evaluate the PFC system's performance under this condition, we consider the worst-case scenario from the perspective of the ZCVC approach. If a step-up in ac voltage occurs precisely at the zero crossing, the current waveform will increase at the same rate during the first half-cycle. This rapid change could potentially exceed the maximum current ratings of the switches or passive components and could cause maximum delay in ZCVC controller action. To mitigate this risk, a reference current limiter, as shown in Fig. 3, is implemented. Figs. 14, 15, and 16 illustrate the PFC voltage and current states in response to an input ac voltage step-up from 120 to 240 V under a 9-A output current. The ZCVC approach demonstrates a settling time of just 1.5 grid cycles, producing clean sinusoidal current waveforms without deformation and with near-zero voltage drift.

In this worst-case scenario, the output voltage may increase during the half-cycle delay of RMS voltage sampling in the ZCVC approach, as depicted in Fig. 14. This half-cycle output voltage rise during the ac voltage step-up limits the permissible range of voltage increase to protect the output capacitors from peak voltage stress. Fig. 17 shows the output voltage peak overshoot when a step-up ac voltage occurs from 120 V to a range of 150 to 240 V at zero crossing, under various output current conditions. This curve is critical for selecting appropriate output capacitors and protection circuitry.

Moreover, the proposed ZCVC can handle large step ac voltage changes at the arbitrary point in about 1.5 grid cycles.

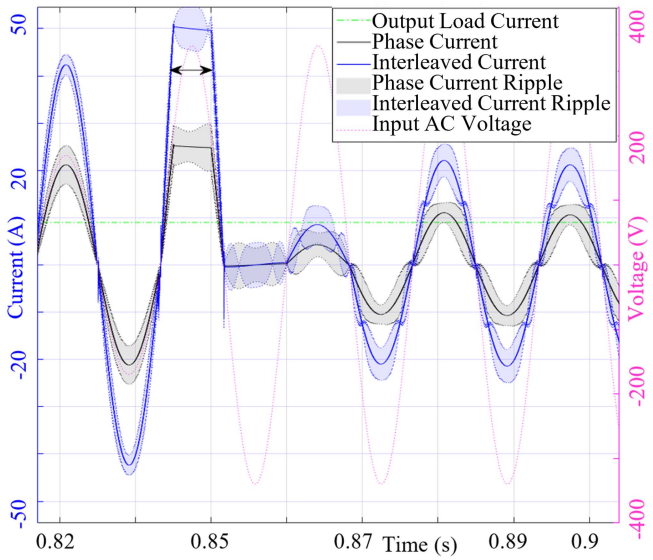

Fig. 16. Interleaved current waveforms of proposed ZCVC method in response to 100% AC voltage step up.

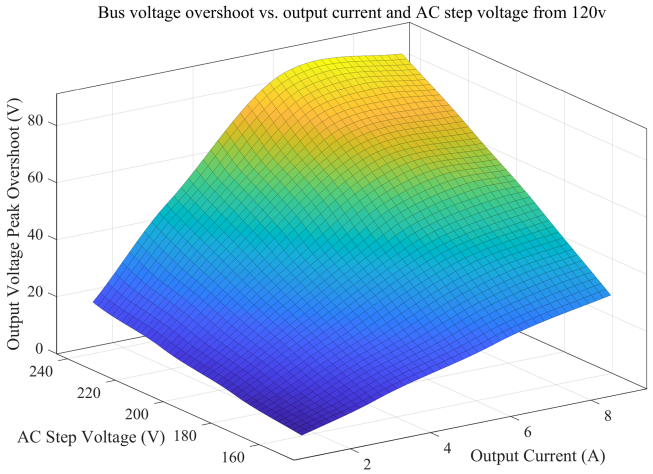

Fig. 17. Output voltage overshoot (above 400 V) versus output current and step-up AC voltage from 120 V.

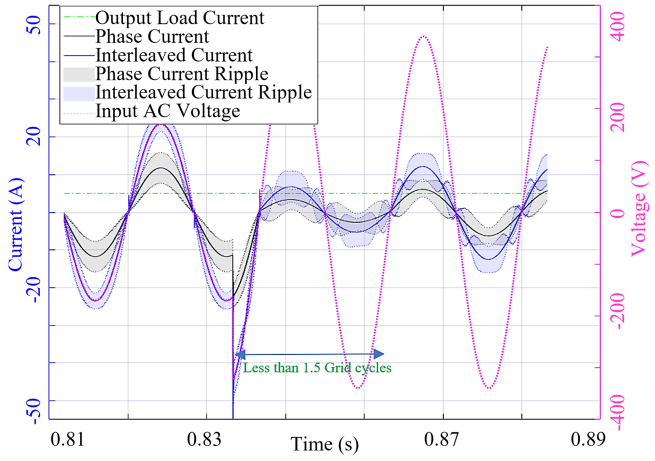

Fig. 18. Interleaved current waveforms of proposed ZCVC method in response to 100% AC voltage step up at nonzero crossing voltage point.

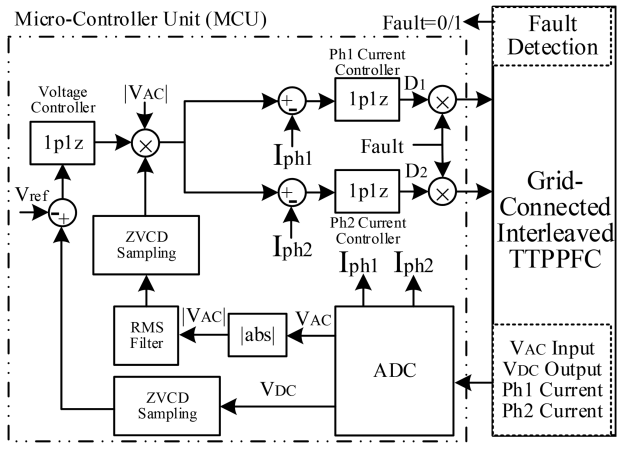

Fig. 19. Control block diagram of the proposed interleaved TTPPFC.

The response to sharp ac voltage change is only related to the stability of current controllers that is considered with 50° phase margin in our proposed current controller. Fig. 18 illustrates the fast dynamic response to a nonzero crossing ac voltage change. The robustness and stability of the proposed controller are verified through large step responses to both output load and input ac voltage, as emphasized in this manuscript. To mitigate the effects of noise at the zero-crossing point, several measures have been implemented: the RMS filter serves as a low-pass filter, and the ac reference voltage measurement is processed through a second-order Op-Amp conditioning circuit, which significantly reduces higher harmonics and voltage spikes or dips before sampling by the MCU's ADCs. Additionally, an adjustable zero-crossing window is incorporated in practical implementation to further reduce susceptibility to noise during zero-crossing detection.

IV. PFC MCU Implementation

Fig. 19 shows the closed loop controller block diagram implemented in MCU with relevant measurements and fault protection. The PFC stage needs protection and soft start/stop for a proper and safe operation. Hence, a state machine controller design is essential. Fig. 20 illustrates the proposed state machine algorithm implemented in MCU.

The following system states are considered:

1) WAIT/IDLE: Calibration, and check if PFC is ready.
2) INIT: Initializing the registers and peripherals.
3) START: Soft-starting and bus voltage ramp-up.
4) RUN: Continuous load following.
5) STOP/FAULT: If any fault or error occurs.

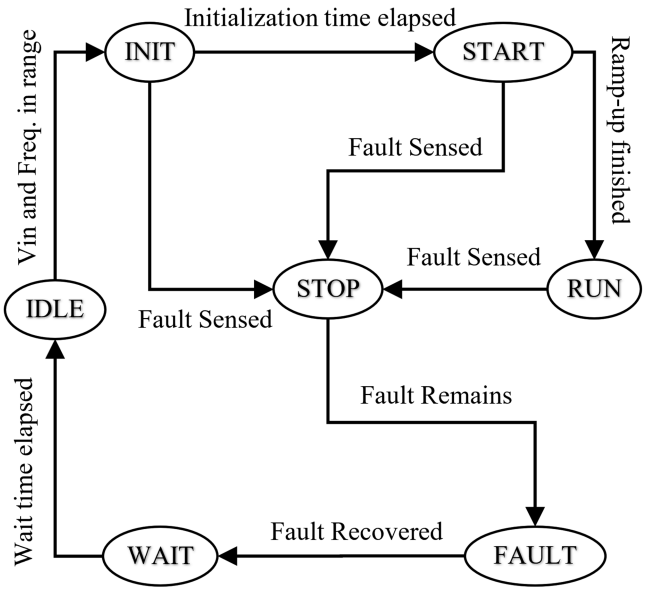

Fig. 20. PFC controller state machine.

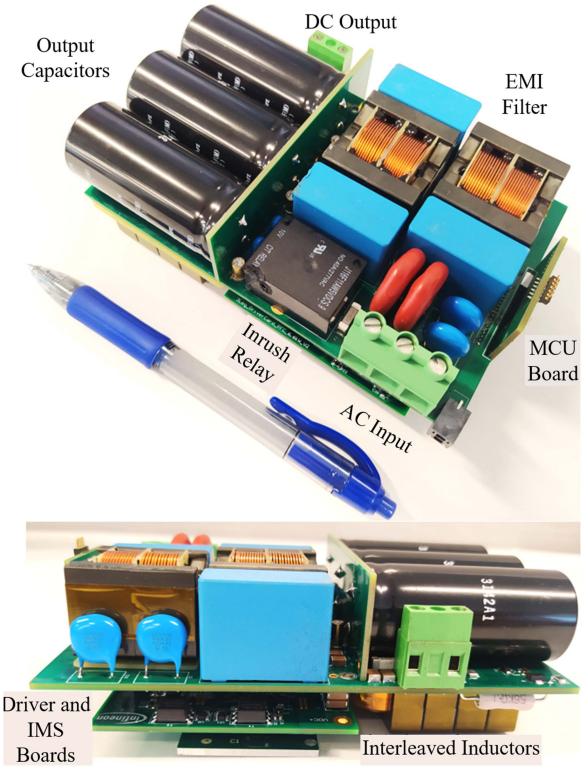

Fig. 21. Top and side view of designed 7.2 kW interleaved TTPPFC [14].

V. Experimental Results

A. Interleaved PFC Hardware

The Interleaved TPPFC design, as shown in Fig. 21, uses automotive grade Enhanced mode GaN device GS-065-060-5-B-A and IPT60R028G7 Si CoolMOS from Infineon for the two interleaved high frequency legs and the grid frequency leg,

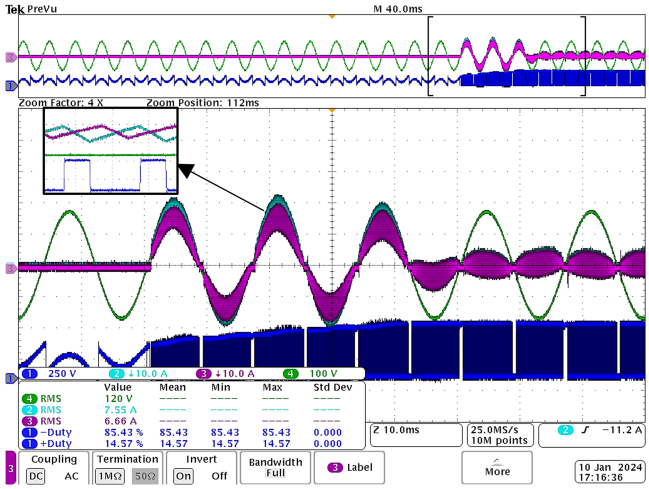

Fig. 22. Rectifier mode soft start performance.

Fig. 23. Dynamic response of ZCVC PFC controller for step-up load change (400 to 3200W).

respectively [14]. The prototype in Fig. 21 is mounted on a $14 \times 8 \times 4$ cm aluminum Heatsink with two 4×4 cm axial fans, each providing 7 CFM airflow, to ensure active cooling under ambient lab conditions. The input ac voltage and power ratings as well as passive component values are given in Table I.

Soft start implementation is critical and the soft-start experimental test under no-load conditions in rectifier mode is shown on Fig. 22. Fig. 22 also shows zoomed inductors' currents and V_{DS}. The designed TTPPFC shows smooth operations with stable voltage and current loops under proposed ZCVC.

B. PFC Dynamic Responses

The transient response of the proposed ZCVC has been evaluated by applying negative and positive step changes to output power and input ac voltage.

The results provided in Figs. 23 and 24 verifies stable and smooth dynamic response under load step changes.

The step changes in output load are regulated by ZCVC and the step changes in ac input voltage are regulated by high BW feedforward control and ZCVC.

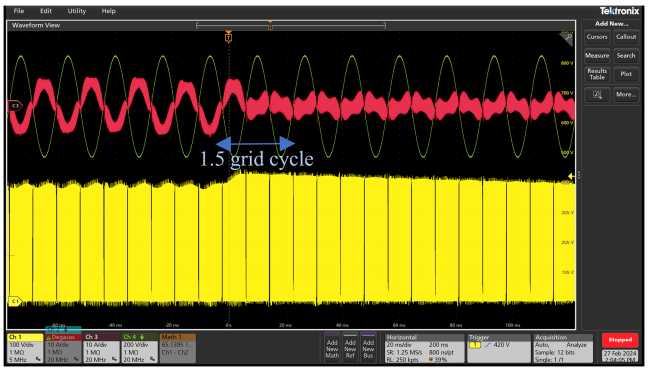

Fig. 24. Dynamic response of ZCVC PFC controller for step-down load change (3200 to 400 W).

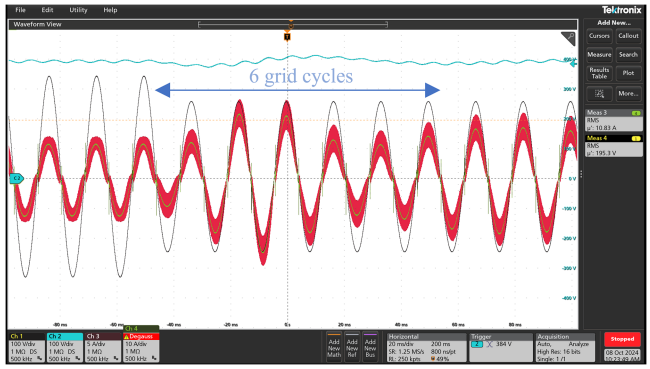

Fig. 27. NF dynamic response for input voltage step change (240to 150 V) at 3 kW load.

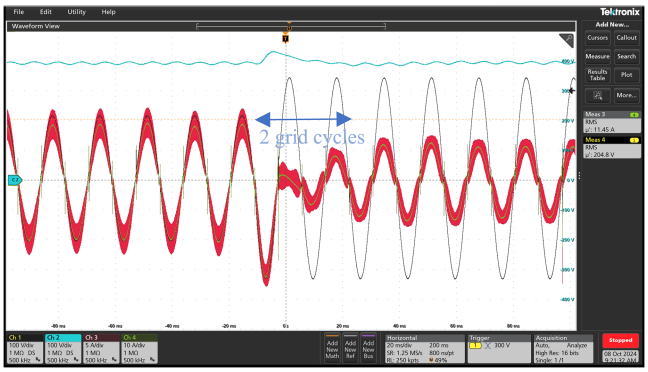

Fig. 25. ZCVC dynamic response for input voltage step change (120 to 240 V) at 2 kW load.

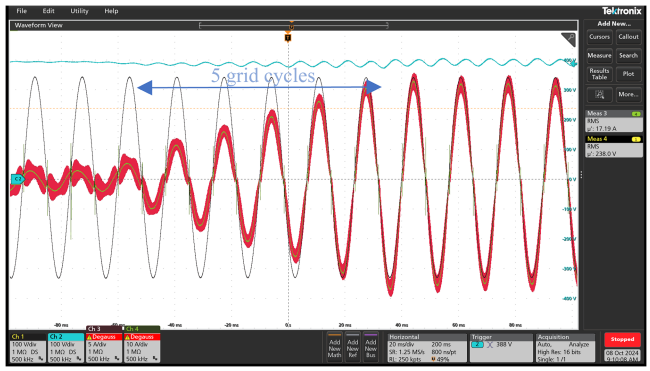

Fig. 28. Dynamic response of MA control approach with $N_{\mathrm{MA}} = 8$ for step-up load change (800 to 6000W).

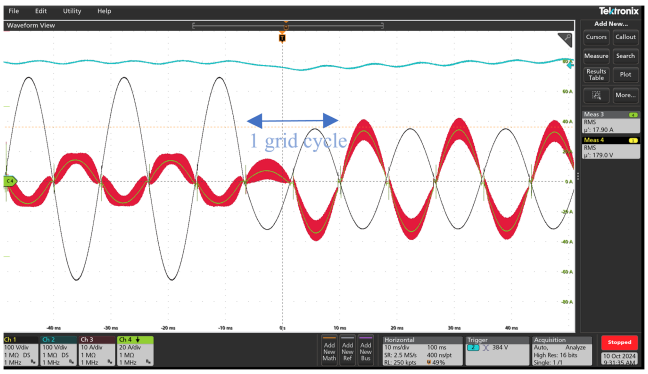

Fig. 26. ZCVC dynamic response for input voltage step change (240 to 120 V) at 3 kW load.

The RMS value of input ac voltage is sampled in zero crossing voltage, and the changes are applied to the next half-cycle ac reference current to ensure a stable, robust, and smooth transient response.

The results provided in Figs. 25 and 26 verify stable and smooth dynamic response under ac input voltage step change.

Experimental results for ac input voltage change using NF approach, and for load change using MA approach are shown in Figs. 27 and 28.

TABLE II
PERFORMANCE COMPARISON WITH PRIOR APPROACHES

Index	Conventional [1], [6], [9], [13]	NF [4], [7], [10]	MA [5], [8]	ZCVC
Settling time	85 ms	82 ms	78 ms	20-30 ms
Inductor Current Distortion	High	High	High	Low
Robustness to state variations	Low	Low	Medium	High
Design Process	Simple	Complex	Complex	Simple
Power Factor	0.982	0.986	0.989	0.999
Voltage drift at full load	High	High	High	Very Low
Max load step change	40%	42%	40%	90%
loop calculations and sampling	200 per grid cycle	200 per grid cycle	$200/N_{\mathrm{MA}}$ per grid cycle	Two times per grid cycle
Extra Filter	No	Yes (200 per grid cycle)	Yes ($200/N_{\mathrm{MA}}$ per grid cycle)	No

The settling time for the NF and MA voltage controllers are measured between 5 to 6 grid cycles. The proposed ZCVC shows over four times faster dynamic response. Table II compares the performance of the proposed ZCVC approach with prior controllers based on the specifications and the PFC hardware

TABLE III
POWER FACTOR COMPARISON WITH PRIOR APPROACHES

	Conventional	NF	ZCVC
1.5 kW	0.932	0.945	0.979
3.6 kW	0.965	0.969	0.996
7.2 kW	0.972	0.974	0.999

TABLE IV
THD COMPARISON WITH PRIOR APPROACHES

	Conventional	NF	ZCVC
1.5 kW	13.7%	12.4%	4.8%
3.6 kW	11.6%	11.1%	3.7%
7.2 kW	10.4%	10.1%	3.3%

TABLE V
EFFICIENCY COMPARISON WITH PRIOR APPROACHES

	Conventional	NF	ZCVC
1.5 kW	98.85%	98.89%	99.02%
3.6 kW	98.68%	98.72%	98.85%
7.2 kW	98.15%	98.21%	98.35%

design given in Table I. The ZCVC approach demonstrates a significantly improved dynamic response and robustness to variations in load, RMS voltage, and frequency, requiring 100 times fewer computations than conventional methods. Additionally, the proposed method eliminates the need for extra filters, such as notch, comb, or MA filters, resulting in substantial savings in processing time and memory compared to more advanced approaches.

C. Steady State Results

PF and THD of the grid current as well as the PFC efficiency are measured for light-load, half-load and full-load conditions.

Conventional, NF, and proposed ZCVC approaches are implemented for comparison. Tables III, IV, and V give the PF, THD, and efficiency results, respectively. The test condition is as in Table I with high BW RMS filter. The difference between results in the conventional methods studied are incremental and compared in Tables II, III, and IV. On the other hand, the proposed ZCVC shows considerably improved performance.

VI. CONCLUSION

This article introduces a novel digital ZCVC methodology for PFC applications, offering significantly improved dynamic performance. The ZCVC strategy maintains constant peak ac current, eliminates second harmonic distortion, and achieves high-BW input ac RMS filtering without compromising THD.

Simulation and experimental results validate the ZCVC method's effectiveness, demonstrating improved dynamic response, faster settling time, and reduced computational burden compared to conventional techniques. Implementation on a 7.2 kW GaN-based high power density interleaved totem pole PFC confirmed its practical viability.

The proposed controller offers significantly faster settling time (approximately 1.5 grid cycles) compared to conventional methods (4–6 grid cycles). The ZCVC method demonstrates improved dynamic response to load and ac voltage changes, with the ability to handle up to 90% step load changes. It maintains unity PF and low THD across a wide range of operating conditions. Additionally, the ZCVC approach substantially reduces computational burden, requiring only two executions per grid cycle compared to a typical range of 200 for conventional methods.

This research contributes significantly to power electronics, offering a promising solution for high-performance and high-density power conversion systems. Future work could explore ZCVC applications in other power conversion topologies and its potential for optimization in specific industrial applications.

APPENDIX
PROOF OF ZCVC AVERAGE VALUE SAMPLING

The output voltage contains a dc value and an ac component. The output capacitor current can be written in the steady state as follows:

$$I_{\text{Cout}}(t) = |I_{\text{in}}\sin(\omega_g t)| - \frac{2I_{\text{in}}}{\pi}. \tag{A1}$$

Hence, the ac variation of output voltage can be derived as follows:

$$\begin{aligned}\tilde{V}_{\text{out}}(t) &= \int_0^{2\pi/\omega_g} I_{\text{Cout}}(t) \\ &= \begin{cases} -\frac{2I_{\text{in}}t}{\pi} - \frac{I_{\text{in}}\cos(\omega_g t)}{\omega_g} + \frac{I_{\text{in}}}{\omega_g} & 0 \le t \le \frac{\pi}{\omega_g} \\ -\frac{2I_{\text{in}}t}{\pi} + \frac{I_{\text{in}}\cos(\omega_g t)}{\omega_g} + \frac{3I_{\text{in}}}{\omega_g} & \frac{\pi}{\omega_g} \le t \le \frac{2\pi}{\omega_g} \end{cases}.\end{aligned} \tag{A2}$$

As shown above, the ac component of output voltage is sinusoidal with double grid frequency. Therefore, its value at ZVCD is zero, and we only sample the dc component of output voltage using ZCVC.

The rectified ac input voltage is the input of the first order RMS filter in (8). Assuming the sampling frequency to be much higher than grid frequency, we can show the normalized output of the RMS filter in time domain as follows:

$$V_{\text{RMS}}(t) = 1.11 \times \left(\frac{2}{\pi} + \frac{4}{3\pi} \sum_{k=1}^{N} \frac{\alpha}{\sqrt{\alpha^2 + \left(\frac{2k\omega_g}{f_s}\right)^2}} \cos(2k\omega_g t) \right) \tag{A3}$$

where f_s is the sampling frequency. The above equation shows that the ac value of calculated RMS at ZVCD is zero. However, sampling the input RMS voltage at ZVCD may lead to an error for higher values of α, $\alpha > 0.01$, and due to the sampling delay. Therefore, a correcting factor can be driven and added to (8) to compensate for the error as follows:

$$H_{\text{RMS\_comp}}(z) = \frac{H_{\text{RMS}}(z)}{\sin(k_1\alpha + k_2)} \tag{A4}$$

where k_1 and k_2 are constant values to correct the ZCVC RMS filter error for higher values of α. We can approximate these values with high accuracy for applicable range of α using (A4).

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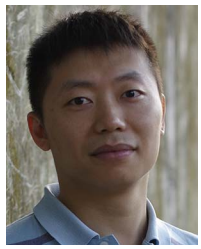

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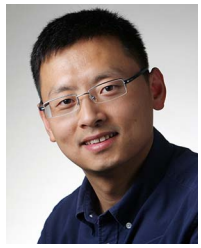

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