# Turn-OFF Delay Time Based Online Junction Temperature Monitoring for SiC MOSFETs Over Aging

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***Abstract*—Junction temperature ($T_j$) is a crucial quantity for monitoring the working condition of semiconductors in power converter operation. Online $T_j$ measurement can be achieved by the thermo-sensitive electrical parameters (TSEPs), which should have an appropriate correspondence between itself and $T_j$. Among various TSEPs, the turn-OFF delay time ($t_{d\_off}$) shows good performance of sensitivity and linearity for online $T_j$ measurement. However, parameter offset may occur in TSEPs during the aging process of devices, which causes errors in temperature measurement. This article proposes an online condition monitoring method to achieve junction temperature assessment for SiC MOSFETs over aging. The error caused by aging can be eliminated by updating $t_{d\_off}$ versus $T_j$ relationship with the proposed aging compensation method. Moreover, an auxiliary circuit is proposed for accurate and fast detection of $t_{d\_off}$. Experimental results have been given to verify that the proposed condition monitoring method can achieve accurate temperature detection under both healthy conditions and aging conditions of SiC MOSFETs.**

***Index Terms*—Aging detection, condition monitoring, junction temperature, SiC MOSFETs, thermo-sensitive electrical parameters (TSEP).**

## I. Introduction

JUNCTION temperature is one of the critical parameters for evaluating reliability of power semiconductor devices [1]. Under severe operational conditions, semiconductor devices have potential risks of failure if their junction temperatures exceed the safe temperature range for operation. Frequent repetition of thermomechanical stresses caused by long-term temperature variations will also damage the device internal structure, thus leading to chip-related and package-related degradations [2]. Research works have shown that thermally induced failure accounts for 55% of all failures in semiconductor devices [3].

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Temperatures can be measured by optical sensors, infrared (IR) camera and contact-based temperature transducers [4]. However, these methods for junction temperature measurement are usually invasive to devices because the sensors and transducers have to be mounted inside the devices. On the other hand, the methods like finite element method (FEM), electro-thermal model, and thermo-sensitive electrical parameters (TSEPs), are noninvasive measurement methods. By modeling the structure of device package, FEM can simulate chip temperature and spatial temperature distribution with high accuracy [2]. However, low computational efficiency of FEM makes it unsuitable for real-time temperature measurement. Electro-thermal model is another way to extract junction temperature indirectly [5]. Thermal characteristics of power conversion system can be described as thermal equivalent circuits, where the parameters can be obtained by manufacturers' datasheet. However, the practicability and accuracy of this method have been doubted, since electro-thermal parameters in the datasheet may often anticipate worst-case scenarios [6]. In other words, junction temperature calculated by electro-thermal model is expected to be higher than actual temperature. In addition, parameters of thermal equivalent circuits vary with degradation level of devices [7]. Thus, calculation results are not always accurate if the electro-thermal model is not calibrated for device aging condition.

TSEPs have been widely adopted for temperature monitoring of power devices [8]. TSEP method can be performed on fully packaged devices, and temperature monitoring is effective for steady-state and transient conditions [4]. Although the measurement of TSEP requires additional auxiliary circuits, extra circuits composed of cost-effective components can be simply plug-in or integrated into driver circuits during the design stage. Therefore, the TSEP method is an effective way to determine junction temperature of semiconductor devices.

Proper TSEP needs to be selected to be specifically suitable for online junction temperature measurement. Classical TSEPs for semiconductor devices include voltage drop at low current [9], short-circuit current [10], and saturation current [11]. Paper [12] lists the main existing TSEPs for semiconductor devices, and the detailed performance of different TSEP candidates is analyzed on the basis of the sensitivity, linearity, genericity, calibration, and online implementation. However, these research

TABLE I
SUMMARY OF TSEPS FOR ONLINE JUNCTION TEMPERATURE MEASUREMENT IN SIC MOSFET

| TSEP | Linearity | Sensitivity | Aging Mode |
|---|---|---|---|
| $V_{\text{th}}$ [16] | Medium | Good | Gate oxide |
| $R_{ds\_on}$ [13] | Not good | Low in SiC device | Gate oxide Packaging |
| Turn-ON $dI_d/dt$ [14] | Medium | Good at large $R_g$ | Gate oxide Packaging |
| $t_{d\_on}$ [17] | Good | Good at large $R_g$ | Gate oxide |
| $t_{d\_off}$ [15] | Good | Good at large $R_g$ | Gate oxide Packaging |

works mainly focus on insulated-gate bipolar transistors (IGBTs), and the use of TSEPs in silicon carbide (SiC) devices is relatively less. Due to the difference in physical structure and aging mechanisms between Si devices and SiC devices, there are differences in selection criteria for evaluating TSEPs. In addition, SiC devices have lower ON-state resistance and faster switching speed than IGBTs, which raises new requirements for the accuracy and bandwidth in TSEP measurement. For instance, ON-state resistance $R_{ds\_on}$ has been utilized as the TSEP for SiC devices [13]. However, the variation of millivolt-level ON-state voltage drop $V_{ds\_on}$ needs to be identified to ensure the accuracy of temperature monitoring. Turn-ON current rate $dI_d/dt$ also has been used for temperature measurement of SiC devices [14]. But the imperfectly linear relationship between $dI_d/dt$ and $T_j$ in SiC MOSFET makes it unsuitable for accurate estimation of $T_j$. Table I summarizes various TSEPs of SiC MOSFET for online $T_j$ measurement. Based on comparison, turn-OFF delay time $t_{d\_off}$ has been proven to be a good TSEP candidate for online temperature measurement of SiC MOSFETs [15]. It has almost a linear relationship between temperature and $t_{d\_off}$ under a given load current. In addition, the accuracy of $T_j$ measurement can be improved by adjusting the sensitivity of $t_{d\_off}$.

However, there are still some challenges in the turn-OFF delay time $t_{d\_off}$ based online junction temperature $T_j$ monitoring methods: First, the slower turn-OFF transient and increased switching loss are introduced into system operation with the $t_{d\_off}$ detection based method, whose sensitivity is usually guaranteed by increasing gate resistance. For example, paper [15] presents the online implementation of junction temperature estimation based on $t_{d\_off}$ monitoring, and it takes several switching periods to obtain $t_{d\_off}$ until the rising and falling edges are accurately captured. To avoid the impact on normal operation during $t_{d\_off}$ measurement, it is a challenging issue to achieve both accurate and fast estimation for junction temperature of SiC MOSFETs.

Another issue is that almost all TSEPs vary with the degradation of semiconductor devices, which brings difficulties in monitoring junction temperatures over aging. Both the statistic and the dynamic electrical parameters will be affected by degradation in SiC MOSFETs. For instance, a gradual increase of threshold voltage $V_{\text{th}}$ has been observed during the chip-level degradation of SiC MOSFET [18], while ON-state resistance $R_{ds\_on}$ also has a positive shift during package-level degradation of SiC MOSFET [19]. If aging effects are not considered in TSEPs, this parameter variation will cause error to junction temperature measurement. The value of $t_{d\_off}$ is also affected by both chip-level degradation and package-level degradation [8]. Consequently, the junction temperature monitoring with $t_{d\_off}$ detection will be inaccurate without considering the aging effects on devices.

For solving the two issues of employing $t_{d\_off}$ as TSEP of SiC MOSFETs, two main work will be presented: First, an adaptive recalibration method for $t_{d\_off}$ versus $T_j$ relationship is proposed for online $T_j$ estimation during the degradation of SiC MOSFETs. After analyzing the impact factors and variation mechanism of $t_{d\_off}$, in particular its relationship with $T_j$ over aging, the curves of $t_{d\_off}$ versus $T_j$ are recalibrated adaptively. Thus, the monitoring error caused by the degradation process can be considered. Second, an auxiliary circuit has been designed for detecting $t_{d\_off}$ accurately and rapidly. By applying the auxiliary circuit, the entire measurement process could be completed in less than two switching cycles. Thus, faster data acquisition is achieved and less impact occurs on system operation. In addition, $t_{d\_off}$ measurement can be employed to detect device degradation for SiC MOSFETs. By comparing $t_{d\_off}$ in healthy conditions and aging conditions, the aging states can be detected in SiC MOSFETs for degradation monitoring, which can be employed to schedule maintenance before serious deterioration or break down occurs in devices.

The rest of this article is organized as follows: In Section II, the feasibility of turn-OFF delay time as TSEP, i.e., $t_{d\_off}$, is discussed. Then, the aging impacts on typical TSEPs including $t_{d\_off}$ are analyzed. In Section III, the $t_{d\_off}$ based online junction temperature monitoring methods are proposed for aging devices. In Section IV, the auxiliary circuit is proposed and analyzed for fast and rapid $t_{d\_off}$ measurement. In Section V, an experimental platform has been built to validate the effectiveness of the proposed online temperature monitoring methods for SiC MOSFETs. Finally, Section VI concludes this article.

## II. RELATIONSHIP BETWEEN TURN-OFF DELAY TIME AND JUNCTION TEMPERATURE OVER AGING

In this section, the relationship between the turn-OFF delay time and the junction temperature of SiC MOSFETs over aging is analyzed. Two types of accelerating aging tests are performed on SiC MOSFETs to identify the influence from chip-level degradation and package-level degradation independently. Afterward, the aging effects on turn-OFF delay time $t_{d\_off}$ versus junction temperature $T_j$ is discussed for SiC MOSFETs.

### A. Validation of Turn-OFF Delay Time as the TSEP

Before applying TSEP methods, the definition of junction temperature must be clarified for accurate thermal analysis. Junction temperature refers to the temperature assigned to an area inside a semiconductor device, where a virtual heat source provides thermal output originating from electrical power losses [20]. It corresponds to the localized hotspot temperature within power semiconductor devices, e.g., PN-junction or conductive channel. The junction temperature is a virtual parameter, which cannot be measured directly [20]. As an alternative, the hotspot

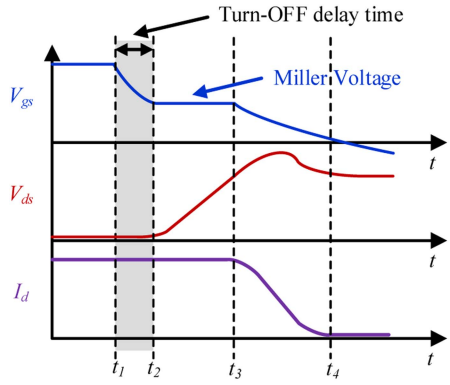


Fig. 1. Turn-OFF transient of SiC MOSFET.

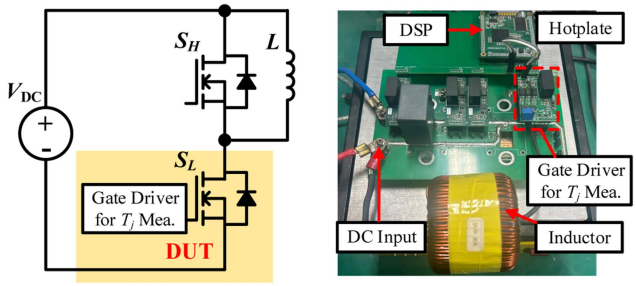


Fig. 2. Schematic and photograph of experimental platform for double-pulse test circuit.

temperature over the chip is used to approximate the junction temperature. Thus, the hotspot temperature over the chip serves as the focus for analyzing the turn-OFF delay time based junction temperature monitoring method in this article.

Turn-OFF delay time is defined as the time interval from the instant gate–source voltage starting to drop to the instant the drain–source voltage starting to rise [15], as shown in Fig. 1. Turn-OFF delay time, i.e., $t_{d\_\text{off}}$ can be expressed as follows [21], [22]:

$$t_{d\_\text{off}} = R_g \cdot C_{iss} \cdot \ln\left(\frac{V_{gs\_\text{on}}}{V_{\text{th}} + I_L/g_m}\right) \tag{1}$$

where $R_g$ is the total gate loop resistance, $C_{iss}$ is the input capacitance, $I_L$ is the load current, and $V_{gs\_\text{on}}$ is the ON-state gate–source voltage. The variation of $t_{d\_\text{off}}$ at different temperatures is mainly caused by the threshold gate–source voltage $V_{\text{th}}$ and the transconductance value $g_m$, which are both TSEPs. Thus, $t_{d\_\text{off}}$ is closely related to the junction temperature and it therefore can be used as the TSEP. In addition, the load current $I_L$ and the gate loop resistance $R_g$ also have impacts on the value of $t_{d\_\text{off}}$ [15].

To verify the impacts of load current $I_L$ and gate loop resistance $R_g$ on the value of $t_{d\_\text{off}}$, a double-pulse test (DPT) circuit has been built with 1200 V-25 A SiC MOSFET module FF45MR12W1M1_B11, as shown in Fig. 2. The power module of half-bridge configuration is connected to the dc bus voltage source. In the half bridge, the lower switch is selected as the device under test (DUT), while the upper switch is paralleled with load inductor. A gate driver controlled by the microcontroller is used to generate the gate signals of the DUT, and a hot plate is applied to control the junction temperature of DUT.

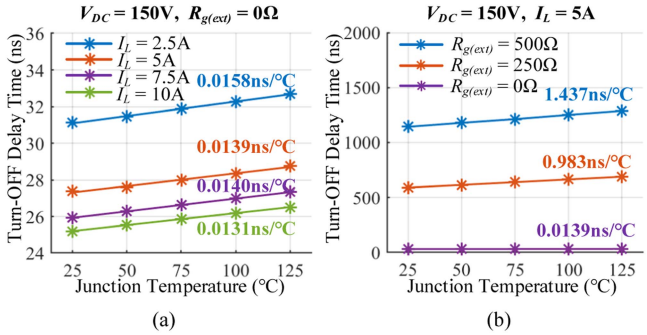


Fig. 3. Relationship between $t_{d\_\text{off}}$ and $T_j$. (a) Different load currents. (b) Different gate resistance values.

Before measuring $t_{d\_\text{off}}$, the baseplate of DUT is attached to the hotplate to stand the thermal stress. After the long-term heating, the hotplate reaches the target temperature, which agrees well with junction temperature $T_j$ of SiC MOSFET. Subsequently, $t_{d\_\text{off}}$ measurement starts. The gate loop resistance $R_g$ is adjusted by the gate driver, while the load current $I_L$ is adjusted by precise timing control of gate signal pulses. Then, $t_{d\_\text{off}}$ is captured and measured by an oscilloscope.

Fig. 3(a) shows $t_{d\_\text{off}}$ versus $T_j$ under different values of $I_L$. For the fixed $I_L$, $t_{d\_\text{off}}$ is increasing with the rise of $T_j$, which exhibits the linear relationship with temperature at a given load current. Fig. 3(b) shows $t_{d\_\text{off}}$ versus $T_j$ under different external gate resistance values $R_{g(\text{ext})}$. As the external gate resistance increases from 0 to 500 Ω, the sensitivity rises from 0.0139 to 1.437 ns/°C. Therefore, sufficient sensitivity of $t_{d\_\text{off}}$ can be guaranteed by increasing the gate loop resistance. Consequently, the high linearity and adjustable sensitivity make the $t_{d\_\text{off}}$ a suitable TSEP candidate for junction temperature evaluation of SiC MOSFETs.

### B. Degradation Mechanisms of SiC MOSFETs

To analyze the aging effects on $t_{d\_\text{off}}$, the degradation mechanisms of SiC MOSFETS are investigated. For SiC MOSFETS, main reliability issues can be classified into two categories: the chip-level degradation mechanisms and the package-level degradation mechanisms [23]. The chip-level degradation mechanisms are mainly induced by electrical overstress, while the package-level degradation mechanisms are mostly related to thermo-chemical overstress. Fig. 4(a) shows the typical chip-level structure of SiC MOSFET. The mostly common chip-level failure mechanisms of SiC MOSFETS occur at the gate oxide and the body diode [23]. The gate oxide degradation is usually caused by the tunneling current into the gate oxide layer [24]. The high temperature stress and high electric field stress imposedon SiC MOSFET gate oxide may contribute to the time-dependent dielectric breakdown [25]. In addition, high electric field stress may cause the avalanche breakdown in the gate oxide, which will further lead to the device failure [26]. The degradation of body diode is basically caused by the recombination-induced stacking fault mechanism [27]. The forward-voltage bias stress

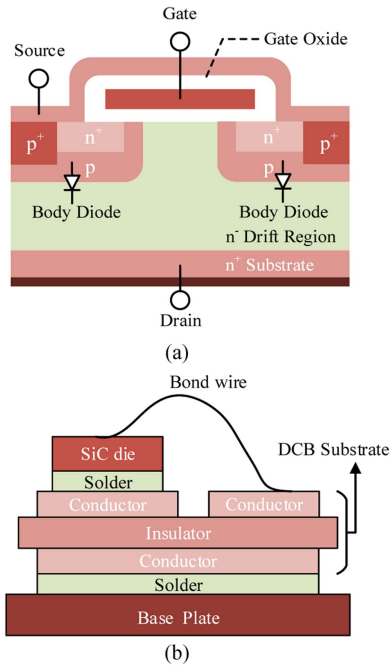


Fig. 4. Typical SiC MOSFET structure. (a) Chip-level structure. (b) Package-level structure.

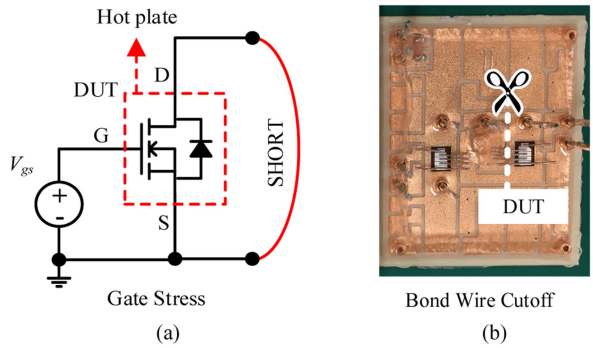


Fig. 5. Accelerated aging tests. (a) HTGB. (b) Bond wire cutoff.

has been proven to be the primary reason of the degradation of body diode [27].

Fig. 4(b) shows the typical package-level structure for SiC MOSFET. The mechanisms of common package-level failure in SiC MOSFET include bond-wire fatigue and solder-layer degradation [23]. By heating and cooling during device operation, the mismatch among coefficients of thermal expansion (CTE) for the bond wire and the adjacent layers in the package will lead to the thermo-mechanical stress, which may cause the bond-wire liftoff or the bond-wire fracture [28]. Meanwhile, the CTE mismatch between the SiC material and the die attach solder layer could result in the degradation of solder layer during long-term thermo-mechanical stress [28]. In addition to the thermo-mechanical stress, the relative humidity stress may increase the crack growth rate at the tail of the bond wire, and high current density stress may accelerate the electromigration related degradation [23]. These stresses could also be the cause of package-level degradation for SiC MOSFET.

### C. Variation of Turn-OFF Delay Time Over Aging

In practical applications, both the chip-level degradation and the package-level degradation occur in SiC MOSFET during the aging process. Electrical parameters will be affected by aging processes due to the aforementioned degradation mechanisms. In order to investigate the variation trends of turn-OFF delay time throughout the aging process, accelerated aging tests are used to obtain reliability related data in a shorter time. Power cycling test is one of the most popular accelerated aging tests. Both the chip-level and the package-level degradation mechanisms are induced by thermo-mechanical stress in power cycling test [28]. It is revealed that the linear relationship between $t_{d\_\mathrm{off}}$ versus $T_j$ curves moves downward as device degrades in power cycling test [8]. For further distinguishing these two types of degradation, the representative accelerated aging tests for each category are selected to analyze the degradation of SiC MOSFET. High-temperature gate bias (HTGB) test is utilized to trigger chip-level degradation mechanisms [29], while the cutoff of bond wires is used to simulate package-level degradation mechanisms [30]. Fig. 5 shows the accelerated aging test setups designed for SiC MOSFETS. In HTGB test, high E-field in the gate oxide is generated by the positive gate bias across the gate-source, and the drain and source electrodes are shorted [18]. The DUT is placed in a hotplate to stand the thermal stress. The stress is applied to the DUT with 30 V gate bias and 125 °C junction temperature. In the bond-wire degradation, the package of DUT is decapsulated and bond wires are exposed. The bond wires are cut off to simulate practical bond-wire fatigue in package-level degradation.

Two 1200-V 25-A half-bridge SiC MOSFET modules (FF45MR12W1M1_B11) are selected as DUTs. The upper and the lower switches of two half-bridge modules are used as four DUTs for test: DUT1 and DUT2 are aged by HTGB test, while the aging of DUT3 and DUT4 are accelerated by cutting off bond wires. To analyze the aging effects on $t_{d\_\mathrm{off}}$ by two degradation mechanisms, $t_{d\_\mathrm{off}}$-related failure precursors corresponding to degradation mechanisms are investigated during the aging process. After each degradation stage, all the failure precursors are measured at junction temperature of 25 °C to trace the variation caused by device aging.

*1) Failure Precursors Indicating Chip-Level Degradation:* Threshold voltage $V_{\mathrm{th}}$ is often presented as the failure precursor for chip-level degradation in the literature [18]. Since it has been indicated in (1) that $V_{\mathrm{th}}$ has impacts on $t_{d\_\mathrm{off}}$, $V_{\mathrm{th}}$ is investigated during two degradation processes. $V_{\mathrm{th}}$ is determined as the gate–source voltage that generates the 10-mA drain–source leakage current $I_{dss}$, when the drain–source voltage $V_{ds}$ equals the gate-source voltage $V_{gs}$ [31]. Before each $V_{\mathrm{th}}$ measurement, critical preconditioning procedures, i.e., residual charge dissipation and device state initialization, are performed to ensure the accuracy and repeatability of $V_{\mathrm{th}}$. Fig. 6 shows the variations of $V_{\mathrm{th}}$ over two types of aging mechanisms. The measured results indicate that $V_{\mathrm{th}}$ increases consistently throughout the HTGB test, while no obvious variation of $V_{\mathrm{th}}$ occurs over bond-wire degradation.

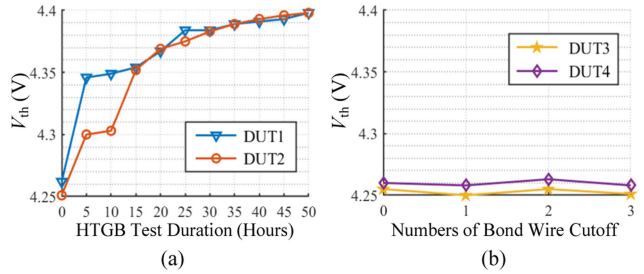


Fig. 6. Variations of $V_{\rm th}$ during accelerated aging tests. (a) HTGB. (b) Bond wire cutoff.

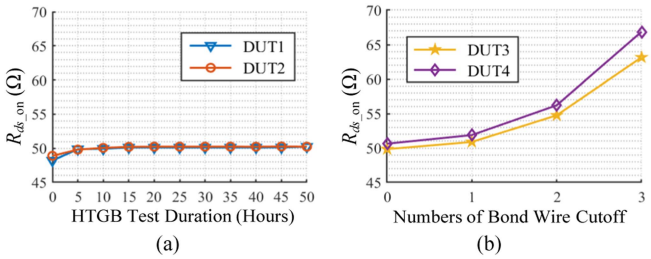


Fig. 7. Variation of $R_{ds\_on}$ during accelerated aging tests. (a) HTGB. (b) Bond wire cutoff.

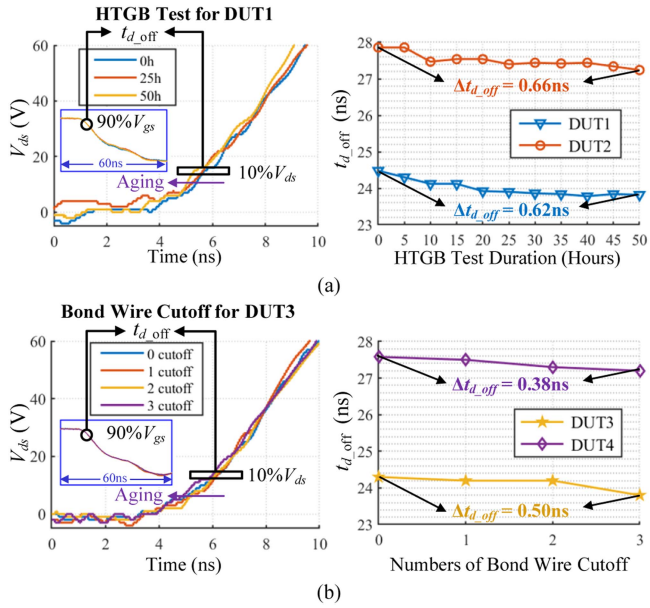


Fig. 8. Turn-OFF delay time variation without external gate resistance at 150 V/5 A during accelerated aging tests. (a) HTGB. (b) Bond wire cutoff.

For $V_{\rm th}$, a positive shift of 0.15 V is observed in the HTGB test in Fig. 6. The deviation of threshold voltage is mainly caused by the gate oxide trap [32]. The gate oxide degradation leads to reliability problems on the SiC/SiO2 interface of SiC MOSFET. Since traps are related to the roughness of SiC/SiO2 interface, electrons can tunnel into the gate oxide and charge the oxide traps by applying positive gate bias. These charged traps cause gradual generation of defects and lead to the positive $V_{\rm th}$ shift over time [32].

*2) Failure Precursors Indicating Package-Level Degradation:* To further analyze package-level degradation, the ON-state resistance $R_{ds\_on}$ is selected as the failure precursor that indicates the package-level degradation [19]. $R_{ds\_on}$ is measured by combining ON-state voltage $V_{ds\_on}$ with drain current $I_d$. The variations of $R_{ds\_on}$ over two types of aging are shown in Fig. 7. Fig. 7 shows that a gradual increase of $R_{ds\_on}$ is observed for all the DUTs in two degradation mechanisms, and the impact of package-level degradation on $R_{ds\_on}$ is higher than that of chip-level degradation on $R_{ds\_on}$.

To explain the gradual increase of $R_{ds\_on}$, the main composition of ON-state resistance $R_{ds\_on}$ is investigated as follows [8]:

$$R_{ds\_on} \approx R_{\rm ch} + R_d + R_{\rm sub} + R_{\rm package} \tag{2}$$

where $R_{\rm ch}$ is the channel resistance, $R_d$ is the drift region resistance, $R_{\rm sub}$ is the substrate resistance, and $R_{\rm package}$ is the package resistance. The channel resistance $R_{\rm ch}$ can be further expressed as follows:

$$R_{\rm ch} = \frac{L_{\rm ch}}{W_{\rm ch} \cdot \mu_{n\_\rm ch} \cdot C_{\rm ox} \cdot (V_{gs} - V_{\rm th})} \tag{3}$$

where $L_{\rm ch}$ is the channel length, $W_{\rm ch}$ is the channel width, $\mu_{n\_\rm ch}$ is the channel electron mobility, and $C_{\rm ox}$ is the oxide capacitance. Since bond wires are cut off to simulate the bond wire crack and the bond wire liftoff, the package-level degradation causes $R_{\rm package}$ to rise, which leads to the increase of $R_{ds\_on}$. In addition, the gate oxide degradation causes $V_{\rm th}$ to increase as mentioned above. With a positive shift of $V_{\rm th}$, the lower term of ($V_{gs}$ -$V_{\rm th}$) in (3) results in the higher value of $R_{\rm ch}$, which also causes the increase of $R_{ds\_on}$.

*3) Turn-OFF Delay Time Over Aging:* Then, the variation of $t_{d\_off}$ over aging is investigated directly with the chip-level degradation and the package-level degradation independently. Turn-OFF delay time $t_{d\_off}$ can be defined as the time from 90% of $V_{gs}$ to 10% of $V_{ds}$ [33]. During $t_{d\_off}$ measurement, the same commercialized differential probes are used to detect $V_{gs}$ and $V_{ds}$ to avoid the possible signal delay error. $t_{d\_off}$ is measured with and without external gate resistance to show the aging effects under different sensitivities respectively. The variations of $t_{d\_off}$ at 5 A load current over two types of aging mechanisms are shown in Figs. 8 and 9.

The measured results show that both chip-level degradation and package-level degradation will affect turn-OFF delay time. During the aging process, the value of $t_{d\_off}$ decreases gradually. To explain this, the impacts of two degradation mechanisms on $t_{d\_off}$ are analyzed. For the chip-level degradation, the threshold voltage $V_{\rm th}$ has been observed to have a positive shift in SiC MOSFET. Input capacitance $C_{iss}$ is related to gate-source voltage $V_{gs}$, and the $C_{iss}$–$V_{gs}$ characteristic curve exhibits a left shift parallel to the $V_{gs}$ axis owing to gate-oxide degradation [34]. In addition, the transconductance $g_m$ is also affected by the gate oxide degradation. The charges trapped in gate oxide may capture charge carriers in the conduction channel, thereby reducing electron mobility and decreasing $g_m$ [35]. From (1), these three factors lead to a negative shift of $t_{d\_off}$ in the chip-level degradation.

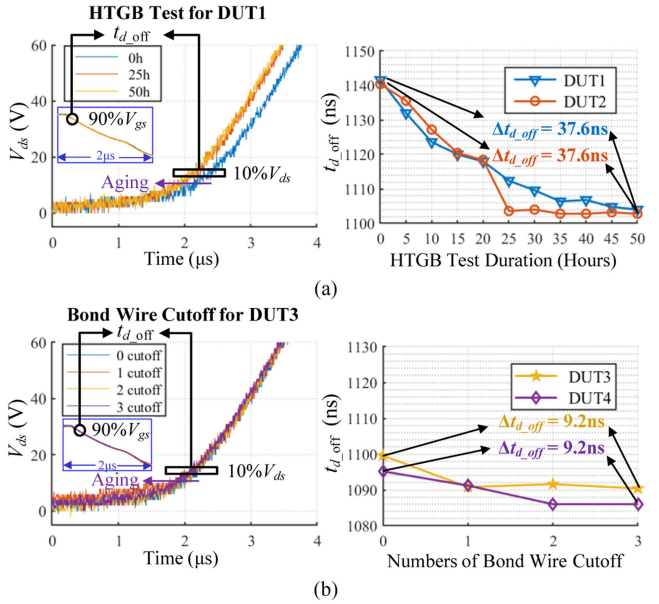


Fig. 9. Turn-OFF delay time variation with 500 Ω external gate resistance at 150 V/5 A during accelerated aging tests. (a) HTGB. (b) Bond wire cutoff.

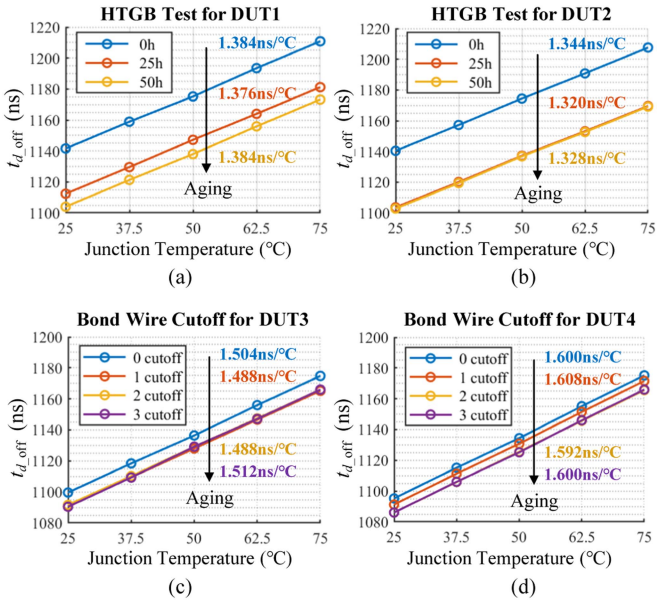


Fig. 10. Relationship of $t_{d\_off}$ versus $T_j$ over aging with 500 Ω external gate resistance at 150 V/5 A. (a) DUT1. (b) DUT2. (c) DUT3. (d) DUT4.

For package-level degradation, bond wire package resistance $R_{\text{package}}$ is increased when bond wire deteriorates [8]. The ON-state gate–source voltage $V_{gs\_on}$ of SiC MOSFET can be calculated as follows:

$$V_{gs\_on} = V_{CC} - I_d \cdot R_{\text{package}} \tag{4}$$

where $I_d$ is the drain current, and $V_{CC}$ is the positive gate drive voltage. When the package degrades, the increased $R_{\text{package}}$ makes the voltage drop noticeable across bond wire package. According to (4), $V_{gs\_on}$ of SiC MOSFET before turning-OFF action is reduced, and thus the gate voltage change during the turn-OFF transient is decreased accordingly. Based on (1), a lower value of $V_{gs\_on}$ leads to the decreased turn-OFF delay time in the package-level degradation [8].

In addition, a negative shift of $t_{d\_off}$ from healthy state to 50 h HTGB test, approximated as 0.6 ns, is observed without external gate resistance in Fig. 8(a), while an external gate resistance of 500 Ω expands this difference up to around 37.6 ns in Fig. 9(a). In bond-wire degradation, the negative shift of $t_{d\_off}$ is also increased from around 0.4 to 9.2 ns with the aid of external gate resistance in Figs. 8(b) and 9(b). Therefore, aging impacts on $t_{d\_off}$ can be enlarged by increasing the gate loop resistance. If the measurement resolution is not high enough to identify the variation of 0.4 ns, it is recommended that adjustable value of gate resistance is utilized for sufficient sensitivity.

To further investigate the aging effects on turn-OFF delay time as TSEP, $t_{d\_off}$ versus $T_j$ relationship curves under two degradation mechanisms are analyzed. Considering the aging effects, the maximum thermal stress imposed on the DUT is set as 75 °C, which ensures the safe operation of the aging device. Fig. 10 shows the experimental results of $t_{d\_off}$ versus $T_j$ for all DUTs with 500 Ω external gate resistance at 5 A load current. It can be observed that the curves of $t_{d\_off}$ versus $T_j$ have the negative shifts in both HTGB test and bond wire cutoff. If $t_{d\_off}$ versus $T_j$ relationship are not calibrated during the aging process, the negative shifts of $t_{d\_off}$ will lead to underestimation of junction temperature by using TSEP. Meanwhile, the sensitivity of $t_{d\_off}$ as TSEP remains the same in both chip-level degradation and package-level degradation because the slope in $t_{d\_off}$ versus $T_j$ is almost constant. Therefore, the calibrated curve slope of $t_{d\_off}$ versus $T_j$ at healthy states can be reused during the aging process. With the help of curve slope, only the measurement data of $t_{d\_off}$ under one point is needed to obtain the whole shifted curve over aging. This greatly simplifies complexity of recalibration process for $t_{d\_off}$, which can be used as the TSEP to achieve accurate $T_j$ assessment over aging.

## III. Proposed Junction Temperature Monitoring Method Over Aging

As mentioned above, the turn-OFF delay time is a TSEP with high sensitivity and high linearity for SiC MOSFET junction temperature evaluation. The degradation of SiC MOSFETs will cause negative shift of $t_{d\_off}$, which leads to the underestimation of junction temperature by using TSEP. In this section, a simple method is proposed to compensate aging effects and achieve on-line $T_j$ monitoring throughout the device lifetime. Meanwhile, a case study of the proposed condition monitoring method is given to illustrate the flow chart of junction temperature monitoring method.

### A. Proposed Junction Temperature Monitoring Method

Based on the aforementioned analysis, the degradation of power semiconductor devices will cause positive or negative shifts of TSEPs, which may induce the systematic error in $T_j$ measurement results. Recalibration is an approach to compensate aging effects on TSEPs, which makes it possible to achieve accurate measurement of $T_j$ for SiC MOSFETs over aging. A

simple way of recalibration is to perform routine examination and maintenance of power devices. The target devices are removed from the converter system, and the relationship between TSEP and $T_j$ is reestablished by extra experimental platform. However, the offline recalibration method is time-consuming and not cost-effective. Moreover, it is not suitable for situations where power devices are difficult to access. Therefore, the online aging compensation is attractive, which has been studied in many literatures. A sudden-stop control strategy has been presented in [36] to identify on-state voltage drop for compensation over aging. However, the sudden-stop control strategy will cause abnormal operation of system for seconds. An aging compensation scheme is given in [17] by tracing $V_{\rm th}$ to mitigate the aging effects on turn-ON delay time as TSEP. However, the introduction of $V_{\rm th}$ requires additional measurement circuits, and $V_{\rm th}$ only indicates the gate-oxide degradation.

To solve these issues, this article proposes an online compensation method for turn-OFF delay time based junction temperature observation of SiC MOSFETS over aging. This method takes advantage of the characteristic of $t_{d\_\rm off}$, i.e., $t_{d\_\rm off}$ versus $T_j$ curve slope remains unchanged during the aging process. To be specific, the first step is to determine the slope of $t_{d\_\rm off}$ versus $T_j$ relationship, which can be obtained by calibration offline before system operation. Then, the next step is to identify the $t_{d\_\rm off}$ data point. Influential factors of $t_{d\_\rm off}$ include gate loop resistance, drain current and junction temperature. Among them, the gate loop resistance can be regulated initially, and the drain current can be measured by current sensor.

The junction temperature needs to be obtained in another way, since $t_{d\_\rm off}$ is already unavailable for temperature monitoring due to the aging effects. The proposed method is to measure the junction temperature at the start-up stage. Before the system starts operating, the device junction temperature is approximately equal to the ambient temperature $T_a$, and the self-heating of device during $t_{d\_\rm off}$ measurement can be negligible due to the relative short measurement time [35]. Therefore, an ambient temperature sensor can be utilized for junction temperature estimation at the start-up stage. Finally, the curve of $t_{d\_\rm off}$ versus $T_j$ can be updated based on the slope and the $t_{d\_\rm off}$ data point. With the help of aging compensation, $t_{d\_\rm off}$ can be utilized as TSEP for online $T_j$ measurement during the aging process.

Fig. 11 shows the flowchart of the proposed junction temperature monitoring method. Initially, a thermal-electrical calibration curve is produced and programmed in the microcontroller before system operation. The calibration curve contains information of $t_{d\_\rm off}$ versus $T_j$ relationship at different load currents $I_L$. Before the measurement starts, $T_a$ is acquired by the ambient temperature sensor to represent $T_j$ of target devices considering the ignorance of self-heating in devices. At the start-up stage, system starts to operate and $I_L$ rises from 0 to steady state. When $I_L$ reaches the given value based on calibration, the measurement signal for turn-OFF delay time is triggered, and $t_{d\_\rm off}$ is measured by the auxiliary circuit. Then, the difference between the measurement data and the healthy calibration curve of $t_{d\_\rm off}$ is compared. A threshold value is set to determine whether the measured data of $t_{d\_\rm off}$ against $T_a$ and $I_L$ on the healthy calibration curve. If the difference is less than the

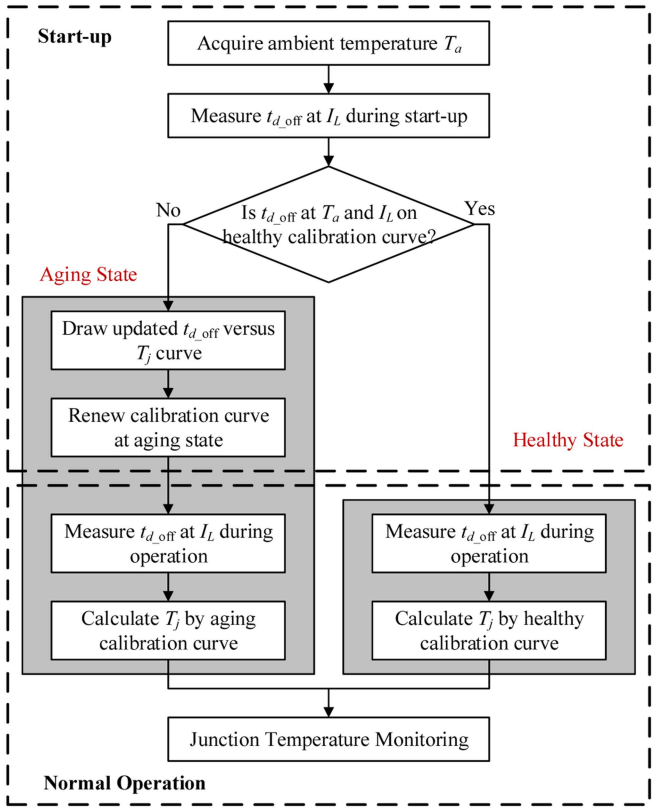


Fig. 11. Flowchart of the proposed junction temperature monitoring method.

threshold, the device is considered to be at healthy state and the calibration curve can be used to obtain $T_j$ without compensation. If the difference exceeds the threshold, the device is at aging state and the calibration curve needs to be modified. The updated curve can be determined by the $t_{d\_\rm off}$ measurement data and the slope of $t_{d\_\rm off}$ versus $T_j$. By modifying calibration curve, the error caused by aging is excluded and $t_{d\_\rm off}$ can be served as TSEP during the aging process. In addition, the modified $t_{d\_\rm off}$ versus $T_j$ relationship can be preserved to avoid frequent updates of calibration curves at aging state. After $t_{d\_\rm off}$ versus $T_j$ relationship is determined at the start-up stage, online $T_j$ estimation can be achieved during system normal operation. For $T_j$ assessment, $t_{d\_\rm off}$ at $I_L$ can be obtained by the auxiliary circuit. These online measurement results will be served as inputs of the calibration curve, and the junction temperature can be estimated by lookup table in real time.

### B. Case Exemplification

A case study of the proposed junction temperature monitoring method is given in this article. Fig. 12 shows an example of thermal-electrical calibration curve for a SiC MOSFET at healthy state, which establishes the relationship between junction temperature $T_j$ and turn-OFF delay time $t_{d\_\rm off}$ at different load currents $I_L$. By curve fitting in the lookup table, $t_{d\_\rm off}$ at 5 A load current can be expressed as follows:

$$t_{d\_\rm off} = 1.437T_j + 1108 \tag{5}$$

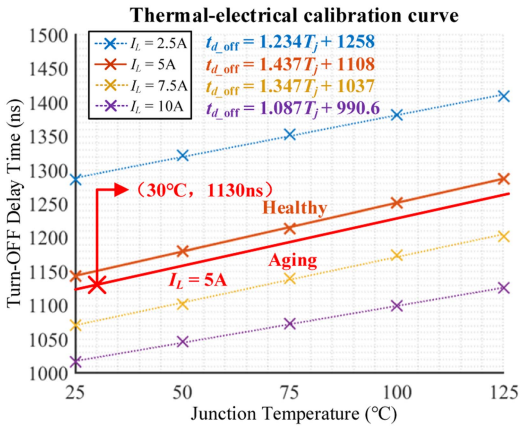


Fig. 12. Calibration curve of turn-OFF delay time versus junction temperature.

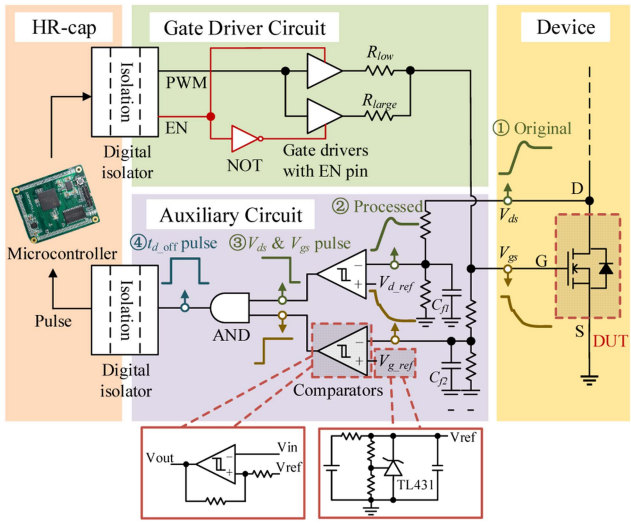


Fig. 13. Proposed online turn-OFF delay time measurement circuit for junction temperature estimation.

where the sensitivity of $t_{d\_off}$ is 1.437 ns/°C, and the $y$-axis intercept is 1108 ns in the case study.

After the occurrence of chip-level and package-level degradation, a negative shift of $t_{d\_off}$ will be observed in SiC MOSFET. To achieve accurate $t_{d\_off}$ measurement over aging, the time shift caused by two types of degradation needs to be eliminated. It is assumed that $t_{d\_off}$ of the aging device is measured to be 1130 ns at 5 A load current and 30 °C ambient temperature during system start-up. On the other hand, $t_{d\_off}$ at 5 A and 30 °C is supposed to be 1151 ns for device at healthy state according to (5). As aforementioned, it is the device degradation that causes the negative shift of 21 ns in $t_{d\_off}$. Therefore, the recalibration of $t_{d\_off}$ curve is required for aging compensation of the device at aging states. The recalibration curve can be depicted based on (5) and the measured $t_{d\_off}$ data. After aging compensation, $t_{d\_off}$ can be expressed as follows:

$$t_{d\_off} = 1.437T_j + 1087 \tag{6}$$

where the sensitivity of $t_{d\_off}$ is kept at 1.437 ns/°C, and the $y$-axis intercept decreases from 1108 to 1087 ns. By using the updated recalibration curve, $T_j$ can be directly obtained at the measurement values of $t_{d\_off}$ and $I_L$ during the sequent operation with loads.

Actually, the turn-OFF delay time can be utilized as an aging indicator to monitor the health status of SiC MOSFETS in addition to estimation of junction temperature. Based on the aforementioned analysis, $t_{d\_off}$ gradually decreases during the process of chip-level degradation and package-level degradation. By judging the negative shift of $t_{d\_off}$ measurement results compared to the value at healthy state, the aging-related changes can be detected. The value of negative shift represents the degree of device degradation. The deviation value is higher, and the aging effect is more severe in SiC MOSFET.

## IV. Dedicated Online Measurement Circuit for Turn-OFF Delay Time

To online measure $t_{d\_off}$, the auxiliary circuit of gate driver needs to be designed dedicatedly. There are the following design objectives for online measurement circuit of $t_{d\_off}$ .

1) The start and end instants of $t_{d\_off}$ are to be sensed and detected accurately, and the low time delay is required for signal processing.
2) The gate-loop resistance in the gate drive circuit is adjustable. Large gate resistance is employed to ensure high sensitivity for $t_{d\_off}$ measurement, while low gate resistance is kept most of the time for normal operation.
3) The measurement process is achieved within only a few switching periods to avoid the impact on normal operation.
4) High-resolution capture of the microcontroller is required to ensure the accuracy for time interval calculation.
5) Online measurement circuit for $t_{d\_off}$ should be simple and cost-effective, which can be easily integrated in the gate driver.

To satisfy these requirements, an online measurement circuit of $t_{d\_off}$ is proposed, as shown in Fig. 13. As mentioned above, the turn-OFF delay time can be defined as the time from 90% of $V_{gs}$ to 10% of $V_{ds}$. Based on the definition of $t_{d\_off}$, the falling edge of $V_{gs}$ and the rising edge of $V_{ds}$ are detected during the transient of turn-off action. To capture these edges, both $V_{gs}$ and $V_{ds}$ are scaled down by voltage dividers. During high-frequency switching transients of SiC MOSFETS, the stray inductance of resistors in voltage dividers may influence the fidelity of voltage signal. Therefore, parallel capacitors can be utilized to compensate the parasitic parameters at high switching frequencies. Then, the output signals of voltage dividers are compared by two comparators respectively. To shorten the response time, comparators are required to have the features of high bandwidth and high slew rate. Meanwhile, the same commercialized comparators or the dual channels of a single comparator are selected as the two comparators for reducing the possible parameter differences in measurement. After that, a pulse corresponding to detection of $t_{d\_off}$ is generated by AND logic gate. Using a digital isolator, the system controller is decoupled from the auxiliary circuit. The detected pulse by the auxiliary circuit is transmitted to the controller to calculate

$t_{d\_off}$. Based on the experimental results in Fig. 10, the sensitivity of $t_{d\_off}$ versus $T_j$ with 500 Ω gate resistance is higher than 1.320 ns/°C. To ensure the $t_{d\_off}$ measurement accuracy within 1 °C, the measurement resolution of microcontroller is required to be less than 1.320 ns.

In addition, gate resistance of the driver needs to be adjustable between the measurement process and the normal operation. In this article, two gate drivers are equipped with different gate resistors. The enabling signals are supplied to the two gate drivers complementarily. When the lower driver is enabled, high gate resistance (500 Ω) is achieved to ensure high sensitivity for real-time $t_{d\_off}$ measurement. By extending the turn-OFF transient, $t_{d\_off}$ can be accurately measured during the switching process. On the other hand, the upper driver is enabled and the gate resistance is kept small (5 Ω) for low switching loss during most of the time. The turn-OFF delay time can be obtained during turn-OFF transient within one switching cycle, if no accidental error or no noise injection occurs. In reference [15], the $t_{d\_off}$ measurement circuit takes several switching periods to capture the desired edges of voltage in the experiment. In this article, the number of switching periods during measurement can be minimized to 1, which could greatly eliminate the disturbance of measurement on system normal operation.

Since $t_{d\_off}$ measurement is expected to be finished within one switching period, the noise immunity needs to be considered to mitigate the risk of unexpected signal error in the auxiliary circuit. For accurate capture of $t_{d\_off}$ within a single measurement, additional design of noise immunity has been implemented for the auxiliary circuit. First, a filtering capacitor is paralleled to the lower voltage divider. The capacitor helps filter the high-frequency signals and suppress the ringing noise from original voltage signals. Then, a hysteresis comparator is used for stable transmission of processed signals. The hysteresis comparator prevents false triggering events caused by input voltage fluctuations and improves the anti-interference ability of the circuit. After that, the stability of voltage reference is considered. The implementation of a shunt regulator enables precise voltage reference stabilization to attenuate noise components. These additional design countermeasures improve the noise immunity of the proposed $t_{d\_off}$ measurement circuit.

The control scheme of the proposed circuit can be given as follows. First, the signal for $t_{d\_off}$ measurement is triggered and generated when $I_L$ reaches the given value. After that, the gate resistance will be transformed from a low value (5 Ω) to a high value (500 Ω) based on the EN signal controlled by microcontroller. Then, the auxiliary circuit will provide pulse signals that contain information of $t_{d\_off}$. Finally, the detected pulses by the auxiliary circuit are transmitted to the controller to obtain the value of $t_{d\_off}$.

It is worth mentioning that the propagation delay is inevitable due to the signal processing in operation amplifier, the logic gate and the isolator. Fig. 14 shows the captured waveform of $t_{d\_off}$ with the proposed driver circuit in experiment. The experimental results show that nanoseconds of propagation delay are observed. However, this delay does not influence the accuracy of junction temperature measurement because this propagation delay is almost unchanged in experiments. Since

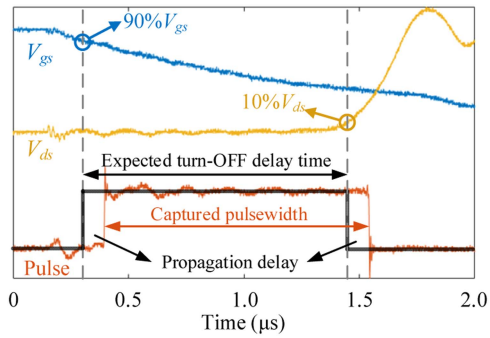


Fig. 14. Experimental waveform of turn-OFF delay time.

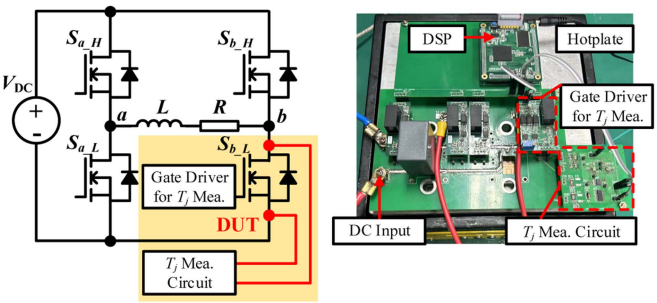


Fig. 15. Schematic and photograph of experimental platform for the 150-V single-phase full-bridge inverter.

almost the same error exists in all measurement results, the slope of $t_{d\_off}$ versus $T_j$ relationship remains unchanged. Therefore, the time delay due to signal processing will affect the value of $t_{d\_off}$ measurement instead of $T_j$ results. With the proposed method in Section III, the detection of $t_{d\_off}$ with this dedicated driver circuit can be used to monitor the junction temperature of SiC MOSFET over aging. In addition, the proposed $t_{d\_off}$ measurement circuit can be used to judge the occurrence and degree of device degradation monitoring.

## V. Experimental Validation

In order to verify effectiveness of the proposed method and circuit for condition monitoring, an experimental prototype has been built based on single-phase full-bridge inverter, as shown in Fig. 15. Two 1200 V/25 A SiC-MOSFET power modules (FF45MR12W1M1_B11) are employed to construct the phase legs, and one of the lower switches is selected as the DUT. To achieve measurement of $t_{d\_off}$, an additional measurement circuit and a gate driver with adjustable gate loop resistance are connected to the terminal of DUT. A microcontroller is employed to generate PWM signals for the inverter, and also deal with the turn-OFF delay pulse signal, which is fed back from $t_{d\_off}$ measurement circuit. Since the junction temperature needs to be regulated for the thermo-electrical calibration, a hot plate is attached to the baseplate of DUT. The dc-link voltage is set as 150 V and the switching frequency is set as 10 kHz.

A thermo-electrical calibration curve of the DUT is depicted before implementation of $T_j$ measurement. The experimental prototype is built based on the experimental platform of a DPT in

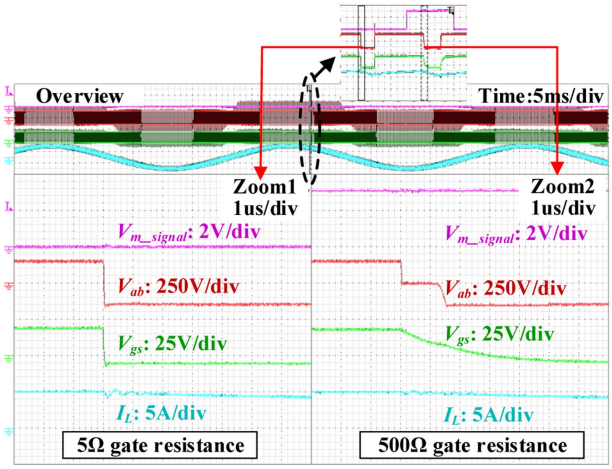


Fig. 16. Waveforms of two adjacent switching cycles under steady-state operation of inverter at 150V/5A.

Fig. 2, which is a part of the platform for single-phase full-bridge inverter in Fig. 15. In addition, the proposed measurement circuit is employed to acquire $t_{d\_\text{off}}$ in the calibration process. The methodology for depicting the $t_{d\_\text{off}}$ versus $T_j$ curves has been illustrated in Section II. Based on the platform in Fig. 2, the $t_{d\_\text{off}}$ versus $T_j$ relationship under different $I_L$ with 500 Ω gate resistance can be obtained offline.

At first, the effectiveness of online measurement circuit for $t_{d\_\text{off}}$ is demonstrated. Fig. 16 shows the measured waveforms of two adjacent switching periods at 5 A load current when the full-bridge inverter operates in the steady state. In normal operation, the measurement signal is kept low, and the low gate resistance of 5 Ω is applied to prevent high switching loss in the DUT. The gate signal of DUT and the phase voltage show fast switching transient, as can be seen in the left-side waveform, i.e., Zoom1 in Fig. 16. During the converter operation, the current transductor employed for control purposes continuously tracks the transient current to determine the time for $t_{d\_\text{off}}$ measurement. Precise current detection can be achieved by increasing the sampling frequency or applying the model-based current ripple prediction method in [37]. After the measurement signal is triggered at the load current of 5 A, the gate resistance is adjusted to 500 Ω for high sensitivity during the measuring process of $t_{d\_\text{off}}$. As shown in the right-side waveform, i.e., Zoom2 in Fig. 16, the switching transient process lasts for several microseconds, during which $t_{d\_\text{off}}$ is obtained. After $t_{d\_\text{off}}$ measurement is completed, the gate resistance is switched back to the low value for the subsequent normal operation of inverter. It is worth mentioning that there is a period of time when phase voltage remains 1/2 of its maximum value in the switching transient. This is due to the effect of dead time in half bridge, which will also be expanded with the slower switching transient in $t_{d\_\text{off}}$ measurement. Based on the duration of the extended switching transient, the dead time is set to 10 $\mu$s during $t_{d\_\text{off}}$ measurement to ensure that $V_{gs}$ stabilizes at the low-level voltage for safe operation. Fortunately, the measurement is fast, which can be completed within one switching cycle, and it will induce small perturbation to the inverter's operation.

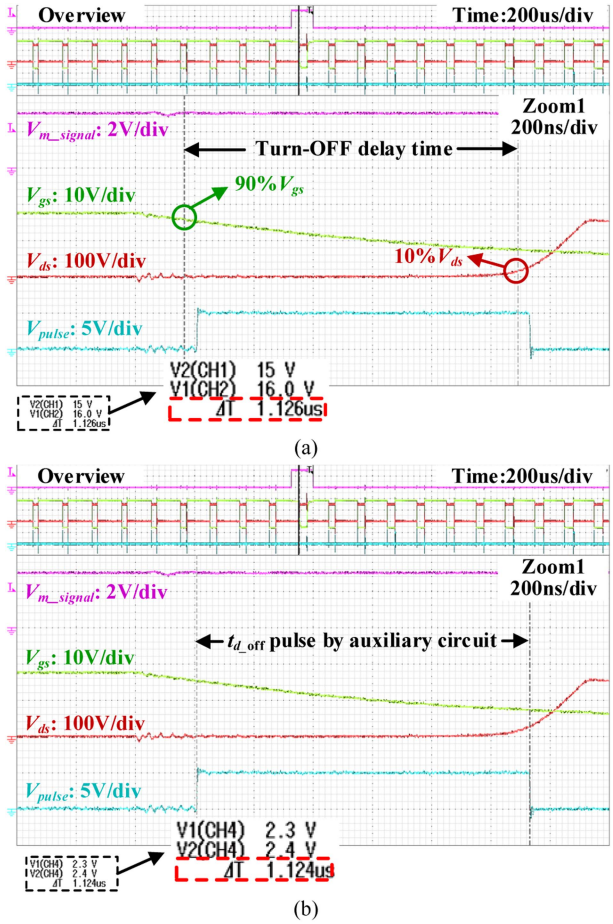


Fig. 17. Online monitoring of $t_{d\_\text{off}}$ at load current of 5A. (a) $t_{d\_\text{off}}$ results from direct measurement of $V_{gs}$ and $V_{ds}$. (b) $t_{d\_\text{off}}$ results obtained by designed driver circuit.

Then, the accuracy of measurement results for $t_{d\_\text{off}}$ with the designed auxiliary circuit is investigated. Fig. 17 illustrates the experimental waveforms when measurement signal is triggered. In Fig. 17(a), the cursor is used to identify the starting and ending points of $t_{d\_\text{off}}$, which are in the waveforms of $V_{gs}$ and $V_{ds}$ on oscilloscope according to its definition. This directly measured value is 1126 ns based on the definition. For $t_{d\_\text{off}}$ measured by the designed auxiliary circuit, the rising and falling edges of the output signal from measurement circuit are identified. The experimental results show that $t_{d\_\text{off}}$ is measured to be 1124 ns by using the dedicated measurement circuit in Fig. 17(b). Compared to the direct measurement with device's waveform in Fig. 17(a), the measurement difference is around 2 ns. It indicates that the designed auxiliary circuit is effective for detecting the variations of $t_{d\_\text{off}}$.

In sequence, the output signal pulse is imported into the relationship curve of $t_{d\_\text{off}}$ versus $T_j$ for the DUT at healthy state in Fig. 18(a), which has already been calibrated and programmed in the microcontroller. Junction temperature of 39.6 °C is obtained by the curve. For analyzing the accuracy of temperature, an IR camera with ±2 °C measurement accuracy is also used to monitor the temperature distribution at the same condition, as shown in Fig. 18(b). The IR camera monitors hotpot temperature

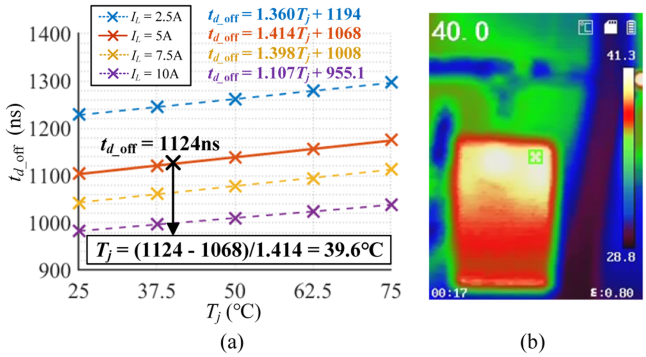


Fig. 18. Validation of $T_j$ evaluation. (a) TSEP measurement results. (b) IR camera measurement results.

TABLE II
TEMPERATURE MEASUREMENT RESULTS UNDER HEALTHY CONDITION

| $T_j$ by IR camera | $t_{d\_off}$ by circuit | $T_j$ by $t_{d\_off}$ | $T_j$ error |
|---|---|---|---|
| 29.9 °C | 1115 ns | 33.2 °C | 3.3°C |
| 40.0 °C | 1124 ns | 39.6 °C | 0.4°C |
| 49.8 °C | 1136 ns | 48.1 °C | 1.7 °C |
| 60.2 °C | 1152 ns | 59.4 °C | 0.8 °C |
| 70.0 °C | 1168 ns | 70.7 °C | 0.7 °C |

on the chip surface to minimize the error from nonuniform temperature distribution. The temperature in the chip center is observed to be 40.0 °C, which can be approximately served as junction temperature of SiC MOSFET. Thus, the error of junction temperature measurement is estimated around 0.4 °C in real time operation.

The comparison of $T_j$ measurement is further investigated under different temperature conditions for the full-bridge inverter. During system normal operation, the thermal stress is applied in the DUT using the hotplate. Within the temperature range ensuring the safe operation, five standard reference temperature points, i.e., 30, 40, 50, 60, and 70 °C are selected to analyze the accuracy of $T_j$ evaluation at different temperature points. Table II lists errors of $T_j$ measurement in the temperature range from 30 to 70 °C. The actual $T_j$ values are obtained by an IR camera, and then they are compared with the $T_j$ measurement results obtained by $t_{d\_off}$ at different temperatures. As shown in Table II, the maximum error of $T_j$ measurement results is 3.3 °C at different temperatures, which verifies the accuracy of $T_j$ assessment under different temperature conditions.

To further validate the proposed online junction temperature monitoring method for SiC MOSFETS over aging, the accelerated aging tests are performed on the DUT. The 30-h HTGB test and cutting 1 bond wire are conducted on the DUT to imitate the chip-level and package-level degradation of SiC MOSFETS in power conversion system implementations. Auxiliary temperature sensor is attached on the hot plate to measure ambient temperature. According to the proposed method in Section III, $t_{d\_off}$ measurement is performed at the start-up state before the inverter operates. At this time, the device self-heating can be ignored due to the low dissipation loss at the relative short start-up time, and ambient temperature can be approximated to be the junction temperature. The experimental waveforms of

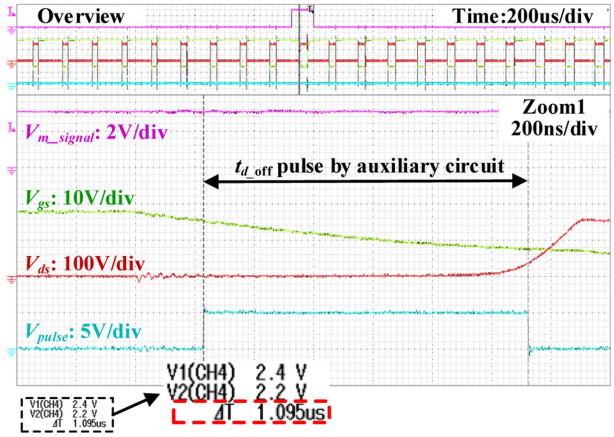


Fig. 19. Online monitoring of $t_{d\_off}$ at steady state of 150 V/5 A and 40 °C ambient temperature over aging under 30 h HTGB test and 1-bond-wire cutoff.

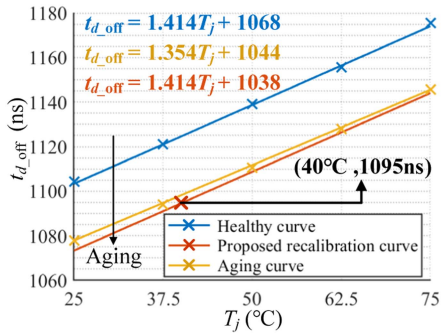


Fig. 20. Comparison of calibration curves at healthy state, over aging and prediction by the proposed method.

$t_{d\_off}$ over SiC MOSFET after aging tests is shown in Fig. 19. The $t_{d\_off}$ of aging DUT at 40 °C ambient temperature is measured to be 1095 ns by using the measurement circuit. Based on the data point in Fig. 19 and the slope from the calibration curve at healthy state, the relationship curve of $t_{d\_off}$ versus $T_j$ after aging is depicted in Fig. 20.

Fig. 20 shows the three calibration curves obtained under different conditions. By comparing the proposed updated calibration curve and the offline $t_{d\_off}$ versus $T_j$ relationship over aging, it is shown that these two curves show high consistency in terms of slope and $y$-axis value. Thus, the proposed online recalibration method has good performance of accuracy. Compared with calibration curve at healthy state, the recalibration curve shows a negative shift of around 30 ns in $y$-axis, which indicates the occurrence of device degradation.

Fig. 20 also indicates that the linearity relationship of $t_{d\_off}$ versus $T_j$ is almost unchanged over aging. Therefore, the junction temperature of SiC MOSFET over aging can be obtained by using the recalibration curve, as mentioned in Section III. Fig. 21 shows the validation of online $T_j$ measurement of SiC MOSFET over aging using the proposed monitoring method of $t_{d\_off}$. The junction temperature of DUT is obtained to be 59.4 °C by the recalibration curve of $t_{d\_off}$ versus $T_j$, while the measured value by IR camera is 59.9 °C. The error of measurement is around 0.5 °C. Thus, it verifies that the proposed monitoring method

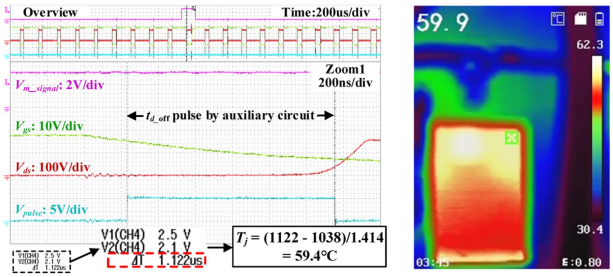


Fig. 21. Validation of $T_j$ monitoring for SiC MOSFET over aging under 30 h HTGB test and 1-bond-wire cutoff. (a) TSEP measurement results. (b) IR camera measurement results.

of $t_{d\_\mathrm{off}}$ is effective to evaluate the junction temperature of SiC MOSFET over aging.

## VI. Conclusion

This article proposes a turn-OFF delay time, i.e., $t_{d\_\mathrm{off}}$ based online monitoring method for junction temperature of SiC MOSFET over aging. The turn-OFF delay time shows good performance of sensitivity and linearity as an indicator for junction temperature monitoring of SiC MOSFETs. By studying the characteristic of $t_{d\_\mathrm{off}}$ versus $T_j$ for SiC MOSFETs over aging, a negative shift of $t_{d\_\mathrm{off}}$ has been disclosed under both chip-level degradation and package-level degradation. Consequently, a simple method has been proposed to achieve online monitoring of $T_j$ over aging based on variation of $t_{d\_\mathrm{off}}$. Meanwhile, an optimal auxiliary circuit has been proposed for fast and accurate measurement of $t_{d\_\mathrm{off}}$. Experimental results have shown that the proposed $t_{d\_\mathrm{off}}$ based monitoring method can achieve accurate evaluation for $T_j$ of SiC MOSFETs at both healthy and aging states. Therefore, the proposed turn-OFF delay time based online measurement of $T_j$ can be applied for condition monitoring throughout lifetime of SiC MOSFETs.

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