Overview of Efficient and Reliable Control Strategies for Three-Level NPC-Based DAB Converters

Chaochao Song, *Member, IEEE*, Ning Wang, *Member, IEEE*, Ariya Sangwongwanich, *Senior Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*, and Pooya Davari, *Senior Member, IEEE*

***Abstract*—Dual-active-bridge (DAB) converter has been widely employed in isolated dc–dc power transmission applications due to its advantages of high power density, inherent soft-switching capability, galvanic isolation, high step-up ratio, and bidirectional power transfer. With the advancement of medium-voltage dc (MVDC) systems, some multilevel dc–dc converters, evolved from two-level DAB converter, have emerged to meet the high-voltage and high-power demands. Among various multilevel variants of DAB converter, the neutral-point-clamping (NPC)-based DAB converters have gained increasing attention in recent years due to simplified control structure, relatively low costs, and widespread commercialization. The overall performance of MVDC systems depends highly on the efficiency and reliability of DAB converters. Therefore, this article presents a comprehensive overview of the state-of-the-art control strategies aimed at enhancing efficiency and reliability in NPC-based DAB converters. The review covers modulation schemes designed to optimize converter efficiency, categorized by degrees of freedom, solution types, optimization objectives, and algorithms. Furthermore, control strategies to improve converter reliability, including neutral-point voltage balancing, fault diagnosis and tolerance, transient-state dc bias suppression, and power loss balancing, are exhibited in detail. Finally, the challenges remaining in prior efficiency- and reliability-oriented design are discussed, and corresponding potential research directions are identified to further advance the performance of multilevel DAB converters.**

***Index Terms*—Control strategies, dual-active-bridge (DAB) converters, efficiency, neutral-point-clamping (NPC)-based, overview, reliability.**

NOMENCLATURE

α, β, γ	Thresholds in FD methods.
$\alpha_{i/o\text{TS}}$	Phase-shift angle in transient state.
$\alpha'_{i/o}$	Phase-shift angle in steady state II.
α_i, α_o	Inner and outer phase-shift angle.
λ, μ_i	KKT multipliers.
C_p	Output capacitance of power semiconductor.
d	Duty cycle.
d'	Duty cycle in steady state II.
E	Lagrangian function.
E_{VC}	Error of dc-link capacitor voltages.
$f_{\text{con},i}$	Inequality constraints.
f_{obj}	Optimization objective model.
f_{sw}	Switching frequency.
I_{end}	Current at end point of steady state I.
I_{ini}	Current at initial point of steady state II.
i_{Lp}	Peak value of inductor current.
i_{LRMS}	RMS value of inductor current.
i_L, i_o	Inductor current, neutral-point current.
k	Voltage conversion ratio.
k_{pt}	Indicator of HB and FB topology in primary side.
k_{st}	Indicator of HB and FB topology in secondary side.
l_{max}	Maximum current slope in SFT control.
L_s	Series-connected inductance.
m	Number of equivalent square waveforms of v_{xy} in EWM.
N	Transformer turns ratio.
N_1, N_2	Transformer turns in primary and secondary side.
P	Transferred power.
P_b	backflow power.
P_N	Maximum transferred power.
P_o	Normalized transferred power.
$S(t)$	Basic square waveform in EWM.
t_{TS}	Transient-state time in SFT control.
t_i	Rising instants of gate pulses.
T_{sw}	Switching period.
v_{ab}, v_{cd}	Terminal voltage of primary- and secondary-side bridges.
$V_{\text{CU}}, V_{\text{CL}}$	Upper and lower capacitor voltages.
V_{dc}	DC-link voltages, $V_{\text{dc}} = V_{\text{in}}$ in primary side, and $V_{\text{dc}} = V_{\text{out}}$ in secondary side.
$V_{\text{in}}, V_{\text{out}}$	Input and output dc-link voltages.
$V_{\text{out\_ref}}$	Reference output dc-link voltage.
v_{xn}, v_{yn}	Midpoint voltage of bridge arm.
v_{xy}	Terminal voltages of bridges, $v_{xy} = v_{ab}$ in primary side, and $v_{xy} = v_{cd}$ in secondary side.
2L,3L	Two-level, three-level.
AI	Artificial intelligence.
ANPC	Active NPC.
AVD	Average-value-detecting.
BD	Body diode.
CF	Curve fitting.

Received 7 April 2025; revised 31 July 2025; accepted 7 September 2025. Date of publication 11 September 2025; date of current version 13 November 2025. This work was supported by the CLEAN-Power (Compatibility and Low electromagnetic Emission Advancements for Next generation Power electronic systems) project at the Department of Energy, Aalborg University, Aalborg, Denmark, funded by Independent Research Fund Denmark (DFF). Recommended for publication by Associate Editor F. Dijkhuizen. *(Corresponding author: Ning Wang.)*

The authors are with AAU Energy, Aalborg University, 9220 Aalborg, Denmark (e-mail: chso@energy.aau.dk; nwa@energy.aau.dk; ars@energy.aau.dk; fbl@energy.aau.dk; pda@energy.aau.dk).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3608789.

Digital Object Identifier 10.1109/TPEL.2025.3608789

CIS	Complementary inner switch.
CSB	Complementary-switch-blocking.
CSS	Complementary-switching-state.
D-NPC	Diode-clamped NPC.
DAB	Dual active bridge.
DDPG	Deep deterministic policy gradient.
DEM	Differential extremum method.
DoF	Degree of freedom.
DPS	Dual-phase-shift.
DRL	Deep reinforcement learning.
ECSS	Enhanced-complementary-switching-state.
EMI	Electromagnetic interference.
EPS	Extended-phase-shift.
EWM	Equivalent-waveform method.
FC-NPC	Flying capacitor-clamped NPC.
FD	Fault diagnosis.
FSM	Fourier-series method.
FSS	Fixed-switching-state.
FT	Fault tolerant.
GA	Genetic algorithm.
GOC	Global optimal condition.
H-NPC	Hybrid-clamped NPC.
HB,FB	Half bridge, full bridge.
HFB	Hybrid full bridge.
HVdc	High-voltage dc.
IGBT	Insulated-gate bipolar transistor.
KKT	Karush–Kuhn–Tucker.
LMM	Lagrange multiplier method.
MDC	Modified-duty-cycle.
MIA	Mid-level-interval-adjustment.
MMC	Modular multilevel converter.
MOSFET	Metal-oxide-semiconductor field-effect transistor.
MPSDC	Modified-phase-shift-and-duty-cycle.
MVDC	Medium voltage dc.
NPC	Neutral-point-clamped.
NSA	Numerical solution analysis.
NSGA II	Nondominated sorting genetic algorithm II.
OCF	Open-circuit fault.
PI	Proportional integral.
PIM	Piecewise integration method.
PLP	Primary-side lower power.
PLT	Piecewise-linear transient.
PSO	Particle swarm optimization.
RMS	Root-mean-square.
SBA	Secondary-side bypass arm.
SCF	Short-circuit fault.
SFT	Straightforward transient.
SPS	Single-phase-shift.
SS	Steady state.
SSB	Same-position switch blocking.
SST	Solid-state transformer.
TPS	Triple-phase-shift.
TS	Transient state.
VL	Voltage level.
ZVS, ZCS	Zero-voltage switching, zero-current switching.

I. Introduction

MEDIUM-VOLTAGE dc (MVDC) architecture has garnered global attention along with the rise of dc loads such as batteries and electric vehicles, and growing demands for enhanced power-transfer capacity, power quality, and efficiency [1], [2]. This is because the MVDC networks offer notable advantages in terms of efficiency, flexibility, and reliability compared to ac systems [3], [4], [5]. Fig. 1 illustrates a typical MVDC system with distributed generation, energy storage system, and dc loads. The key techniques in MVDC networks, including protection and insulation, network configuration, and medium-voltage (MV) interfacing converters, have been increasingly investigated by industry and academia [6], [7], [8], [9], [10]. Isolated dc–dc converters applied to MVDC systems play a crucial role in maintaining dc-link voltages and transferring power between MVDC bus and other dc components. These converters are generally required to have large step-up ratios, high voltage-blocking and power-transfer capability, and bidirectional power-flow capability in energy storage systems [11]. However, due to technical complexity, limitation of power devices, and lack of standardization, isolated dc–dc converters designed specifically for MVDC systems are still under development and have not yet been fully commercialized [10].

Among prior dc–dc topologies, DAB converter, proposed in 1990s [12], has been applied as interfacing dc–dc converters in various scenarios due to high power density and efficiency, inherent soft-switching capability, bidirectional power-transfer capability, and galvanic isolation [13], and its generic structure is shown as Fig. 2(a). Unfortunately, a traditional 2L DAB converter is challenging to implement in an MVDC system operating at several kilovolts (kVs) or higher due to the limitation of commercial MV power devices [14]. Thus, multilevel variants developed based on 2L DAB converter were proposed to reduce voltage stress on each power semiconductor and increase step-up ratio. The most popular 3L topologies applied to DAB converters are exhibited in Fig. 2(b), including D-NPC topology [15], [16], [17], FC-NPC topology [18], [19], H-NPC topology [20], [21], [22], T-type topology [23], [24], [25], and ANPC topology [26], [27], where $V_{\rm dc}$ is the dc-link voltage, i.e., $V_{\rm dc} = V_{\rm in}$ in the primary side and $V_{\rm dc} = V_{\rm out}$ in the secondary side. Among various topologies, the D-NPC topology is the most widely applied to multilevel DAB converters due to its advantages of simple control, relatively low cost, and commercial maturity. Therefore, to avoid excessive length when discussing various topologies, this article reviews the optimal control strategies based on the D-NPC topology (hereinafter referred to as NPC). However, it is important to note that many of the control strategies proposed for this topology are also applicable to other 3L topologies, such as certain multi-DoF optimal control and neutral-point voltage balancing control methods.

Control strategies for NPC inverters have been widely researched; however, the efficiency- and reliability-oriented control strategies developed based on NPC inverters and NPC-based DAB converters exhibit significant differences. For NPC inverters, the efficiency can be improved by reducing

switching times in each fundamental period through suitably selecting space vectors [28]. Moreover, the efficiency of NPC inverters can be further improved by employing soft-switching strategies, which are commonly implemented through resonant circuits with auxiliary components or by utilizing boundary conduction mode [29]. Nevertheless, the efficiency of NPC-based DAB converters is generally enhanced by minimizing inductor current (i.e., i_L) or realizing soft switching through modifying phase relationship between terminal voltages (i.e., v_{ab} and v_{cd}) and inductor current. On the other hand, some reliability-oriented strategies such as neutral-point voltage balancing and FD require current polarity identification [30], [31], [32], which can be easily obtained in NPC inverters since the phase current exhibit periodic variations in fundamental frequency (e.g., 50Hz). However, in NPC-based DAB converters, as the direction of inductor current change at least twice within each switching period, it is challenging to determine the current polarity under a specific switching state especially with a high switching frequency. Due to these differences, the prior-art research developed for NPC inverters cannot be directly applied in the NPC-based DAB converters.

Efficiency-oriented control constitutes the majority of research on NPC-based DAB converters. The modulation schemes with various DoFs and VLs provide different potential for efficiency improvement. In traditional 2L DAB converters, the modulation schemes can be mainly divided into SPS control, EPS control, DPS control, and TPS control [13], [33], [34]. These modulation schemes achieve symmetrical waveforms of terminal voltages and inductor current during a switching period by modifying the phase-shift angles among gate pulses. In addition, some asymmetrical modulation schemes have also be proposed for further increasing optimization potential by regulating duty cycles [35], [36], [37]. The increased DoFs are introduced to improve converter efficiency by extending soft-switching range especially in light-load conditions and reducing rms values of inductor current [33]. The above modulation schemes of 2L DAB converters can be directly applied to 3L NPC-based DAB converters when the two switches in a same upper/lower bridge arm turn-ON and -OFF synchronously; however, they failed to fully utilize the increased DoFs provided by multilevel topology. A five-level modulation scheme was applied to NPC-based DAB converters in recent efficiency-oriented control strategies [38], [39], [40], [41], [42], [43], [44], [45], [46], [47]. In addition to SPS control where only one variable (i.e., a phase-shift angle between two bridges) is used to control power transfer, multiple solutions can be applied to achieve a certain reference power and output voltage with the multi-DoF modulation schemes. Therefore, identifying the optimal solution is a key issue in efficiency-oriented control strategies. Solution types, optimization objectives, optimization algorithms, and the number of DoFs will determine the optimal solutions, and further affect the converter efficiency, as shown in Fig. 3. When the DoFs in modulation schemes are determined, certain operating modes satisfying the constraints of optimization objective, e.g., ZVS constraints, can be selected, and then the mathematical models

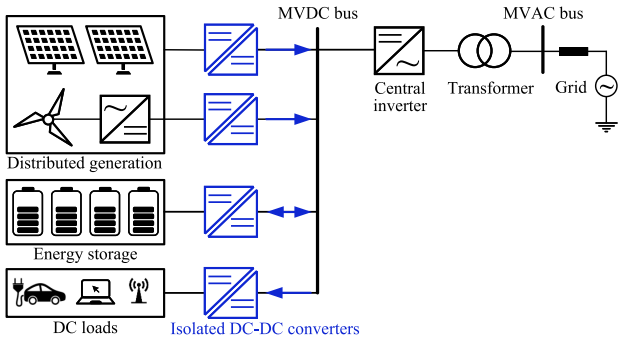

Fig. 1. Typical MVDC system.

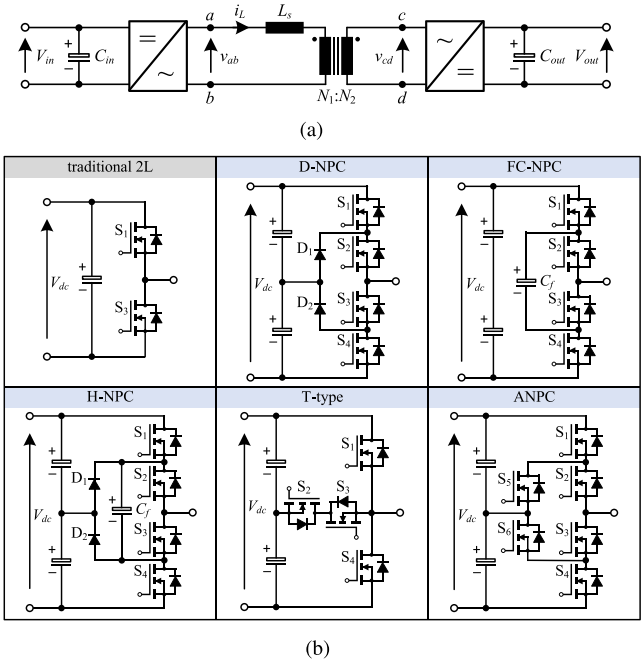

Fig. 2. Topology of a DAB converter. (a) DAB structure. (b) 2L and 3L topologies (per arm).

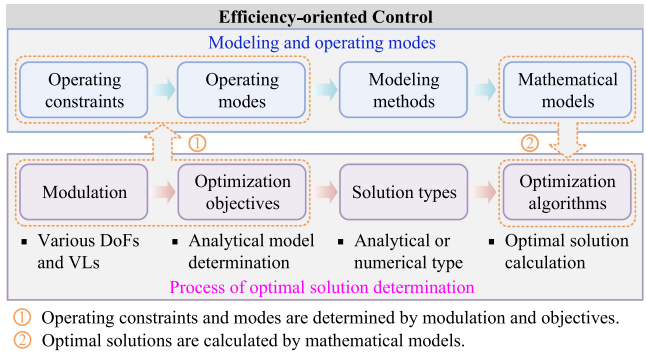

Fig. 3. Flowchart of optimal solution calculation for improving the efficiency of NPC-based DAB converters.

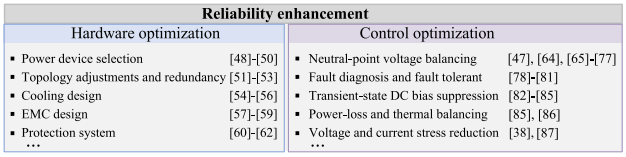

Fig. 4. Typical reliability enhancement methods including hardware optimization and control optimization.

of transferred power and optimization objective can be obtained. Subsequently, based on a certain solution type, i.e., analytical or numerical solutions, corresponding optimization algorithms can be employed to calculate the optimal solutions. Control strategies with different combinations of the above factors have been proposed for NPC-based DAB converters, which will be reviewed in this article.

In addition to efficient control, reliability enhancement also occupies a large proportion in the prior research of NPC-based DAB converters. The reliability of power electronic converters can be improved by hardware optimization and control optimization. The former improves system reliability by power device selection [48], [49], [50], topology adjustments and redundancy [51], [52], [53], thermal management and cooling design [54], [55], [56], electromagnetic compatibility (EMC) considerations [57], [58], [59], protection system against overvoltage, overcurrent, and overheating [60], [61], [62], and so on. On the other hand, reliable control aims to enhance converter reliability by adjusting parameters or structures of control system to decrease the electrical and thermal stresses on power devices and extend their lifespan [63]. This article focuses on the performance optimization of NPC-based DAB converters through control strategies. Thus, only control optimization for enhancing reliability will be discussed, while the hardware optimization design will not be covered. Among the reliable control strategies, neutral-point voltage balancing is an additional issue on 3L NPC topology compared to 2L DAB converters, and thus has been widely explored to suppress high voltage stresses on certain power semiconductors and dc-link capacitors [47], [64], [65], [66], [67], [68], [69], [70], [71], [72], [73], [74], [75], [76], [77]. In addition, FD and FT control strategies were proposed to avoid dc bias and increased peak current caused by OCFs on NPC-based DAB converters [78], [79], [80], [81]. TS control strategies have been developed to reduce dc bias current with load variations [82], [83], [84], [85]. Furthermore, other control strategies that can achieve power-loss and thermal balancing and voltage/current stress reduction will enhance the reliability of NPC-based DAB converters [38], [85], [86], [87]. Fig. 4 summarizes the typical reliability enhancement methods for power electronic converters, and this article will review the reliable control strategies for NPC-based DAB converters. The main contributions of this work can be summarized as follows.

1) A thorough review of control strategies for improving the efficiency of NPC-based DAB converters is developed. The main factors affecting the converter efficiency by control system, i.e., modulation schemes with various DoFs, optimization objectives, solution types, and optimization algorithms, are evaluated, which can inspire further control research into enhancing efficiency and compromising efficiency and implementation complexity.
2) Control strategies for enhancing the reliability of NPC-based DAB converters by reducing voltage/current stresses and balancing voltage/power distribution are reviewed, including neutral-point voltage balancing control, FD and FT control, dc-bias current suppression control, power-loss balancing control, and so on. The characteristics, advantages and disadvantages, and applicable scenarios of these reliable control strategies are discussed, providing a foundation for selecting appropriate control strategies in a certain application.
3) The challenges and potential solutions of efficiency and reliability related issues in the multilevel DAB converters are discussed, which offers valuable insights and guidance for future research and development in this area.

The rest of this article is organized as follows. Section II analyzes the modulation schemes with various DoFs and VLs, operating modes, and modeling methods of NPC-based DAB converters. The efficiency-oriented control strategies based on various modulation schemes, solution types, optimization objectives, and algorithms are reviewed in Section III. In Section IV, the prior control strategies for enhancing converter reliability including neutral-point voltage balancing control, OCF diagnosis, and tolerant control, and TS dc bias suppression control are detailed. In addition, other reliable control such as power loss balancing, voltage and current stress reduction, and conducted EMI suppression is also briefly discussed in Section IV. The interaction of efficiency- and reliability-oriented control is discussed in Section V. Section VI analyzes the existing challenges on efficiency- and reliability-oriented design, and provides some potential solutions for future research. Finally, Section VII concludes this article.

II. Modulation Schemes and Modeling for NPC-Based DAB Converters

For the NPC-based DAB converters, a 3L NPC bridge is employed to the higher voltage side, and a 2L or 3L NPC topology can be applied to the other side according to dc-link VL. Furthermore, based on power rating, half- or full-bridge topology can be used. Fig. 5 depicts five general topologies in the NPC-based DAB converters, including 2L half-bridge (2LHB), 2L full-bridge (2LFB), 3L half-bridge (3LHB), 3L full-bridge (3LFB), and hybrid 2 and 3L full-bridge (HFB), where v_{xy} denotes the input or output terminal voltage (i.e., $v_{xy} = v_{ab}$ or $v_{xy} = v_{cd}$). Some studies have adopted three-phase topology to further increase power levels [88], [89]; however, corresponding research on NPC-based DAB converters is limited. Therefore, the control strategies of three-phase topology will not be introduced in detail.

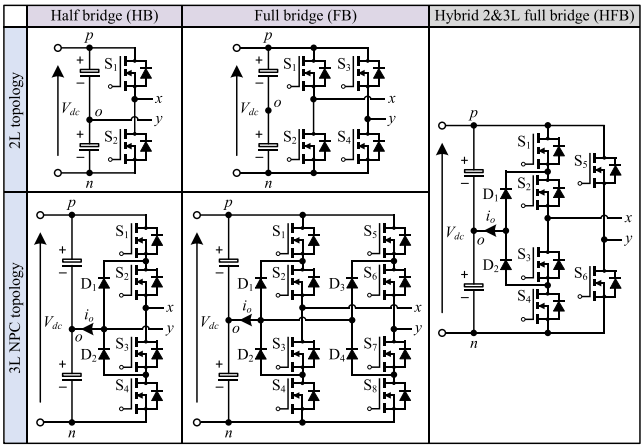

Fig. 5. Various 2L and 3L topologies used to NPC-based DAB converter.

TABLE I
SWITCHING STATES OF 2L AND 3L NPC BRIDGE ARM

Switching state	Switching state at first arm	Switching state at second arm (for full-bridge)	Arm voltage
2L bridge arm			
[P]	$\{S_1\}$	$\{S_3\}$	$v_{xo/yo} = 0.5V_{dc}$
[N]	$\{S_2\}$	$\{S_4\}$	$v_{xo/yo} = -0.5V_{dc}$
3L bridge arm			
[P]	$\{S_1, S_2\}$	$\{S_5, S_6\}$	$v_{xo/yo} = 0.5V_{dc}$
[O]	$\{S_2, S_3\}$	$\{S_6, S_7\}$	$v_{xo/yo} = 0$
[N]	$\{S_3, S_4\}$	$\{S_7, S_8\}$	$v_{xo/yo} = -0.5V_{dc}$

A. Basic Analysis of Modulation Schemes

The switching states and corresponding arm voltages of 2L and 3L NPC bridge arm are summarized in Table I. For the HB topologies, the ac terminal voltage of a bridge is the same as that of the first arm voltage, i.e., $v_{xy} = v_{xo}$. Therefore, two and three VLs can be generated for 2L and 3L HB topologies, respectively. On the other hand, as for the FB topologies, the ac terminal voltage is the difference of two arm voltages, i.e., $v_{xy} = v_{xo} - v_{yo}$. Thus, there will be five potential VLs on terminal voltage, i.e., $\pm V_{\rm dc}$, $\pm 0.5V_{\rm dc}$, and 0. When applying different switching states in certain time slots during a switching period, the terminal voltages in NPC-based DAB converters will exhibit various VLs, which will result in different converter performance. The switching states can be selected by phase-shift angles and duty cycles of gate pulses with various modulation schemes. Fig. 6 shows the waveform of terminal voltage v_{xy} with different DoFs for the five topologies, where α_i and d denote inner phase-shift angle and duty cycle of each bridge, respectively, and $T_{\rm sw}$ is the switching period. For a certain topology, different cases of modulation can be divided based on DoFs, which are denoted by Case A, B, and C. Note that for the 2LFB DAB converters, in addition to symmetrical modulation schemes with 50%-duty-cycle gate pulses (Case A and B), asymmetrical modulation (Case C) was also proposed to extend the soft-switching range, where a DoF related to duty cycle is used in the modulation system in addition to the phase-shift angle [35], [36], [37]. Therefore,

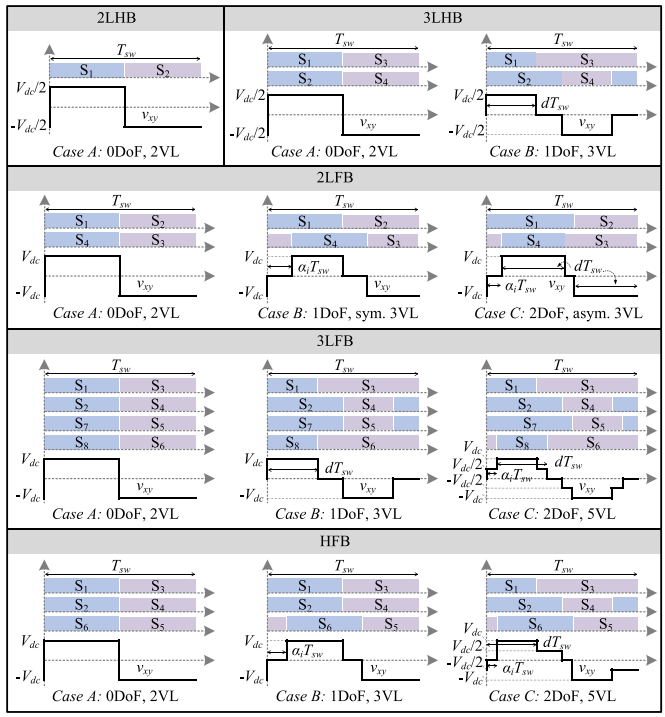

Fig. 6. Gate pulses and terminal voltage of each bridge with various topologies.

although the terminal voltage v_{xy} exhibits three VLs in both Case B and C in 2LFB topology, the asymmetrical modulation of Case C applies one more DoF. The asymmetrical modulation can be directly used in 3L DAB topologies when they operate in 2L mode, i.e., the two switches in the same upper/lower NPC bridge arm turn-ON and -OFF synchronously. However, the asymmetrical modulation specifically designed for 3L NPC-based DAB converters is not discussed, since it has not been explored in existing literature. When this issue is discussed in the future, the tradeoff between efficiency improvement and control complexity should be considered, since multilevel converters inherently offer increased DoFs.

In addition to control variables of each bridge, the NPC-based DAB converters are also controlled by an outer phase-shift angle α_o between primary- and secondary-side bridges, i.e., between v_{ab} and v_{cd}. The inductor current can be determined by the two ac terminal voltages, i.e.,

$$\frac{di_L(t)}{dt} = \frac{v_{ab}(t) - Nv_{cd}(t)}{L_s} \tag{1}$$

where $N = N_1/N_2$ is the turns ratio of transformer. For instance, when a 2LFB and a 3LFB are applied to primary and secondary side, respectively (denoted as "2LFB–3LFB" topology), the normalized waveforms with different modulation schemes are illustrated in Fig. 7. When the phase-shift angles and duty cycles are set to different values, the modulation will be in various cases. By combining these cases on the primary and secondary sides, the overall DoFs and VLs of the DAB converter can be determined, where the overall DoFs are the sum of inner

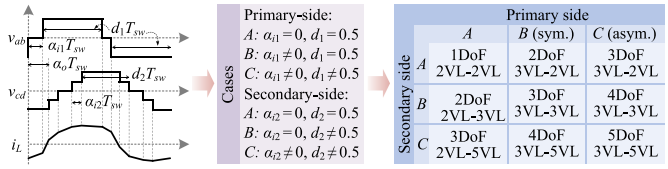

Fig. 7. Waveforms and modulation schemes under various DoFs and VLs for a DAB converter with 2LFB–3LFB topology.

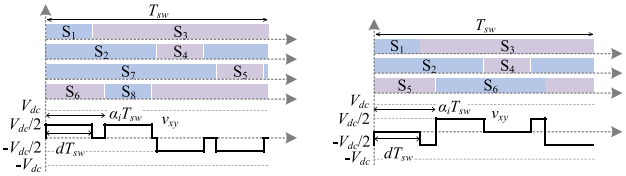

Fig. 8. Waveforms with the condition of $\alpha_i > d$ in: (a) 3LFB topology and (b) HFB topology.

DoFs of each bridge (i.e., α_i and d) and the outer phase-shift angle between the two bridges (i.e., α_o).

With different modulation schemes, the NPC-based DAB converters will exhibit various performance in terms of efficiency, reliability, and so on. In general, high-DoF modulation scheme can provide more optimization potential while also increase the control complexity. Thus, the optimum modulation scheme for a certain NPC-based DAB converter should be determined by compromising optimization results and control complexity, which will be detailed in Section III.

B. Operating Modes

With a certain modulation scheme and DAB topology, the waveform of inductor current i_L will show distinct characteristics when the relationships of control variables, i.e., phase-shift angles and duty cycles, are different. Thus, various operating modes can be differentiated accordingly. In the NPC-based DAB converters, due to the increased DoFs and VLs, the amount of operating modes will be numerous, making it difficult to exhaustively enumerate them. Fortunately, with certain inherent features and constraints related to control objectives, the analysis of operating modes can be simplified, which can be described as follows.

1) For an FB topology, regardless of whether the leading bridge arm is the first or second (corresponding to a positive or negative inner phase-shift angle α_i), the voltage and current waveforms remain unaffected [38], [90]. Therefore, unless in neutral-point voltage balancing analysis, the first leg can be fixed as the leading leg, i.e., $\alpha_i > 0$.
2) Under the condition of $\alpha_i > d$ in 3LFB and HFB topologies, the switching states [PN] and [NP] corresponding to the highest VL $\pm V_{\rm dc}$ will not exist, as shown in Fig. 8. As a result, the dc-link voltage is not fully utilized, which will limit the transferred power range of the NPC-based DAB converters. Furthermore, the peak current will be significantly increased compared to the condition of $\alpha_i \leq d$ under the same power level [38]. Therefore, the constraint $\alpha_i \leq d$ should be satisfied in the DAB converters with 3LFB and HFB topologies.
3) Certain operating modes can be used to achieve specific optimization objectives. For example, ZVS is widely considered to reduce switching loss as it is dominant in the DAB converters with high switching frequency [91], [92]. In order to achieve ZVS, the current should flow from emitter to collector of IGBT or from source to drain of MOSFET [93], [94]. Thus, the current polarity of each power semiconductor at turn-ON instant can be determined. Fig. 9 shows the operating modes which can satisfy ZVS constraints for all power semiconductors of the 2LFB–3LFB DAB converter with the 4DoF modulation, where the relationships among turn-ON instants of all power semiconductors (i.e., mode constraints) are depicted.

With the boundaries of control variables and constraints of control objectives, the selection of operating modes can be limited, which in turn simplifies subsequent modeling, control, and optimization.

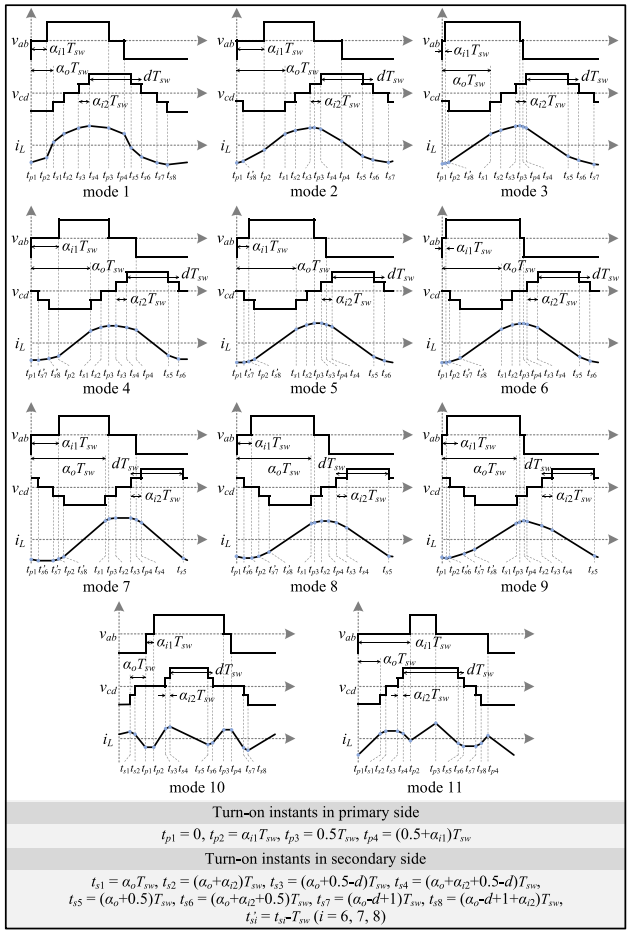

Fig. 9. Operating modes which can achieve ZVS for all power semiconductors in 2LFB–3LFB DAB converter.

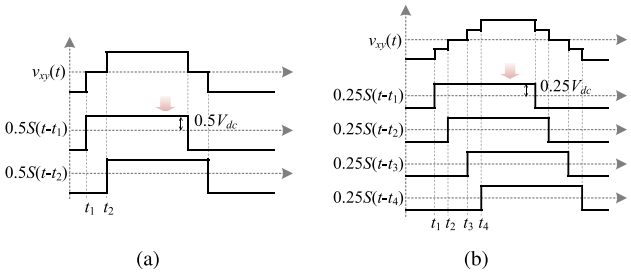

Fig. 10. Equivalent waveforms of the terminal voltage v_{xy} with: (a) 3VL and (b) 5VL.

C. Mathematical Modeling

Modeling of transferred power and inductor current for NPC-based DAB converters is the prerequisite for further performance analysis such as efficiency and reliability. The generic power model of the DAB converters is

$$P = \frac{1}{T_{\text{sw}}} \int_0^{T_{\text{sw}}} v_{ab}(t) i_L(t) dt. \tag{2}$$

Three modeling methods can be used to calculate the transferred power in various operating modes, i.e.,

PIM [14], [35]: It can be seen from Fig. 7 that the inductor current is piecewise in a switching period. Thus, the voltage v_{ab} and inductor current i_L can be integrated piece by piece to obtain the transferred power based on (2). With the PIM, the initial value and slope of i_L during each interval should be determined by (1). The PIM can achieve high modeling accuracy and can be used to various modulation schemes and operating modes. However, as the initial values and slopes of inductor current will change in different operating modes, there is no generic expression of inductor current and transferred power for various modes. Thus, the calculation for inductor current during different intervals and corresponding transferred power should be repeated, causing heavy calculation burdens.

FSM [37], [95], [96], [97]: The modeling of DAB converters, especially with multi-DoF modulation, can also be developed based on Fourier analysis, where the terminal voltages v_{ab} and v_{cd} are expressed using Fourier series. The major advantage of FSM is that it provides a generic model without requiring repetitive calculations for various operating modes [33]. By superimposing multiple harmonics, FSM can achieve relatively high modeling accuracy; however, the modeling complexity remains high [33]. On the other hand, some research only applies the fundamental component to calculate transferred power and other issues [96], [97]. Nevertheless, the accuracy can be significantly affected, especially when the inductor current deviates substantially from a sinusoidal waveform, such as modes 10 and 11in Fig. 9.

EWM [38], [90], [98]: In symmetrical modulation schemes, the terminal voltage (i.e., v_{ab} or v_{cd}) with 3VL and 5VL can be decomposed to two and four 50%-duty-cycle square waveforms, respectively [38], as shown in Fig. 10. $S(t)$ is the basic square waveform with 50% duty cycle, and the equivalent square waveforms are phase shifting by $S(t)$ based on the phase-shift angles and duty cycles in modulation. The terminal voltage can be expressed by the equivalent square waveforms as

$$v_{xy} = \frac{1}{m} \sum_{i=1}^{m} S(t - t_i) \tag{3}$$

where m is the number of equivalent square waveforms, i.e., m =1, 2, and 4 for the voltage with 2VL, 3VL, and 5VL, respectively, and t_i denotes the turn-ON instants of power semiconductors (i.e., t_{pi} or t_{si} in Fig. 9). With the equivalent expression of terminal voltage in (3), the inductor current and transferred power can be calculated based on (1) and (2). In this manner, the generic power model can be simplified without calculation of initial values and current slopes in various intervals under each operating mode [38], [90], [98]. Thus, the modeling accuracy with the EWM is the same as that of PIM while with reduced calculation burdens. The EWM can be used in different topologies (including HFB topology) with various symmetrical modulation schemes, as the terminal voltages can be decomposed into a sum of square waveforms with 50% duty cycles. On the other hand, when the EWM is used in asymmetrical modulation schemes, an additional variable related to duty cycle will be employed during the modeling as the duty cycle of specific equivalent square waveforms is not 50%. Therefore, the calculation process will be different. This condition has not been discussed in the existing literature, and thus, the applicability of this method in asymmetric modulation requires further exploration.

III. Control Strategies for Enhancing Efficiency

With high-DoF modulation schemes, the phase-shift ratios and duty cycles can be differently combined to achieve the reference output voltage and transferred power, and meanwhile, the efficiency of NPC-based DAB converters will vary along with the control variables. Therefore, certain combinations of the control variables should be applied to optimize the converter performance based on certain optimization objectives. The optimization for efficiency improvement can be generally expressed as

$$\begin{aligned} \min \quad & f_{\text{obj}}(\boldsymbol{X}) \\ \text{s.t.} \quad & P_o(\boldsymbol{X}) - P_o^* = 0 \\ & f_{\text{con},i}(\boldsymbol{X}) \le 0, i = 1, 2, \ldots, n \end{aligned} \tag{4}$$

where $f_{\text{obj}}(\boldsymbol{X})$ is the model of optimization objective, $f_{\text{con},i}(\boldsymbol{X})$ is the set of inequality constraints including mode and ZVS constraints, $\boldsymbol{X}$ is the optimum combination of the control variables. $P_o = P/P_N$ is the normalized transferred power, and P_N is the maximum transferred power, defined as

$$P_N = \frac{N(k_{\text{pt}} V_{\text{in}})(k_{\text{st}} V_{\text{out}})}{8 f_{\text{sw}} L_s} \tag{5}$$

where $k_{\text{pt}} = 1$ or 0.5 denotes that an FB or HB topology is applied to primary side, and $k_{\text{st}} = 1$ or 0.5 denotes the two topologies in secondary side, respectively. In addition, P_o^* denotes the reference transferred power.

For specific operation conditions and parameters, the optimum control variables are determined by various factors, such

TABLE II
STATE-OF-THE-ART OPTIMAL CONTROL STRATEGIES FOR IMPROVING EFFICIENCY OF NPC-BASED DAB CONVERTERS

Objective type	Optimization objectives	Topology type	Reference	Specific topology	Modulation method	Optimization algorithm	Solution type
single-objective	peak current	2L DAB	[102]	2LFB-2LFB	3DoF, 3VL-3VL	LMM	analytical
			[103]	2LFB-2LFB	3DoF, 3VL-3VL	KKT conditions	
			[35]	2LFB-2LFB	2DoF, 3VL-2VL (asym.)		
			[36]	2LFB-2LFB	3DoF, 3VL-3VL (asym.)		
			[105]	2LFB-2LFB	2DoF, 2VL-3VL ($k<1$) 2DoF, 3VL-2VL ($k>1$) 2DoF, 3VL-3VL	AI-based	numerical
		3L DAB	[99]	3LFB-3LFB	3DoF, 3VL-3VL	PSO	numerical
			[38]	2LFB-3LFB	4DoF, 3VL-5VL	KKT + NSA	analytical
			[100], [101]	3LFB-3LFB	2DoF, 3VL-3VL	PSO	numerical
	RMS current	2L DAB	[98]	2LFB-2LFB	3DoF, 3VL-3VL	GOC	analytical
			[106]	2LFB-2LFB	3DoF, 3VL-3VL	not mention	numerical
			[37]	2LFB-2LFB	5DoF, 3VL-3VL (asym.)	PSO	numerical
		3L DAB	[39]	3LFB-3LFB	5DoF, 5VL-5VL	not mention	numerical
			[40]	HFB-2LFB	4DoF, 5VL-3VL	GOC	analytical
	reactive/backflow power	2L DAB	[104]	2LFB-2LFB	2DoF, 3VL-2VL	KKT conditions	analytical
			[107]	2LFB-2LFB	3DoF, 3VL-3VL	PSO	numerical
		3L DAB	[41]	3LFB-2LFB	4DoF, 5VL-3VL	PSO	numerical
			[108]	3LHB-3LHB	3DoF, 3VL-3VL	solved by MATLAB, not mention the algorithm	numerical
	total power loss	2L DAB	[109]	2LFB-2LFB	2DoF, 3VL-3VL		
			[110]	2LFB-2LFB	3DoF, 3VL-3VL		
		3L DAB	[42]	3LFB-3LFB	5DoF, 5VL-5VL	AI-based	numerical
	soft-switching	3L DAB	[43]	3LFB-3LFB	5DoF, 5VL-5VL	-	-
			[44]	3LHB-2LHB	4DoF, 5VL-3VL		
			[120]	3LFB-3LFB	1DoF, 2VL-2VL		
			[121]	3LFB-3LFB	2DoF, 3VL-3VL		
multi-objective	RMS current + ZVS	2L DAB	[117]	2LFB-2LFB	2DoF, 2VL-3VL ($k<1$) 2DoF, 3VL-2VL ($k>1$)	DEM	analytical
			[118]	2LFB-2LFB	3DoF, 3VL-3VL	LMM	
			[122]	2LFB-2LFB	3DoF, 3VL-3VL	GOC	
		3L DAB	[123]	2LFB-3LHB	3DoF, 3VL-3VL	not mention	analytical
			[45]	HFB-2LFB	4DoF, 5VL-3VL	GOC	analytical
			[111]	3LHB-3LHB	3DoF, 3VL-3VL	solved by MATLAB, not mention the algorithm	numerical
			[115]	3LHB-3LHB	3DoF, 3VL-3VL	NSGA-II	numerical
	peak current + ZVS	2L DAB	[119]	2LFB-2LFB	5DoF, 3VL-3VL	KKT conditions	analytical
		3L DAB	[46]	2LFB-3LFB	4DoF, 3VL-5VL	KKT + NSA	analytical
			[112]	3LHB-3LHB	3DoF, 3VL-3VL	GA	numerical
	reactive power + ZVS	2L DAB	[115]	2LFB-2LFB	3DoF, 3VL-3VL	AI-based	numerical
	peak and RMS current + ZVS	2L DAB	[114]	2LFB-2LFB	3DoF, 3VL-3VL	NSGA-II + CF	analytical
	RMS + instantaneous current	3L DAB	[47]	3LFB-3LFB	5DoF, 5VL-5VL	solved by MATLAB, not mention the algorithm	numerical

as DoFs, solution types, optimization algorithms, and objectives. The main characteristics of prior efficiency-oriented control strategies for NPC-based DAB converters with these factors are summarized in Table II. In order to compromise efficiency improvement and implementation complexity, some prior-art control strategies apply 2VL- and 3VL-modulation in the 3L NPC-based DAB converters [78], [99], [100], [101]. In this condition, the control for 2L and 3L NPC-based DAB converters is the same, and thus the efficiency-oriented control strategies developed for 2L DAB can be directly applied in 3L NPC-based DAB. Therefore, the advanced control strategies for 2L DAB converters are also included in Table II. With the similar reason, the reliability-oriented control strategies such as FD and tolerant control and TS dc bias suppression control developed for 2L DAB are also discussed in Section IV. In Table II, the voltage conversion ratio k is defined as

$$k = \frac{k_{\text{pt}} V_{\text{in}}}{N(k_{\text{st}} V_{\text{out\_ref}})} \tag{6}$$

where $V_{\text{out\_ref}}$ is reference output voltage.

A. Solution Types

The optimum solutions for the optimization control strategies can be divided into analytical solutions and numerical solutions [33]. With the analytical solutions, the control variables, i.e., phase-shift angles and duty cycles, can be expressed by the dc-link voltages and transferred power. Therefore, when the operating conditions and parameters change, the control variables can be automatically modified to keep the converter operating in optimum status [35], [36], [38], [40], [98], [102], [103], [104]. On the other hand, for the numerical solutions, the optimum control variables should be calculated offline, and then stored in a look-up table in the microcontroller [37], [39], [41], [42], [99], [100], [101], [105], [106], [107], [108], [109], [110]. By comparing the two solution types, it is evident that the analytical-solution-based control strategies are preferred for practical applications, especially in the cases where the dc-link voltages, transferred power, and other operating parameters vary in a wide range, because the optimum control variables are not needed to recalculated offline and updated to the look-up table as with the numerical solutions [38], [46]. However, the calculations of analytical solutions are more challenging than that of the

numerical solutions, especially when the models of optimization objectives and inequality constraints are complicated.

For the NPC-based DAB converters, the optimization potential of efficiency can be enhanced with increased DoFs, while the complexity of calculating analytical solutions will also be increased. A similar condition applies between single-objective and multiobjective control strategies. With an increased optimization objective in multiobjective control, e.g., ZVS, the inequality constraints become more complicated, making the analytical solutions challenging to be obtained compared to single-objective control. Therefore, the efficiency enhancement and calculation complexity should be compromised to make the control strategies applicable. In general, when the operating conditions change in a limited range, numerical solutions can be employed to achieve higher efficiency with increased DoFs and multiple objectives. Otherwise, analytical solutions should be applied to avoid frequent calculations and updates when the operating parameters change widely [33], [38].

B. Optimization Algorithms

Optimization algorithms are used to calculate the optimum solutions of control strategies. The numerical solutions are relatively easy to be obtained as certain platforms with optimization tool, e.g., MATLAB and Wolfram Mathematica, can be used to carry out the calculations [47], [108], [109], [110], [111], where different optimization algorithms such as PSO [41], [99], [100], [101], [107], GA [112], [113], and NSGA-II [114], [115] can be chosen. With the development of AI technology, AI-based algorithms, e.g., deep reinforcement learning-deep deterministic policy gradient, were utilized to accelerate the optimization process and improve optimization accuracy [42], [105], [116].

On the other hand, for the analytical solutions, which are preferred to practical applications, when the DoFs in modulation are limited, the optimum solutions can be solved by DEM [117]. Otherwise, LMM and GOC were applied to obtain the analytical solutions in high-DoF modulation schemes [98], [102], [118]. The general expression of LMM is

$$\begin{cases} E = f_{\text{obj}}(\boldsymbol{X}) + \lambda(P_{\text{o}}(\boldsymbol{X}) - P_{\text{o}}^{*}) \\ \left.\frac{\partial E}{\partial \boldsymbol{X}}\right|_{\mathbf{X}=\mathbf{X}^{*}} = 0, \lambda \neq 0 \end{cases} \tag{7}$$

where E is the Lagrangian function, composed of the optimization objective and transferred power model, and λ is the Lagrangian multiplier. As shown in (7), the inequality constraints including soft-switching and operating-mode constraints are not considered during the solving process in LMM. Therefore, LMM can only yield fixed analytical solutions. Subsequently, these analytical solutions are substituted into the inequality constraints to determine the feasible power range. As a result, the optimum solutions for a certain operation mode can be solved in a limited power range rather than the entire feasible region, which may affect the global optimization in certain power ranges. In order to address this issue, LMM with inequality constraints, i.e., KKT conditions, is applied widely to the optimization of DAB converters [35], [36], [38], [46], [103], [104], [119], which can be expressed as

$$\begin{cases} E = f_{\text{obj}}(\boldsymbol{X}) + \lambda(P_{\text{o}}(\boldsymbol{X}) - P_{\text{o}}^{*}) + \sum_{i=1}^{n} \mu_i f_{\text{con},i}(\boldsymbol{X}) \\ \left.\frac{\partial E}{\partial \boldsymbol{X}}\right|_{\mathbf{X}=\mathbf{X}^{*}} = 0 \\ \mu_i f_{\text{con},i}(\boldsymbol{X}^{*}) = 0, f_{\text{con},i}(\boldsymbol{X}^{*}) \leq 0, \lambda \neq 0, \mu_i \geq 0 \end{cases} \tag{8}$$

where μ_i is the KKT multiplier related to the inequality constraints. Since the inequality constraints are included in the algorithm, the expressions of optimum solutions will be different under various power ranges in a specific operating mode [103], and thus, the KKT conditions can be used to obtain the optimum solutions during the entire feasible region.

However, in control strategies with higher DoFs and multiple optimization objectives, the increased number of operating modes, complex objective models, and intricate inequality constraints make it very challenging to calculate analytical solutions using the above algorithms. To address this issue, two methods were discussed during the calculation and data processing: 1) an optimization algorithm combining the KKT conditions and NSA was applied in [38], [46], and [113]. In this algorithm, the numerical solutions are used to determine specific operating modes and boundaries of inequality constraints where the optimum solutions are located. In this manner, the objective models and inequality constraints can be simplified, and then the analytical solutions can be solved by the streamlined KKT conditions; 2) the global optimum numerical solutions are collected, and then, the analytical solutions are obtained by CF of the numerical results [114]. This method reduces the computation load; however, the optimization accuracy will be impacted by the effectiveness of CF.

C. Optimization Objectives

As shown in Table II, the efficiency-oriented control strategies of DAB converters generally applied total power losses [42], [109], [110], peak value of inductor current [35], [36], [38], [99], [100], [101], [102], [103], [105], rms value of inductor current [37], [39], [40], [98], [106], backflow/reactive power [41], [104], [107], [108], and soft-switching [43], [44], [120], [121] as optimization objectives. Furthermore, various combinations of the above objectives were applied in multiobjective control strategies [45], [46], [47], [111], [112], [114], [115], [116], [117], [118], [119], [122], [123].

a) Total power loss reduction: The power loss models of power semiconductors, magnetics (i.e., transformer and auxiliary inductor), dc-link capacitors, gate drivers, and other components of DAB converters were developed in [117], [124], and [125]. Accordingly, the optimal control strategies with minimum total power losses were proposed for the traditional 2L [109], [110] and 3L NPC-based DAB converters [42]. Applying the total power loss model as optimization objective can improve converter efficiency to the utmost extent. Nevertheless, the model of total power losses is affected by various factors including operating parameters and modes, coefficients of power devices (e.g., on-resistance of power semiconductors, and core material and size of transformer), and control strategies, and thus, it

is challenging to develop an accurate and generic total power loss model. In addition, the complicated optimization objective model will make the calculations for optimum control variables, especially analytical solutions, very challenging to be processed.

b) Peak current minimization: In order to reduce the complexity of optimization objective models, certain efficiency-related indices are applied to the optimization rather than total power losses. Among these optimization objectives, peak value of inductor current offers the simplest model, which is defined as

$$i_{Lp} = \max\left\{|i_L(t)|\right\}, \quad 0 < t \le T_{\text{sw}}. \tag{9}$$

By reducing the peak current, the efficiency of DAB converter can be enhanced. This is because: 1) the rms values of inductor current can be decreased with the reduction in peak current during most operating modes, and thus, the conduction losses of power devices can be reduced [34]; 2) the instantaneous currents at turn-ON/OFF instants for certain power semiconductors can be reduced, resulting in decreased switching losses.

Minimum-peak-current control strategies for the 2L-DAB converter were proposed in [35], [36], [102], [103], [105], and [119], where both symmetrical and asymmetrical modulation methods were discussed. As the model of peak current is simple, the analytical solutions can be obtained by the LMM and KKT conditions. On the other hand, the 3L NPC topology can provide increased DoFs; however, most of the control strategies still applied the same modulation schemes as the 2L DAB converters, e.g., symmetrical 3VL modulation [99], [100], [101]. The above control strategies use numerical solutions calculated by PSO technique, which are not suitable for the cases where the operating conditions/parameters change in a wide range. In order to fully utilize the increased DoFs of NPC topology and simplify the control implementation, a minimum-peak-current control scheme based on 5VL modulation was proposed in [38], where the analytical solutions are obtained by combining the KKT conditions and NSA.

c) RMS current minimization: In addition to peak current, rms value of inductor current is another widely applied optimization objective in DAB converters [37], [39], [40], [98], [106], which is defined as

$$i_{\text{LRMS}} = \sqrt{\frac{1}{T_{\text{sw}}}\int_0^{T_{\text{sw}}} i_L^2(t)dt}. \tag{10}$$

The rms current affects the conduction losses of power switches and copper losses of the magnetics directly [117]. Therefore, the efficiency of DAB converters can be improved when the rms current is minimized under certain operating parameters. In [39], rms current minimization is applied as optimization objective to a 3LFB–3LFB DAB converter, where a look-up table with numerical solutions is employed to determine the optimum phase-shift angles and duty cycles. A minimum-rms-current control scheme was proposed based on an HFB–2LFB DAB converter in [40], and the analytical solutions are obtained by the GOC technique.

d) Backflow/reactive power minimization: As shown in (2), when the polarity of v_{ab} and i_L is the same, the power will flow from the primary side to the secondary side, and vice versa.

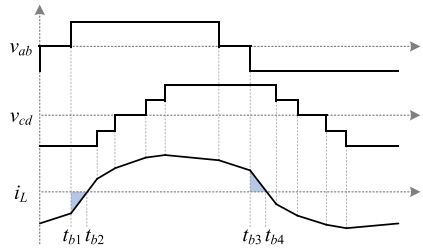

Fig. 11. Voltage and current waveforms with backflow power.

Therefore, the power will flow reversely in certain time slots (i.e., $[t_{b1}, t_{b2}]$ and $[t_{b3}, t_{b4}]$), as shown in the shaded area of Fig. 11. Thus, the backflow power (also referred to as reactive power) is defined as

$$P_b = \frac{1}{T_{\text{sw}}}\left(\int_{t_{b1}}^{t_{b2}} v_{ab}(t)i_L(t)dt + \int_{t_{b3}}^{t_{b4}} v_{ab}(t)i_L(t)dt\right). \tag{11}$$

Due to the backflow power, more power should be generated from input side to compensate the reverse power to achieve the reference transferred power (i.e., active power). As a result, the power losses on power devices will increase with a large backflow power [41], [104], [107], [108], [116]. Therefore, the converter efficiency can be improved by reducing the backflow power. Minimum-backflow-power control schemes were proposed for the traditional 2L DAB converters in [104] and [107] and NPC-based DAB converters in [41] and [108]. Nevertheless, these control strategies apply a limited number of DoFs and cannot fully exploit the optimization potential of multilevel topology.

e) Soft-switching operation: The above control strategies mainly focus on reducing the conduction losses. On the other hand, soft-switching operation, e.g., ZVS control, has been researched to reduce the switching losses of power semiconductors, especially when the switching frequency is high and the switching losses dominate the power losses [43], [44], [120], [121]. As analyzed in Section II-B, the current at turn-ON instants should satisfy certain polarity to achieve ZVS. Furthermore, the currents at turn-ON instants should be larger than a certain value to fully discharge the output capacitance of power semiconductor, ensuring that the voltage at turn-ON instants is zero [46], i.e.,

$$\frac{1}{2}L_s I_{\text{on}}^2 \ge n_{\text{cap}} \cdot \frac{1}{2}C_p(k_t V_{\text{dc}})^2 \tag{12}$$

where C_p is the output capacitance of power semiconductors and I_{on} is the instantaneous current at turn-ON instants. $k_t \in \{k_{\text{pt}}, k_{\text{st}}\}$ denotes the HB or FB topology in primary- and secondary-side bridge, and n_{cap} is the number of charging or discharging output capacitors at switching instants. Thus, the minimum current value for ZVS can be obtained as

$$|I_{\text{on\_min}}| = \sqrt{n_{\text{cap}}C_p(k_t V_{\text{dc}})^2/L_s}. \tag{13}$$

The ZVS operation for all power semiconductors can be achieved during the entire power ranges with the SPS (i.e., 1DoF and 2VL–2VL) modulation scheme when the voltage

conversion ratio k is unity. However, when k is significantly larger or lower than unity, the ZVS range will become limited, and certain power semiconductors will be turned-ON in hard-switching in light-load condition, resulting in higher power losses. Therefore, increased DoFs including inner phase-shift angles and duty cycles, are generally employed to extend ZVS range [13], [34]. However, if soft-switching is considered a single optimization objective, only ranges of control variables can be derived according to the ZVS constraints, rather than specific values. It means that the optimal control variables cannot be determined by only considering soft-switching as the optimization objective. Therefore, soft-switching is usually discussed together with another performance factor (e.g., peak or rms current) to identify certain optimal solutions, which will be discussed in the following multiobjective control.

f) Multiobjective control: The aforementioned control strategies are all based on a single optimization objective. On the other hand, certain multiobjective control strategies considering more than one objectives were proposed for the DAB converters, which can generally reduce both the conduction and switching losses. Peak or rms current minimization and ZVS is the most typical combination in multiobjective control strategies [45], [46], [111], [112], [115], [117], [118], [119], [122], [123]. In such an optimization problem, the peak or rms current model is taken as optimization objective $f_{\text{obj}}(\boldsymbol{X})$, and ZVS constraints are included in the inequalities $f_{\text{con},i}(\boldsymbol{X}) \leq 0$ [see (4)]. The calculation of analytical solutions is a main challenge in the multiobjective control strategies, especially with a high-DoF modulation scheme. Although the analytical solutions can be obtained by certain improved algorithms detailed in Section III-B, the expressions of control variables will be very complicated, and thus not applicable in practice, especially in closed-loop control system [46]. In order to overcome this issue, some control strategies made a tradeoff between efficiency and control complexity by using quasi-ZVS to simplify the inequality constraints, where the minimum current for ZVS, i.e., $I_{L\min}$ in (13), is set as 0 [46], [112], [122]. In this manner, certain switches cannot achieve ZVS; however, ZCS can be fulfilled at turn-OFF process. Therefore, the converter efficiency can still be maintained in a relatively high level. Simultaneously, the complexity for analytical solution calculation and closed-loop control design can be reduced significantly. Furthermore, a control strategy combining three objectives including peak current, rms current, and ZVS was proposed in [114], where the analytical solutions are obtained by CF the optimum numerical solutions. The instantaneous current at switching instants, which can affect the switching losses, were take as an objective together with RMS current to enhance the efficiency of NPC-based DAB converters in [47].

D. Performance Comparison of Various Control Strategies: A Case Study

To quantitatively evaluate converter performance under different control strategies, a case study is conducted using various modulation schemes, all targeting the same optimization objective, i.e., minimization of peak current. Minimum-peak-current control strategies developed based on SPS (2VL-2VL with 1DoF), EPS (3VL–2VL with 2DoF), DPS (3VL–3VL with 2DoF), TPS (3VL–3VL with 3DoF), and five-level (3VL–5VL with 4DoF) modulation are applied in a 2LFB–3LFB DAB converter in the case study. Table III shows the expressions of normalized peak current with these control strategies under the entire ranges of transferred power and voltage conversion ratio. The normalized peak current is defined as $i_o = i_{Lp}/I_N$, where $I_N = N(k_{\text{st}}V_{\text{out}})/(8f_{\text{sw}}L_s)$. Comparison of normalized peak current with various control strategies is shown in Fig. 12. It can be seen from Fig. 12 that the peak current reduces along with the DoFs under different voltage conversion ratios and transferred powers. Compared to the basic modulation, i.e., SPS control, the optimization benefits of multi-DoF control strategies become more significant when the voltage conversion ratio k deviates further from unity. In addition, under the condition of $k > 1$, the peak current with EPS, TPS, and five-level modulation is the same during certain power ranges. This is because the terminal voltages (v_{ab} and v_{cd}) with the TPS and five-level control strategies are the same as those of EPS control in such a condition. Furthermore, the peak current and power losses with various control strategies are evaluated based on a simulation prototype in piecewise linear electrical circuit simulation (PLECS), and the results are shown in Fig. 13. As shown in Fig. 13(a), compared to SPS, the peak currents can be effectively reduced by the multi-DoF modulation schemes, especially with the five-level modulation. The percentage improvement over the basic SPS modulation is also given in Fig. 13(a), which is defined as

$$E_{\text{EPS/DPS/TPS/5-level}} = \frac{i_{Lp\_\text{SPS}} - i_{Lp\_\text{EPS/DPS/TPS/5-level}}}{i_{Lp\_\text{SPS}}} \quad (14)$$

TABLE III
NORMALIZED PEAK CURRENT OF MINIMUM-PEAK-CURRENT CONTROL STRATEGIES WITH VARIOUS MODULATION SCHEMES

Control	Range of k	Range of P_o	Normalized peak current i_o
SPS [13]	$k \leq 1$	$[0, 1]$	$2(1-k\sqrt{1-P_o})$
	$k > 1$	$[0, 1]$	$2(k-\sqrt{1-P_o})$
EPS [102]	$k < \frac{1}{2}$	$[0, 2(k-k^2)]$	$2((2k-1)\frac{1+\sqrt{1-2P_o}}{2} - k + 1)$
		$(2(k-k^2), 1]$	$2(1-\sqrt{(2k^2-2k+1)(1-P_o)})$
	$\frac{1}{2} \leq k \leq 1$	$[0, 2(k-k^2)]$	$2((2k-1)\frac{1-\sqrt{1-2P_o}}{2} - k + 1)$
		$(2(k-k^2), 1]$	$2(1-\sqrt{(2k^2-2k+1)(1-P_o)})$
	$1 < k < 2$	$[0, \frac{2(k-1)}{k^2}]$	$2((2-k)\frac{1-\sqrt{1-2P_o}}{2} + k - 1)$
		$(\frac{2(k-1)}{k^2}, 1]$	$2(k-\sqrt{(2k^2-2k+2)(1-P_o)})$
	$k \geq 2$	$[0, \frac{2(k-1)}{k^2}]$	$2\sqrt{2(k-1)P_o}$
		$(\frac{2(k-1)}{k^2}, 1]$	$2(k-\sqrt{(2k^2-2k+2)(1-P_o)})$
DPS [102]	$k \leq 1$	$[0, \frac{-3k^2+2k+1}{2}]$	$\sqrt{2(1-k)(3k+1)P_o}$
		$(\frac{-3k^2+2k+1}{2}, 1]$	$2-\sqrt{2(3k^2-2k+1)(1-P_o)}$
	$k > 1$	$[0, \frac{k^2+2k-3}{2k^2}]$	$\sqrt{2(k-1)(k+3)P_o}$
		$(\frac{k^2+2k-3}{2k^2}, 1]$	$2k-\sqrt{2(k^2-2k+3)(1-P_o)}$
TPS [102]	$k \leq 1$	$[0, 2(k-k^2)]$	$2\sqrt{2k(1-k)P_o}$
		$(2(k-k^2), 1]$	$2(1-\sqrt{(2k^2-2k+1)(1-P_o)})$
	$k > 1$	$[0, \frac{2(k-1)}{k^2}]$	$2\sqrt{2(k-1)P_o}$
		$(\frac{2(k-1)}{k^2}, 1]$	$2(k-\sqrt{(k^2-2k+2)(1-P_o)})$
Five-level [38]	$k \leq \frac{1}{2}$	$[0, k(2-3k)]$	$2\sqrt{k(2-3k)P_o}$
		$(k(2-3k), 1]$	$2(1-\sqrt{(3k^2-2k+1)(1-P_o)})$
	$\frac{1}{2} < k \leq 1$	$[0, (1-k))(3k-1)]$	$2\sqrt{(-3k^2+4k-1)P_o}$
		$((1-k))(3k-1), 1]$	$2(1-\sqrt{(3k^2-4k+2)(1-P_o)})$
	$k > 1$	$[0, \frac{2(k-1)}{k^2}]$	$2\sqrt{2(k-1)P_o}$
		$(\frac{2(k-1)}{k^2}, 1]$	$2(k-\sqrt{(k^2-2k+2)(1-P_o)})$

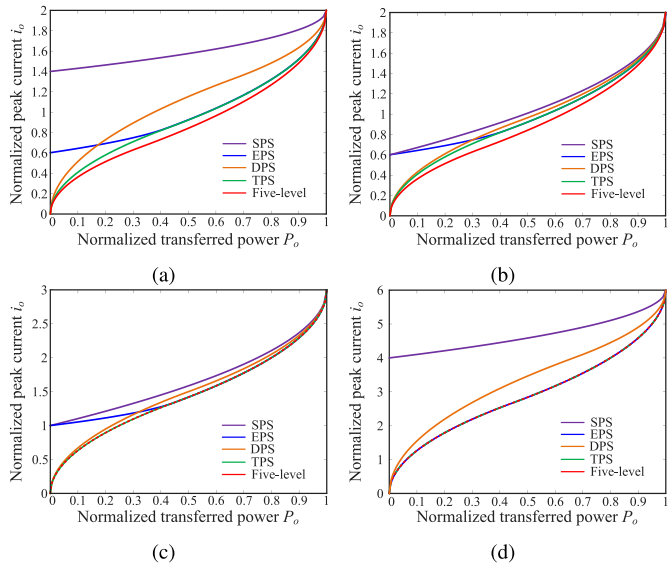

Fig. 12. Comparison of normalized peak current with various control strategies under: (a) $k = 0.3$, (b) $k = 0.7$, (c) $k = 1.5$, and (d) $k = 3$.

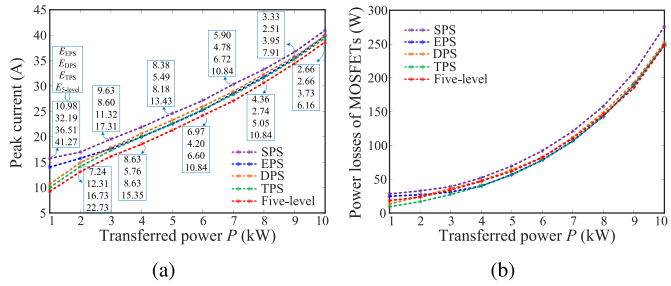

Fig. 13. Simulation comparison of various control strategies under the condition of $V_{in} = 400$ V, $V_{\text{out}} = 500$ V, $N = 1$, $L_s = 100$ μH, $f_{\text{sw}} = 20$ kHz based on C2M0040120D (MOSFET) in terms of: (a) peak current, and (b) power losses.

where $i_{Lp\_\text{EPS/DPS/TPS/5-level}}$ denotes the peak current with each modulation scheme. It is worth noting that, under a single-objective optimization, such as minimizing peak current, the effectiveness of efficiency optimization is not always positively correlated with the DoFs provided by the modulation methods. For instance, although the five-level modulation achieves the lowest peak current across the entire power ranges and voltage conversion ratios, its power losses exceed those of TPS control in specific power regions, which can be seen in Fig. 13(b). This is primarily because soft-switching conditions are not considered in these control strategies, making it difficult to actively reduce switching losses. As a result, under specific operating conditions where devices undergo hard switching, the overall converter efficiency may not be optimal even with increased DoFs. Furthermore, the optimization performance of a given control strategy can vary depending on the characteristics of the power devices, e.g., on-state resistance of power semiconductors. Therefore, the selection of an optimal control strategy should be tailored to the specific hardware implementation of the DAB converter.

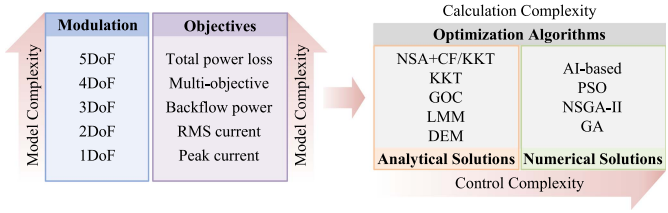

Fig. 14. Various factors in optimal control strategies to improve efficiency of DAB converters.

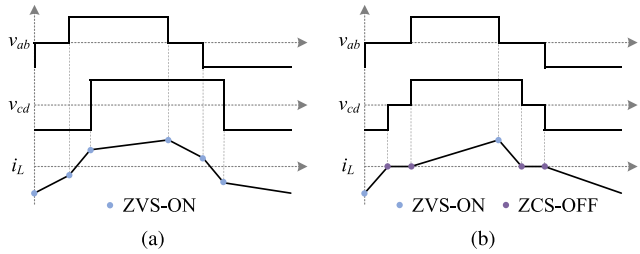

Fig. 15. Waveforms with the minimum-current-stress control proposed in [102] during: (a) high power level and (b) low power level.

E. Discussions on Various Control Strategies

Fig. 14 illustrates the overall structure of optimal control strategies for efficiency improvement with various factors, including modulation schemes, optimization objective, solution types, and optimization algorithms. The model complexity increases along with the number of DoFs. Furthermore, multi-objective control typically results in greater model complexity compared to single-objective control, except when total power loss minimization is the optimization objective. With certain modulation and optimization objective, the optimization algorithms can be selected to obtain the optimum solutions based on the solution type, i.e., analytical or numerical solutions. As discussed in Section III-A, the calculation of analytical solutions is more complicated than that of numerical solutions. However, the control implementation with analytical solutions will be much easier. Furthermore, the control strategies with higher model complexity can usually provide increased optimization potential. Therefore, a tradeoff between efficiency enhancement and implementation complexity should be made in practical applications by comprehensively considering the factors of optimization.

As all the optimization indices, e.g., soft-switching and current stress, are affected by the phase-shift angles and duty cycles, the optimal solutions obtained based on a certain optimization objective will also affect other issues. The coupling of various optimization indices can be mainly summarized as the following two aspects.

1) Even though some control strategies applied single optimization objective, the obtained optimal solutions can also affect other optimization effects. For instance, with the analytical solutions obtained by a minimum-peak-current control strategy proposed in [102], the waveforms of v_{ab}, v_{cd}, and i_L are shown in Fig. 15. As shown in Fig. 15(a),

during the high power range, the current polarity at turn-ON instants satisfies the ZVS constraints. Therefore, all switches in the DAB converters can achieve ZVS-ON in high power level. On the other hand, although part of instantaneous currents cannot satisfy the ZVS constraints during low power range, certain switches can be turned-OFF in ZCS as the currents are zero at their turn-OFF instants, as shown in Fig. 15(b). Thus, even though soft-switching was not considered in the optimization algorithm in [102], the obtained optimal solutions can achieve good soft-switching capability. Furthermore, it can be seen from Fig. 11 that the backflow power can be decreased to zero when the current at $t = t_{b1}$ is positive. However, the ZVS operation cannot be achieved in this manner. Thus, the backflow power should be optimized under the condition that ZVS is ensured.

2) In the single-objective control strategies, e.g., rms current minimization, the feasible region for optimization is determined by the operating-mode constraints, i.e., the relationships among control variables for each operating mode, which can be seen in Fig. 9. However, after considering another objective into the optimization, e.g., ZVS, the feasible region will narrow by the increased ZVS constraints. As a result, the optimization effect of multiobjective control on specific performance issue will decrease compared to single-objective control. For instance, the minimum rms current obtained from a multiobjective control considering both rms current minimization and ZVS is higher than that of a single-objective control only considering rms current minimization.

Therefore, it is challenging to directly evaluate the performance of various control strategies according to the optimization objectives due to the coupling of various optimization indices. Instead, the control strategy that can improve the converter efficiency to utmost extent should be determined based on power devices and operating conditions of specific applications.

IV. Control Strategies for Improving Reliability

Reliable control strategies improve the converter reliability by reducing the voltage and current stresses, or balancing the power losses on various power devices, which have been discussed from different perspectives including neutral-point voltage balancing, FD and tolerant control, dynamic current overshoots and dc bias suppression, power-loss sharing, and so on.

A. Neutral-Point Voltage Balancing Control

Neutral-point voltage balancing, also referred to as capacitor voltage balancing, is a crucial issue in NPC-based DAB converters. Due to the nonideal factors, e.g., asymmetrical gate pulses, power devices, or layout, the neutral-point voltage will drift, and the two capacitor voltages will be different [30], [126]. The neutral-point voltage imbalance will exacerbate voltage stress on certain devices, reducing their lifetime, and impacting the optimal operation of DAB converters due to voltage distortion [127], [128]. The prior neutral-point voltage balancing control of NPC-based DAB converters can be mainly divided

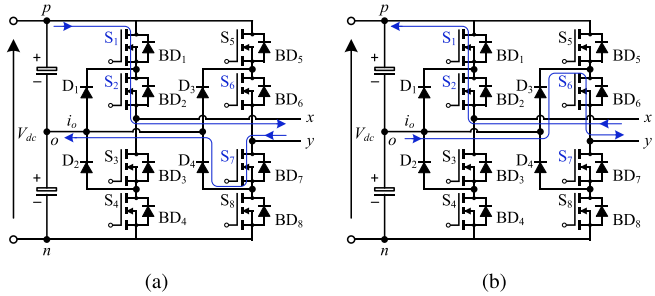

Fig. 16. Current conduction path for the switching state [PO] with a: (a) positive bridge current and (b) negative bridge current.

TABLE IV
Relationships Between Neutral-Point Current Direction and Bridge Current Polarity Under Various Switching States

Switching State	v_{xy}	Bridge Current	Current Flow Path	Direction of i_o
[OP]	$-0.5V_2$	positive	$D_1 \rightarrow S_2 \rightarrow S_6 \rightarrow D_5$	$i_o < 0$
		negative	$S_5 \rightarrow S_6 \rightarrow S_3 \rightarrow D_2$	$i_o > 0$
[PO]	$0.5V_2$	positive	$S_1 \rightarrow S_2 \rightarrow S_7 \rightarrow D_4$	$i_o > 0$
		negative	$D_3 \rightarrow S_6 \rightarrow S_2 \rightarrow S_1$	$i_o < 0$
[ON]	$0.5V_2$	positive	$D_1 \rightarrow S_2 \rightarrow S_7 \rightarrow S_8$	$i_o < 0$
		negative	$S_8 \rightarrow S_7 \rightarrow S_3 \rightarrow D_1$	$i_o > 0$
[NO]	$-0.5V_2$	positive	$D_3 \rightarrow S_6 \rightarrow S_3 \rightarrow D_4$	$i_o < 0$
		negative	$S_4 \rightarrow S_3 \rightarrow S_7 \rightarrow D_4$	$i_o > 0$

$i_o > 0$ denotes that i_o is injected into the neutral point, and vice versa.

into three approaches, i.e., MIA method [47], [64], [65], [66], [67], [68], [69], [70], [71], [72], CSS method [73], [74], [75], and FSS method [76], [77]. Due to applying different techniques to regulate neutral-point charges, these voltage balancing methods exhibit various characteristics, and thus are suitable for different applications.

a) Voltage balancing with MIA method: As current i_o only flows through the neutral point when terminal voltage v_{xy} is in mid-level, i.e., $\pm 0.5V_{\rm dc}$, the neutral-point voltage can be controlled by adjusting the mid-level intervals. In each mid-level interval, the direction of neutral-point current i_o is determined by the polarity of bridge current (i.e., the current flowing through a bridge). For instance, Fig. 16 illustrates the current conduction path for the switching state [PO] with different bridge current polarity. The bridge current polarity is defined as positive when it flows out through terminal x and into the bridge through terminal y, as shown in Fig. 16(a). Similarly, the relationship between direction of i_o and bridge current polarity under the other three switching states in mid-level intervals, i.e., [OP], [NO], and [ON], is summarized in Table IV, where it can be seen that the direction of neutral-point current i_o will change along with different bridge current polarity. Therefore, the neutral-point voltage balancing control with MIA method should be developed based on bridge current polarity.

According to the approaches of adjusting mid-level intervals, the MIA method can be further divided into MDC method [64], [65] and MPSDC method [47], [66], [67], [68], [69], [70], [71], [72]. The former regulates the charges injected into the neutral point by adjusting duty cycles of gate pulses, while the latter modifies both duty cycles and inner phase-shift angles

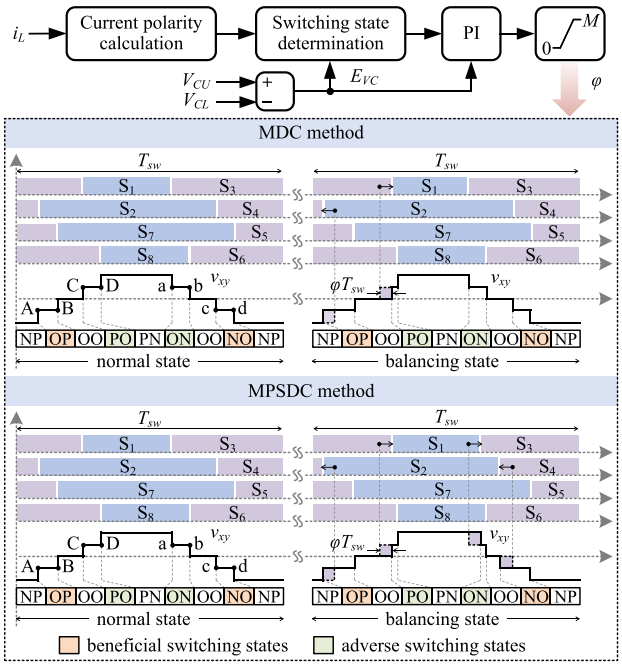

Fig. 17. Neutral-point voltage balancing with MIA method including MDC method and MPSDC method when $V_{CU} > V_{CL}$, $I_{[A,B]} < 0$ and $I_{[C,D]} < 0$.

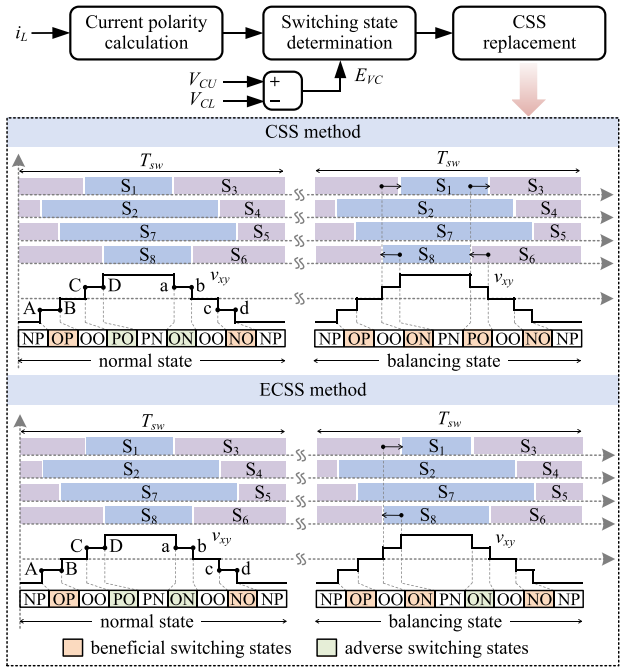

Fig. 18. Neutral-point voltage balancing with CSS method and ECSS method when $V_{CU} > V_{CL}$, $I_{[A,B]} < 0$ and $I_{[C,D]} < 0$.

of NPC bridge. Fig. 17 shows the voltage balancing control structure with MIA method under the condition of $E_{VC} > 0$, $I_{[A,B]} < 0$, and $I_{[C,D]} < 0$, where E_{VC} is the difference of two dc-link capacitors of NPC bridge, defined as $E_{VC} = V_{CU} - V_{CL}$, and $I_{[A,B]/[C,D]}$ is the average current during interval [A, B]/[C, D]. The current polarity during [a, b] and [c, d] is opposite to that of [A, B] and [C, D], respectively, in symmetrical modulation schemes. Thus, the polarity of $I_{[a,b]}$ and $I_{[c,d]}$ will not be mentioned in the following discussion. If an asymmetrical modulation is applied to the NPC-based DAB converters, the current polarity during the four intervals should be analyzed independently. In Fig. 17 (as well as Figs. 19 and 22), the dashed line in v_{xy} denotes the waveform before voltage balancing, and the solid line denotes that after applying a voltage balancing method. For the condition of $V_{CU} > V_{CL}$, the charges injected into neutral point should be increased, i.e., the intervals of $i_o > 0$ should be lengthened. Therefore, the switching states [OP] and [NO] which can achieve required positive neutral-point current are beneficial for voltage balancing, and they are defined as beneficial switching states. Conversely, the other two switching states, which will provide opposite neutral-point current are defined as adverse switching states. As shown in Fig. 17, the intervals of beneficial switching states are increased while those of adverse switching states are decreased by an additional variable φ, which is controlled by a PI controller.

b) Voltage balancing with CSS method: The MIA method balances neutral-point voltage of NPC-based DAB converters by dynamically modifying duty cycles and/or phase-shift angles of gate pulses. Thus, the waveform of terminal voltage v_{xy} will change, and the inductor current i_L will fluctuate due to (1),

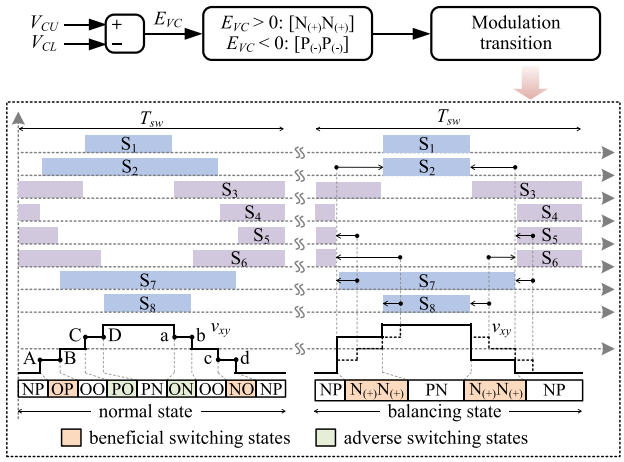

Fig. 19. Neutral-point voltage balancing with FSS method when $V_{CU} > V_{CL}$.

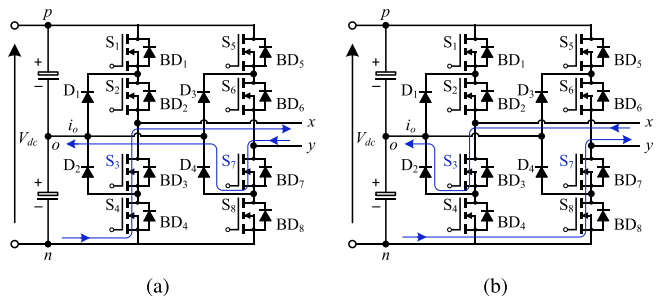

Fig. 20. Current conduction paths under the switching state $[N_{(+)}N_{(+)}]$ when the bridge current is: (a) positive and (b) negative for $V_{CU} > V_{CL}$.

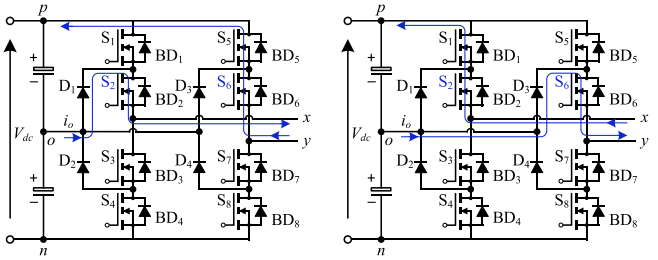

Fig. 21. Current conduction paths under the switching state $[P_{(-)}P_{(-)}]$ when the bridge current is: (a) positive and (b) negative for $V_{\mathrm{CU}} < V_{\mathrm{CL}}$.

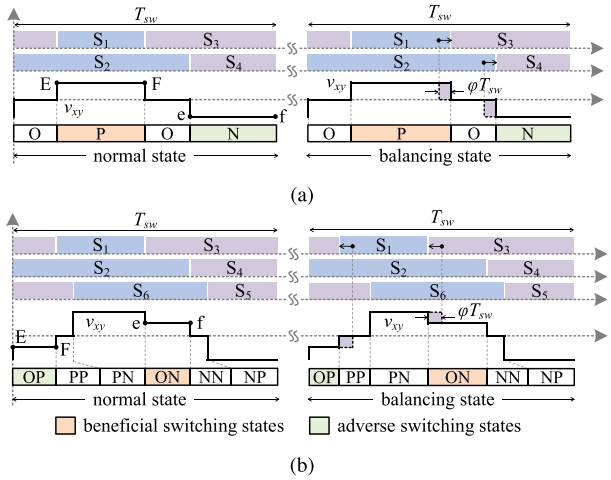

Fig. 22. Neutral-point voltage balancing with MIA method when $V_{\mathrm{CU}} > V_{\mathrm{CL}}$ and $I_{[\mathrm{E,F}]} > 0$ in: (a) HB NPC topology and (b) HFB NPC topology.

resulting in increased peak current, output voltage oscillations, and longer settling time [73]. To overcome this issue, a CSS method was proposed to the neutral-point voltage balancing control to smooth the dynamics [73], [74]. A CSS pair is defined as two switching states which can achieve opposite neutral-point charges/current under the same terminal VL and bridge current polarity. According to this definition, it can be seen from Table IV that [OP] and [NO], [PO] and [ON] are two pairs of CSSs. Fig. 18 shows a voltage balancing control strategy based on CSS method with the same operating condition of Fig. 17. Therefore, the beneficial and adverse switching states are also the same as those in Fig. 17. With the CSS method, the adverse switching states, i.e., [PO] and [ON] in normal state, are replaced by their CSSs [ON] and [PO] in balancing state, and the beneficial switching states [OP] and [NO] are kept unchanged, as shown in Fig. 18. In this manner, the waveform of terminal voltage v_{xy} can remain unchanged, and thus, the current fluctuations and increased peak current can be suppressed. At the same time, the direction of the neutral-point charges during all the four intervals becomes beneficial for voltage balancing after the replacement. Therefore, the difference between two capacitor voltages can be eliminated. Based on the CSS method, an ECSS method was proposed for the NPC-based DAB converters in [75] to reduce

TABLE V
SWITCHING STATES OF NPC BRIDGE APPLIED TO FSS METHOD

Switching state	Switching state at first arm	Switching state at second arm
$P_{(+)}$	$\{S_1\}$	$\{S_5\}$
$P_{(-)}$	$\{S_2\}$	$\{S_6\}$
$N_{(+)}$	$\{S_3\}$	$\{S_7\}$
$N_{(-)}$	$\{S_4\}$	$\{S_4\}$

capacitor voltage ripples. In the ECSS method, one of the two adverse switching states is replaced by its CSS to avoid large neutral-point voltage fluctuations when the error of two capacitor voltages is relatively low, as shown in Fig. 18.

c) Voltage balancing with FSS method: Based on the above analysis, MIA and CSS approaches require the determination of bridge current polarity. However, when the operating conditions and parameters (e.g., voltage and power levels) of NPC-based DAB converters change in a wide range, it will be challenging to identify the current polarity during each mid-level interval. Therefore, an FSS voltage balancing control method was proposed to decouple the neutral-point current direction from bridge current polarity [76], [77]. To achieve this, two new switching states $[N_{(+)}N_{(+)}]$ and $[P_{(-)}P_{(-)}]$ (as defined in Table V) are employed to the FSS method, as shown in Fig. 19, since the original four switching states in normal state cannot achieve decoupling between the neutral-point current direction and bridge current polarity. Figs. 20 and 21 illustrate the current conduction paths of the two new switching states with different bridge current polarity, where it can be seen that the neutral-point current depicts fixed direction regardless of whether the bridge current is positive or negative with the switching states $[N_{(+)}N_{(+)}]$ and $[P_{(-)}P_{(-)}]$. Thus, $[N_{(+)}N_{(+)}]$ and $[P_{(-)}P_{(-)}]$ will be used to balance the neutral-point voltage under the condition of $V_{\mathrm{CU}} > V_{\mathrm{CL}}$ and $V_{\mathrm{CU}} < V_{\mathrm{CL}}$, respectively.

d) Comparisons and discussions: The main characteristics and performance of various neutral-point voltage balancing control strategies for NPC-based DAB converters are presented in Table VI. Key features, including current polarity identification, the number of modified intervals, applied switching states, the use of an additional PI controller, and different balancing cases, have been discussed above. These features play a decisive role in shaping the performance of different voltage balancing methods with respect to factors such as inductor current fluctuations, robustness against parameter variations, applicability across various modulation schemes, and control complexity [129]. The performance characteristics and appropriate applications of these neutral-point voltage balancing control strategies are outlined as follows.

1) Due to similar balancing techniques, the voltage balancing performance with MDC and MPSDC methods is close. The two methods can be used to various modulations schemes by modifying certain phase-shift angles and/or duty cycles; however, the robustness to operating parameter and condition change is relatively low owing to the current model-dependent feature. Furthermore, as the inductor current polarity should be identified and the upper boundary of regulated control variable φ (i.e., M in

TABLE VI
MAIN CHARACTERISTICS OF VARIOUS NEUTRAL-POINT VOLTAGE BALANCING CONTROL METHODS

References	Method	Current polarity identification	Number of modified intervals	Applied switching states	Additional PI controller	Advantages (✓) and disadvantages (✗)
[64], [65]	MDC	Yes	2	[PO],[OP],[ON],[NO] (four original)	Yes	✓ applicable to various modulation and topology ✓ relatively low current fluctuations ✗ low robustness, complicated control ✗ dependent on inductor current model
[66], [67], [47], [68], [69], [70], [71], [72]	MPSDC	Yes	4	[PO],[OP],[ON],[NO] (four original)	Yes	✓ applicable to various modulation and topology ✗ relatively high current fluctuations ✗ low robustness, complicated control ✗ dependent on inductor current model
[73], [74]	CSS	Yes	2	[PO],[OP],[ON],[NO] (four original)	No	✓ very low current fluctuations ✗ long settling time with low error ✗ dependent on inductor current model
[76]	ECSS	Yes	2: high voltage error 1: low voltage error	[PO],[OP],[ON],[NO] (four original)	No	✓ very low current fluctuations ✓ short settling time with low error ✗ dependent on inductor current model
[76], [77]	FSS	No	2	$[N_{(+)}N_{(+)}]$,$[P_{(-)}P_{(-)}]$ (two new)	No	✓ inductor current model free ✓ high robustness, easy control ✗ high current fluctuations

Fig. 17) should be selected by compromising the current fluctuations and settling time, the implementation of MDC and MPSDC methods is relatively complicated. With the same control parameters, the MPSDC method can achieve faster voltage balancing while larger current fluctuations compared to MDC method due to doubled modified intervals. According to the above performance analysis, the MIA method including MDC and MPSDC methods can be suitably used to the condition where various modulation schemes are employed during different voltage and power levels [129]. For instance, the modulation scheme proposed in [38] applies 3VL and 5VL under different voltage conversion ratios. As for other NPC-based topologies, e.g., HB and HFB, the MIA method can be applied for voltage balancing by regulating the duty cycles or phase-shift angles, as shown in Fig. 22. Therefore, the MIA control is suitable for different NPC-based topologies and various modulation methods.

2) The CSS and ECSS methods can balance neutral-point voltage without changing the terminal voltage waveform, and thus, current fluctuations will be significantly suppressed during balancing process. However, the CSS and FSS methods cannot be used to the HB or HFB topology, as the switching states related to inner switches on both the two NPC bridge arms (i.e., S_2/S_3 and S_6/S_7) should work in coordination in these two methods. Furthermore, these methods are not applicable in modulation schemes with 2VL or 3VL terminal voltage due to no mid-level interval. The inductor current polarity is also required in CSS and ECSS methods; however, as the current waveform keeps unchanged during balancing state, the current polarity is relatively easy to be determined by steady-state current model. As a result, the implementation complexity of CSS and ECSS methods is lower than that of MDC or MPSDC method. The ECSS method adjusts the number of modified intervals based on the level of neutral-point voltage error, which can achieve lower oscillations of dc-link capacitor voltages and shorter settling time during balancing. Due to the superior dynamic performance, CSS and ECSS methods are suitable for applications with a continuous imbalance source. Furthermore, the current polarity remains fixed under soft-switching operation, making CSS and ECSS methods applicable for such scenarios.
3) The model-free feature of FSS method can significantly reduce the control complexity as the balancing cases are only determined by capacitor voltage error rather than inductor current polarity. Therefore, the robustness against parameter and condition variations with FSS method is high due to decoupling from current polarity change. However, significant change of the switching sequences during balancing state causes high current fluctuations, making the FSS method not suitable for conditions with a continuous imbalance source. This method is mainly suitable for the conditions where the inductor current polarity is difficult to determine and operating parameters change in a wide range, e.g., wide-input/output-voltage applications.

Based on the above analysis, the applicable and nonapplicable scenarios of these neutral-point voltage balancing control strategies are summarized in Table VII.

B. OCF Diagnosis and FT Control

SCF and OCF are two typical reliability issues for power electronic converters. An SCF will generally cause overcurrent, which subsequently triggers the protection system and halts the converters [52]. On the other hand, the OCF also introduces voltage and current distortions, and impacts normal operation. However, by applying an FT control, it is possible to bring the system back to safe operation instead of shutting it down [52], [78], [130]. An OCF on the NPC-based DAB converters will cause dc bias on inductor current, which will further result in a high peak current and potential saturation of transformer. Furthermore, when an OCF occurs on an outer switch of NPC bridge (e.g., S_1), the neutral-point voltage will become unbalanced [78]. These effects will increase the voltage or current

TABLE VII
APPLICABLE AND NONAPPLICABLE SCENARIOS OF VARIOUS VOLTAGE BALANCING CONTROL METHODS

Method	Applicable (✓) and non-applicable (✗) scenarios
MIA (MDC and MPSDC)	✓ NPC-based DAB with HB and HFB topology ✓ control strategies with various modulation methods ✗ voltage and power levels change in a wide range and inductor current polarity is challenging to determine
CSS and ECSS	✓ soft-switching control ✓ applications with a continuous imbalance source ✗ NPC-based DAB with HB and HFB topology ✗ control strategies with 2VL and 3VL modulation methods ✗ voltage and power levels change in a wide range and inductor current polarity is challenging to determine
FSS	✓ voltage and power levels change in a wide range and inductor current polarity is challenging to determine ✗ NPC-based DAB with HB and HFB topology ✗ control strategies with 2VL modulation method ✗ applications with a continuous imbalance source

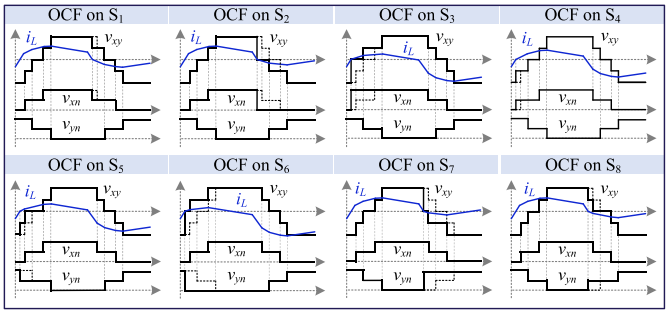

Fig. 23. Postfault waveforms when an OCF occurs on the eight switches of an NPC bridge (3LFB is used to secondary side).

stresses on power semiconductors and passive components, affecting their lifetimes and reliability of the entire system [52], [78]. To mitigate the negative effects and ensure the NPC-based DAB converters operate within safe operating limits, an FD method should be used to locate the faulty position, after which an FT control will be activated to restore the converter to safe operation.

a) FD methods: When an OCF occurs on the DAB converters, the waveforms of voltages and currents will change, as shown in Fig. 23, where v_{xn} and v_{yn} denote the midpoint voltages, which are the voltages at midpoint x/y of each bridge arm referred to the negative dc-link port n. In Fig. 23, the dashed and solid lines in voltages denote the waveforms in prefault and postfault conditions, respectively. Thus, the faulty switch can be determined by certain postfault information extracted from these waveforms. FD methods of power electronic converters typically require the following:

1) precise identification of faulty devices;
2) rapid detection speed;
3) compatibility with various operating conditions;
4) minimal reliance on additional hardware;
5) low computation burdens.

Prior research on FD techniques for various converters focused on addressing some of these demands. OCF diagnosis methods have been widely researched for the NPC topology in inverters/rectifiers, which can be divided into signal-processing-based method, model-based method, and data-based method [131]. Unfortunately, due to different modulation strategies and switching characteristics, the FD methods proposed based on NPC inverters/rectifiers cannot be directly applied to the NPC-based DAB converters [79]. On the other hand, some FD methods were proposed for DAB converters, whose main characteristics are summarized in Table VIII. Similar to three-phase inverters and rectifiers, phase currents are also widely applied as diagnostic signal to locate the faulty switch in three-phase DAB converters [132], [133], [134]. These FD methods can be easily implemented; however, six current sensors are needed to detect the phase currents in primary and secondary sides. In addition, terminal voltage of each bridge arm is detected by an FD circuit composed of an attenuator and instrumentation amplifier to identify the faulty switch in three-phase DAB converters [135], which requires minimal additional hardware costs. As for single-phase DAB converters, various voltages and/or currents are employed as diagnostic signals in FD methods, including terminal voltage v_{xy}, inductor current i_L, and midpoint voltages v_{xn} and v_{yn} [136], [137], [138], [139], [140], [141], [142], [143]. The terminal voltage of a 2LFB can be used to determine two possible faulty switches in diagonal position, e.g., S_1 and S_4, as the postfault waveform of terminal voltage is the same when an OCF occurs on the two switches [136]. Thus, a specific faulty switch cannot be determined. To address this issue, the inductor current is added to FD system together with terminal voltage, and specific switching states are inserted into the modulation during faulty state to locate the specific faulty switch [137]. In this method, a current sensor and a winding of magnetic core is used to detect the terminal voltage and inductor current. When applying the midpoint voltage of each bridge arm, the faulty conditions of two diagonal switches can be easily differentiated, and then, the upper and lower switches in a same arm can be determined by the average midpoint voltage value, as shown in Fig. 24(a) [139], [140], [141], [142], [143]. However, four voltage sensors should be added to the DAB system, which will increase the hardware costs and volume.

The above FD methods were developed based on 2L DAB converters, and when applying them to the 3L NPC bridge, the differentiation of two switches in a same upper/lower arm, e.g., S_1 and S_2, should be further discussed. In [78], an FD method was proposed by utilizing the midpoint voltage of each bridge arm as diagnostic signals for the NPC-based DAB converters, as shown in Fig. 24(b). In this method, the variation of average midpoint voltage is used to locate two possible faulty switches in a same upper/lower arm. Subsequently, the midpoint voltage waveforms are converted to square waveforms with different duty cycles to identify the specific faulty switch. The calculation of average midpoint voltages, waveform transition, and identification of duty cycles are all carried out in the microcontroller. In addition, multisampling is needed during the calculations in each switching period to collect sufficient data during faulty intervals. Thus, the computation burdens of the microcontroller will be heavy. Furthermore, four additional voltage sensors are needed to monitor the midpoint voltage of all bridge arms, which will increase the hardware costs and volume. In order

TABLE VIII
PRIOR-ART FD METHODS FOR DAB CONVERTERS

References	Topology	Diagnostic signal	Diagnostic position	Detection time	Hardware	Advantages (✓) and disadvantages (✗)
[132]	3-phase 2L DAB	DC component of phase and magnetization currents	faulty switch	not mention	6 current sensors	✓ suitable for various operating modes ✓ easy to be implemented ✗ high sampling frequency and hardware costs ✗ not suitable for 3L NPC topology
[133]	3-phase 2L DAB	DC component of phase currents	faulty phase	not mention	6 current sensors	✓ the same as [132] ✗ the same as [132] ✗ cannot locate certain faulty switch
[134]	3-phase 2L DAB	DC component of phase currents	faulty switch	$< 5T_{sw}$	3 current sensors	✓ low-bandwidth sensing and high trip level ✓ suitable for various operating modes ✗ additional sensors are needed ✗ relatively long diagnostic time ✗ not suitable for 3L NPC topology
[135]	3-phase 2L DAB	terminal voltages	faulty switch	$< 1T_{sw}$	6 FD circuit composed of attenuator and instrumentation amplifier	✓ fast diagnostic speed ✓ low hardware costs ✗ complicated implementation
[136]	2L DAB	terminal voltages	2 diagonal switches	$< 1T_{sw}$	2 voltage sensors	✓ easy to be implemented ✗ additional sensors are needed ✗ high sampling frequency ✗ cannot locate certain faulty switch
[137]	2L DAB	residual of terminal voltage and inductor current with certain switching state injection	faulty switch	$< 3T_{sw}$	1 current sensor & 1 auxiliary winding	✓ relatively low hardware costs ✗ complicated implementation ✗ cannot locate certain switch in NPC topology
[138]	2L DAB	midpoint voltage & inductor current	faulty switch/diode	not mention	4 voltage sensors & 1 current sensor	✓ faulty switch and diode can be determined ✗ high hardware costs ✗ cannot locate certain switch in NPC topology
[139], [140], [141], [142], [143]	2L DAB	average midpoint voltages	faulty switch	$< 1T_{sw}$	4 voltage sensors	✓ suitable for various operating conditions ✓ fast diagnostic speed ✓ easy to be implemented ✗ high sampling frequency and hardware costs ✗ cannot locate certain switch in NPC topology
[78]	3L NPC DAB	average midpoint voltage with waveform transition	faulty switch	$< 2T_{sw}$	4 voltage sensors	✓ suitable for various operating conditions ✓ fast diagnostic speed ✗ high sampling frequency and hardware costs
[79]	3L NPC DAB	average midpoint voltage with CIS	faulty switch	$< 4T_{sw}$	4 AVD circuits	✓ suitable for various operating conditions ✓ low hardware costs and sampling frequency ✗ relatively long diagnostic time

to reduce the hardware costs and computation burdens, an FD method proposed in [79] applies an average-value-detecting (AVD) circuit composed of operational amplifiers and passive components. The average midpoint voltages are obtained by the AVD circuit, and thus, the sampling rate in the microcontroller can be reduced. The postfault conditions of the outer and inner switches are differentiated by blocking a certain CIS. If an OCF occurs on an inner switch, the average midpoint voltage will fluctuate around half of dc voltage, i.e., $0.5V_{\rm dc}$, as the midpoint voltage waveform will become symmetrical after blocking its CIS. Otherwise, the average value of the midpoint voltage will be higher or lower than $0.5V_{\rm dc}$ when an OCF occurs on an outer switch, as shown in Fig. 24(c).

During the FD process, the noises on the diagnostic signals can significantly degrade the accuracy and reliability of the FD methods. To mitigate this issue, appropriate thresholds should be incorporated into FD methods, e.g., α, β, and γ in Fig. 24. These thresholds are influenced by a variety of nonideal factors, including EMI, measurement and switching noise, and parasitic parameters within the circuit and power modules. Deriving precise analytical expressions for these thresholds is highly challenging due to the complex dependence of noise on the circuit design and operational environment. As a result, in practical applications, these thresholds are typically determined based on the overall noise level in the system [78], [79].

b) FT control: After the faulty switch is located, an FT control should be applied to suppress the negative OCF effects. In general, the FT control strategies should be evaluated according to the following:

1) required additional hardware;
2) dc bias and current stress;
3) postfault power-transfer capability;
4) implementation complexity.

The FT control can be achieved by adding redundant components or modifying modulation scheme. The former method is generally applied to the systems with a large amount of power devices, e.g., cascaded DAB converters in the SST, and MMC [144], [145]. As for a single DAB converter, the modulation reconfiguration is typically applied to reduce the peak current and dc offset to bring the converter back to safe operation. The FT control strategies of the DAB converters are summarized in Table IX.

Two typical FT control schemes can be applied to the three-phase DAB converters, i.e., frozen faulty arm and open faulty arm [133], [146], [147]. The former blocks gate pulses of switches in the faulty arm while the corresponding body diodes can keep working to provide certain current conduction paths. On the other hand, the latter uses a relay to put aside the faulty arm, and thus, the three-phase bridge will operate in single-phase mode. The open-faulty-arm method can increase postfault

TABLE IX
PRIOR-ART FT CONTROL METHODS FOR DAB CONVERTERS

References	Topology	FT method	FD requirement	Additional hardware	DC bias	Advantages (✓) and disadvantages (✗)
[145]	hybrid cascaded 2L DABs	redundant module replacement	location of faulty DAB	a redundant DAB converter	no	✓ low requirement of FD complexity ✓ possible to keep power constant ✗ high hardware costs ✗ not suitable for a single DAB converter
[146]	3-phase 2L DAB	frozen faulty arm	location of faulty arm	no	no	✓ no additional hardware costs ✗ low power-transfer capability ✗ high current stress
[133], [147]	3-phase 2L DAB	open faulty arm	location of faulty arm	6 relays	no	✓ high power-transfer capability ✓ low current stress ✗ increased hardware costs and volume
[140], [141], [142], [143], [148], [149]	2L DAB	PLP-SBA method	location of faulty arm	no	yes: OCF on primary side no: OCF on secondary side	✓ easy to be implemented ✓ relatively low requirement of FD ✗ low power-transfer capability in 3L NPC
[150]	2L DAB	SSB-SBA method	location of faulty switch	no	yes: OCF on primary side no: OCF on secondary side	✓ easy to be implemented ✓ relatively high power-transfer capability ✗ high requirement of FD
[78]	3L NPC DAB (2LFB-3LFB)	PLP-CSB method	location of faulty switch	no	the same as [150]	the same as [150]
[80]	3L NPC DAB (3LFB-3LFB)	CSB method	location of faulty switch	no	yes: OCF on inner switches in primary side no: OCF on other switches	✓ easy to be implemented ✓ relatively high power-transfer capability ✓ higher DC-bias free possibility ✗ high requirement of FD
[81]	3L NPC DAB (3LFB-2LFB)	CSB-SBA method	location of faulty switch	no	the same as [80]	the same as [80]

power-transfer capability and reduce current stress compared to the frozen-faulty-arm method [147]. However, the hardware costs and volume will increase with the open-faulty-arm method, and the additional relays will also negatively affect the system reliability. The open-faulty-arm method cannot be used to single-phase DAB converters owing to lack of redundant bridge arm. As for the single-phase DAB converters, a primary side lower power-secondary side bypass arm (PLP-SBA) method was widely applied to the FT control system [140], [141], [142], [143], [148], [149]. In this method, when an OCF occurs on the secondary side, the other switches in faulty arm will be blocked, which is the same as the frozen-faulty-arm method for three-phase DAB converters. However, the faulty arm in the primary side cannot be bypassed; otherwise, the transferred power will be zero [78], [141]. Thus, in the PLP-SBA method, when an OCF occurs on the primary side, the topology will not be reconfigured by modifying gate pulses; instead, the transferred power will be reduced to make sure the converter operates in safe range [140], [141], [142], [143], [148], [149]. In general, the maximum peak value of inductor current is selected as the upper threshold to limit the transferred power [148]. However, the dc bias on inductor current cannot be eliminated when an OCF occurs in primary side. When applying the bypass arm method in secondary-side 3L NPC bridge, the other three switches in faulty arm will be blocked. Thus, the postfault topology with FT control will be the same regardless of which switch in a bridge arm is the faulty one. Therefore, identifying the faulty bridge arm is sufficient, and it is not necessary to locate the specific faulty switch. The postfault topology with the FT method is shown in Fig. 25, where the primary-side and secondary-side power devices are denoted by the subscripts p and s, respectively, e.g., S_{p1} and S_{s1}. When an OCF occurs on an inner switch, the corresponding outer switch will also stop working as no current conduction path exists, as shown in Fig. 25. An SSB method was proposed to primary side to reduce current stress and enhance postfault power-transfer capability in [150]. In this method, when an OCF occurs on a primary-side switch, e.g., S_{p1}, the switch in the same position of secondary side, i.e., S_{s1}, will be blocked.

In order to fully utilize the increased power devices (also means more current conduction paths) in the 3L NPC topology to extend the postfault power range, a CSB method is used to the FT control for NPC-based DAB converters in [78], [80], and [81]. In this method, two switches located symmetrically on the bridge leg are defined as a complementary-switch pair, i.e., S_1 and S_4, S_2 and S_3, S_5 and S_8, S_6, and S_7. When an OCF occurs on a switch (e.g., S_1), its complementary switch (i.e., S_4) will be blocked to bring the postfault waveforms back to be symmetrical. As shown in Fig. 25, when an OCF occurs on an outer switch, the CSB method can be applied to both primary and secondary sides. On the other hand, when an OCF occurs on an primary-side inner switch, the transferred power will be zero if blocking the other inner switch in the same arm. Thus, the PLP method should be applied rather than CSB method in this condition. As for the secondary side, after blocking the CIS, the equivalent topology will be the same as that of SBA method, as the two outer switches in the same arm will stop working.

C. TS DC Bias Suppression Control

DC bias on inductor current will increase current stress on power devices, potentially cause saturation on transformer, and result in higher power losses, which significantly affect reliable operation of NPC-based DAB converters [151], [152], [153]. DC bias exists during both steady and TSs due to asymmetrical circuit layout, asynchronous trigger pulses, tolerances in component parameters, and so on [151]. DC bias can be reduced by regulating hardware topology, e.g., adding a dc-blocking

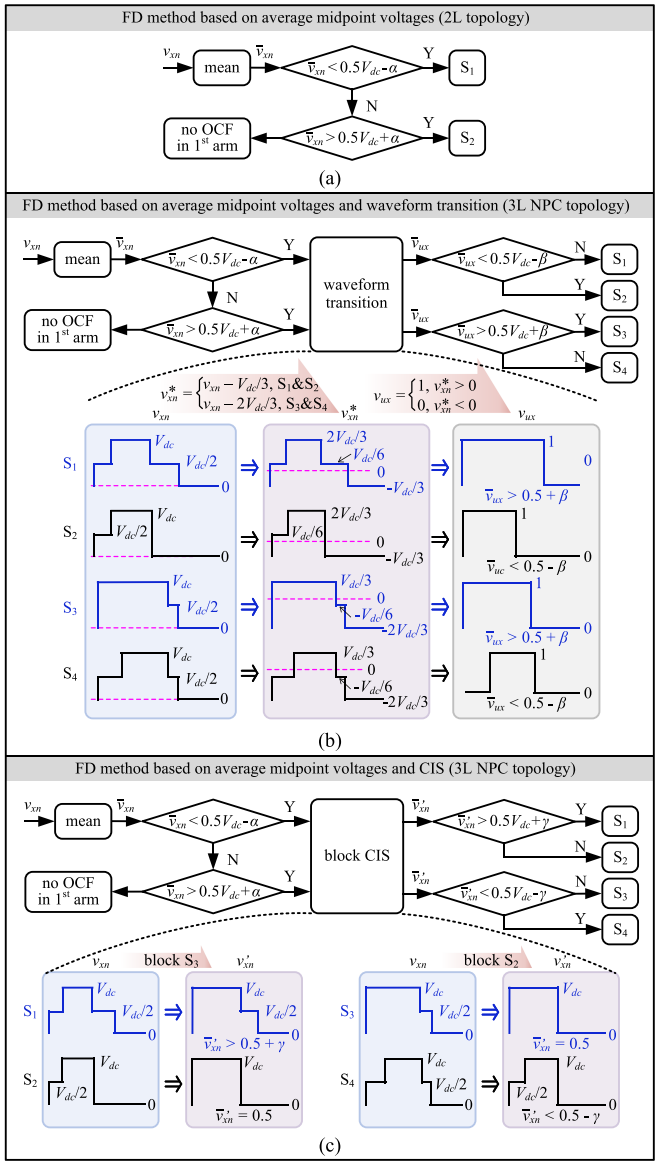

Fig. 24. Structures of FD methods applied to the NPC-based DAB converters based on: (a) average midpoint voltages, (b) average midpoint voltages and waveform transition, and (c) average midpoint voltage and CIS.

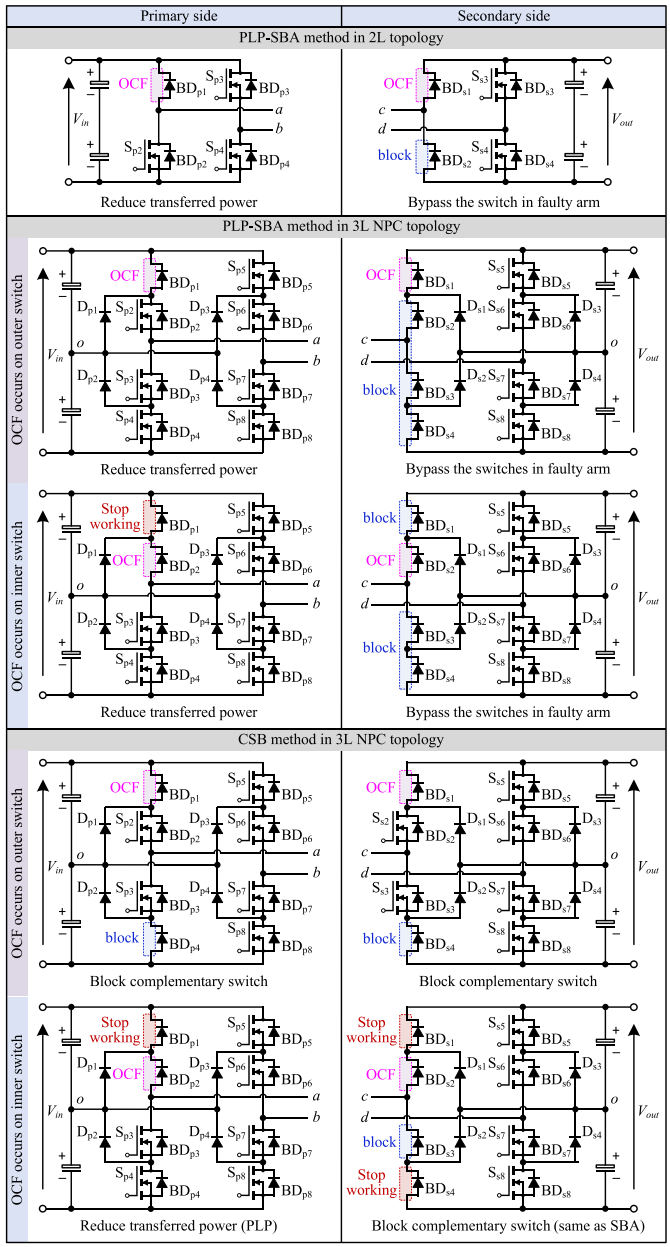

Fig. 25. Postfault topologies after applying the FT control with PLP-SBA and CSB methods.

capacitor or auxiliary core to the transformer [154], [155], [156]. In addition to the passive suppression methods, some dynamic control strategies are applied to reduce the dc bias, current overshoots, and settling time. Fig. 26 reveals the TS dc bias caused by control-variable change, where $\alpha'_{i/o}$ and d' denote the phase-shift angles and duty cycles after the load changes, respectively. The dc bias occurs because the voltage-second balance on inductor will fail at the moment when the control variables (i.e., phase-shift angles and duty cycles) change due to variations of transferred power.

To reduce the transient-state dc bias and peak current, various dynamic control strategies have been proposed for the DAB converters. In [34], the dynamic control methods were divided into load feedforward control [157], [158], power-based

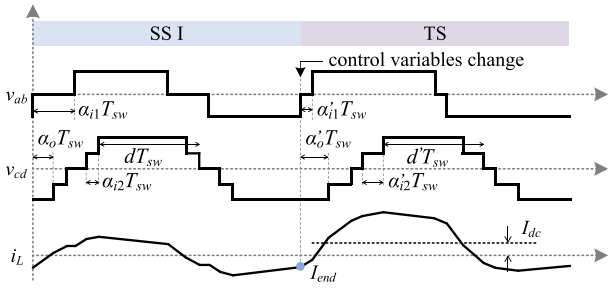

Fig. 26. DC bias during TS when control variables change.

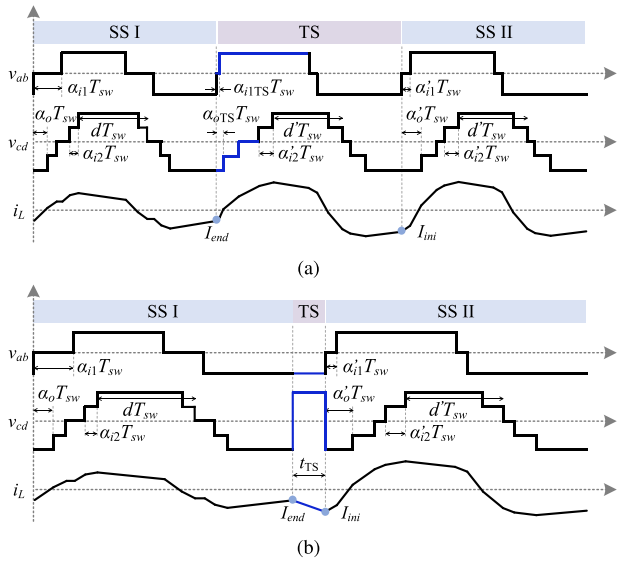

Fig. 27. Waveforms during steady and TSs to reduce dc bias with: (a) PLT control and (b) SFT control.

control [159], [160], and direct-inductor-current control. The former two control methods are mainly used to reduce dynamic fluctuations and settling time. The dc bias can also be reduced with these two methods; however, as the inductor current is not the direct control objective, the dc bias will still exist for a relatively long time during TS. On the other hand, the direct-inductor-current control modifies the inductor current directly based on inductor current model, which can complete TS within one switching period [151]. Based on the shape of inductor current, the direct-inductor-current control strategies for reducing dc bias can be mainly divided into PLT control and SFT control, as shown in Fig. 27. As shown in Fig. 27, I_{end} and I_{ini} are the currents at the end point of steady state I (SS I) and initial point of steady state II (SS II), respectively. A TS control is added between the two steady states to smoothly convert inductor current from I_{end} to I_{ini} without significant dc bias [151]. Table X summarizes main characteristics of prior direct-inductor-current control strategies. In the PLT control, the time interval of TS is the same of switching period, and the dc bias reduction can be completed within one switching period. During the TS, the control variables will be regulated according to inductor current model. Due to the two terminal currents I_{end} and I_{ini} are different, the inductor current waveform during TS will not be symmetrical, as shown in Fig. 27(a). $\alpha_{i1\mathrm{TS}}$ and $\alpha_{o\mathrm{TS}}$ are the modified control variables during TS, which can be obtained by the two terminal currents I_{end} and I_{ini}, and further calculated by the steady-state inductor current model based on the control variables of the two steady states. The phase-shift angles and duty cycles during TS can be regulated in one or both two of the terminal voltages v_{ab} and v_{cd}. Therefore, the PLT control can be accordingly divided into single-side PLT [161], [162], [163], [164], [165], [166] and double-side PLT methods [82], [83], [84], [85], [167], [168], [169]. Both approaches can be further classified into half-switching-period (HSP) regulation, full-switching-period (FSP) regulation, and

TABLE X
MAIN CHARACTERISTICS OF DIRECT-INDUCTOR-CURRENT CONTROL TO REDUCE TS DC BIAS OF DAB CONVERTERS

Reference	Topology	Modulation	Method	Settling time	Computational complexity
[161], [162], [163]	2LFB-2LFB	1DoF (2VL-2VL)	single-side HSP-PLT	$< 0.5T_{sw}$	★★☆
[164]	2LFB-2LFB	3DoF (3VL-3VL)	single-side HSP-PLT	$< 0.5T_{sw}$	★★★★
[165]	2LFB-2LFB	1DoF (2VL-2VL)	single-side FSP-PLT	$< 1T_{sw}$	★★★
[166]	2LFB-2LFB	2DoF (3VL-2VL)	single-side AVL-PLT	$< 0.5T_{sw}$	★★★
[82], [85]	3LFB-3LFB	5DoF (5VL-5VL)	double-side HSP-PLT	$< 0.5T_{sw}$	★★★★
[168]	2LFB-2LFB	1DoF (2VL-2VL)	double-side FSP-PLT	$< 1T_{sw}$	★★☆
[169]	2LFB-2LFB	1DoF (2VL-2VL)	double-side AVL-PLT	$< 1T_{sw}$	★★★☆
[170]	2LFB-2LFB	3DoF (3VL-3VL)	SFT	$< 0.12T_{sw}$	★★
[171]	2LFB-2LFB	1DoF (2VL-2VL)	SFT	$< 1T_{sw}$	★★

Computational complexity increases with more ★.

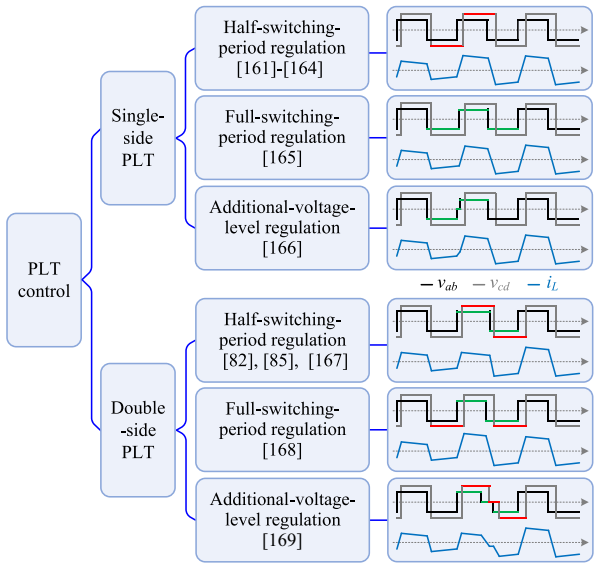

Fig. 28. Classification of PLT control in DAB converters.

additional-voltage-level (AVL) regulation methods, as shown in Fig. 28. In HSP regulation, the phase-shift angle and/or duty cycle are adjusted within half of a switching period, enabling the inductor current to settle into a steady-state profile over that half cycle. In contrast, FSP regulation performs these adjustments over the FSP. As for AVL regulation, a zero-VL is added to the terminal voltages to modify the inductor current. Note that SPS control is taken as an example in Fig. 28, and the PLT methods with multi-DoF modulation are classified similarly.

On the other hand, the SFT control employs a specific switching state during the TS, and thus, the inductor current waveform during TS is a straight line [170], [171], as shown in Fig. 27(b). The regulation time of TS is affected by the two terminal currents

and current slope, which is further determined by the switching states used to TS. In order to accelerate the transient control, the maximum current slope should be applied, i.e.,

$$l_{\max} = \frac{k_{\text{pt}} v_{ab} + N k_{\text{st}} v_{cd}}{L_s}. \tag{15}$$

Therefore, the TS time can be calculated by

$$t_{\text{TS}} = \frac{|I_{\text{ini}} - I_{\text{end}}|}{l_{\max}}. \tag{16}$$

The computational complexity of TS dc bias suppression control strategies is mainly determined by the following issues:

1) number of operating modes;
2) calculation complexity of TS control variables;
3) implementation of TS gate pulses.

In SFT control strategies, an FSS is employed during the TS regardless of modulation schemes [170], [171]. In addition, the calculation of TS time t_{TS} and implementation of gate pulses is simple. Therefore, the computational complexity of SFT control strategies is low. On the other hand, the PLT control strategies modify the control variables according to the operating modes. When SPS control is applied in the steady state, only a single operating mode is involved, which simplifies the implementation of PLT control. However, different operating modes are used in multi-DoF modulation, and the TS control variables should be calculated according to the models of specific operating modes. Moreover, during TS under multi-DoF modulation, increased duty cycles and/or phase-shift angles are computed, resulting in high computational complexity. Furthermore, with the AVL regulation method in SPS modulation [166], [168], the gate pulses of the two switches located diagonally in a 2LFB (e.g., S_1 and S_4) should be separately generated. Thus, additional gate pulses are required to be created, which also increases the computational burden. Based on the analysis, the computational complexity of various TS dc bias suppression control strategies can be evaluated, as shown in Table X.

Furthermore, most of the above TS dc bias suppression control strategies neglected the output voltage fluctuations when the dc load changes, especially with closed-loop control system. A feedforward compensation is added to the TS control system, where the MDCs are calculated based on DAB model, and then are added to the output voltage and dc-bias current control loops [172]. Thus, the dc overshoot and settling time caused by load variation can be reduced.

D. Other Reliability-Related Control

In addition to the capacitor voltage balancing control, FD and tolerant control, and TS dc bias suppression control, the reliability of NPC-based DAB converters can be improved by some other control schemes.

a) Power loss balancing: For the 3L NPC topology, power loss distribution on various power semiconductors will be different, especially between: 1) leading and lagging bridge arms, and 2) outer and inner switches. The unbalanced power losses imply that certain power devices withstand higher voltage and current stresses, which will accelerate the aging process and reduce their lifetime. In addition, such imbalance can lead to variations in parameters of power devices, e.g., on-state resistance. This, in turn, exacerbates the hardware imbalance over time. Therefore, the overall reliability of NPC-based DAB converters will be affected by the unbalanced power losses [173]. In addition to the modulation with 2VL terminal voltage, the power losses of two diagonal switches in leading and lagging bridge arms will be different as the instantaneous currents at switching instants and/or rms current during conducting period are different. In order to balance the power losses of leading and lagging bridge arms, a control scheme alternating leading and lagging gate pulses at certain intervals (e.g., $2T_{\text{sw}}$) was proposed in [85] and [86], as shown in Fig. 29. This is because when exchanging the leading and lagging arms, the terminal voltage v_{xy} will not change, and thus, the power transfer will not be affected by arm switching. In this manner, the power losses of the four outer/inner switches in NPC-FB will be close.

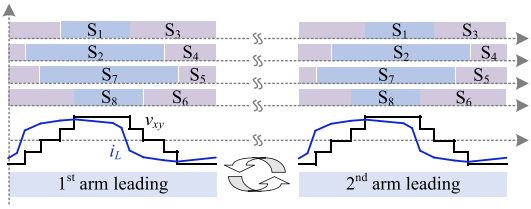

Fig. 29. Power loss balancing for two bridge arms by exchanging leading and lagging arms at certain intervals.

On the other hand, the conduction and switching losses of outer and inner switches in a same upper/lower arm are also different when their duty cycles are not the same, e.g., in 5VL modulation. Unfortunately, to the best of authors' knowledge, no research has yet been conducted on loss balancing control for the inner and outer switching devices of NPC-based DAB converters. This issue will be discussed with potential solutions in Section VI-A.

b) Voltage and current stress reduction: High voltage and current stresses will accelerate power device aging and negatively affect the reliability of power electronic converters. Thus, the control strategies of current stress reduction analyzed in Section III will not only enhance the efficiency of NPC-based DAB converter but also improve its reliability. A voltage-swing-reduction control scheme was proposed for a reconfigurable 3L NPC-based DAB converter in wide input and output voltage applications [87], where the clamping diode D_4 in the second arm is replaced by a switch S_9, as shown in Fig. 30(a). The topology will be reconfigured as FB and HB modes by the modulation, as shown in Fig. 30(b) and (c), according to input VL. According to (6), when FB topology is used during low-voltage range while HB is applied to high-voltage scenario, the voltage conversion ratio will be limited, and can be designed around unity. In this manner, soft switching and reduced current stress are effectively achieved [13]. Moreover, the control strategy employed in the reconfigurable NPC-based DAB converter obviates the need for additional relays or contactors, further contributing to system reliability enhancement [87].

c) Conducted EMI suppression: EMI will affect the reliability of power electronic converters by interfering with control

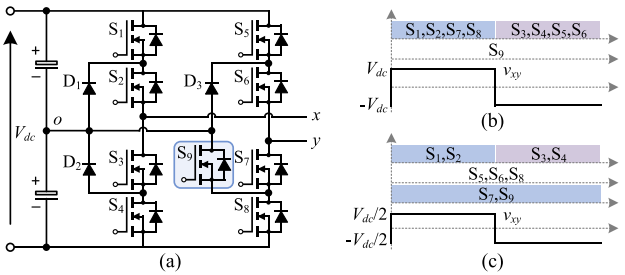

Fig. 30. Reconfigurable 3L NPC topology and corresponding control scheme proposed in [87]. (a) topology when replacing D_4 by S_9. (b) FB control mode. (c) HB control mode.

signals, accelerating component aging, increasing thermal effects, and causing EMC issues. Therefore, suppressing EMI is crucial for improving system stability and extending its service life [174], [175], [176]. The conducted EMI can be suppressed by reducing common-mode (CM) voltage and current, which can be achieved by certain hardware components such as passive CM EMI filters and special designed transformer with shielding layer [58], [59]. However, these methods will increase hardware costs, volume, and design complexity. On the other hand, the CM voltage and current can also be mitigated according to modulation schemes. An improved modulation-based method was proposed for 3L NPC-based DAB converters to suppress CM voltage [175]. In this control strategy, certain relationship among phase-shift angles and duty cycles of gate pulses should be satisfied to keep the switching-node voltages constant, and further to suppress CM EMI. In [176], a CM current cancellation technique was developed for paralleled NPC-based DAB converters, where dv/dt cancellation with complementary switching is used to suppress low-frequency CM conducted EMI, and power sharing is applied together with dv/dt cancellation to reduce the resonant peaks during high-frequency range.

V. Interaction of Efficiency- and Reliability-Oriented Control Strategies

The efficiency-oriented and reliability-oriented control strategies for the NPC-based DAB converters are discussed separately in Sections III and IV, respectively. However, most of these control strategies are determined by the phase-shift angles and duty cycles, and thus, despite the different optimization objectives, the efficiency- and reliability-oriented control strategies inevitably influence each other due to their reliance on these shared control variables.

A. Synergistic Interaction

The control strategies aimed at enhancing both efficiency and reliability can exert mutually reinforcing effects, which can be summarized as follows.

1) Minimum-rms/peak-current control strategies for efficiency improvement can reduce the current stresses on power devices. Therefore, the reliability of these devices can be significantly enhanced, as lower current stresses mitigate thermal loading, and minimize the risks of failure mechanisms such as solder fatigue and bond wire degradation. By alleviating these stress factors, such control strategies not only improve efficiency, but also extend the operational lifetime of the DAB converters.
2) ZVS control schemes, proposed to improve the converter efficiency, can also enhance the reliability of power semiconductors by reducing the switching losses and junction temperatures. Furthermore, ZVS operation mitigates dv/dt-related electrical stress and EMI, contributing to a more robust and stable operating environment for long-term device reliability.
3) When an OCF occurs on NPC-based DAB converters, the increased dc bias causes higher inductor current, which results in increased power losses on power semiconductors, auxiliary inductor, and transformer. Therefore, when an FT control scheme is applied to bring the postfault inductor current back to symmetrical, both the reliability and efficiency of NPC-based DAB converters can be enhanced. A similar condition applies to the TS dc bias suppression control strategies.
4) Neutral-point voltage imbalance with a large voltage deviation will cause waveform distortion on terminal voltage v_{cd}, which further result in zero-current-point drifting of the inductor current i_L. As a result, the ZVS operation will fail under certain conditions. When the CSS technique is applied to balance the capacitor voltages, the phase relationship between terminal voltages and inductor current remains constant, and thus, the ZVS control proposed for normal state (i.e., without voltage imbalance) can also be achieved during balancing state. Therefore, both the reliability and efficiency can be enhanced with the neutral-point voltage balancing control scheme.

B. Conflicting Interaction

While some control strategies can simultaneously improve both efficiency and reliability, others may present tradeoffs between the two objectives. These conflicts arise when optimizing one aspect inadvertently compromises the other, primarily due to the shared modulation parameters and operational constraints. These conflicting interaction can be mainly summarized as follows.

1) Efficiency-oriented control schemes generally take total power loss minimization as their primary optimization objective. As a result, the power loss distribution across individual semiconductor devices cannot be actively regulated. However, for reliability-oriented operation, the power loss and corresponding thermal stress need to be more evenly balanced among different power devices, particularly between the outer and inner switches of the NPC legs, to mitigate localized overheating and extend device lifespan. On the other hand, when loss and thermal balancing is considered as the major reliability-oriented objective, the improvement of total converter efficiency will be impacted. Therefore, achieving an optimal tradeoff

between global efficiency and device-level thermal reliability remains a key challenge in the coordinated design of control strategies.

2) Control strategies for efficiency optimization are typically designed with steady-state performance as the primary objective, such as achieving soft-switching operation and reducing rms current under steady conditions. However, when additional reliability-oriented control is introduced, the control variables may change, potentially compromising the effectiveness of these efficiency optimization methods. For instance, when applying MIA or FSS method to balance the neutral-point voltage, the inductor current will increase and the ZVS constraints will not be satisfied under certain operating conditions due to the varying phase-shift angles and/or duty cycles. Therefore, the efficiency during the balancing process will be impacted [76].
3) Some reliability-oriented control strategies are developed in conjunction with topology modifications. When additional power devices or circuit components are integrated into the NPC-based DAB converters, the overall converter efficiency may be adversely affected due to increased conduction losses, added parasitic elements, or reduced power density. For instance, passive dc-bias suppression techniques introduce extra passive components such as capacitors or auxiliary transformer cores, which increase the overall volume and conduction paths, potentially degrading efficiency under certain operating conditions. Similarly, the voltage-stress-reduction approach proposed in [87] replaces a diode with a power semiconductor (see Fig. 30), which incurs additional switching and gate-drive losses. These examples illustrate that structural modifications aimed at improving reliability may introduce new loss mechanisms or increase system complexity, thus highlighting an inherent tradeoff between efficiency and reliability in converter design and control.

VI. Challenges and Future Directions

The prior control strategies can address certain issues related to efficiency and reliability enhancement of NPC-based DAB converters; however, some challenges still pose significant barriers. Simultaneously, promising research directions are emerging that could unlock new potential to further improve the efficiency and reliability of multilevel DAB converters.

A. Power Loss Balancing Between Outer and Inner Switches

In Section IV-D, the power loss balancing between leading and lagging arms has been discussed. However, a severe power loss imbalance also exists between outer and inner switches (e.g., S_1 and S_2). This is because the inner switches conduct current in a longer time, and the current values at switching instants of outer and inner switches are different. Some loss balancing control schemes have been proposed based on ANPC inverters [27], [177], [178] and ANPC-based DAB converters [179]. However, there is no necessary redundant zero switching states to reduce the switching losses on inner switches for loss balancing in the NPC-based DAB converters.

When the outer and inner switches turn-ON and -OFF synchronously, the power loss imbalance can be significantly reduced. Thus, the 2VL modulation (see Fig. 6) can satisfy the requirement for all NPC topologies such as 3LHB, 3LFB, and HFB. Furthermore, 3VL modulation can be used to 3LFB and HFB topologies to enhance optimization performance due to increased DoFs compared to 2VL modulation. It should be noted that the 3VL modulation of 3LFB in Fig. 6 cannot achieve synchronous switching for outer and inner switches due to the duty cycle difference. Therefore, a phase-shift angle $\alpha_i T_{\rm sw}$ should be applied rather than a duty cycle $dT_{\rm sw}$ to achieve the 3VL modulation, which is similar to that of 2LFB topology. However, the 2VL and 3VL modulation has limited potential for efficiency improvement compared to 5VL modulation. On the other hand, the power loss distribution can also change by hardware modification. A hybrid Si + SiC 3LFB is used to primary side of NPC-based DAB converters, where Si IGBTs and SiC MOSFETs are applied as inner and outer switches, respectively [180], [181], [182]. With a ZVS-on control strategy, the turn-OFF losses of inner Si IGBTs can be reduced by lower turn-OFF currents, and outer SiC MOSFETs benefit from less conduction time.

B. Power Estimation in TS DC Bias Suppression

As analyzed in TS dc bias reduction control, the control variables during SS I and SS II should be determined to calculate the modified control variables during TS. However, in certain conditions such as output load changes, the transferred power in SS II may not be immediately known at the instant when parameter variation occurs. Therefore, the implementation of TS DC bias suppression control becomes challenging under these circumstances. As analyzed in Section IV-C, a TS control with feedforward compensation was employed to suppress the impact of output voltage fluctuation in [172]. Nevertheless, the duty cycles in SS II are still required to develop the feedforward control.

A potential solution of the above issue is to add power estimation to the TS dc bias suppression. It mentioned in [166] that the transferred power and corresponding control variables can be predicted by the dc load, which can be obtained by sampling output voltage and current. However, the inductance and capacitance in practical dc loads lead to a slow dynamic response of the output current with a load change, resulting in inaccurate power estimation based on sampled voltage and current. Thus, extracting the resistance component of dc load and predict the active power will be the future task for TS dc bias suppression control.

C. Performance Prediction for Optimization Design

The efficiency and reliability of NPC-based DAB converters depends highly on the factors including topologies, control strategies, operating parameters, and coefficients of power devices. Thus, the converter performance should be evaluated during design phase to determine the optimum combination of these factors. Commercial simulation platforms such as MATLAB/Simulink and PLECS can be applied to predict certain

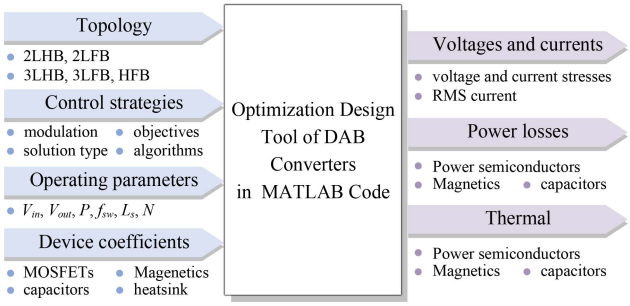

Fig. 31. Optimization design tool for NPC-based DAB converters to predict performance under various topologies, control strategies, operating parameters, and power devices.

performance issues of NPC-based DAB converters. However, the following three limitations restrict their effectiveness:

1) slow simulation speed, especially when numerous combinations of various factors need to be compared during the design phase;
2) limited functionality, with some desired features not available in these simulation platforms;
3) complexity of simulation system, as modifying parameters such as topologies generally requires manual adjustments or creation of different simulation files, leading to redundant simulation system and increased complexity.

In order to predict the performance under various factors and achieve optimization design, some optimization design tools have been developed based on digital modeling in MATLAB code for 2L DAB converters, where the calculation speed is fast, and various factors can be easily switched [183], [184]. An optimization design tool for NPC-based DAB converters can be proposed in a similar way in the future with structure as shown in Fig. 31. The topologies including 2/3L FB and HB, control strategies, operating parameters, and coefficients of power devices should be included in a database, and a specific factor can be selected by a certain variable. Therefore, various factors can be switched smoothly by only changing the variables. The efficiency- and reliability-related issues such as current and voltage stresses, power losses, and thermal can be obtained by digital models of DAB converters. In this manner, the optimization design process can be significantly accelerated. Furthermore, models related to certain functionality can be added to the optimization design tools according to optimization requirements.

D. Multilevel DC–DC Converters in MVDC/HVdc Scenarios

This work mainly focuses on the issues of 3L NPC-based DAB converters. However, as MVDC systems continue to evolve, there is a clear trend toward even higher VLs. When the dc-link voltage in MVDC applications is tens of kVs or higher, a single NPC-based DAB converter is hard to meet the voltage-blocking capability with commercial power semiconductors. Therefore, it is also necessary to briefly discuss relevant research on higher level converters to better contextualize this study within the broader development of MVDC systems. Various multilevel

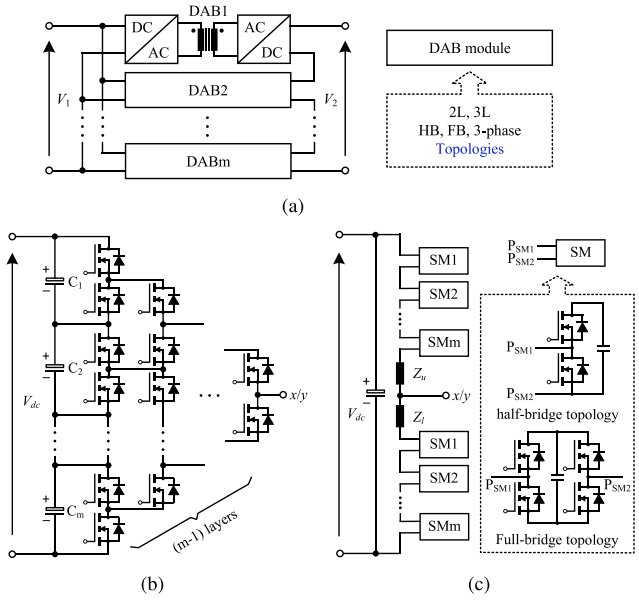

Fig. 32. Isolated DC–DC converters applied to MVDC and HVdc systems. (a) SST with cascaded DAB. (b) multilevel ANPC topology in DAB (per arm). (c) Modular multilevel DAB (per arm).

dc–dc converters developing from DAB topology have been discussed such as cascaded NPC-based DAB converters, cascaded 2L DAB converters [8], [185], [186], multilevel NPC-based DAB converters [70], [187], [188], and modular multilevel DAB converters [189], [190], [191], [192], as shown in Fig. 32. Several work has compared the characteristics of certain multilevel dc–dc converters applied to MVDC and HVdc systems [193], [194]. However, the criteria for evaluating the performance of different MV dc–dc converters remain insufficiently defined, and a comprehensive comparison of these topologies is still lacking. Note that the main scope of this work remains centered on the 3L NPC-based DAB converter,

According to prior research, the major characteristics of MV dc–dc converters encompass hardware costs, power density, efficiency, reliability, control complexity and flexibility, voltage gain, insulation performance, footprint, and other relevant factors [195]. Thus, the evaluation of various multilevel DAB variants should be carried out from these aspects. Due to the high-power high-voltage features and complicated implementations, it is very challenging to obtain the performance indices and develop following comparisons from physical prototypes of all multilevel dc–dc converters. A potential method to achieve the evaluation is to develop the electro-thermal model of these converters, and then assessment models of different performance indices such as efficiency and reliability will be added to the evaluation system based on the results of electro-thermal model, as shown in Fig. 33. The evaluation system can be achieved by digital modeling in MATLAB or by hardware-in-the-loop with RT Box/Typhoon. In this manner, the performance-related data can be collected from the digital evaluation system, and the most suitable converter for a certain MVDC scenario can be selected by comparing the data among various multilevel DAB variants.

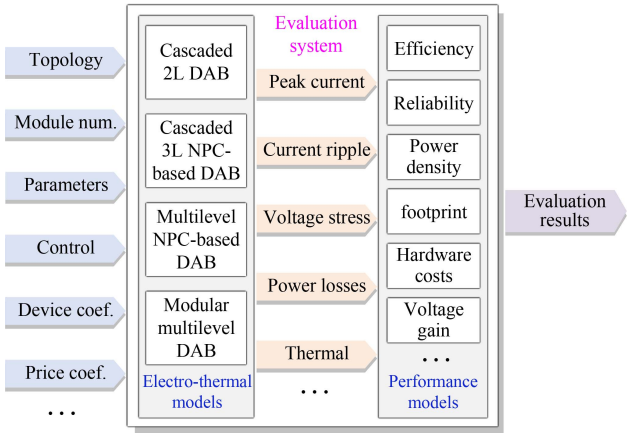

Fig. 33. Evaluation system of various multilevel DC–DC converters applied to MVDC systems.

VII. Conclusion

3L NPC topology offers increased voltage-blacking capability and step-up ratios compared to 2L topology in DAB converters. Thus, the NPC-based DAB converters have potential to be applied to MVDC scenarios. This article has reviewed prior efficient and reliable control strategies for NPC-based DAB converters applied to MVDC systems. First, modulation schemes with various DoFs based on HB, FB, and HFB structures with NPC topology were analyzed. In addition, operating modes under certain constraints of optimization objectives and modeling methods for calculating transferred power were discussed. Subsequently, the control strategies that can increase converter efficiency were discussed in terms of modulation schemes with various DoFs, solution types, optimization objectives, and algorithms. On the other hand, control strategies for reliability enhancement of NPC-based DAB converters were reviewed in detail including neutral-point voltage balancing control, FD and FT control, TS dc bias current suppression control. Other reliability-related control strategies such as power-loss balancing control, voltage/current stress reduction control, and conducted EMI suppresion control were also sketched. Furthermore, the interaction of efficiency- and reliability-oriented control strategies was discussed. Finally, the challenges and potential solutions of NPC-based DAB converters and related MVDC/HVdc converters were discussed, which can provide guidance for future research.

References

[1] S. Du, B. Wu, K. Yian, D. Xu, and N. R. Zargari, "A novel medium-voltage modular multilevel DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7939–7949, Dec. 2016.

[2] I. Alhurayyis, A. Elkhateb, and J. Morrow, "Isolated and nonisolated DC-to-DC converters for medium-voltage DC networks: A review," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 6, pp. 7486–7500, Dec. 2021.

[3] X. Pei, O. Cwikowski, D. S. Vilchis-Rodriguez, M. Barnes, A. C. Smith, and R. Shuttleworth, "A review of technologies for MVDC circuit breakers," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, 2016, pp. 3799–3805.

[4] J. Yao, W. Chen, C. Xue, Y. Yuan, and T. Wang, "An ISOP hybrid DC transformer combining multiple SRCs and DAB converters to interconnect MVDC and LVDC distribution networks," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11442–11452, Nov. 2020.

[5] CIGRE, "Medium voltage direct current (MVDC) grid feasibility study," 2020. [Online]. Available: https://electra.cigre.org/309-april-2020/technical-brochures/medium-voltage-direct-current-mvdc-grid-feasibility-study.html

[6] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. De Doncker, "Comparison of the modular multilevel DC converter and the dual-active bridge converter for power conversion in HVDC and MVDC Grids," *IEEE Trans. Ind. Electron.*, vol. 30, no. 1, pp. 124–137, Jan. 2015.

[7] A. Giannakis and D. Peftitsis, "MVDC distribution grids and potential applications: Future trends and protection challenges," in *Proc. 20th Eur. Conf. Power Electron. Appl.*, 2018, pp. 1–9.

[8] Y. Wang, Q. Song, Q. Sun, B. Zhao, J. Li, and W. Liu, "Multilevel MVDC link strategy of high-frequency-link DC transformer based on switched capacitor for MVDC power distribution," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2829–2835, Apr. 2017.

[9] V. M. Hrishikesan, C. Kumar, and M. Liserre, "An MVDC-Based meshed hybrid microgrid enabled using smart transformers," *IEEE Trans. Ind. Electron.*, vol. 69, no. 4, pp. 3722–3731, Apr. 2022.

[10] E. A. Gunther, "The state of medium voltage DC architectures for utility-scale PV," 2018. [Online]. Available: https://www.pv-tech.org/the-state-of-medium-voltage-dc-architectures-for-utility-scale-pv/

[11] J. Pang, K. Wang, M. Wu, W. Zhou, Z. Zheng, and Y. Li, "Modulation and soft-switching optimization control of multilevel dual active bridge DC-DC converters," *IEEE Trans. Power Electron.*, vol. 40, no. 1, pp. 1936–1951, Jan. 2025.

[12] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three- phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Feb. 1991.

[13] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC-DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[14] C. Song, Y. Yang, Z. Tang, and F. Blaabjerg, "Modulation of 2/3-Level dual-active-bridge DC-DC converters for soft-switching and minimum current stress," in *Proc. 46th Annu. Conf. IEEE Ind. Electron. Soc.*, 2020, pp. 2913–2918.

[15] M. A. Moonem and H. Krishnaswami, "Analysis and control of multilevel dual active bridge DC-DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Raleigh, NC, USA, 2012, pp. 1556–1561.

[16] B. Li, X. Wu, G. J. Kish, and Y. R. Li, "Dual 3L-NPC converter system with improved power quality for bipolar DC distribution," *IEEE Trans. Power Electron.*, vol. 39, no. 12, pp. 16553–16565, Dec. 2024.

[17] J. H. Jung, S. I. Hwang, and J. M. Kim, "A common-mode voltage reduction method using an active power filter for a three-phase three-level NPC PWM converter," *IEEE Trans. Ind. Appl.*, vol. 57, no. 4, pp. 3787–3800, Jul./Aug. 2021.

[18] A. Ruderman, B. Reznikov, and M. Margaliot, "Simple analysis of a flying capacitor converter voltage balance dynamics for DC modulation," in *Proc. Int. Power Electron. Motion Control Conf.*, Poznan, Poland, 2008, pp. 260–267.

[19] A. Ruderman and B. Reznikov, "Three-level H-bridge flying capacitor converter voltage balance dynamics analysis," in *Proc. 13th Eur. Conf. Power Elect. Appl.*, Barcelona, Spain, 2009, pp. 1–10.

[20] H. Feng et al., "Passive capacitor voltage balancing of SiC-Based three-level dual-active-bridge converter using hybrid NPC-Flying capacitor structure," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4183–4194, Apr. 2022.

[21] X. Ruan, L. Zhou, and Y. Yan, "Soft-switching PWM three-level converters," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 612–622, Sep. 2001.

[22] H. Sheng, F. Wang, and C. W. Tipton IV, "A fault detection and protection scheme for three-level DC-DC converters based on monitoring flying capacitor voltage," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 685–697, Feb. 2012.

[23] C. Li, J. Liu, S. Du, H. Dang, Z. Deng, and H. Chen, "A T-type DAB-Based isolated DC-DC-AC three-port converter with high power efficiency," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 14178–14194, Nov. 2023.

[24] L. Song, H. Yu, L. Hang, Y. He, S. Tang, and Z. He, "A T-type three-level DAB AC/DC converter with multi-mode optimized modulation strategy," in *Proc. IEEE 2nd Int. Power Electron. Appl. Symp.*, Guangzhou, China, 2023, pp. 1191–1194.

[25] H. Watanabe, K. Kusaka, and J. Itoh, "Output capacitor current reduction with T-type dual active bridge converter for wide output voltage condition," in *Proc. Int. Exhib Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2020, pp. 1–6.

[26] T. Bruckner, S. Bernet, and P. K. Steimer, "Feedforward loss control of three-level active NPC converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 6, pp. 1588–1596, Nov./Dec. 2007.

[27] T. Bruckner, S. Bernet, and H. Guldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855–868, Jun. 2005.

[28] G. Zu, X. Zhu, and S. Yang, "Using DPWM method to improve system efficiency of the machine drive system," in *Proc. 22nd Int. Conf. Elect. Mach. Syst.*, Harbin, China, 2019, pp. 1–4.

[29] Y. Chen and D. Xu, "Review of soft-switching topologies for single-phase photovoltaic inverters," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1926–1944, Feb. 2022.

[30] A. Zorig, S. Barkat, and A. Sangwongwanich, "Neutral point voltage balancing control based on adjusting application times of redundant vectors for three-level NPC inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5604–5613, Oct. 2022.

[31] M. Zhang, Z. Zhang, Z. Li, H. Chen, and D. Zhou, "A unified open-circuit-fault diagnosis method for three-level neutral-point-clamped power converters," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3834–3846, Mar. 2023.

[32] U. M. Choi, J. S. Lee, F. Blaabjerg, and K. B. Lee, "Open-circuit fault diagnosis and fault-tolerant control for a grid-connected NPC inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7234–7247, Oct. 2016.

[33] D. Mou et al., "Overview of multi-degree-of-freedom modulation techniques for dual active bridge converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 6, pp. 5724–5737, Dec. 2023.

[34] N. Hou and Y. W. Li, "Overview and comparison of modulation and control strategies for a nonresonant single-phase dual-active-bridge DC-DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3148–3172, Mar. 2020.

[35] M. Wang, S. Wei, D. Mou, and P. Wu, "Research on efficient single-sided asymmetric modulation strategy for dual active bridge converters in wide voltage range," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5738–5748, Oct. 2022.

[36] D. Mou et al., "Optimal asymmetric duty modulation to minimize inductor peak-to-peak current for dual active bridge DC-DC converter," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4572–4584, Apr. 2021.

[37] J. Li, Q. Luo, D. Mou, Y. Wei, P. Sun, and X. Du, "A hybrid five-variable modulation scheme for dual-active-bridge converter with minimal RMS current," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 336–346, Jan. 2022.

[38] C. Song, A. Sangwongwanich, Y. Yang, Y. Pan, and F. Blaabjerg, "Analysis and optimal modulation for 2/3-Level DAB converters to minimize current stress with five-level control," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4596–4612, Apr. 2023.

[39] P. Liu, C. Chen, and S. Duan, "An optimized modulation strategy for the three-level DAB converter with five control degrees of freedom," *IEEE Trans. Ind. Electron.*, vol. 67, no. 1, pp. 254–264, Jan. 2020.

[40] Z. Zhang et al., "Optimized modulation strategy of NH3L-DAB converter to minimize RMS current for wide voltage range applications," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7789–7808, Jul. 2022.

[41] Y. Li, F. Xiao, J. Liu, and R. Zhou, "Reactive power minimization modulation strategy for NPC-SRDAB based on particle swarm optimization," in *Proc. IEEE Energy Convers. Congr. Expo. Asia*, Chengdu, China, 2024, pp. 763–768.

[42] Z. Feng, H. Wen, X. Han, G. Wang, and Y. Zhu, "Artificial intelligence-aided optimization strategy for three-level DAB converters modulated with five DoFs," in *Proc. 13th Int. Conf. Renewable Energy Res. Appl.*, Nagasaki, Japan, 2024, pp. 1457–1462.

[43] Y. Ikai and N. Hoshi, "Expanding ZVS range for dual active bridge DC-DC converter using three-level neutral-point-clamped inverter topology," in *Proc. Int. Conf. Renewable Energy Res. Appl.*, Birmingham, U.K., 2016, pp. 472–477.

[44] Y. Li, F. Xiao, J. Liu, P. Chen, and R. Zhou, "ZVS boundaries for NPC-Type series resonant dual active bridge converter using frequency domain analysis," in *Proc. IEEE Energy Convers. Congr. Expo. Asia*, Chengdu, China, 2024, pp. 2818–2823.

[45] H. Yu, C. Shao, A. Tong, L. Hang, and Y. He, "Optimized modulation scheme of three-level dual active bridge converter," in *Proc. IEEE Energy Convers. Congr. Expo. Asia*, Nanjing, China, 2020, pp. 3128–3131.

[46] C. Song, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Optimal control of multilevel DAB converters for soft-switching and minimum current stress," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 5707–5720, May 2024.

[47] A. Filba-Martinez, S. Busquets-Monge, J. Nicolas-Apruzzese, and J. Bordonau, "Operating principle and performance optimization of a three-level NPC dual-active-bridge DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 678–690, Feb. 2016.

[48] D. Zhou, G. Zhang, and F. Blaabjerg, "Optimal selection of power converter in DFIG wind turbine with enhanced system-level reliability," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3637–3644, Jul./Aug. 2018.

[49] I. Vernica, K. Ma, and F. Blaabjerg, "Optimal derating strategy of power electronics converter for maximum wind energy production with lifetime information of power devices," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 267–276, Mar. 2018.

[50] J. V. M. Farias, A. F. Cupertino, V. D. N. Ferreira, H. A. Pereira, S. I. Seleme, and R. Teodorescu, "Reliability-oriented design of modular multilevel converters for medium-voltage STATCOM," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6206–6214, Aug. 2020.

[51] D. Krishnachaitanya and A. Chitra, "Quantitative analysis of asymmetric multilevel inverters with reduced device count from reliability and cost function perspective—A review," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11068–11086, Oct. 2021.

[52] S. S. Khan, H. Wen, H. Shi, Y. Hu, L. Jiang, and G. Chen, "Multiple open-circuit fault detection and isolation using universal low-cost diagnosis circuits for reconfigurable dual-active-bridge converters," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 6504–6521, May 2023.

[53] P. Tu, S. Yang, and P. Wang, "Reliability- and cost-based redundancy design for modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2333–2342, Mar. 2019.

[54] T. Wu, Z. Wang, B. Ozpineci, M. Chinthavali, and S. Campbell, "Automated heatsink optimization for air-cooled power semiconductor modules," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5027–5031, Jun. 2019.

[55] M. Enmark, M. Murugesan, A. Nkansah, Y. Fu, T. M. J. Nilsson, and J. Liu, "Reliability characterization of graphene enhanced thermal interface material for electronics cooling applications," in *Proc. Nordic Conf. Microelectronics Packag.*, Gothenburg, Sweden, 2022, pp. 1–6.

[56] A. Castelan, B. Cougo, J. Brandelero, D. Flumian, and T. Meynard, "Optimization of forced-air cooling system for accurate design of power converters," in *Proc. 24th IEEE Int. Symp. Ind. Electron.*, Buzios, Brazil, 2015, pp. 367–372.

[57] S. Jeong, J. Park, and J. Kim, "A customized integrated circuit for active EMI filter with high reliability and scalability," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12631–12645, Nov. 2021.

[58] L. Xie, X. Ruan, H. Zhu, and Y. K. Lo, "Hybrid passive cancelation method for reducing common-mode noise in isolated power converters," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 391–400, Jan. 2021.

[59] S. Gulur, V. M. Iyer, and S. Bhattacharya, "Passive CM filter configuration for a multistage grid-tied solid state transformer," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 710–717, Jul. 2023.

[60] F. Deng et al., "Protection scheme for modular multilevel converters under diode open-circuit faults," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2866–2877, Apr. 2018.

[61] M. E. Baran and N. R. Mahajan, "Overcurrent protection on voltage-source-converter-based multiterminal DC distribution systems," *IEEE Trans. Power Del.*, vol. 22, no. 1, pp. 406–412, Jan. 2007.

[62] L. Jin, Z. Zhou, R. Zhan, G. Yang, and Y. Zhang, "Optimal layout and overheat monitoring for components of highly reliable relay protection equipment," *IEEE Access*, vol. 11, pp. 85615–85625, 2023.

[63] R. Han et al., "Modulated model predictive control for reliability improvement of extremely low frequency power amplifier via junction temperature swing reduction," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 302–313, Jan. 2022.

[64] X. Wu, Y. Zhang, and J. Yang, "Neutral-point voltage balancing method for three-phase three-level dual-active-bridge converters," *Energies*, vol. 15, 2022, Art. no. 6463.

[65] J. Yang et al., "Online digital implementation of wide voltage range RMS-current-optimized control with voltage balancing capability for DAB converter," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4360–4377, Apr. 2023.

[66] J. Pang, K. Wang, Z. Zheng, and Y. Li, "Modulation and capacitor voltage balancing control of a hybrid four-level DAB with reduced switches," in *Proc. Int. Conf. Elect. Mach. Syst.*, Zhuhai, China, 2023, pp. 3698–3703.

[67] P. Joebges, A. Gorodnichev, and R. W. De Doncker, "Modulation and active midpoint control of a three-level three-phase dual-active bridge DC-DC converter under non-symmetrical load," in *Proc. IEEE Energy Convers. Congr. Expo. Asia*, Niigata, Japan, 2018, pp. 375–382.

[68] M. A. Moonem, T. Duman, and H. Krishnaswami, "Capacitor voltage balancing in a neutral-point clamped multilevel DC-DC dual active bridge converter," in *Proc. IEEE 8th Int. Symp. Power Electron. Distrib. Gener. Syst.*, Brazil, 2017, pp. 1–7.

[69] J. Pang, K. Wang, Z. Zheng, T. Zheng, and Y. Li, "Quasi two-level operation and neutral-point voltage balance method for a four-level ANPC based dual active bridge DC-DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Detroit, MI, USA, 2022, pp. 1–7.

[70] A. F. Martinez, S. B. Monge, and J. Bordonau, "Modulation and capacitor voltage balancing control of multilevel NPC dual active bridge DC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 2499–2510, Apr. 2020.

[71] G. Niyitegeka, E. M. Harerimana, G. Park, and J. Choi, "Phase shift modulation and DC-Link's voltage balancing control for a DAB DC-DC converter," in *Proc. Int. Conf. Smart Grid*, Nagasaki, Japan, 2018, pp. 70–75.

[72] X. Yu, K. Jin, and Z. Liu, "Capacitor voltage control strategy for half-bridge three-level DC/DC converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1557–1561, Apr. 2014.

[73] C. Song, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Capacitor voltage balancing for multilevel dual-active-bridge DC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 70, no. 3, pp. 2566–2575, Mar. 2023.

[74] J. Lee, H. Choi, and J. Jung, "Three level NPC dual active bridge capacitor voltage balancing switching modulation," in *Proc. IEEE Int. Telecommun. Energy Conf.*, Broadbeach, Australia, 2017, pp. 438–443.

[75] C. Liu and C. Li, "Capacitor voltage balancing strategy of NPC three-level dual-active bridge converter based on redundant vector," (in Chinese), *Control Inf. Technol.*, vol. 1, pp 45–51, 2023.

[76] C. Song, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "A model-free capacitor voltage balancing method for multilevel DAB converters," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 79–84, Jan. 2023.

[77] M. A. Awal et al., "Capacitor voltage balancing for neutral point clamped dual active bridge converters," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 11267–11276, Oct. 2020.

[78] C. Song, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Open-circuit fault diagnosis and tolerant control for 2/3-Level DAB converters," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 5392–5410, Apr. 2023.

[79] C. Song, A. Sangwongwanich, and F. Blaabjerg, "Sensorless open-circuit-fault diagnosis method for NPC-Based DAB converter," *IEEE Trans. Power Electron.*, vol. 39, no. 9, pp. 10699–10703, Sep. 2024.

[80] J. Wu, H. Wang, M. Ma, Q. Chen, and J. Liang, "Mode analysis and fault-tolerant method of open-circuit fault for a three-level dual active bridge DC-DC converter," *Microelectronics Rel.*, vol. 150, 2023, Art. no. 115100.

[81] G. Zhou, D. Wang, Y. Ma, and H. Wang, "Fault-tolerant scheme of multi-level dual active bridge converter," in *Proc. Int. Electrical. Energy Conf.*, Harbin, China, 2024, pp. 3394–3399.

[82] Z. Feng, H. Wen, Q. Bu, Y. Zhu, and X. Han, "Transient DC-bias suppression strategy of three-level dual-active- bridge converter with five control degrees of freedom," in *Proc. IEEE Energy Convers. Congr. Expo.*, Detroit, MI, USA, 2022, pp. 1–7.

[83] C. Du, W. Guo, S. Guo, W. Cai, and Q. Shi, "Transient current optimal control of the hybrid three level dual active bridge converters based on triple-phase-shifting control," in *Proc. IEEE 12th Int. Symp. Power Electron. Distrib. Gener. Syst.*, Chicago, IL, USA, 2021, pp. 1–8.

[84] G. Yang, A. Wang, and D. Zhang, "Transient DC bias suppression for three-level dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 40, no. 9, pp. 12084–12094, Sep. 2025, doi: 10.1109/TPEL.2024.3444770.

[85] Z. Feng et al., "Loss balance and transient DC-Bias suppression strategies in three-level DAB converters modulated with five DoFs," *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 8150–8164, Jul. 2023.

[86] S. Wang, C. Li, K. Wang, Z. Zheng, and Y. Li, "Loss imbalance and transient DC-Bias mitigation in dual-active-bridge DC/DC converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1399–1409, Apr. 2021.

[87] R. Pradhan, S. B. Shah, M. I. Hassan, Z. Wang, and A. Emadi, "A 15-kW wide-input reconfigurable three-level DAB converter for on-board charging of 1.25-kV electric vehicle powertrains," *IEEE Trans. Transp. Electrific.*, vol. 10, no. 4, pp. 9144–9162, Dec. 2024.

[88] M. J. Heller, F. Krismer, and J. W. Kolar, "Duty-cycle dependent phase shift modulation of dual three-phase active bridge four-port AC-DC/DC-AC converter eliminating low frequency power pulsations," *IEEE Open J. Power Electron.*, vol. 3, pp. 705–722, 2022.

[89] A. Agarwal, S. K. Rastogi, and S. Bhattacharya, "Performance evaluation of two-level to three-level three-phase dual active bridge (2L-3L DAB3)," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Houston, TX, USA, 2022, pp. 361–368.

[90] C. Song, Y. Yang, A. Sangwongwanich, Y. Pan, and F. Blaabjerg, "Modeling and analysis of 2/3-Level dual-active-bridge DC-DC converters with the five-level control scheme," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Phoenix, AZ, USA, 2021, pp. 1958–1963.

[91] Z. Fan, H. Lu, J. Chai, and X. Sun, "Quantum power pulse combination modulation to achieve full load range ZVS of DAB converters in wide voltage gain," *IEEE Trans. Power Electron.*, vol. 40, no. 4, pp. 4767–4774, Apr. 2025.

[92] Z. Lu, M. Su, G. Xu, L. Li, W. Xiong, and J. Fang, "Switch-multiplexed quasi-two-stage isolated bidirectional Buck-DAB converter with full load ZVS range," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 10541–10546, Sep. 2023.

[93] J. Everts, "Closed-form solution for efficient ZVS modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7561–7576, Oct. 2017.

[94] Y. Yan, H. Gui, and H. Bai, "Complete ZVS analysis in dual active bridge," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1247–1252, Feb. 2021.

[95] D. Mou, Q. Luo, J. Li, Y. Wei, and J. Chen, "The novel single phase-shift modulation scheme for dual active bridge converter," in *Proc. IEEE Energy Convers. Congr. Expo. Asia.*, Nov. 2020, pp. 2686–2690.

[96] W. Choi, K. M. Rho, and B. H. Cho, "Fundamental duty modulation of dual-active-bridge converter for wide-range operation," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4048–4064, Jun. 2016.

[97] H. Bai, Z. Nie, and C. C. Mi, "Experimental comparison of traditional phase-shift, dual-phase-shift, and model-based control of isolated bidirectional DC-DC converters," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1444–1449, Jun. 2010.

[98] A. Tong, L. Hang, G. Li, X. Jiang, and S. Gao, "Modeling and analysis of a dual-active-bridge-isolated bidirectional DC/DC converter to minimize RMS current with whole operating range," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5302–5316, Jun. 2018.

[99] Y. Wang et al., "Minimum-current-Stress scheme of three-level dual-active-bridge DC-DC converters with the particle swarm optimization," *IEEE Trans. Transp. Electrific.*, vol. 7, no. 4, pp. 2067–2084, Dec. 2021.

[100] Y. Wang, Y. Zhu, and H. Wen, "PSO-based current stress optimization for three-level dual active bridge DC-DC converters," in *Proc. Chin. Autom. Congr.*, Shanghai, China, 2020, pp. 4283–4287.

[101] S. Chaurasiya and B. Singh, "A bidirectional fast EV charger for wide voltage range using three-level DAB based on current and voltage stress optimization," *IEEE Trans. Transp. Electrific.*, vol. 9, no. 1, pp. 1330–1340, Mar. 2023.

[102] N. Hou, W. Song, and M. Wu, "Minimum-current-Stress scheme of dual active bridge DC-DC converter with unified phase-shift control," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8552–8561, Dec. 2016.

[103] J. Huang, Y. Wang, Z. Li, and W. Lei, "Unified triple-phase-shift control to minimize current stress and achieve full soft-switching of isolated bidirectional DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4169–4179, Jul. 2016.

[104] H. Shi et al., "Minimum-backflow-Power scheme of DAB-Based solid-state transformer with extended-phase-shift control," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3483–3496, Jul./Aug. 2018.

[105] F. Lin et al., "AI-Based design with data trimming for hybrid phase shift modulation for minimum-current-stress dual active bridge converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 2268–2280, Apr. 2024.

[106] N. Noroozi et al., "RMS current minimization in a SiC-Based dual active bridge converter using triple-phase-shift modulation," *IEEE Trans. Ind. Electron.*, vol. 70, no. 7, pp. 7173–7182, Jul. 2023.

[107] H. Shi, H. Wen, Y. Hu, and L. Jiang, "Reactive power minimization in bidirectional DC-DC converters using a unified-phasor-based particle swarm optimization," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10990–11006, Dec. 2018.

[108] H. Deng, Y. Wang, J. Tian, F. Wang, and F. Zhuo, "A backflow power optimization method for three-level ANPC-DAB converter," in *Proc. IEEE 2nd Int. Power Electron. Appl. Symp.*, Guangzhou, China, 2023, pp. 1137–1142.

[109] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional DC-DC converter based on dual-phase-shift control for DC distribution application," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1711–1727, Apr. 2013.

[110] F. Krismer and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2745–2760, Jul. 2012.

[111] J. Tian, C. Zhuo, F. Wang, and H. Deng, "An RMS current minimization method for three-level ANPC-DAB-Based distributed energy storage system with full operation ZVS," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 3, pp. 2388–2405, Jun. 2024.

[112] H. Deng, J. Tian, Y. Liu, Y. Wang, F. Wang, and F. Zhuo, "Minimum peak current optimization scheme based on genetic algorithm for three-level ANPC-DAB converter with all switches ZVS," in *Proc. IEEE 14th Int. Symp. Power Electron. Distrib. Gener. Syst.*, Shanghai, China, 2023, pp. 288–294.

[113] C. Song, A. Chen, Y. Pan, C. Du, and C. Zhang, "Modeling and optimization of dual active bridge DC-DC converter with dead-time effect under triple-phase-shift control," *Energies*, vol. 12, 2019, Art. no. 973.

[114] L. Zhou, Y. Gao, H. Ma, and P. T. Krein, "Wide-load range multiobjective efficiency optimization produces closed-form control solutions for dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8612–8616, Aug. 2021.

[115] J. Tian, C. Zhuo, F. Wang, and H. Deng, "Full-power-Range multiobjective optimization scheme for three-level ANPC-DAB-Based distributed generation system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1754–1768, Apr. 2024.

[116] Y. Tang et al., "Artificial intelligence-aided minimum reactive power control for the DAB converter based on harmonic analysis method," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 9704–9710, Sep. 2021.

[117] B. Liu, P. Davari, and F. Blaabjerg, "An optimized hybrid modulation scheme for reducing conduction losses in dual active bridge converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 921–936, Feb. 2021.

[118] L. Gong et al., "A dynamic ZVS-Guaranteed and seamless-mode-transition modulation scheme for the DAB converter that maximizes the ZVS range and lowers the inductor RMS current," *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13119–13134, Nov. 2022.

[119] D. Mou, Q. Luo, J. Li, Y. Wei, and P. Sun, "Five-degree-of-freedom modulation scheme for dual active bridge DC-DC converter," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10584–10601, Sep. 2021.

[120] J. Liu, W. Chen, X. Ma, R. Zhang, and R. Yan, "A zero voltage switching range optimization strategy for NPC dual-active-bridge converter," in *Proc. 4th Int. Conf. HVDC*, Xi'an, China, 2020, pp. 966–970.

[121] L. Jin, B. Liu, and S. Duan, "ZVS soft switching operation range analysis of three-level dual-active bridge DC-DC converter under phase shift control strategy," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1963–1972, Mar./Apr. 2019.

[122] H. Yu et al., "Globally unified ZVS and quasi-optimal minimum conduction loss modulation of DAB converters," *IEEE Trans. Transp. Electrific.*, vol. 8, no. 3, pp. 3989–4000, Sep. 2022.

[123] Z. Guo and K. Sun, "Three-level bidirectional DC-DC converter with an auxiliary inductor in adaptive working mode for full-operation zero-voltage switching," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8537–8552, Oct. 2018.

[124] M. Turzyński et al., "Analytical estimation of power losses in a dual active bridge converter controlled with a single-phase shift switching scheme," *Energies*, vol. 15, 2022, Art. no. 8262.

[125] Z. Guo, R. Yu, W. Xu, X. Feng, and A. Q. Huang, "Design and optimization of a 200-kW medium-frequency transformer for medium-voltage SiC PV inverters," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10548–10560, Sep. 2021.

[126] E. T. Wodajo, M. E. Elbuluk, S. Choi, and H. Abu-Rub, "Three parts modulation and hybrid DC capacitor voltage balancing for a single-phase two-leg five-level NPC inverter," *IEEE Trans. Ind. Electron.*, vol. 70, no. 7, pp. 6765–6775, Jul. 2023.

[127] Z. Gao, L. Zhao, Q. Ge, Y. Li, and B. Zhang, "Neutral-point voltage balancing strategy for three-level neutral point clamped inverter based on on-line calculating redundant vector duty cycles," in *Proc. Int. Conf. Elect. Mach. Syst.*, Harbin, China, 2019, pp. 1–6.

[128] G. Chen, C. Gong, J. Bao, L. Zhu, and Z. Wang, "Compensation voltage injection based neutral point voltage fluctuation suppression for NPC converter," in *Proc. Asia Power Electr. Technol. Conf.*, Shanghai, China, 2022, pp. 203–208.

[129] C. Song, N. Wang, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Evaluation of capacitor voltage balancing control strategies for multilevel DAB converters," *IEEE Trans. Power Electron.*, vol. 39, no. 12, pp. 15548–15564, Dec. 2024.

[130] C. Song, Y. Yang, A. Sangwongwanich, and F. Blaabjerg, "Open-circuit fault analysis and fault-tolerant control for 2/3-Level DAB converters," in *Proc. IEEE 12th Energy Convers. Congr. Expo.-Asia*, 2021, pp. 696–701.

[131] M. K. Puthiyapurayil, M. N. Nasirudeen, Y. A. Saywan, M. W. Ahmad, and H. Malik, "A review of open-circuit switch fault diagnostic methods for neutral point clamped inverter," *Electronics*, vol. 11, no. 19, 2022, Art. no. 3169.

[132] A. Davoodi, D. Sadeghpour, M. Kashif, S. A. Albahrani, S. M. Atarodi, and M. Zolghadri, "A novel transistor open-circuit fault localization scheme for three-phase dual active bridge," in *Proc. Australas. Universities Power Eng. Conf.*, Auckland, New Zealand, 2018, pp. 1–6.

[133] A. Davoodi, N. Noroozi, and M. R. Zolghadri, "A fault-tolerant strategy for three-phase dual active bridge converter," in *Proc. 10th Int. Power Electron., Drive Syst. Technol. Conf.*, Shiraz, Iran, 2019, pp. 253–258.

[134] S. K. Rastogi, S. S. Shah, B. N. Singh, and S. Bhattacharya, "Mode analysis, transformer saturation, and fault diagnosis technique for an open-circuit fault in a three-phase DAB converter," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7644–7660, Jun. 2023.

[135] S. S. Khan and H. Wen, "A fast and low-cost open-circuit fault detection and isolation technique for three-phase dual-active-bridge converters based on finite state machines," *IEEE Trans. Power Electron.*, vol. 39, no. 2, pp. 2751–2766, Feb. 2024.

[136] E. Ribeiro, A. J. M. Cardoso, and C. Boccaletti, "Fault analysis of dual active bridge converters," in *Proc. 38th Annu. Conf. IEEE Ind. Electron. Soc.*, Montreal, QC, Canada, 2012, pp. 398–403.

[137] D. Xie and X. Ge, "Open-circuit fault diagnosis of dual active bridge DC-DC converter based on residual analysis," in *Proc. Int. Power Electron. Appl. Conf. Expo.*, Shenzhen, China, 2018, pp. 1–6.

[138] A. M. Airabella, G. G. Oggier, L. E. Paris-Botalla, C. A. Falco, and G. O. Garcia, "Semi-conductors faults analysis in dual active bridge DC-DC converter," *IET Power Electron.*, vol. 9, no. 6, pp. 1103–1110, May 2016.

[139] M. Zheng, H. Wen, H. Shi, Y. Hu, Y. Yang, and Y. Wang, "Open-circuit fault diagnosis of dual active bridge DC-DC converter with extended-phase-shift control," *IEEE Access.*, vol. 7, pp. 23752–23765, 2019.

[140] H. Wen, J. Li, H. Shi, Y. Hu, and Y. Yang, "Fault diagnosis and tolerant control of dual-active-bridge converter with triple-phase-shift control for bidirectional EV charging systems," *IEEE Trans. Transp. Electrific.*, vol. 7, no. 1, pp. 287–303, Mar. 2021.

[141] H. Shi, H. Wen, and J. Li, "Fault analysis and fault-tolerant method of dual active bridge converter under triple phase shift control," in *Proc. IEEE Energy Convers. Congr. Expo. Asia*, Busan, Korea, 2019, pp. 1121–1127.

[142] H. Shi, H. Wen, G. Chen, Q. Bu, G. Chu, and Y. Zhu, "Multiple-fault-Tolerant dual active bridge converter for DC distribution system," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1748–1760, Feb. 2022.

[143] S. P. Kamble, P. Chaturvedi, H. Bhawane, and V. B. Borghate, "PSAM and TM based fault tolerant scheme for open switch faults in dual active bridge converters," in *Proc. IEEE Int. Telecommun. Energy Conf.*, Bengaluru, India, 2024, pp. 1–6.

[144] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke, and H. S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6319–6331, Dec. 2014.

[145] H. Zhang et al., "A redundant design and control strategy for hybrid dual active bridges based DC transformer," in *Proc. IEEE Energy Convers. Congr. Expo. Asia*, Nanjing, China, 2020, pp. 2668–2674.

[146] S. Haghbin, F. Blaabjerg, and A. S. Bahman, "Frozen leg operation of a three-phase dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4239–4248, May 2019.

[147] M. Berger, I. Kocar, H. Fortin-Blanchette, and C. Lavertu, "Open-phase fault-tolerant operation of the three-phase dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3651–3662, Apr. 2020.

[148] N. Zhao, J. Liu, Y. Shi, J. Yang, J. Zhang, and X. You, "Mode analysis and fault-tolerant method of open-circuit fault for a dual active-bridge DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6916–6926, Aug. 2020.

[149] P. Pal, M. Poshtan, A. R. Beig, R. K. Behera, K. Al Hosani, and U. R. Muduli, "Enhancing resilience of DAB converters with fault-tolerant approach," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, 2024, pp. 453–460.

[150] N. Wang, Y. Wang, Z. Chen, and S. Liu, "A novel fault-tolerant control strategy for dual active bridge converter under open circuit fault," in *Proc. Int. Power Electron. Conf.*, Himeji, Japan, 2022, pp. 1621–1625.

[151] Q. Bu, H. Wen, H. Shi, and Y. Zhu, "A comparative review of high-frequency transient DC bias current mitigation strategies in dual-active-bridge DC-DC converters under phase-shift modulations," *IEEE Trans. Ind. Appl.*, vol. 58, no. 2, pp. 2166–2182, Mar./Apr. 2022.

[152] C. Yang, J. Wang, C. Wang, X. You, and L. Xu, "Transient DC bias current reducing for bidirectional dual-active-bridge DC-DC converter by modifying modulation," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 13149–13161, Nov. 2021.

[153] T. Dai et al., "Research on transient DC bias analysis and suppression in EPS DAB DC-DC converter," *IEEE Access*, vol. 8, pp. 61421–61432, 2020.

[154] G. Ortiz, L. Fässler, J. W. Kolar, and O. Apeldoorn, "Flux balancing of isolation transformers and application of 'the magnetic ear' for closed-loop volt-second compensation," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4078–4090, Aug. 2014.

[155] D. Atkar, P. Chaturvedi, F. Pellitteri, P. Nachankar, and S. Chaitanya, "DC bias abatement in dual active bridge converter using covalent active and passive components," in *Proc. 16th Int. Conf. Compat., Power Electron., Power Eng.*, Birmingham, United Kingdom, 2022, pp. 1–6.

[156] R. Redl, N. O. Sokal, and C. W. Schaefer, "Transformer saturation and unusual system oscillation in capacitively coupled half-bridge or full-bridge forward converters: Causes, analyses, and cures," in *Proc. Annu. IEEE Power Electron. Specialists Conf.*, 1988, vol. 2, pp. 820–829.

[157] Z. Shan, J. Jatskevich, H. H. C. Iu, and T. Fernando, "Simplified load-feedforward control design for dual-active-bridge converters with current-mode modulation," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 2073–2085, Dec. 2018.

[158] W. Wang, T. Liu, S. Cheng, C. Cheng, S. Niu, and A. Chen, "Feedback linearization-based load-current feedforward control strategy for fast dynamic response of hybrid modular DC transformers," *IEEE Trans. Power Electron.*, vol. 40, no. 6, pp. 7709–7726, Jun. 2025, doi: 10.1109/TPEL.2025.3530078.

[159] W. Song, N. Hou, and M. Wu, "Virtual direct power control scheme of dual active bridge DC-DC converters for fast dynamic response," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1750–1759, Feb. 2018.

[160] Y. Dai, S. Luo, and Z. Li, "Direct power based control strategy for DAB DC-DC converter with cooperative triple phase shifted modulation," *IEEE Access*, vol. 9, pp. 147791–147800, 2021.

[161] B. Zhao, Q. Song, W. Liu, and Y. Zhao, "Transient DC bias and current impact effects of high-frequency-isolated bidirectional DC-DC converter in practice," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3203–3216, Apr. 2016.

[162] J. Lu and J. Yin, "Unified phase shift control strategy to optimize transient current response in a dual active bridge DC-DC converter during unidirectional and bidirectional power flow changes," in *Proc. IEEE Energy Convers. Congr. Expo. Asia*, Nanjing, China, 2020, pp. 2599–2604.

[163] R. Chattopadhyay, U. Raheja, G. Gohil, V. Nair, and S. Bhattacharya, "Sensorless phase shift control for phase shifted DC-DC converters for eliminating DC transients from transformer winding currents," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, San Antonio, TX, USA, 2018, pp. 1882–1889.

[164] J. Hu, S. Cui, D. V. d. Hoff, and R. W. De Doncker, "Generic dynamic phase-shift control for bidirectional dual-active bridge converters," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6197–6202, Jun. 2021.

[165] C. Sun, X. Jiang, J. Liu, L. Cao, Y. Yang, and K. H. Loo, "A unified design approach of optimal transient single-phase-shift modulation for nonresonant dual-active-bridge converter with complete transient DC-Offset elimination," *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13217–13237, Nov. 2022.

[166] Z. Zhang et al., "An improved DC bias elimination strategy with extended phase shift control for dual-active-bridge DC-DC converter," in *Proc. Chin. Autom. Congr.*, Hangzhou, China, 2019, pp. 4274–4279.

[167] Y. Tang, X. Li, S. Zhou, C. Sun, and G. Chen, "Comprehensive study of fast load modulation with volt-second balance in a dual-active-bridge converter," *IET Power Electron.*, vol. 12, no. 6, pp. 1357–1367, 2019.

[168] X. Li and Y. Li, "An optimized phase-shift modulation for fast transient response in a dual-active-bridge converter," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2661–2665, Jun. 2014.

[169] K. Takagi and H. Fujita, "Dynamic control and performance of a dual-active-bridge DC-DC converter," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7858–7866, Sep. 2018.

[170] Q. Bu, H. Wen, H. Shi, Y. Hu, and Y. Yang, "Universal transient DC-Bias current suppression strategy in dual-active-bridge converters for energy storage systems," *IEEE Trans. Transp. Electrific.*, vol. 7, no. 2, pp. 509–526, Jun. 2021.

[171] J. Yin, J. Lu, Y. Liu, J. Peng, and H. Jiang, "Novel phase-shift method for fast power reversal with transient zero voltage switching in a bidirectional dual active bridge DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 8028–8038, Sep. 2021.

[172] Z. Ji, Q. Wang, D. Li, and Y. Sun, "Fast DC-Bias current control of dual active bridge converters with feedforward compensation," *IEEE Trans. Circuits Syst. II, Exp. Briefs.*, vol. 67, no. 11, pp. 2587–2591, Nov. 2020.

[173] H. Qiu, J. Wang, and Y. Tang, "Modular multilevel converter device-level loss balancing control for better lifetime," in *Proc. IEEE Energy Convers. Congr. Expo.*, Detroit, MI, USA, 2020, pp. 2909–2914.

[174] C. Hua, C. Huang, C. Yang, and P. Yang, "A hybrid EMI filter for CM EMI suppression in DC-DC converter," in *Proc. 14th Int. Symp. Antennas, Propag. EM Theory*, Hefei, China, 2024, pp. 1–3.

[175] X. Zhao, Z. Wang, D. Jiang, and Z. Liu, "Common-mode voltage analysis and suppression strategy for three-level dual-active-bridge converter," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 13107–13119, Oct. 2024.

[176] S. Kumar, S. K. Voruganti, B. Akin, and G. Gohil, "Common-mode current analysis and cancellation technique for dual active bridge converter based DC system," *IEEE Trans. Ind. Appl.*, vol. 58, no. 4, pp. 4955–4966, Jul./Aug. 2022.

[177] Y. Deng, J. Li, K. H. Shin, T. Viitanen, M. Saeedifard, and R. G. Harley, "Improved modulation scheme for loss balancing of three-level active NPC converters," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2521–2532, Apr. 2017.

[178] G. Zhang, Y. Yang, F. Iannuzzo, K. Li, F. Blaabjerg, and H. Xu, "Loss distribution analysis of three-level active neutral-point-clamped (3L-ANPC) converter with different PWM strategies," in *Proc. IEEE 2nd Annu. Southern Power Electron. Conf.*, Auckland, New Zealand, 2016, pp. 1–6.

[179] Q. Guan, Y. Zhang, H. Zhao, and Y. Kang, "Optimized switching strategy for ANPC-DAB converter through multiple zero states," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2885–2898, Mar. 2022.

[180] J. Dong, J. Pou, X. Li, S. Mukherjee, A. K. Gupta, and Y. Zeng, "Hybrid duty ratio phase-shift modulation for a Si SiC neutral-point-clamped dual-active-bridge converter," *IEEE Access*, vol. 11, pp. 129866–129881, 2023.

[181] J. Dong et al., "Hybrid si SiC neutral-point-clamped dual-active-bridge converter for high-voltage battery energy storage systems," in *Proc. 12th IEEE Energy Convers. Congr. Expo. Asia*, 2021, pp. 632–637.

[182] J. Dong, J. Pou, S. Mukherjee, A. K. Gupta, and Y. Zeng, "Efficiency optimization for hybrid Si SiC neutral-point-clamped dual-active-bridge converter for energy storage systems," in *Proc. IEEE Innov. Smart Grid Technol. Asia*, 2022, pp. 345–348.

[183] Y. Wei, T. Pereira, Y. Pan, M. Liserre, F. Blaabjerg, and H. A. Mantooth, "A general and automatic RMS current oriented optimal design tool for LLC resonant converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7318–7332, Dec. 2022.

[184] J. Sun, L. Yuan, Q. Gu, R. Duan, Z. Lu, and Z. Zhao, "Design-oriented comprehensive time-domain model for CLLC class isolated bidirectional DC-DC converter for various operation modes," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3491–3505, Apr. 2020.

[185] Y. Wang, K. Wang, C. Li, Z. Zheng, and Y. Li, "System-level efficiency evaluation of isolated DC/DC converters in power electronics transformers for medium-voltage DC systems," *IEEE Access*, vol. 7, pp. 48445–48458, 2019.

[186] J. Saha, N. B. Y. Gorla, and S. K. Panda, "Implementation of power balance control scheme for a cascaded matrix-based dual-active-bridge (CMB-DAB) MVAC-LVDC converter," *IEEE Trans. Ind. Appl.*, vol. 58, no. 1, pp. 388–399, Jan./Feb. 2022.

[187] A. Filba-Martinez, S. Busquets-Monge, and J. Bordonau, "Modulation and capacitor voltage balancing control of a four-level active-clamped dual-active-bridge DC-DC converter," in *Proc. Eur. Conf. Power Electron. Appl.*, Karlsruhe, Germany, 2016, pp. 1–8.

[188] S. Busquets-Monge, R. Rafiezadeh, S. Alepuz, A. Filba-Martinez, and J. Nicolas-Apruzzese, "Fast reliability assessment of neutral-point-clamped topologies through markov models," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13449–13459, Dec. 2021.

[189] S. Cui, N. Soltau, and R. W. De Doncker, "A high step-up ratio soft-switching dc–dc converter for interconnection of MVDC and HVDC grids," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2986–3001, Apr. 2018.

[190] W. Cui, S. Shao, J. Zhang, Y. Li, and J. Zhang, "Bidirectional modular multilevel resonant DC-DC converter for medium voltage power conversion," in *Proc. IEEE Energy Convers. Congr. Expo.*, Detroit, MI, USA, 2020, pp. 4380–4385.

[191] B. Zhao, Q. Song, J. Li, Y. Wang, and W. Liu, "Modular multilevel high-frequency-link DC transformer based on dual active phase-shift principle for medium-voltage DC power distribution application," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1779–1791, Mar. 2017.
[192] B. Zhao, Q. Song, J. Li, Y. Wang, and W. Liu, "High-frequency-Link modulation methodology of DC-DC transformer based on modular multilevel converter for HVDC application: Comprehensive analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3413–3424, May 2017.
[193] B. Zhao, Q. Song, J. Li, X. Xu, and W. Liu, "Comparative analysis of multilevel-high-frequency-link and Multilevel-DC-Link DC-DC transformers based on MMC and dual-active bridge for MVDC application," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2035–2049, Mar. 2018.
[194] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. De Doncker, "Comparison of the modular multilevel DC converter and the dual-active bridge converter for power conversion in HVDC and MVDC Grids," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 124–137, Jan. 2014.
[195] G. P. Adam, F. Alsokhiry, Y. Al-Turki, M. O. Ajangnay, and A. Y. Amogpai, "DC-DC converters for medium and high voltage applications," in *Proc. 45th Annu. Conf. IEEE Ind. Electron. Soc.*, Lisbon, Portugal, 2019, pp. 3337–3342.

Chaochao Song (Member, IEEE) received the B.S. degree in automation and the M.S. degree in power electronics from Shandong University, Jinan, China, in 2016 and 2019, respectively, and the Ph.D. degree in energy technology from Aalborg University, Aalborg, Denmark, in 2023.

He was a Visiting Researcher with Fraunhofer ISE, Freiburg, Germany, from June to September 2022. He is currently a postdoc with Aalborg University. His current research interests include control of DAB converters, multilevel converters, and modeling of SiC-based power electronic converters.

Ning Wang (Member, IEEE) received the B.Eng. degree in electrical engineering from Jilin University, Changchun, China, in 2015, the M.Sc. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2018, and the Ph.D. degree in energy from Aalborg University, Aalborg, Denmark, in 2025.

He is currently a Postdoctoral Researcher with Aalborg University. His research interests include dc–dc converter, advance control algorithm and renewable energy system.

Ariya Sangwongwanich (Senior Member, IEEE) received the B.Eng. degree in electrical engineering from Chulalongkorn University, Bangkok, Thailand, in 2013 and the M.Sc. and Ph.D. degrees in energy engineering from Aalborg University, Aalborg, Denmark, in 2015 and 2018, respectively.

He is currently an Associate Professor with the Department of Energy, Aalborg University, where he is also a Research Group-Leader of Sustainable Power Electronics and Electrification research program. He was a Visiting Researcher with RWTH Aachen, Aachen, Germany, in 2017 and University of Cambridge, Cambridge, U.K., in 2023. His research interests include control of grid-connected converters, photovoltaic systems, and reliability and sustainability in power electronics.

Dr. Sangwongwanich was the recipient of the Danish Academy of Natural Sciences Ph.D. Prize and the Spar Nord Foundation Research Award for his Ph.D. thesis in 2019.

Frede Blaabjerg (Fellow, IEEE) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. He received the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 1995.

He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of Power Electronics and Drives in 1998. From 2017, he became a Villum Investigator. He is honoris causa with University Politehnica Timisoara (UPT), Timişoara, Romania, and Tallinn Technical University (TTU), Tallinn, Estonia. He has authored or coauthored more than 600 journal papers in the fields of power electronics. He is the coauthor of four monographs and editor of ten books in power electronics and its applications. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics, and adjustable speed drives.

Dr. Blaabjerg was the recipient of 33 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019, and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019–2020, he was a President of IEEE Power Electronics Society. He has been Vice-President of the Danish Academy of Technical Sciences. He is nominated in 2014–2020 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.

Pooya Davari (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in electronic engineering from Mazandaran University, Babolsar, Iran, in 2004 and 2008, respectively, and the Ph.D. degree in power electronics from Queensland University of Technology (QUT), Brisbane, QLD, Australia, in 2013.

From 2005 to 2010, he was involved in several electronics and power electronics projects as a Development Engineer. From 2013 to 2014, he was with QUT, as a Lecturer. He joined Aalborg University (AAU), in 2014, as a Postdoc, where he is currently a Full Professor. He has authored or coauthored more than 200 technical papers. He has been focusing on EMI, power quality, and harmonic mitigation analysis and control in power electronic systems.

Prof. Davari was a Guest Associate Editor of *IET journal of Power Electronics*, IEEE ACCESS Journal, *Journal of Electronics*, and JOURNAL OF APPLIED SCIENCES. He is currently an Area Editor for IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION and Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS, *Transactions on Transportation Electrification*, *Journal of Emerging and Selected Topics in Power Electronics*, Editorial board member of *Journal of Applied Sciences* and *Journal of Magnetics*. He has been an Editor-in-Chief of *Circuit World* Journal 2020–2025. He is member of Joint Working Group six and Working Group eight at the IEC standardization TC77 A. He was the recipient of Equinor 2022 Prize (oldest Denmark Engineering Award) and 2020 IEEE EMC Society Young Professional Award for his contribution to EMI and Harmonic Mitigation and Modeling in Power Electronic Applications. He was also the recipient of five journal and conference best paper awards. He is founder and chair of IEEE EMC Society Chapter Denmark.