Investigation of an Easy-Structured and Cost-Effective Energy-Storage System in the DC-Bus

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***Abstract*—This article presents a new approach of an energy-storage technique for feedback-energy of drive-systems. A well-known state-of-the-art technology for high-power application, is to feed the energy back into the grid using a three-phase full-bridge. However, for smaller drive-systems this is not feasible due to cost and efficiency reasons. Here it is more advantageous to store the fed-back energy directly in the dc-bus. The simplest approach of storing energy directly in the capacitor of the rectifier is limited due to capacitance and voltage issues. Using additional large storage capacitors, such as ultracapacitors, directly in the dc-bus is limited by their voltage ratings. Therefore, a prior and bidirectional dc/dc-conversion is required, which has also disadvantages in terms of costs and efficiency. The new approach presented in this article allows storage capacitors to be operated directly in the dc-bus without prior dc/dc-conversion, which reduces costs, increases the efficiency, and results in an optimal cost-benefit ratio. The principal function of this new current-source-based energy-storage is shown by a detailed description of the topology, its modeling, and an evaluation using simulations and measurements. It turns out that the disclosed new approach is a promising alternative to the prior dc/dc-conversion.**

***Index Terms*—Costs, current-source-based energy-storage, EDLC, energy-storage in the dc-bus, industrial electronics, ultra-capacitor.**

I. Introduction

EFFICIENT energy conversion and storage is one of the most relevant topics with regard to the energy transition in the field of power electronics. It becomes increasingly important to use energy efficiently, particularly at industrial applications in machines with drive systems. Besides the efficiency also the quantity of such systems is important, so these systems should be both efficient and cost-effective.

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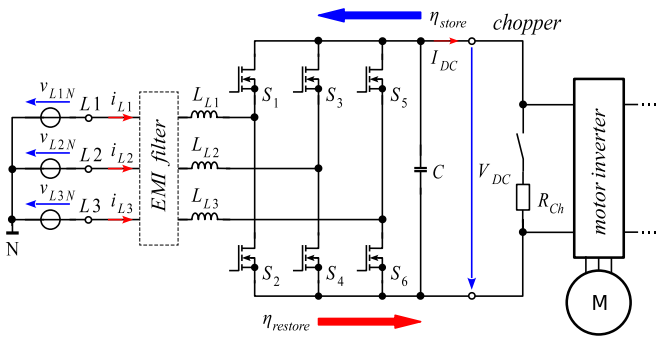

Fig. 1. Drive-system with three-phase full bridge (six-switch-rectifier).

At the first generations of drive systems with unidirectional rectifiers, no emphasis was placed on storing energy. To ensure that the voltage in the dc-bus does not become too high, the backfeed energy was converted into heat by the chopper-resistor R_{Ch} to be released into the environment, which resulted in a very bad system efficiency. With respect to the number of drive systems worldwide, this is an enormous amount of energy that is simply wasted. Therefore, the trend shifted to make this wasted energy usable again.

The most common structure of a drive system consists of a bidirectional grid inverter, which is also known as three-phase full-bridge or as six-switch rectifier, a dc-bus and chopper-resistor followed by one or more parallel downstream motor inverters, as can be seen in Fig. 1.

The main feature of this topology is the possibility for a bidirectional power-flow, as described in [1]. While energy is drawn from the grid to the motor when accelerating, it is fed back from the motor into the dc-bus and further back into the grid during braking. This allows the backfeeding energy to be stored in the grid.

However, there are some disadvantages. One big disadvantage, especially in the past, remains still the total efficiency of this energy storage topology. It is a common process within a machine that a motor accelerates cyclically and then brakes again. This causes so-called pendulum energies, which are essential for considering the total efficiency η_{tot} of the three-phase full bridge. Therefore, the motor-inverter and the motor are considered as loss-free. When the motor M is braked, the energy is fed back from the motor via the inverter into the dc-bus and further back into the grid by passing the three-phase full-bridge, which is marked with the left-pointing blue arrow in Fig. 1.

If the motor M then reaccelerates, the energy has to pass the three-phase full-bridge again into the other direction toward the motor inverter, which is marked with the right-pointing red arrow in Fig. 1. So the energy passes the three-phase full-bridge twice, which has the effect of cascading in terms of efficiency. The overall efficiency η_{tot} results from the product of efficiencies from the first dc–ac-conversion η_{store} to store the energy in the grid, followed by the ac–dc-conversion η_{restore} to get the energy back from the grid according to the following:

$$\eta_{\text{tot}} = \eta_{\text{store}} \cdot \eta_{\text{restore}}. \tag{1}$$

Assuming an efficiency of 0.95 for one conversion of the three-phase full-bridge, so $\eta_{\text{store}} = \eta_{\text{restore}} = 0.95$, a total efficiency of 0.9 results, which is not quite good. By using SiC or GaN transistors here, which are quite efficient, the efficiency of the three-phase full-bridge has been increased in recent years. [2] there shows an Sic-based three-phase full-bridge for a battery charger with a efficiency of round about 98%. However, the total efficiency is still reduced due the cascading by the double pass of the energy. In addition to the disadvantage in terms of the total efficiency, the cost-benefit ratio must be taken into account. Especially in the industrial sector, costs are always a limiting factor due to the large quantities to be used. Therefore, six transistors are required here, which can be implemented as IGBTs or MOSFETs based on SiC or GaN. These types of transistors are very expensive, which strongly increases the costs.

In the large power range there is no promising alternative to the principle of Fig. 1, since the backfeeding energy is too large to be removed by the chopper or stored in any other way. But here too, attempts are being made to reduce costs by a smaller dimensioning of the power switches in practice. For this purpose, only a reduced portion of the energy is fed back, the rest of the energy is removed by the chopper-resistor. The chopper-resistor is required anyway and has to be dimensioned for the full amount of the backfeed energy due to possible grid interruptions. In the small power range there is often the problem that the amount of the backfeed energy is just so large that, on the one hand, it is too large to be removed by the chopper-resistor, and on the other hand, feeding it back into the grid is not reliable. In other words, the backfeeding of the energy is often not worthwhile in terms of the cost-benefit ratio.

Therefore it would be favorable to store the energy in the dc-bus without feeding it back to the grid. In consequence only an unidirectional rectifier topology is required. In addition, a state-of-the-art energy-storage module is connected to the dc-bus, as can be seen from Fig. 2.

This principle has been used for a long time in many areas of drive technology, where the cost-benefit ratio plays an important role for the reasons described previously. It leads to reduced costs compared to the three-phase full-bridge, due to the fact that only unidirectional power flow and therefore a standard B6-rectifier is sufficient and is therefore still state of the art. Further is has the advantage, that no high startup currents are drawn from the grid when the machines reaccelerate. Depending on the capacity of the energy-storage system, no or a reduced current is drawn from the grid for a short period of time. In [3], this energy-storage

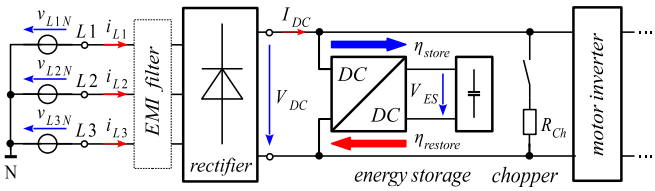

Fig. 2. Additional energy-storage module in the DC-bus [3].

principle itself as well as its advantages are described in detail. Further various applications of this principle in drive systems are considered. In [4], the specific application in an injection molding machine is described. Is is mentioned here that 49 % of the energy can be saved compared to the chopper-operation. This principle is also applied to port cranes, where economic efficiency plays a very important role, as described in [5].

The energy-storage module itself is usually relayed with supercaps, ultracaps, electric double-layer capacitors (EDLCs), or related technologies. For further information on the properties of ultracapacitors as well as the precise design of the capacity of the energy-storage module in relation to the overall performance of the drive system it is referred to [6] and [7]. Since these capacitors are only suitable for low voltages, the dc/dc converter shown in Fig. 2 is required upstream of the energy-storage device. This dc/dc converter offers a wide range between efficiency and cost depending on its topology. The simplest and most cost-effective form consists of a bidirectional buck-boost converter, which is mentioned in [8] and [9]. The principle itself with the operation modes, the mathematical modeling and simulation regarding the whole drive system is described in [8] and [10]. A detailed description of the design and dimensioning can be found in [11], while Zhang et al. [12] presented a control strategy for this type of dc/dc converter. However, these control strategies are also subject to nonideal influences, which are analyzed in more detail in [13].

In addition to the simple bidirectional buck-boost converter, any other dc/dc converter topology can theoretically be used here. A simple extension to this is the three-level buck-boost converter described in [14], which is mainly characterized by a lower voltage stress. A further alternative is represented by the dual-input converter, which is described in detail in [15]. Another alternative of nongalvanic-isolated converters are Cuk-, SEPIC-, or Zeta-converters and their derivations mentioned in [9] and [16], which are characterized by the capacitive decoupling between the dc-bus and the energy-storage. This feature protects against the destruction of the energy-storage capacitors in the event of a failure. However, no advantage can be taken from the main advantage of these topologies, which is the ability to convert from an input voltage to a lower or higher output voltage. It is important to note, that these topologies must always be implemented in a bidirectional design. This increases the component complexity, which can be seen for the mentioned Boost–Cuk converter presented in [16] and for a bidirectional SEPIC-Zeta dc–dc converter presented in [17]. By using the corresponding soft-switching techniques for this topologies, the

efficiency can be further improved, but also the component complexity is further increased.

Of course, the dc/dc converter can also be implemented as a galvanic-isolated variant with soft-switching mentioned in [18]. Another comparable topology is the DAB-converter mentioned in [19], the exemplary derivations mentioned in [20] and [21] as well as the application of special control algorithms described in [22]. The most widely used topology with potential isolation and soft-switching is the well-known LLC-converter, which is described in [19] and [23] as well as with some efficiency optimizations in [24]. A further derivative is the CLLC-converter described in [25], which enables improved efficiency due to its operating behavior.

However, each topology has its specific advantages and disadvantages, which must be weighed according to the requirements. All topologies share two major disadvantages compared to the newly approach topology presented later. The first one concerns the number of semiconductor components and the associated costs for the more complex topologies. Compared to the simple bidirectional buck-boost converter, all topologies have a larger number of components, which increases the limiting factor of costs and therefore makes the topologies less interesting for industrial use. The second disadvantage concerns the total efficiency of all topologies, or rather the entire approach to an energy-storage system with prior dc/dc conversion. In comparison, it is initially expected that the efficiency is better than that of the three-phase full-bridge. Now, considering a load cycle in pendulum operation, the energy fed back by the motor must pass through the upstream dc/dc converter before being stored in the energy-storage system, as indicated by the right-pointing blue arrow η_{store} in Fig. 2. When the machine re-accelerates and the energy-storage is discharged, the energy must pass the dc/dc converter a second time, which is indicated by the left-pointing red arrow η_{restore}. In terms of efficiency, this again corresponds to a cascading arrangement comparable to the three-phase full-bridge according to (1). The total efficiency is therefore reduced accordingly here as well. For example, the efficiency of [17] for the bidirectional SEPIC-Zeta-converter is given with $\eta_{\text{store}} = 92.6\,\%$ and $\eta_{\text{restore}} = 94.3\,\%$, which will result in a total efficiency of $\eta_{\text{tot}} \approx 87.3\,\%$ according to (1).

It can be summarized that the cost-benefit ratio for energy-storage with prior dc/dc conversion is still not optimal. An improvement of this problem is achieved by the new approach presented in the following, which stores energy directly in the dc-bus eliminating the required prior dc/dc conversion in its previous form. This smooth out the cascading in terms of efficiency, which is expected to increase the total efficiency and to reduce costs compared to the earlier mentioned converter topologies.

II. Topology and Principle of the Current-Source-Based Energy-Storage at Dc-Bus

Theoretically, the simplest approach of storing energy directly in the dc-bus without prior dc/dc conversion would be to store the energy in the capacitor C of a standard B6-diode-rectifier accordingly, which is designed as an electrolytic capacitor due to the required voltage strength. Other types of capacitors, such as ultracapacitors cannot be used here due to their significantly

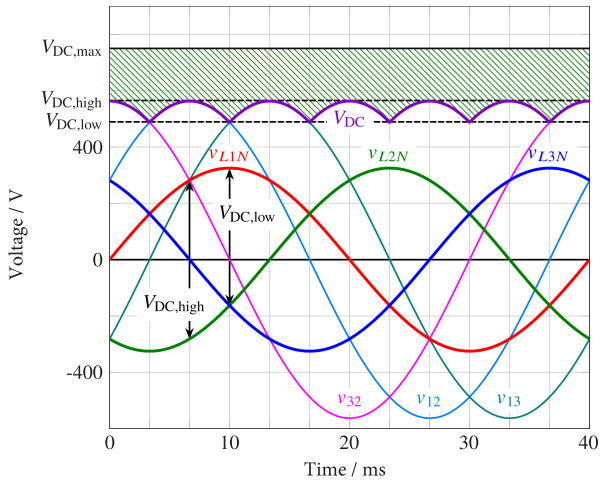

Fig. 3. Voltage levels for rectification and possible energy-storage in the DC-bus (green hatched area) with DC-bus capacitor C.

lower voltage strengths. As simple as the approach seems, it has a further serious physical limitation due to the B6-rectification, which makes it in general not possible to store a larger amount of energy this way.

The storable amount of energy in the dc-bus depends on the dc-bus voltage V_{dc} and the capacitance C of the dc-bus capacitor according to the following:

$$E_{\text{C}} = \frac{1}{2} C \cdot V_{\text{dc}}^2. \tag{2}$$

Having a look at a B6-rectification, the typical pulsating dc-voltage curve V_{dc} occurs for the dc-bus voltage, as can be seen in Fig. 3.

The minimum and maximum values, which correspond to the well-known lower rectification value $V_{\text{dc,low}}$ and the upper rectification value $V_{\text{dc,high}}$ occur periodically. Between this V_{dc} is alternating. Considering the European grid voltage $V_{\text{LL}} = 400\,\text{V}$, which means $V_{\text{LN}} = 230\,\text{V}$, the lower rectification value corresponds to $V_{\text{dc,low}} = 489\,\text{V}$ and the upper rectification value corresponds to $V_{\text{dc,high}} = 565\,\text{V}$. These voltages are always present, so that the voltage range between $0\,\text{V}$ and the actual value of V_{dc} (maximum $V_{\text{dc,high}}$) is blocked due to the rectification and cannot be used for additional energy-storage. In consequence a certain amount of energy is stored in the capacitor, which results purely from the B6 rectification and therefore cannot be obtained from it.

In order to be able to store the backfeed energy into the dc-bus, the value of the dc-bus voltage V_{dc} must be increased to a voltage level above the upper rectification value $V_{\text{dc,high}}$. However, V_{dc} cannot be raised to any desired level. Due to the voltage strengths of the components, such as the semiconductor components and in particular the capacitors used, there is a limiting maximum, which is defined as $V_{\text{dc,max}}$. So the usable voltage level of V_{dc} results in $V_{\text{dc,high}} < V_{\text{dc}} \leq V_{\text{dc,max}}$. With the full voltage range, which results from the difference of the maximum dc-bus voltage $V_{\text{dc,max}}$ and the upper rectification value $V_{\text{dc,high}}$, the backfeed energy from the motor can be stored in the dc-bus. This corresponds to the green hatched area in Fig. 3. The amount of energy $E_{\text{C,fed}}$

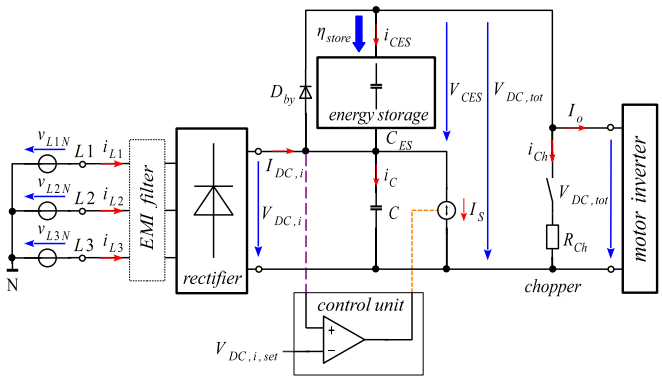

Fig. 4. Novel current-source-based energy-storage topology in the DC-bus.

that can be stored can be calculated according to the following:

$$E_{\mathrm{Cfed}} = \frac{1}{2} C \cdot (V_{\mathrm{dc,max}}^2 - V_{\mathrm{dc,high}}^2). \tag{3}$$

Using (2) and (3), the ratio ρ_{EC} of the usable energy $E_{\mathrm{C,fed}}$ to the total energy $E_{\mathrm{dc,max}}$, which results from $V_{\mathrm{dc,max}}$ put in into (2), can be calculated according to the following:

$$\rho_{\mathrm{EC}} = \frac{E_{\mathrm{C,fed}}}{E_{\mathrm{CDC,max}}} = 1 - \frac{V_{\mathrm{dc,high}}^2}{V_{\mathrm{dc,max}}^2}. \tag{4}$$

For example, if you allow a voltage of $V_{\mathrm{dc,max}} = 700\,\mathrm{V}$, (4) results in a usable energy range of $35\,\%$, which is not particularly good. Qualitatively this can be observed in Fig. 3 based on the hatched areas. The possibility of increasing the capacity C increases the usable energy $E_{\mathrm{C,fed}}$ and the total energy $E_{\mathrm{dc,max}}$ in general, but does not bring any advantage in terms of the ratio ρ_{EC} of the retaliative usable energy. For this basic idea it can be summarized, that the storage of larger amounts of energy is therefore not possible with this topology. In addition, as already mentioned, the required large voltages strengths for the components as the semiconductor components and capacitors makes it further disadvantageous.

These disadvantages can be remedied with the newly proposed current-source-based energy-storage at the dc-bus presented in the following. For this topology, a standard B6 rectifier with capacitor is supplemented with additional components. The main element of the principle is the energy-storage in form of a capacitor C_{ES}, which is located "above" the positive branch of the dc-bus, as to be seen in Fig. 4. This is also described in the pending patent application [26]. By inserting the later described additional components, the energy-storage capacitor C_{ES} can be completely charged and discharged, i.e., down to $0\,\mathrm{V}$. Therefore, the capacitors of the energy-storage module can be also relayed with super-caps, ultracaps, EDLCs or related technologies with low voltage-strengths. The total capacity of the energy-storage capacitor is designed with respect to the backfeeding load, which is described more detailed in Section IV-A. In order for the principle to work as intended, an additional certain dimensioning criterion must be met, which is usually determined by the dimensioning of the capacitance based on the load. According to (5), the capacity for the energy-storage capacitor C_{ES} must be significantly larger than the capacity of the dc-bus capacitor C of the B6-rectifier

$$C_{\mathrm{ES}} >> C. \tag{5}$$

To best meet the criterion of (5), capacitively large types of these capacitors should be used. For the understanding of the functional principle of this topology and the dimensioning criterion of (5), it is also essential to know, that the voltage across a capacitor is determined by the ratio of the charge $Q(t)$ and the capacitance C of the capacitor as presented in the following:

$$v_{\mathrm{C}}(t) = \frac{Q(t)}{C} = \int_{t_0}^{t} i_{\mathrm{C}}(t)dt + v_{\mathrm{C}}(t_0). \tag{6}$$

For $i_{\mathrm{C}}(t) = I_{\mathrm{C}}$ and $t = 0$ (6) simplifies to the linear relationship of

$$v_{\mathrm{C}}(t) = \frac{I_{\mathrm{C}}}{C} \cdot t + v_0. \tag{7}$$

As could be seen, the capacitor voltage $v_{\mathrm{C}}(t)$ is inversely proportional to the capacity C of the capacitor. Having a look at the series connection of the two capacitors C and C_{ES} of Fig. 4 under consideration of $C << C_{\mathrm{ES}}$, the voltage rise of $V_{\mathrm{dc,i}}$, applied at C would be significantly larger than the voltage rise of V_{CES}, applied at C_{ES}. In simpler terms, C is fully charged much faster than C_{ES}.

For charging the energy-storage capacitor C_{ES} the controlled current-source I_S is required, which is connected in parallel to the dc-bus capacitor C. In contrast to introductorily presented state-of-the-art technology with prior dc/dc conversion mentioned among others in [8] and [10], as explained in more detail in Section III, in this arrangement the energy only needs to pass through the controlled current-source I_S during backfeeding by the load once. This is represented with the downward-pointing blue arrow in Fig. 4. In consequence, the total efficiency of the energy storage system corresponds mainly to

$$\eta_{\mathrm{tot}} = \eta_{\mathrm{store}}. \tag{8}$$

The current-source can theoretically be relayed with any type of dc/dc converter that can set the voltage up to an higher level. This can be a simple boost converter or another comparable topology mentioned in [9]. Considering that the backfeeding energy respectively the current only passes the current-source I_S once and taking the introduced aspects with low costs and the best possible efficiency into account, a simple boost converter represents the optimum here. This has the fewest number of components and is therefore the most suitable solution regarding the cost-benefit ratio. The structure and dimensioning of this boost converter in this arrangement is discussed in more detail in Section IV-B.

The third addition is a bypass-diode D_{by} for the energy-storage capacitor C_{ES}. Without this bypass, the principle does not work, because the energy-storage capacitor C_{ES} would form a barrier between the grid side and the output side after it is discharged.

In Fig. 4, the energy-storage capacitor C_{ES} and the further components, such as the controlled current-source I_S and the bypass-diode D_{by} have been inserted into the positive branch of

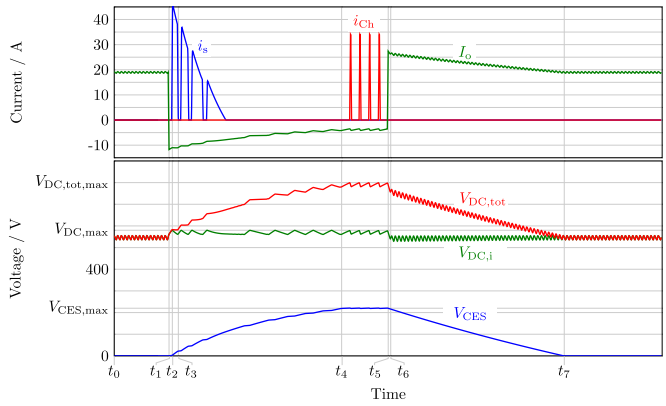

Fig. 5. Simulated voltages $V_{dc,i}$, V_{CES}, $V_{dc,tot}$, and currents i_{Ch}, i_S, I_o for current-source-based energy-storage at DC-bus.

the dc-bus. It is also possible, taking into account the inverse polarities, to insert the corresponding components into the negative branch of the dc-bus.

III. Operation Modes of the Current-Source-Based Energy-Storage at DC-Bus

As is usual with this type of circuit, there are two operating modes. During motor operation, the energy is drawn from the grid and delivered via the drive system to the motor, which converts the electrical energy into mechanical energy. During generator operation, the motor converts the mechanical energy back into electrical energy, which then flows from the motor back into the drive system.

In the following, a full load cycle of the current-source-based energy-storage at dc-bus is considered by a principle simulation with mains voltage in Fig. 5 and the corresponding modes in Fig. 6. The voltage-source block in the schematics of Fig. 6 represents the rectified mains voltage.

The lower plot of Fig. 5 shows the two capacitor–voltages with $V_{dc,i}$ for the dc-bus capacitor C, which also corresponds to the rectified mains voltage, V_{CES} for the energy-storage capacitor C_{ES} and the resulting total dc-bus voltage $V_{dc,tot}$. As is well known, every capacitor has a maximum charging voltage that must not be exceeded; otherwise the capacitor will be destroyed. In order to be able to charge C_{ES} without exceeding this maximum voltage, the controlled current-source I_S in Fig. 4 must continuously take over the current during generator operation. Therefore, a maximum allowed voltage $V_{dc,i,max}$ for C is set, which is equal to the parametrized threshold voltage of $V_{dc,CS}$, at which the controlled current-source will become active. As for the capacitor C there is also a maximum allowed charging voltage $V_{CES,max}$ for the energy-storage capacitor C_{ES}. If this value $V_{dc,i} > V_{dc,i,max}$ for C, $V_{CES} > V_{CES,max}$ for C_{ES} and further the sum of both maximum allowed charging voltages $V_{dc,tot} > V_{dc,tot,max}$ will be reached, any further backfeeding energy is dissipated into heat by the chopper-resistor R_{Ch} in Fig. 4.

The upper plot of Fig. 5 shows the corresponding currents with the chopper-current i_{Ch}, the current i_S of the controlled current-source, and the output current I_o.

A. Motor Operation

During motor operation, which occurs in the first period from t_0 to t_1 of Fig. 5 the energy is drawn from the grid and delivered to the load via the rectifier and the dc-bus, which is illustrated by mode 1 of Fig. 6. This corresponds to the normal active operating state of a machine. Since the energy storage C_{ES} is completely discharged and inactive, the load is supplied via the bypass-diode D_{by}. The controlled current-source I_S is inactive in this operation mode.

At motor operation the circuit has a slight disadvantage. In comparison to a normal B6-rectifier and subsequent dc-bus, there is an additional diode path in the current path with D_{by}, which slightly worsens the efficiency of the principle in this operating mode due to the losses resulting from that diode path. However, this can be counteracted if instead of a standard diode a diode with a low forward voltage, such as a Schottky-diode, or alternatively a MOSFET with a low $R_{DS,on}$ is used.

B. Transition From Motor to Generator Operation

At time t_1, the motor is braked, so it switches from motor to generator mode so that the mechanical energy is fed back into the circuit as electrical energy. This leads to a negative current $-I_o$ at the output in Fig. 4, which flows back from the load into the circuit and causes the circuit to switch to generator operation. This causes the diodes of the rectifier to block, causing a current i_C to flow through the series connection of the two capacitors C and C_{ES}, which is illustrated by mode 2 of Fig. 6

$$i_C = i_{CES} = -I_o. \tag{9}$$

This current leads to a charge and subsequently to an increase of the total dc-bus voltage $V_{dc,tot}$ at the output of the circuit, which can be seen in Fig. 5. This voltage corresponds to the sum of the input-side voltage $V_{dc,i}$ of the circuit, which is applied at capacitor C, and the voltage V_{CES} applied at the energy-storage, as can be seen from

$$V_{dc,tot} = V_{dc,i} + V_{CES}. \tag{10}$$

As already known, due to the capacity ratio $C_{ES} >> C$ known from (5) $V_{dc,i} >> V_{CES}$ the voltage rise of $V_{dc,i}$ is significantly larger than the voltage rise of V_{CES}. This process ensures that the voltage $V_{dc,i}$ exceeds the upper rectification value $V_{dc,high}$ from t_1 onward.

C. Generator Operation

At t_2, the voltage $V_{dc,i}$ exceeds the parametrized threshold voltage of $V_{dc,CS}$ respectively the maximum allowed capacitor voltage $V_{dc,max}$, which causes the diode D_{by} to block. In consequence, the controlled current-source I_S becomes active and takes over the current, that previously flowed through the dc-bus capacitor C, which is illustrated by mode 3 of Fig. 6. Due to the overtake of the current the charging process of the energy-storage capacitor C_{ES} continues, while the voltage $V_{dc,i}$ is slightly decreased. This time interval is of particular importance for the dimensioning of the controlled current-source I_S considered in the Section IV-B. At time t_3, the voltage $V_{dc,i}$

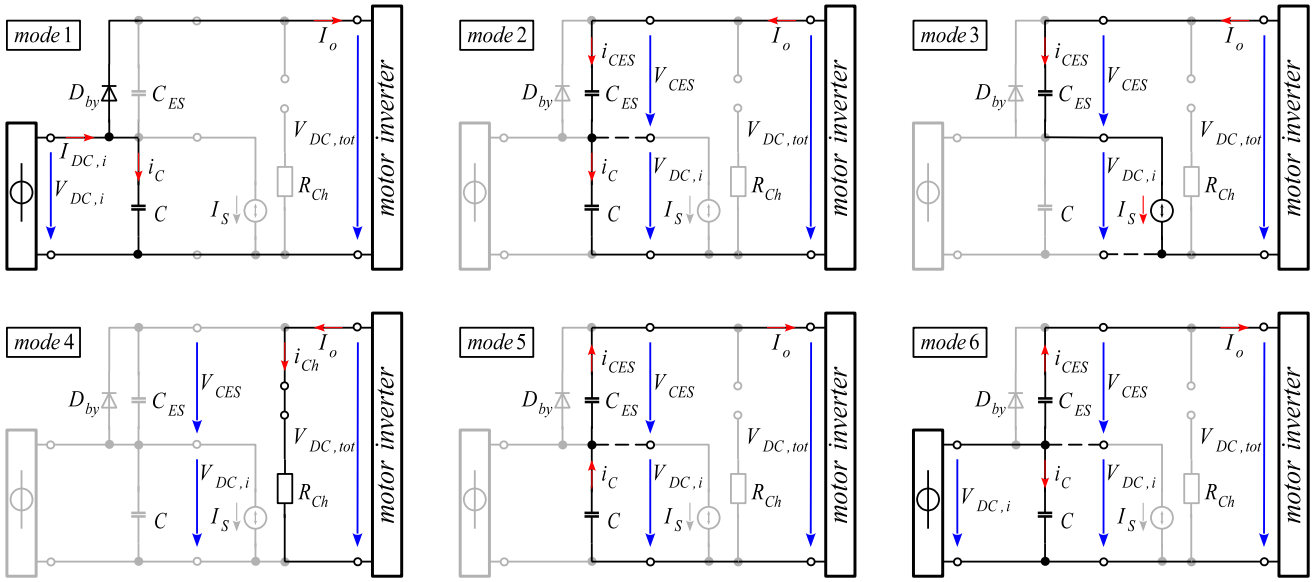

Fig. 6. Circuit modes for current-source-based energy-storage at DC-bus.

falls below the lower threshold voltage. In consequence, the controlled current-source I_S becomes temporarily inactive until $V_{\text{dc,i}}$ reaches the threshold voltage of $V_{\text{dc,CS}}$ again. This process is repeated several times, which corresponds to the behavior of a two-point control and regulates $V_{\text{dc,i}}$ to a constant level. It should be noted, that the controlled current-source I_S only becomes active in the time interval between t_2 and t_4 of generator operation.

At time t_4, the energy-storage capacitor C_{ES} is completely charged. The voltage V_{CES} at C_{ES} reaches the maximum allowed charging voltage $V_{\text{CES,max}}$. In consequence, the sum of both maximum allowed capacitor voltages $V_{\text{dc,tot,max}}$ is also reached by $V_{\text{dc,tot}}$. From this point on, the controlled current-source I_S becomes completely inactive. The energy that continues to be fed back into the circuit is converted into heat by the activation of the chopper-resistor R_{Ch} of Fig. 4, which is illustrated by mode 4 of Fig. 6.

D. Transition From Generator to Motor Operation

When the motor starts or restarts after recovery (generator operation), it is initially supplied via the upstream inverter with the energy stored in the two capacitors C and C_{ES} in the dc-bus. At time t_5, the motor is accelerated. Thus, the circuit switches back to motor operation and draws the power initially from the fully charged capacitors C_{ES} and C, as illustrated by mode 5 of Fig. 6. The dc-bus capacitor C releases its energy in the short period until time t_6. Due to $C << C_{\text{ES}}$ of (5), the voltage $V_{\text{dc,i}}$ drops significantly faster compared to V_{CES}. During this short time interval, the load current is drawn completely from the capacitors and thus from the stored energy.

At time t_6 the voltage $V_{\text{dc,i}}$ falls below the threshold value of the earlier mentioned upper rectification value $V_{\text{dc,high}}$ and is further stabilized by the grid. The upper rectification value $V_{\text{dc,high}}$ is well known physically as predetermined by the three-phase rectification. In consequence, the power transfer to the grid starts. This means that from this point in time the current is increasingly drawn from the grid to further discharge the energy storage capacitor C_{ES}, as can be seen in mode 6 of Fig. 6. The energy-storage's bypass-diode D_{by} is still blocked, since $V_{\text{CES}} > 0$ is applied.

At time t_7 the voltage V_{CES} reaches zero. Therefore, the load transfer to the grid is completed. The current-source-based energy-storage at the dc-bus returns to its initial state from t_0, which again corresponds to mode 1 of Fig. 6. With the complete transfer of the power draw to the grid, the forward voltage $V_{\text{TH,Dby}}$ of the bypass-diode D_{by} can be measured to $V_{\text{CES}} = V_{\text{TH,Dby}}$.

Having a look on the whole transition from generator to motor operation, the controlled current-source I_S becomes not active during the discharging of C_{ES} and C here. Regarding the state of the art technology with prior dc/dc conversion mentioned among others in [8] and [10], the energy has to pass through the dc/dc converter for a second time in transition from generator to motor operation (cf., left-pointing red arrow in Fig. 2). However, this is not the case here. The discharge of the capacitors follows directly and purely the physical relationships via the charge Q according to (6) and (7) without any additional energy flow through the controlled current-source I_S. Due to the fact, that the energy only has to pass the controlled current-source I_S once at generator operation, the cascading in terms of efficiency is eliminated. This is the main advantage of the current-source-based energy-storage at dc-bus, which improves the total efficiency.

IV. Dimensioning of the Current-Source-Based Energy-Storage at DC-Bus

The dimensioning of the current-source-based energy-storage at dc-bus is primarily based on two components. The first step involves calculating the energy storage capacity C_{ES} based on the

backfeed energy, which is described in detail in the following Section IV-A. The second step involves the dimensioning of the components of the controlled current-source I_S, which is described in detail in Section IV-B. This calculation is based on the specified charging voltage V_{CES}, which results in the output-side voltage $V_{\text{dc,tot}}$ according to (10).

It is important to note that the controlled current-source I_S is generally dimensioned to the previously calculated parameters of the energy storage capacitor C_{ES} regardless of its chosen topology. In other words, the energy storage capacitor is always dimensioned using the same procedure, independent of the circuit topology used for the controlled current-source I_S.

A. Energy Storage Capacitor

The total capacity of the energy-storage capacitor is calculated based on the backfeed energy coming from the load. Considering a braking motor as a load connected to the motor inverter, this behaves like a current source during the backfeeding process. For the braking duration t_{brake}, which starts at t_1 of Fig. 5, a negative dc-bus current $-I_o$ is fed back into the circuit.

The required capacity of the storage capacitor C_{ES} can be calculated using a simple charge balance. The charge Q_{backfeed} results from the charge integral of the magnitude of the negative current $-I_o$ during the braking time t_{brake} according to the following:

$$Q_{\text{backfeed}} = \int_0^{t_{\text{brake}}} |-I_o|\, dt. \tag{11}$$

This simplifies to the following:

$$Q_{\text{backfeed}} = |-I_o| \cdot t_{\text{brake}}. \tag{12}$$

The possible charge of the storage capacitor Q_{CES} is composed by the maximum allowed charging voltage $V_{\text{CES}} = V_{\text{CES,max}}$ of the capacitor and its capacity C_{ES} according to the following:

$$Q_{\text{CES}} = C_{\text{ES}} \cdot V_{\text{CES}}. \tag{13}$$

As already described, the energy-storage capacitor can be relayed with supercaps, ultracaps, EDLCs, or related technologies with low voltage-strengths, as described in [7], [11], and [14]. The charging voltage V_{CES} is determined individually based on the capacitor technology used. Since the charging voltage of these technologies is generally lower, it can also be useful to form a stack. This arrangement offers the advantage of an increased charging voltage, but the total capacity will be reduced due to the series connection. The value of V_{CES} is included into the total output voltage $V_{\text{dc,tot}}$, which is required for the subsequent dimensioning of the controlled current-source I_S. Taking this aspect into account, the value of V_{CES} can be varied slightly within certain limits depending on the dimensioning.

The energy storage capacitor C_{ES} is designed to temporarily store the full amount of the backfeed energy. Accordingly, the two charges Q_{backfeed} and Q_{CES} can be equalized to form the charge balance of

$$Q_{\text{CES}} = Q_{\text{backfeed}}. \tag{14}$$

By inserting (12) and 13 into the charge balance of (14), (15) is obtained for calculating the capacitance C_{ES}

$$C_{\text{ES}} = \frac{|-I_o| \cdot t_{\text{brake}}}{V_{\text{CES}}}. \tag{15}$$

This calculation applies regardless of how and with which topology the controlled current-source I_S will be realized in Section IV-B.

Finally, the calculated value from (15) must be verified according to the criterion $C_{\text{ES}} >> C$ described in (5). Typically, the capacitance of the dc-bus capacitor C is determined according to the usual values for a B6 rectifier. If the condition of (5) is met, the current-source can be dimensioned. If this criterion is not met, the capacity C must either be reduced or C_{ES} must be increased accordingly. For the same charging voltage V_{CES} this only increases the amount of storable energy which has no direct impact on the subsequent dimensioning of the controlled current-source I_S.

In general, it is important that the capacity ratio between the energy storage capacitor C_{ES} and the dc-bus capacitor C is not too small, but ideally not too large either. This is important for the short time period between t_1, i.e., the start of backfeeding process and the activation of the controlled current-source I_S at time t_2 of Fig. 5. Therefore, the criterion of (5) can also be reformulated into a ratio according to

$$C_{\text{ES}} = k \cdot C. \tag{16}$$

During the time interval between t_1 and t_2 the two capacitors C and C_{ES} are charge proportionally to their applied voltages $V_{\text{dc,i}}$ and V_{CES}, respectively. This means that if C_{ES} is a factor of k larger than C, C_{ES} will charge by a voltage k times lower than C in the same time interval. In practice, a ratio of $k = 10$ has proven to be very suitable. If the voltage $V_{\text{dc,i}}$ across C changes by $\Delta V_{\text{dc,i}} = 100\,\text{V}$ in the time period between t_1 and t_2, V_{CES} will change by $\Delta V_{\text{CES}} = 10\,\text{V}$.

B. Realization of the Controlled Current-Source

Previously, the controlled current-source I_S was considered as the entire element of the energy-storage circuit. In practice, however, this current-source corresponds to a dc/dc converter. In the simplest case, which will also be considered in the following, this can be implemented as a normal boost converter. At this point, however, the use of other, more complex current-source circuit principles is also conceivable. As an example, the SEPIC- or ZETA-converter should be mentioned here, which are described in [9]. Further the isolated variants up to resonant switching topologies of boost converters, such as LLC converters, which are described in [23] and [24], are also conceivable. Fig. 7 shows the controlled current-source I_S in the form of a boost converter implemented into Fig. 4.

Another possible circuit variant is the implementation of the controlled current-source I_S by a H-bridge, as shown in Fig. 8.

This topology offers several advantages and disadvantages. The main advantage of the topology concerns the peak currents that initially occur when the controlled current-source I_S becomes activated. As known in general for a boost-converter,

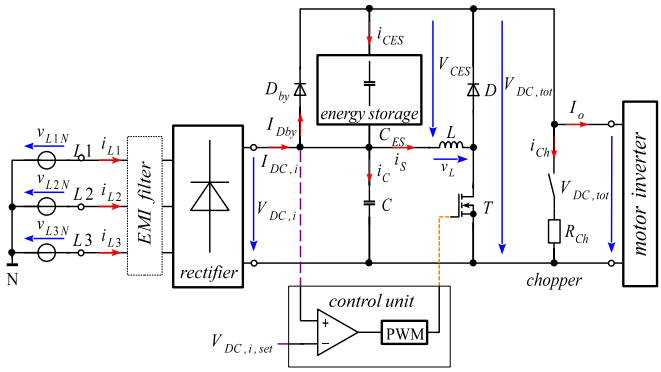

Fig. 7. Boost converter implemented into the current-source-based energy-storage topology in the DC-bus.

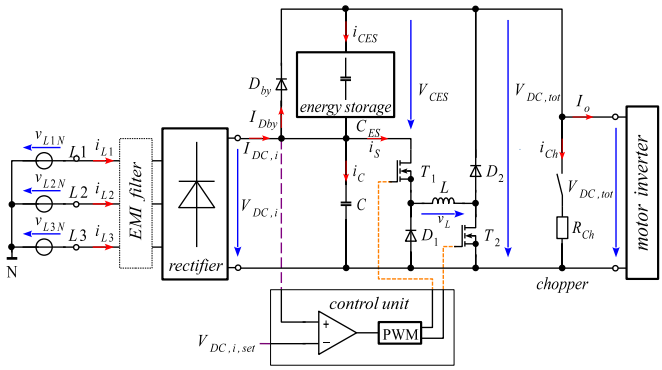

Fig. 8. H-bridge topology implemented into the current-source-based energy-storage topology in the DC-bus.

the voltage–time surface of the inductor voltage results in the typical inductor currents shapes, which can be seen qualitatively in Fig. 11. For the boost-converter of Fig. 7 the inductor voltage v_L results from the voltages $V_{\text{dc,tot}}$, $V_{\text{dc,i}}$ and V_{CES}. During the freewheeling interval of the boost converter, V_{CES} is applied at the inductor L. However, this voltage is very small before the activation of the controlled current-source I_S. This is conditioned by the capacitance ratio k between the capacitors C_{ES} and C according to (16), as explained in Section IV-A. The energy storage capacitor C_{ES} initially charges very slowly. This small voltage, in turn, prevents the decrease of the inductor current i_L, which subsequently leads to high peak currents. To avoid these high peak currents in the high power application, a soft start algorithm for the boost converter is required and therefore used, which is described in Section VI. The diode D_1 of the H-bridge offers a circuit alternative, whereby the inductor voltage v_L is pinned to the negative potential of $V_{\text{dc,i}}$ during the freewheeling interval. The negative voltage applied at the inductor L this way is significantly larger than V_{CES} and thus accelerates the current decrease of i_L. However, since the capacitor C must not be short-circuited during the freewheeling interval, the additional switch T_1 above the diode D_1 is required. This ultimately leads to the H-bridge topology of Fig. 8, where by T_1 is switched on in parallel with T_2 during the enable time.

Of course, each additional device reduces the total efficiency and increases costs, which are the main disadvantages of this H-bridge topology. Therefore, the advantages of improved

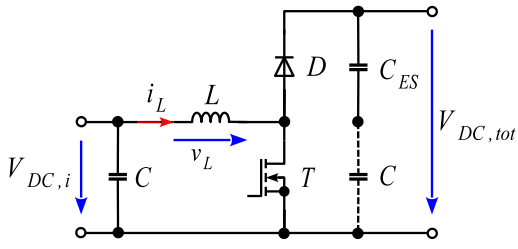

Fig. 9. Extracted and abstracted model of the implemented boost converter.

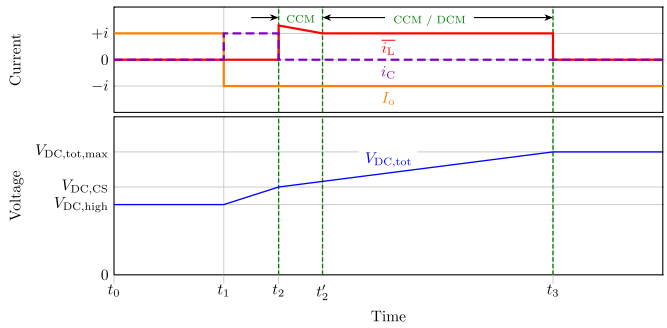

Fig. 10. Voltage and current signals for transition from motor to generator operation.

functionality must always be carefully weighed against the disadvantages of the reduced efficiency and the higher costs, which is the main aspect here. However, the most cost-efficient topology that can be implemented for the controlled current-source I_S is the boost converter of Fig. 7, which will be examined in more detail in the following.

As already mentioned, at motor operation, the controlled current-source I_S and thereby the boost converter is inactive. The consideration of the model, physical variables and the dimensioning of the boost converter are therefore carried out in generator operation. For this purpose, all components are considered ideal and therefore loss-free. The first step corresponds to extract a model of the boost converter from the entire circuit shown in Fig. 7. As can be seen from that topology, the boost converter set up the voltage level from $V_{\text{dc,i}}$ to $V_{\text{dc,tot}}$, which results in the abstract model of Fig. 9. It should be noted here that the correct representation of the components in terms of the voltages $V_{\text{dc,i}}$ and $V_{\text{dc,tot}}$ results in a double representation of the capacitor C, which is referred as C'.

For the dimensioning of the boost converter, a detailed consideration of the backfeeding cycle is considered. This corresponds to the time interval from t_0 to t_3 in Fig. 5. The voltage and current signals can be modeled as linear signals due to short time period, which simplifies the subsequent calculations. Fig. 10 shows the modeled dc-bus voltages $V_{\text{dc,i}}$ and $V_{\text{dc,tot}}$, the capacitor current i_C as well as the specific voltage levels that are important for the operation and dimensioning of the boost converter. Further, it is determined that the energy-storage capacitor C_{ES} is completely charged after the considered backfeeding cycle at t_3, which leads to $V_{\text{CES}} = V_{\text{CES,max}}$.

The current $\bar{i}_L$ must be considered separately here. When considering the boost converter as the current-source I_S according to Fig. 4, its current was defined as i_S. With respect to the boost converter according to the model of Fig. 9 the current

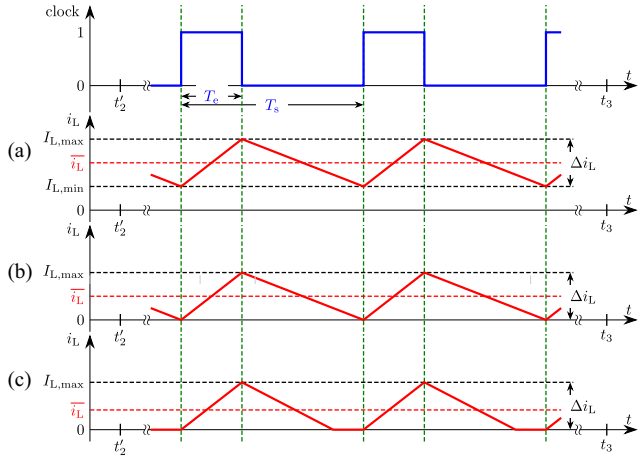

Fig. 11. Current-shapes i_L of a switching-cycle for the inductor (a) completely in CCM. (b) Boundary between CCM and DCM. (c) Completely in DCM.

i_S corresponds to the mean value of the inductor current $\bar{i}_L$ according to the following:

$$i_S = \bar{i}_L. \tag{17}$$

The possible operating modes of a boost converter in form of the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) must also be put into context. Since V_{CES} initially corresponds to $V_{\text{CES}} = 0$ and thus $V_{\text{dc,i}} \approx V_{\text{dc,tot}}$, until time t_2 there is in theory no voltage difference between the input and output of the boost converter. This initially poses a problem for the startup of the boost converter. In practice, however, there is a slight voltage difference due to the forward voltage $V_{\text{TH,Dby}}$ of the energy-storage's bypass-diode D_{by}, so that $V_{\text{CES}} = V_{\text{TH,Dby}}$. This is sufficient for the boost converter to startup. However, the small voltage difference initially after t_2 causes the boost converter first to operate in CCM with the high peak currents. Corresponding to the the average value of the inductor–current $\bar{i}_L$ the current shape of i_L is illustrated for a few switching-cycles in the time interval from t_2 to $t_2\prime$ in Fig. 11(a). The CCM with high peak-currents leads to the initial overshoot after t_2 of the average value $\bar{i}_L$ in Fig. 10. Gradually, the voltage $V_{\text{dc,tot}}$ at the output of the boost converter rises up, so that the peak currents of i_L and thus the average value $\bar{i}_L$ become smaller. This leads to increasingly moving the operating point of the boost converter toward the boundary between CCM and DCM. At $t_2\prime$ the initial overshoot is subsided and $\bar{i}_L$ is constant from this point on until time t_3. During this time interval, the operation mode of the boost converter depends on its dimensioning. It can either continue to be operated in CCM, as already illustrated in Fig. 11(a), at the boundary between the two operation modes, as illustrated in Fig. 11(b) or completely in DCM, as illustrated in Fig. 11(c).

Both operating modes have their advantages and disadvantages. In CCM, the control law is known to be load-independent, which simplifies the control. On the other hand, large peak currents occur, which poses a problem with regard to the limits for the semiconductor components. Further, both the switch's turn-ON and turn-OFF processes are lossy, which in turn reduces the efficiency. In DCM, the control law is load-dependent and thus nonlinear. However, the transistor's turn-ON process is lossless; only the turn-OFF process is lossy, which leads to better efficiency compared to CCM. As a compromise, it is recommended to dimension the boost converter at the boundary between CCM and DCM. This way, the calculation of the duty-cycle D is based on the control law for the CCM, while the advantages of DCM are also taken into account. Especially for applications with higher power, it is recommended to operate the circuit in steady state fully in DCM. The higher the power, the further the operating point should be shifted into the DCM. This leads to a rapid transition of the operating point from CCM to DCM during startup, which reduces the peak currents at the startup.

In order to dimension the boost converter at the boundary between CCM and DCM, the average of the inductor–current $\bar{i}_L$ must be set exactly depending on the capacitor–voltages $V_{\text{dc,i}}$ and V_{CES} in generator operation this way, that the condition $i_C = 0$ at t_2 according to Fig. 5 is maintained. This leads to $\Delta V_{\text{dc,i}} = 0$, so $V_{\text{dc,i}}$ is constant. Taking into account the relationships from (9), the total power $P_{\text{dc,tot}}$, which corresponds to the backfeed power P_o, converted in total in both capacitors C, can be calculated with (18) by including

$$P_{\text{dc,tot}} = P_o = V_{\text{dc,tot}} \cdot I_o = (V_{\text{dc,i}} + V_{\text{CES}}) \cdot I_o. \tag{18}$$

In consequence the total power $P_{\text{dc,tot}}$ can be divided into the two powers, $P_{\text{dc,i}}$, which is converted at C and P_{CES}, which is converted at C_{ES}, according to the following:

$$P_{\text{dc,tot}} = P_{\text{dc,i}} + P_{\text{CES}} = V_{\text{dc,i}} \cdot I_o + V_{\text{CES}} \cdot I_o. \tag{19}$$

At t_2 the power $P_{\text{dc,i}}$, that would have been converted at capacitor C, is taken over by the boost converter (cf., controlled current-source I_S from Fig. 4), which is why this power is referred to P_{boost} in the following. The power P_{boost} results from the voltage V_{CES} applied at the energy-storage C_{ES} and the mean value $\bar{i}_L = I_S$ of the inductor–current to

$$P_{\text{boost}} = V_{\text{CES}} \cdot I_S. \tag{20}$$

For t_2, the power balance shown in (21) can be drawn up for the powers $P_{\text{dc,i}} = P_{\text{boost}}$

$$V_{\text{dci}} \cdot I_o = V_{\text{CES}} \cdot I_S. \tag{21}$$

Changing (21) to the current I_S results in the control law of

$$I_S = I_o \cdot \frac{V_{\text{dc,i}}}{V_{\text{CES}}}. \tag{22}$$

Due to the fact, that $V_{\text{CES}} \approx 0$ applies at the start of the boost converter operation, it is foreseeable with constant backfeed power, that the inductor–current i_L of the boost converter reaches its maximum $I_{L,\text{max}}$ a little after t_2. This operating case is particularly important for dimensioning the inductance L of the boost converter. To dimension the inductance value L, first it is necessary to calculate the duty-cycle D for a given switching-frequency f_S. As already explained, the boost converter is operated at the boundary between CCM and DCM with respect to the maximum possible backfeed current for $\bar{i}_L = I_S = -I_o$. The duty-cycle D can be calculated with the generally

known control law of

$$\frac{V_{\mathrm{dc,tot}}}{V_{\mathrm{dc,i}}} = \frac{1}{1-D}. \tag{23}$$

D is as generally known the relation of the enable time T_e of the switch T to the period duration T_S, which are visible in Fig. 11. For dimensioning, always the largest possible voltage difference between input and output voltages must always be assumed. The input-side voltage $V_{\mathrm{dc,i}}$ therefore corresponds to the maximum allowed voltage $V_{\mathrm{dc,i,max}}$, at which the controlled current-source I_S is initially activated. The voltage $V_{\mathrm{dc,tot}}$ on the output-side corresponds to the maximum allowed voltage of $V_{\mathrm{dc,tot,max}}$ in the dc-bus before the chopper-resistor becomes active. Rearranged from (23), this results in the maximum duty-cycle D_{max} in

$$D_{\mathrm{max}} = \frac{T_e}{T_S} = 1 - \frac{V_{\mathrm{dc,i,max}}}{V_{\mathrm{dc,tot,max}}}. \tag{24}$$

The value of the inductance L can be calculated with (25) using the maximum duty-cycle D_{max} of (24) and the average value of the inductor–current $\bar{i}_{Lg}$ at the boundary between CCM and DCM, which corresponds to I_S ($\bar{i}_L = I_S$)

$$L = \frac{1}{2 \cdot I_S} \cdot D_{\mathrm{max}} \cdot T_S \cdot V_{\mathrm{dc,i,max}}. \tag{25}$$

V. Measurement Evaluation of the Current-Source-Based Energy-Storage at DC-Bus

The functional principle of the new current-source-based energy-storage at dc-bus will be illustrated using the measurements carried out in the following. The voltage and current shapes were recorded with an oscilloscope and exported via csv-files in order to verify those comparatively using suitable simulations. These simulations are carried out with LT-Spice.

Since this article is primary intended to illustrate and prove the functional principle itself, the measurements are done using only safety low-voltages. There are several more reasons for using only safety low-voltages. For the development of the first prototype, the focus was to measure the occurring voltages and currents as simply and, above all, safely as possible. The main reason is consequently to eliminate the risk of electric shock for students involved in this development. Also the extent of damage to components and circuits can be reduced using only low voltage. Using low voltages only corresponds to a downscaling of the measurements; there are no functional disadvantages to high voltages. However, the situation is different when it comes to the efficiencies. At low voltage the conduction losses of the semiconductor components are much more important in percentage terms. In consequence, this results in a reduced efficiency, which is not fully meaningful, but at least indicates a trend. Due to the fact that the controlled current-source I_S becomes only active at generator operation for charging C_{ES} and therefore the energy have to pass it once, it can be expected that the total efficiency of the system will be better than with the state-of-the-art technology with prior dc/dc conversion mentioned among others in [8] and [10].

The measurements are made using the setup shown in the block diagram of Fig. 12. This contains a low-voltage prototype of the current-source-based energy-storage for evaluation, which can be seen in Fig. 13. The supply of the prototype is provided

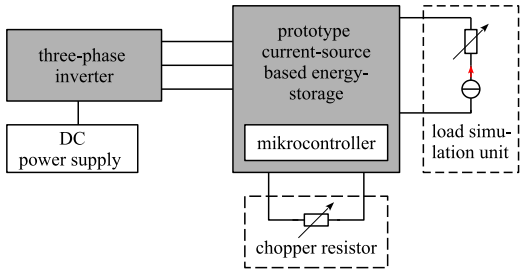

Fig. 12. Measurement setup for the low-voltage prototype.

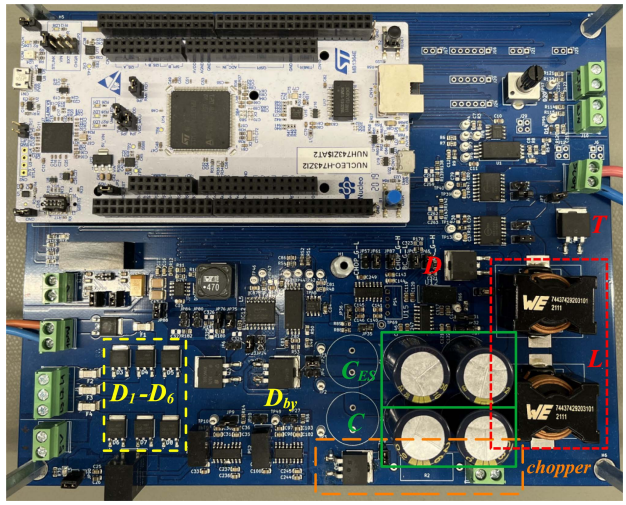

Fig. 13. Low-voltage prototype of the current-source-based energy-storage at DC-bus.

by a three-phase inverter with $3 \times 12\,\mathrm{V_{rms}}$ ac. The output-side filtering of the three-phase inverter signals ensures conditions that are equivalent to the real grid with regard to the network impedance. This three-phase inverter, in turn, is supplied with a dc-voltage of 24 V by a standard laboratory power supply. The grid voltages of the inverter would be rectified by a conventional B6-diode-rectifier on the circuit board of the current-source-based energy-storage, which entails corresponding conduction losses.

For the load of the setup a so-called load simulation unit is used. When the current-source-based energy-storage circuit is in motor operation, i.e., energy is transferred from the grid to this unit, it works as a standard ohmic load, which is also referred to as a sink. In generator operation, this unit automatically becomes a source by increasing the output voltage, which corresponds to the total dc-bus voltage $V_{\mathrm{dc,tot}}$. This reverses the current flow to $-I_o$, which corresponds to the backfeed current (generator operation).

The main components and parameters of the low-voltage prototype of the current-source-based energy-storage, which are indicated in Fig. 13, are listed in Table I. For the calculation of the capacity C_{ES} of the energy-storage, a braking time of $t_{\mathrm{brake}} = 60\,\mathrm{ms}$ is specified. The maximum allowed charging voltage is set to $V_{\mathrm{CES,max}} = 40\,\mathrm{V}$. With (15), a capacity of $C_{\mathrm{ES}} = 15000\ \mu\mathrm{F}$ is calculated. For the use of E-series capacitors a value of $C_{\mathrm{ES}} = 16400\ \mu\mathrm{F}$ is chosen. The capacity of the dc-bus capacitor C is set to 10 % of the capacity of C_{ES}, i.e.,

TABLE I
PARAMETER AND COMPONENTS OF THE LOW-VOLTAGE PROTOTYPE

Parameters and components		Value
maximum power (nominal)	$P_{\max}$	600 W
maximal permissible dc-bus voltage	$V_{\mathrm{dc,tot,max}}$	60 V
maximum allowed charging voltage	$V_{\mathrm{CES,max}}$	40 V
maximal backfeed current	$-I_o$	10 A
energy-storage capacitor	C_{ES}	16 400 µF
Dc-bus capacitor	C	1640 µF
switching frequency	f_S	10 kHz
duty-cycle	$D_{\max}$	0.6
enable time	T_e	60 µs
switch (MOSFET)	T	SiHB065N60E
freewheel / bypass-diodes (Schottky)	D, D_{by}	V40DM100C
rectifier-diodes (Schottky)	D_1–D_6	MBRD20100CT
inductors	L	72 µH

$C = 1640\,\mu\mathrm{F}$, according to the ripple of the input-side dc-bus voltage $V_{\mathrm{dc,i}}$. With this value of C the criterion of (5) is met.

The boost converter of the current-source is dimensioned based on the maximum convertible power $P_{\max}$, which is set to the nominal power, and is composed of the maximum permissible voltage $V_{\mathrm{dc,tot,max}}$ in the dc-bus and the maximum backfeed current $-I_o$. The prototype is operated at a switching frequency $f_S = 10\,\mathrm{kHz}$. The duty-cycle $D_{\max}$ calculates according to (24) with $V_{\mathrm{dc,i,max}} = 24\,\mathrm{V}$ here and $V_{\mathrm{dc,tot,max}} = 60\,\mathrm{V}$ to $D_{\max} = 0.6$. This results in a maximum enable time $T_e = 60\,\mu\mathrm{s}$ of the switch T. The inductance L of the boost converter results in $L = 72\,\mu\mathrm{H}$ according to (25). As is well known with inductors in practice, thermal-related saturation effects occurring, which lead to a reduction of the inductance value due to heating. Due to these saturation effects, the inductance value L of the boost converter must be dimensioned much larger in this specific case. Based on the data sheets, two inductors, each with $L' = 100\,\mu\mathrm{H}$ connected in series, are chosen in order to maintain the calculated inductance values for the existing currents and taking saturation into account. The two diodes D_{by} and D in Fig. 7 are realized with Schottky-diodes. For future implementation in the kilowatt range it is recommended to realize these two diodes as switched diodes using transistors, since their conduction losses are inherently lower.

For the following measurements and simulations, the desired operation modes and their transitions of the current-source-based energy-storage are considered. Figs. 14 and 15 show the simulated (dashed lines) and measured (solid lines) input-side grid-voltage v_{L1N} and corresponding line currents i_{L1}, i_{L2}, i_{L3}, the dc-bus voltages $V_{\mathrm{dc,i}}$ applied at C, V_{CES} applied at the energy-storage capacitor C_{ES} and the total dc-bus voltage $V_{\mathrm{dc,tot}}$ at the output of the circuit as well as the chopper- and output-currents i_{Ch} and I_o. The times t_1 to t_7 are based on the simulated signal shapes.

A. Simulation and Measurements of Transition From Motor to Generator Operation

The characteristic curves shown in Fig. 14 illustrate the intended application of the principle in the transition from motor to generator operation. Both the measurement and the simulations show comparable results. Before time t_1 the circuit initially stays

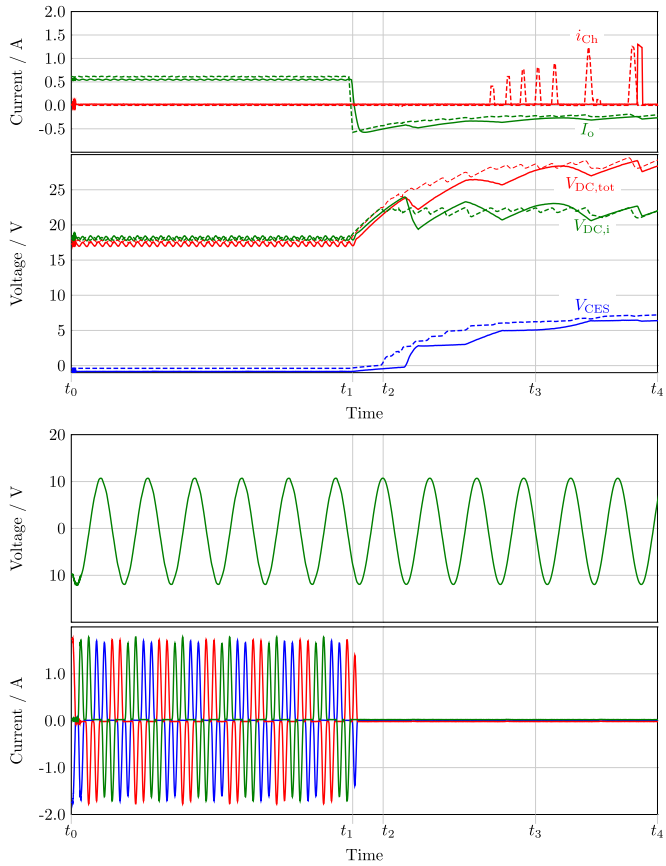

Fig. 14. Transition motor to generator operation: Simulated (dashed lines) and measured (solid lines) grid-voltage v_{L1N}, corresponding line currents i_{L1}, i_{L2}, i_{L3}, DC-bus side voltages $V_{\mathrm{dc,i}}$, V_{CES}, and $V_{\mathrm{dc,tot}}$, and corresponding currents I_o and i_{Ch} of the low-voltage prototype.

in motor operation. The current to the load bypasses the capacitor C_{ES} with the diode D_{by}.

At time t_1 the output-current I_o becomes negative, the load simulation unit and thus the entire current-source-based energy-storage circuit switches to generator operation. Due to the blocking of diode D_{by}, the line currents i_{L1}, i_{L2}, and i_{L3} become zero.

After time t_2 the input-side dc-bus voltage $V_{\mathrm{dc,i}}$ reaches the threshold voltage $V_{\mathrm{dc,CS}}$, which activates the boost converter of the controlled current-source I_S. This takes over the current from the capacitor C, whereby the capacitor C_{ES} continues to be charged. This results in $V_{\mathrm{dc,i}}$ remaining at a nearly constant voltage level, while the voltage V_{CES} applied at the energy-storage capacitor, and further $V_{\mathrm{dc,tot}}$, continues to increase in the simulation. The individual pulses in the voltage curve of $V_{\mathrm{dc,i}}$ and in consequence of $V_{\mathrm{dc,tot}}$ in Fig. 14 result from the implemented type of control of the boost converter in combination with the internal hysteresis of the microcontroller input. This was reproduced accordingly in the simulation. Ideally, the voltages and current shapes from measurement and simulation would correspond to the ideal shapes from Fig. 5.

At time t_3 the mainly charging of the energy-storage capacitor is completed, which results in V_{CES} and $V_{\mathrm{dc,tot}}$ remaining at a constant level in the simulation. From this point on the boost converter of the controlled current-source I_S becomes inactive.

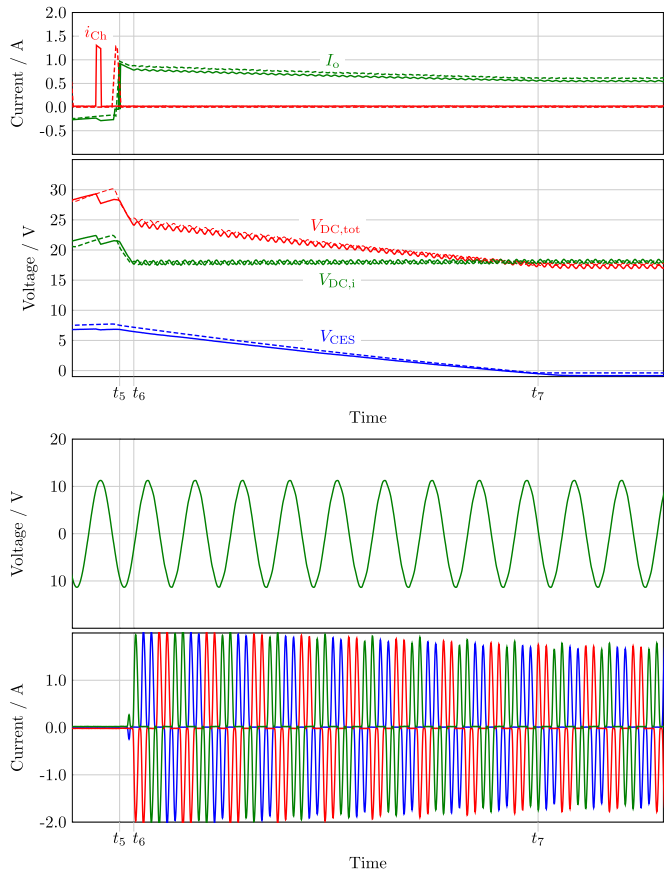

Fig. 15. Transition generator to motor operation: Simulated (dashed lines) and measured (solid lines) grid-voltage v_{L1N}, corresponding line currents i_{L1}, i_{L2}, i_{L3}, DC-bus side voltages $V_{dc,i}$, V_{CES}, and $V_{dc,tot}$, and corresponding currents I_o and i_{Ch} of the low-voltage prototype.

However, since the load continues to feed energy back into the dc-bus, the voltage V_{CES} in the measurement would continue to rise. This further voltage increase is prevented by activating the chopper-resistor R_{Ch}. This is also done via individual pulses comparable to the boost converter. But the activation of the chopper-resistor will cause a pendulum effect. Due to the reduction of the input-side dc-bus voltage $V_{dc,i}$ also $V_{dc,tot}$ is reduced. As a result of that, C_{ES} is repeatedly recharged for a short time until the voltage $V_{dc,tot}$ exceeds the threshold value again. This leads to the slow rise of V_{CES} after t_3 until t_4. This effect could be prevented, in which the algorithms for activating the boost converter and the chopper are implemented differently in the software, which represents an aspect for the further development of this concept.

B. Simulation and Measurements of Transition From Generator to Motor Operation

The characteristic curves shown in Fig. 15 illustrate the intended application of the principle in the transition from generator to motor operation. Both the measurement and the simulations show comparable results again.

Continued at a time after t_4 (cf., Fig. 14), at time t_5 the output-current I_o becomes positive again, the load simulation unit and thus the entire current-source-based energy-storage circuit switches back to motor operation. As a consequence, both capacitors C_{ES} and C begin to discharge directly in proportion to their capacities in accordance with the applicable physical relations. As intended for this principle, the boost converter of the controlled current-source I_S remains inactive, the energy does not pass it a second time. The discharging results in the decreasing voltages of V_{CES} as well as $V_{dc,i}$ and also $V_{dc,tot}$. In the time interval up to time t_6, the energy flowing to the load in form of the positive output-current I_o comes entirely from the capacitor C_{ES} of the energy-storage circuit, no currents are drawn from the grid during this time interval, as explained in Section III-D.

At time t_6, the capacitor C is discharged to its nominal voltage level of $V_{dc,i}$. In consequence the B6-rectification becomes active again, which results in the current draw of the line currents i_{L1}, i_{L2}, i_{L3}. As can be seen, the line currents are initially somewhat larger in the simulation as well as in the measurements immediately after t_6, while their amplitudes decrease slightly over time. This trend results from the continuous discharge of the capacitor C_{ES} until time t_7. Since the capacitor C cannot be further discharged, the current for the discharging of the capacitor C_{ES} must flow from the grid.

At time t_7, the capacitor C_{ES} is completely discharged, so that V_{CES} reaches zero volts. In consequence, the diode D_{by} becomes active again, the current to the load bypasses the capacitor C_{ES} from this point on again. This corresponds to the initial state with motor operation before time t_1. Here is a small time difference between measurement and simulation when reaching $V_{CES} = 0$ after time t_7. This results from the slightly longer discharge at the measurement due to a little decreased discharge current of the capacitor C_{ES}.

C. Efficiency Evaluation

In addition to the functional principle itself, an initial evaluation of the efficiency can also be carried out. As previously described, the boost converter only becomes active during the backfeeding for charging the energy-storage capacitor C_{ES}. Therefore, the efficiency of the boost converter η_{boost} and thus η_{store} from Fig. 4 essentially corresponds to the total efficiency η_{tot} according to (8). In consequence, η_{tot} can be determined by evaluating η_{boost}.

In general, the efficiency is determined in steady operation, i.e., in the time interval between $t_2\prime$ and t_3 of Fig. 10. For this purpose, the boost converter is extracted from the entire energy storage circuit. This applies to both the measurement on the low-voltage prototype and the simulation, whereby the boost converter is operated under the same conditions as in the previous measurements and simulations. At the low-voltage prototype the dc-bus is directly supplied by the voltage $V_{dc,i} = V_{dc,i,max}$, which is applied parallel to C, using an external voltage source. An adequate load is connected the the output. Further the duty cycle is set in such a way that exactly a power P_{out} is converted at the load which leads the input current I_S set in relation to the backfeeding of the real arrangement according to (22). At this point, it should be remembered that I_S corresponds to

TABLE II
EFFICIENCY COMPUTATION OF THE LOW-VOLTAGE PROTOTYPE

	Measurement	Simulation
input voltage $V_{\text{dc,i}}$	19.17 V	19.2 V
input current I_S	0.602 A	0.60 A
input power P_{in}	11.54 W	11.53 W
output voltage V_o	35.40 V	35.57 V
output current I_o	0.313 A	0.317 A
output power P_{out}	11.08 W	11.30 W
efficiency η_{boost}	96.01 %	98.00 %

the average value of the inductor current i_L [cf., (17)]. This procedure applies analogous for the simulation.

To determine the efficiency, the applied input voltage $V_{\text{dc,i}}$, the associated input current I_S, the output voltage V_o, and the output current I_o of the boost converter are recorded both in measurement and simulation. The associated input power P_{in}, output power P_{out}, and the resulting efficiency are computed and presented in Table II. For the measurement the efficiency is $\eta_{\text{boost,meas}} = 96.01\,\%$, while for the simulation it is $\eta_{\text{boost,sim}} = 98.00\,\%$. Taking into account that the backfeeding energy only has to pass through the power source once during the charge-process of the capacitors, η_{boost} corresponds to η_{store} and thus ideally to the total efficiency η_{tot}. In practice, however, the circuit components outside the boost converter, such as the capacitors themselves and other parasitic effects, must also be put into context. The bypass-diode D_{by} requires a somewhat separate consideration with regard to efficiency. The efficiency η_{tot} refers to the energy storage, i.e., to a load cycle itself. This includes the backfeeding from the load, the charging of the capacitor C_{ES}, the subsequent discharge of the capacitor, and the transfer of the energy to the load during the reacceleration. Throughout the entire load cycle this diode is inactive and therefore does not represent a loss factor.

D. Comparison Between Simulations and Measurements

As can be seen in the Figs. 14 and 15, there is a difference in the positions and widths of the current-pulses between the simulated and measured chopper-current i_{Ch}. This effect is comparable to the individual pulses in the voltage curve of $V_{\text{dc,i}}$ in Fig. 14 and results analogous to that from the implemented type of control of the chopper, in combination with the internal hysteresis of the microcontroller-input. Although this hysteresis was reproduced accordingly in the simulations, but is is really difficult to determine an exact value due to tolerances in the recording and the measurement itself. Ideally, the chopper-current shapes from measurement and simulation should correspond to the ideal shape from Fig. 5. In addition to the effects already explained, there are still further small deviations between simulation results and measurement results although the corresponding models of the used semiconductor devices were implemented into the simulation. These deviations are caused by the fact, that not all effects that occur in the real hardware can be included into the simulation. These are especially the trace resistances parasitic inductive and capacitive influences of the layout, such as small trace inductances, small trace resistances or small capacities.

TABLE III
PARAMETER AND COMPONENTS OF THE SIMULATED MAINS-VOLTAGE PROTOTYPE

Parameters & Components		Value
maximum power (nominal)	P_{max}	6 kW
maximal permissible dc-bus voltage	$V_{\text{dc,tot,max}}$	800 V
maximum allowed charging voltage	$V_{\text{CES,max}}$	200 V
maximal backfeed current	$-I_o$	7.5 A
energy-storage capacitor	C_{ES}	18 800 µF
Dc-bus capacitor	C	1640 µF
switching frequency	f_S	100 kHz
duty-cycle	D_{max}	0.25
enable time	T_e	2.5 µs
switch (MOSFET)	T	IMW120R014M1H
freewheel / bypass-diodes (Schottky)	D, D_{by}	IDWD40G120C5
rectifier-diodes (Schottky)	D_1–D_6	IDWD40G120C5
inductors	L	33.3 µH

This fact is also reflected by the difference of the efficiencies between measurement and simulation. The lower efficiency value, which was determined at the measurement, results from the conduction losses of the semiconductor components, especially for the used diode. This confirms the initial statement in this regard at the beginning of Section V. A further improvement of the efficiency can also be achieved in the low-voltage range by replacing the diode D of the boost converter in Fig. 4 with a switched diode using a transistor. Even though this increases the costs slightly, it is worthwhile in terms of the efficiency improvement. However, when operating with mains voltage, the influences of the earlier described parasites become quite small in terms of percentage. This automatically improves the efficiency in the higher power range. Further, the cascading in terms of efficiency is eliminated in general, since the backfeeding energy only has to pass through the power source once during the charge-process of the capacitors. Finally, it can be summarized that the newly proposed current-source-based energy-storage principle fulfills its intended function well.

VI. EVIDENCE OF THE SCALABILITY TO A MAINS-VOLTAGE PROTOTYPE IN THE KILOWATT RANGE

Finally, the scalability of the new topology to a mains-voltage prototype in the kilowatt range will be demonstrated based on the results of the low-voltage prototype. For this purpose, a further simulation is conducted.

The specification and the main components parameters of the simulated prototype in the kilowatt range are listed in Table III. For the calculation of the capacity C_{ES} of the energy-storage in the kilowatt range, a relatively long braking time of $t_{\text{brake}} = 350\,\text{ms}$ is specified. The maximum allowed charging voltage is set to $V_{\text{CES,max}} = 200\,\text{V}$. With (15), a capacity of $C_{\text{ES}} = 13125\ \mu\text{F}$ is calculated. For the use of E-series capacitors and taking a reserve into account, a value of $C_{\text{ES}} = 18800\,\mu\text{F}$ is chosen. The capacity of the dc-bus capacitor C is left to $C = 1640\,\mu\text{F}$, which further meets the criterion of (5).

The boost converter of the current-source is dimensioned on the maximum convertible power of $P_{\text{max}} = 6\,\text{kW}$. The switching frequency f_S is increased by a factor of 10 compared to

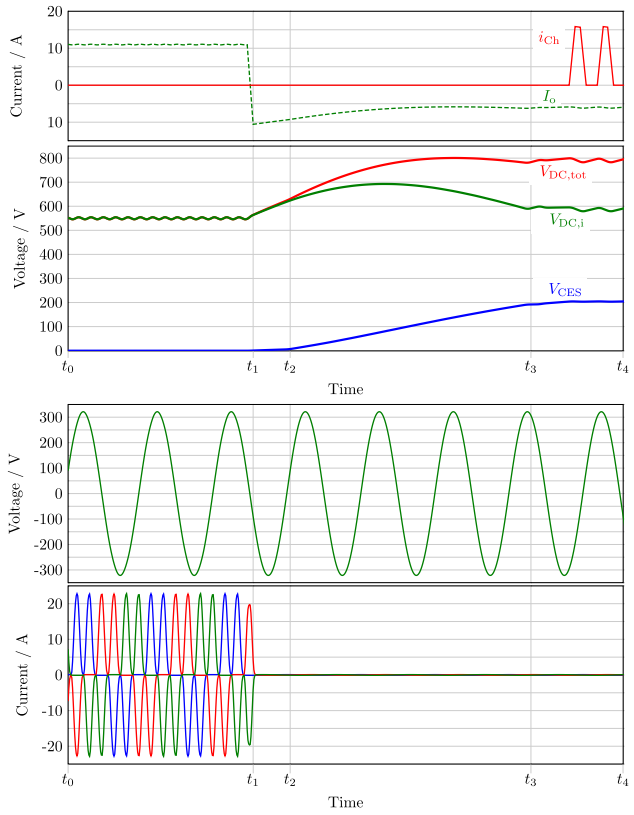

Fig. 16. Transition motor to generator operation: Simulated grid-voltage v_{L1N}, corresponding line currents i_{L1}, i_{L2}, i_{L3}, DC-bus side voltages $V_{dc,i}$, V_{CES}, and $V_{dc,tot}$, and corresponding currents I_o and i_{Ch} of the mains-voltage prototype in the kilowatt-range.

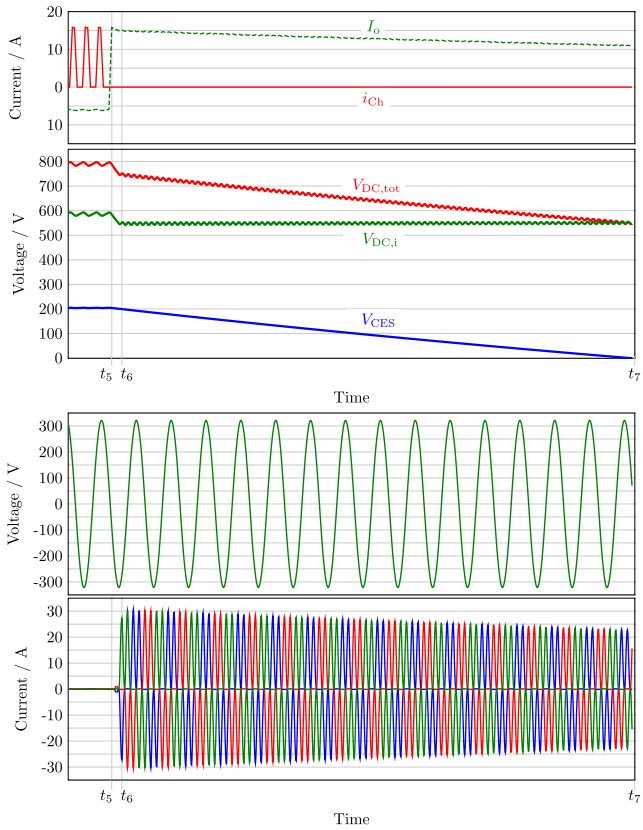

Fig. 17. Transition generator to motor operation: Simulated grid-voltage v_{L1N}, corresponding line currents i_{L1}, i_{L2}, i_{L3}, DC-bus side voltages $V_{dc,i}$, V_{CES}, and $V_{dc,tot}$, and corresponding currents I_o and i_{Ch} of the mains-voltage prototype in the kilowatt-range.

the low-voltage prototype in order to reduce the component dimensions for the higher voltage and power range. Therefore, a switching frequency of $f_S = 100\,\text{kHz}$ is chosen. The duty-cycle D_{max} calculates according to (24) with $V_{dc,i,max} = 600\,\text{V}$ and $V_{dc,tot,max} = 800\,\text{V}$ to $D_{max} = 0.25$. This is lower compared to the low-voltage prototype, since the difference between $V_{dc,i,max}$ and $V_{dc,tot,max}$, which corresponds to the value of $V_{CES} = 200\,\text{V}$, is correspondingly smaller here. With respect to $V_{dc,tot,max}$, semiconductors with voltage strengths of 1200 V must already be used here. The calculated duty-cycle results in a maximum enable time $T_e = 2.5\,\mu\text{s}$ of the switch T. The inductance L results in $L = 33.3\,\mu\text{H}$ according to (25). To minimize peak currents, a soft start algorithm is implemented, which ramps up the enable time from zero to the calculated value of T_e. With a direct enable without using the soft start algorithm, the peak currents would be far too high for all common power-semiconductors.

Comparable to the low-voltage prototype, Figs. 16 and 17 show the simulated input-side grid-voltage v_{L1N}, the corresponding line currents i_{L1}, i_{L2}, i_{L3}, the dc-bus voltages $V_{dc,i}$ applied at C, V_{CES} applied at the energy-storage capacitor C_{ES} and the total dc-bus voltage $V_{dc,tot}$ at the output of the circuit as well as the chopper- and output-currents i_{Ch} and I_o. To confirm the scalability, the voltage and current shapes of the Figs. 16 and 17 are to be compared in total with the Figs. 14 and 15 from the low-voltage prototype. As can be seen, the voltage and current shapes of the simulated mains-voltage prototype correspond in general to the voltage and current shapes of the low-voltage prototype.

However, between times t_2 and t_3 the shapes of $V_{dc,i}$, V_{CES}, and accordingly $V_{dc,tot}$ show a deviation compared to the low-voltage prototype. The voltage $V_{dc,i}$ rises for a much longer time and continues until it decreases again, V_{CES} does not rise gradually as in Fig. 14, here it follows a linear increase. This behavior can be explained by the implemented soft start. Due to the initially very short enable time T_e of the switch T, the capacitor C_{ES} is initially charged very slowly. In consequence, with continued backfeeding, this leads to an increase of $V_{dc,i}$. Since the capacitor C is designed for a voltage of 900 V by a series-connection, this increase is tolerable. Due to the delayed startup of the boost-converter, respectively the controlled current-source I_S, the voltage $V_{dc,i}$ initially falls below the lower threshold voltage. This results in a linear increase of V_{CES}. The undershoot of the lower threshold voltage of $V_{dc,i}$ occurs only once at time t_3, which can be seen from the small flattening of V_{CES}.

The further deviations observable still result from the causes already described previously. In general, the shapes of the mains voltage prototype appear more ideal. This can be explained by the fact that the parasitic influences, which have a stronger percentage effect at the lower voltage range, become negligibly small at mains voltage. Taking the soft start into account, the simulation confirms that the mains-voltage prototype in the kilowatt range of the current-source-based energy-storage works analogous to the low-voltage prototype according to theory.

VII. Conclusion

This article showed the approach of storing energy fed back from the load directly in the dc-bus without prior dc/dc conversion. The current-source-based energy-storage represents a simple, smart, and cost-effective alternative to the state-of-the-art technologies. By adapting the structures in the dc-bus, it is possible to use typical storage-capacitors, such as supercaps, ultracaps, EDLCs, or related technologies with low voltage strengths, but large capacitances directly in the dc-bus without any prior dc/dc conversion. These findings are confirmed by simulations and measurements. Since the simulations agree very well with the reality in the low-voltage range, in the mains voltage range with higher power this can be also assumed. The missing of this upstream dc/dc converter, which is always required in the state-of-the-art technologies, has some benefits. The main disadvantage of the cascading in terms of efficiency is eliminated due to the aspect that the energy has to pass the controlled current-source I_S only once for storing. Due to the improved total efficiency, the simplest possible topology in the form of a boost converter is selected for the controlled current-source I_S, which can be realized most cost-effectively. This results in the best possible cost-benefit ratio, also for the expected use of the current-source-based energy-storage in the higher power range.

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