Input Current Ripple-Free DC–DC Converter With Wide ZVS Range and Auto-Voltage-Sharing for Bipolar DC Microgrids

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***Abstract*—A dual-active-bridge (DAB)–based bipolar dc–dc converter with auto-voltage-sharing is proposed for dc microgrids in this article, where an integrated interleaved boost cell with a fixed duty cycle of 0.5 for the primary active-bridge is utilized. As a result, the input current ripple-free is realized. The primary and secondary active bridges are connected by two high-frequency transformers. Two primary windings are in series directly, whereas two secondary windings are across the secondary active-bridge and bipolar output, respectively. There are two operation modes for the proposed converter. One is single phase shift mode, which is the same as the traditional DAB converter. The other one is the equivalent voltage match (EVM) mode, where the auto-voltage-sharing and wide zero-voltage-switching for all switches can be achieved. The operation principles and characteristics of the EVM mode are analyzed in detail. Finally, a 1-kW prototype is built to verify the feasibility and advantage of the proposed converter.**

***Index Terms*—Auto-voltage-sharing, bipolar dc system, current ripple-free, zero-voltage-switching (ZVS).**

I. Introduction

THE distribution energy sources, electric vehicles, and energy storages are with dc properties. With their rapid development, dc microgrids are increasingly attractive for fewer power conversion stages and higher reliability [1], [2], [3]. According to the number of voltage levels, the dc distribution network system can be divided into unipolar and bipolar systems [4]. As shown in Fig. 1, the bipolar system provides two voltage levels, which can provide higher reliability while reducing the voltage to ground, and can connect dc loads with different bus voltage [5]. In addition, even if one dc pole fails, the power supply can still be allocated to the other functioning dc pole to improve the reliability of the system [5], [6], [7]. However, the bipolar system has the challenge of output voltage unbalance.

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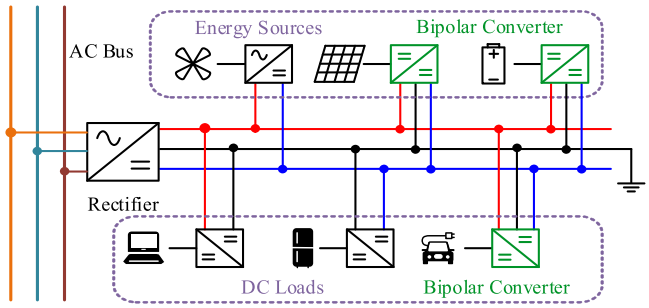

Fig. 1. Structure of bipolar DC microgrid.

The difference between line parameters and loads may lead to deviations from rated bus voltages for both polarities [8].

To achieve bipolar voltage balance, additional circuits are utilized for the bipolar output [9], [10], [11], [12], including the current branch circuit and the independent voltage balancing circuit. A series *LC* branch circuit is introduced into the bipolar dc–dc converter to achieve voltage sharing in [9]. A dual-Buck structure is proposed in [10] in which two inductors can achieve the voltage sharing. In [11] and [12], the Buck/Boost type balancer is introduced and roles as the independent voltage balancer to eliminate the imbalance of bipolar output. However, additional circuits or independent voltage balancer bring lower efficiency and power density.

To avoid extra circuits, some researchers integrate them into or remove them from the original bipolar converters [13], [14], [15], [16], [17], [18], [19], [20], [21]. The interleaved Buck/Boost circuit is integrated into dual-active-bridge (DAB) type converters, where four switches are shared by Buck/Boost and DAB units [13], [14]. Moreover, the auto-voltage-sharing is realized. The triple-active-bridge (TAB) converter with the coupled inductor in series on the secondary windings was studied in [15] and [16], which can achieve voltage balancing naturally with the help of the tightly coupled inductor. However, the TAB converter requires many switches. In [17], a single-stage bipolar dc–dc converter is proposed based on the three-level natural-point-clamped circuit. Nevertheless, the converter proposed in [17] needs to sample bipolar voltage individually and adopt an extra voltage-balancing control loop. A family of multiport converters based on voltage-multiplying rectifiers with auto-voltage-sharing is proposed in [18]. The concept of the coupled-inductor-based Buck-type bipolar converter is proposed

in [19], and a phase-shift full-bridge bipolar converter with rectifiers and two *LC* filters is derived. By coupling the two filter inductors, the auto-voltage-sharing is realized. However, the converters both in [18] and [19] are unidirectional, leading the applications to be limited. The bipolar dc–dc converter in [20] has the same components as the conventional DAB converter. Two secondary windings are adopted on the secondary side, and the auto-voltage-sharing is achieved with the fixed duty cycle of 0.5 for secondary switches. In [21], a series of bipolar output active rectifiers with a center-tapped winding is proposed; however, the soft-switching is hard to achieve under the extremely unbalanced load.

Furthermore, some efforts are made to improve the soft-switching of the bipolar dc–dc converters. The soft-switching range for switches is broadened in [22] by replacing the high-frequency transformer with the coupled inductor and properly designing the magnetizing inductance. To increase the range of input voltage of the bipolar dc–dc converter, a couple-inductor-based dc–dc converter with bipolar voltage output is proposed in [23]. However, [22] and [23] did not solve the dc bias problem of the magnetic components. In [24], the dc bias suppression for the high-frequency transformer is studied based on the conventional dual-active-half-bridge converter with an additional inductor and capacitor. However, the above mentioned converters did not achieve zero input current ripple.

Some efforts are made to achieve the ripple-free input current [25], [26], [27], [28], [29]. The current-fed full bridge dc–dc converter can eliminate the input current ripple [25], [26]. To reduce the input current ripple further, the interleaved current-fed half-bridge converter is proposed [27], [28], [29]. In [27], the interleaved boost structure working in the discontinuous current mode is used to reduce the current ripple of each boost structure. In [28], a three-phase current-fed full bridge structure is proposed to reduce the input current ripple. In [29], the interleaved boost structure working in the continuous current mode is used to realize the input current ripple-free.

Based on the DAB structure, a current-fed bipolar dc–dc converter is proposed to achieve auto-voltage-sharing, as well as the input current ripple-free. On the primary side, an integrated interleaved boost cell with the fixed duty cycle of 0.5 for the primary active-bridge is utilized, then the input current ripple-free can be realized. The primary and secondary active bridges are connected by two high-frequency transformers. Two primary windings are in series directly, whereas two secondary windings are across the secondary active-bridge and bipolar output, respectively. Equivalently, there is a Buck/Boost cell on the secondary, and the secondary magnetizing inductor roles as the Buck/Boost inductor. As a result, the auto-voltage-sharing is achieved under any load conditions. Based on the proposed equivalent-voltage-match (EVM)-based control, there are two different phase-shift angles between the primary and secondary active-bridges. By regulating them properly, the wide zero-voltage-switching (ZVS) of all switches can be achieved. Moreover, the proposed converter has another operation mode, namely the single-phase-shift (SPS) mode, which is the same as the traditional DAB converter. By setting two operating modes, the converter can work in two different applications.

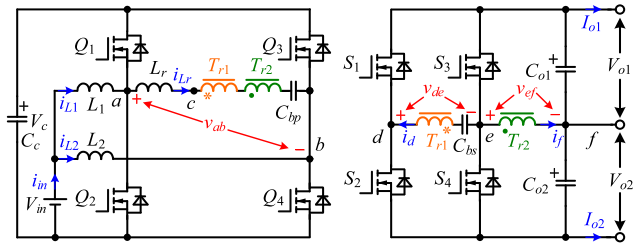

Fig. 2. Topology of the proposed converter.

The rest of this article is organized as follows. Section II introduces the topology and working principle in detail. Section III analyzes the soft switching conditions, the power transmission capability of the proposed converter, and the control strategy of the proposed converter. Section IV provides the experimental verification. Finally, Section V concludes this article.

II. Proposed Topology and Modulation Principles

The proposed converter is shown in Fig. 2. The primary side is composed of an interleaved boost cell with two inductors, L_1 and L_2, a full-bridge cell of switches Q_1–Q_4, and a clamped capacitor C_C, where Q_1–Q_4 are multiplexed as the primary active-bridge. The secondary side is composed of an active-bridge cell of switches S_1–S_4 and two bipolar output capacitors C_{o1} and C_{o2}. The primary and secondary active-bridge cells are connected through two high-frequency transformers, T_{r1} and T_{r2}. The primary windings of T_{r1} and T_{r2} are in series directly with a blocking capacitor C_{bp}, and L_r can be derived by the primary leakage inductor of them. The secondary winding of T_{r1} in series with a blocking capacitor C_{bs} is connected to the midpoints of S_1 and S_2, S_3 and S_4, and that of T_{r2} is connected to the midpoints of S_3 and S_4, C_{o1} and C_{o2}. V_{in} is the input voltage, V_c is the voltage across C_C, V_{o1} and V_{o2} are voltages across C_{o1} and C_{o2}, and V_o is defined as the sum of V_{o1} and V_{o2}. T_{r1} and T_{r2} have the same secondary to primary turns ratio of N.

The proposed converter has two different operation modes. The first mode is named EVM mode, where all the duty cycles of switches are 50%, as shown in Fig. 3. Q_1 and Q_4 have the same gate signal, as well as Q_2 and Q_3. The gate signals of Q_1 and Q_2 are complementary with enough dead time, as well as S_1 and S_2, and S_3 and S_4. The gate signal of Q_1 leads that of S_3 for $\varphi_1 T_s$ while the gate signals of S_3 lead that of S_1 for $\varphi_2 T_s$, where T_s is the switching cycle and the switching frequency $f_s = 1/T_s$. The second mode is SPS mode, where C_{bs} roles as a voltage source, S_1 is always OFF, and S_2 is always ON, whereas all the other switches have the same drive signals as in EVM mode, as shown in Fig. 4.

The voltage v_{ab} across the nodes a and b, and the voltage v_{cb} across the nodes c and b are as shown in Fig. 5. As can be seen, the SPS mode is exactly the SPS modulation of the traditional DAB converter, which is well-known. Hence, this article will focus on the EVM mode, and the SPS mode will be briefly analyzed if needed.

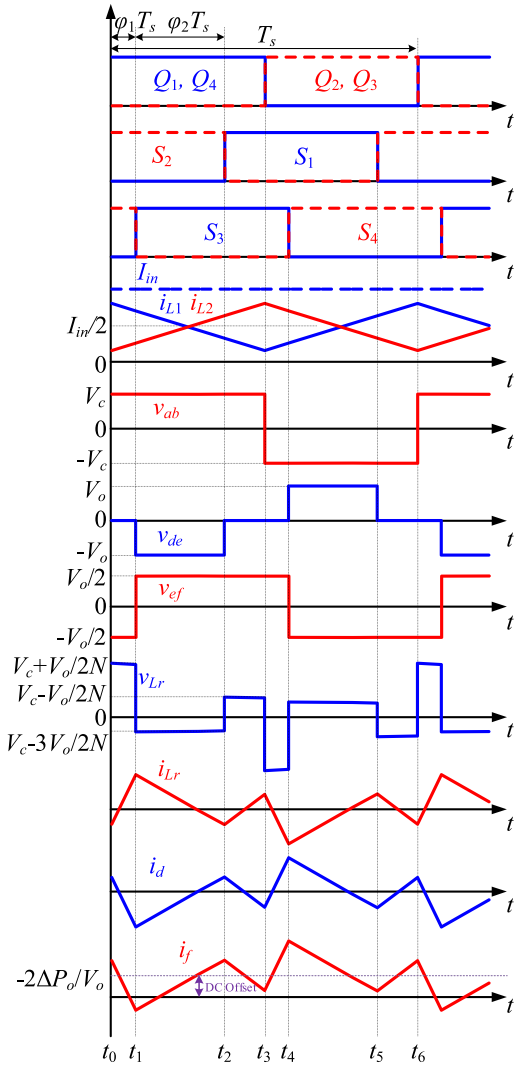

Fig. 3. Typical waveforms of EVM mode.

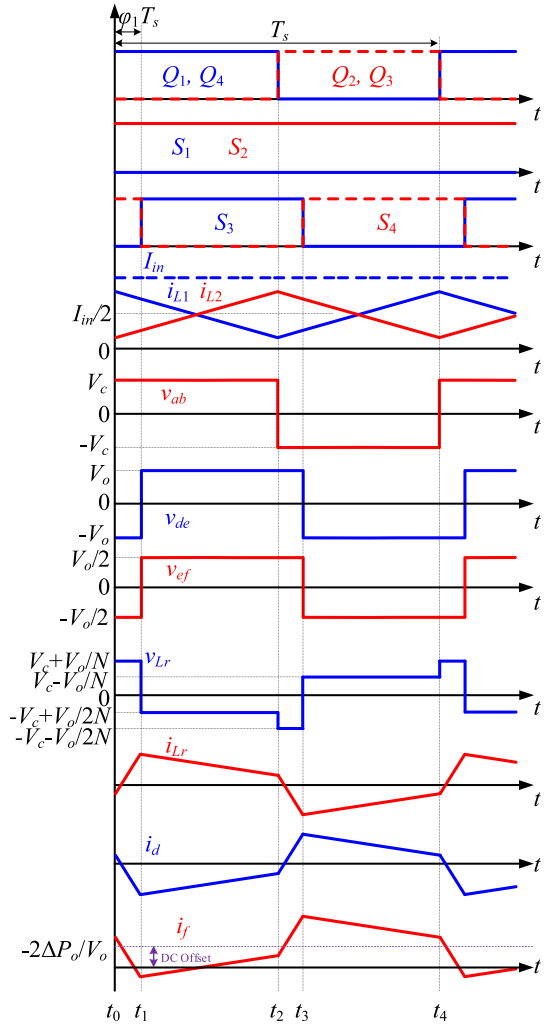

Fig. 4. Typical waveforms of SPS mode.

A. Operation Principles

According to Fig. 3, one switching cycle can be divided into six stages. Only the first three stages shown in Fig. 6 will be analyzed because of the symmetry, where the voltages of C_{bp} and C_{bs} are small and can be ignored.

Stage 1(t_0-t_1)*:* At t_0, Q_1 and Q_4 are turned ON. Hence, v_{ab} equals V_c, and the current i_{L1} of L_1 decreases linearly while the current i_{L2} of L_2 increases linearly. S_2 and S_4 are kept ON while S_1 and S_3 are kept OFF, thus, the voltage v_{de} across the nodes d and e equals zero, and the voltage v_{ef} across the nodes e and f equals $-V_o/2$. Hence, by reflecting v_{de} and v_{ef} to the primary side, the primary current i_{Lr} can be expressed as

$$i_{Lr}(t) = i_{Lr}(t_0) + (V_c + 0.5V_o/N)(t - t_0)/L_r \quad t \in [t_0, t_1]. \tag{1}$$

Stage 2(t_1-t_2)*:* At t_1, S_4 is turned OFF, and S_3 is turned ON. The sum of secondary currents, i_d plus i_f, is negative. Thus, the ZVS of S_3 can be achieved and the ZVS condition can be

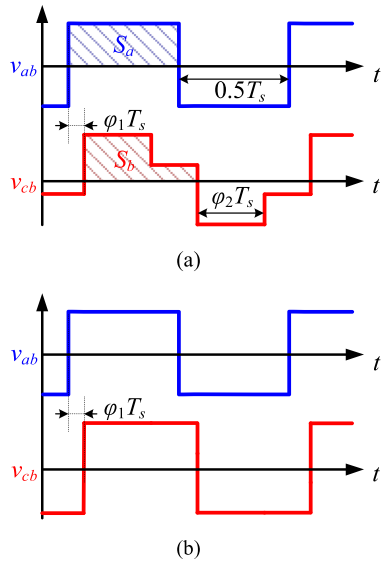

Fig. 5. Voltage waveforms of v_{ab} and v_{cb}. (a) EVM mode. (b) SPS mode.

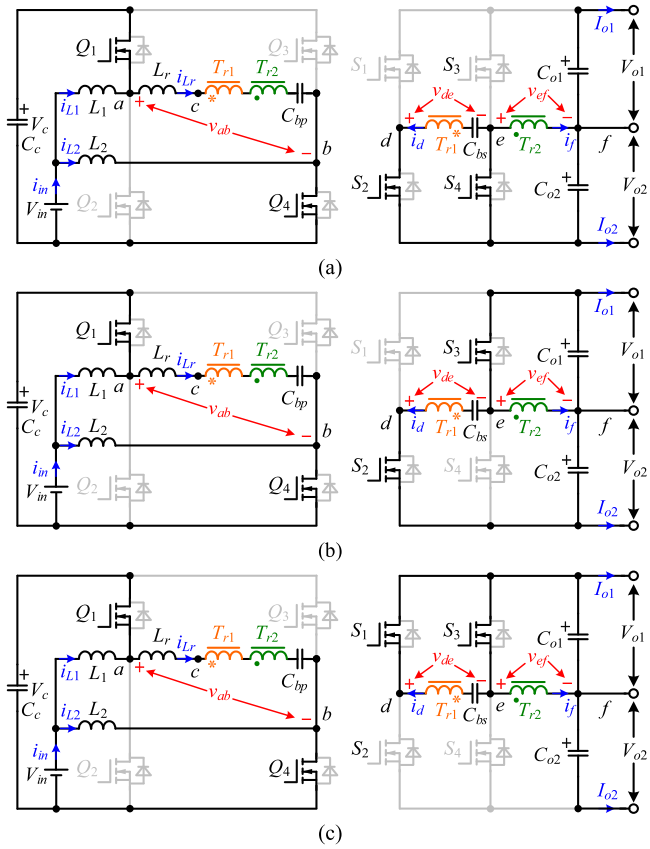

Fig. 6. Operation modes. (a) t_0-t_1. (b) t_1-t_2. (c) t_2-t_3.

expressed as

$$i_d(t_1) + i_f(t_1) < 0. \tag{2}$$

After t_1, S_2 is kept ON while S_1 and S_4 are kept OFF. Thus, v_{de} equals $-V_o$ and v_{ef} equals $V_o/2$. For Q_1 and Q_4 are still ON, v_{ab} still equals V_c, and i_{L1} and i_{L2} still decrease and increase linearly, respectively.

Thus, i_{Lr} can be expressed as

$$i_{Lr}(t) = i_{Lr}(t_1) + (V_c - 1.5\ V_o/N)(t - t_1)/L_r \quad t \in [t_1, t_2]. \tag{3}$$

Stage 3(t_2-t_3): At t_2, S_2 is turned OFF, and S_1 is turned ON. i_d is positive. Thus, the ZVS of S_1 can be achieved and the ZVS condition for S_1 can be expressed as

$$i_d(t_2) > 0. \tag{4}$$

After t_2, S_3 is kept ON while S_2 and S_4 are kept OFF. Thus, v_{de} turns to zero, whereas v_{ef} still equals $V_o/2$. For Q_1 and Q_4 are still ON, v_{ab} still equal V_c, and i_{L1} and i_{L2} still decrease and increase linearly, respectively. Thus, i_{Lr} can be expressed as

$$i_{Lr}(t) = i_{Lr}(t_2) + (V_c - 0.5V_o/N)(t - t_2)/L_r \quad t \in [t_2, t_3]. \tag{5}$$

At t_3, Q_1 and Q_4 are turned OFF. To achieve the ZVS of Q_2, the current of it should be negative, which means the difference between i_{Lr} and i_{L1} should be positive. Similarly, to achieve the ZVS of Q_3, the sum of i_{Lr} and i_{L2} should be positive. Thus, the

TABLE I
ZVS CONDITIONS FOR SWITCHES

Switches	Currents
Q_1	$i_{Lr}(t_0) - i_{L1}(t_0) < 0$
Q_2	$i_{Lr}(t_3) - i_{L1}(t_3) > 0$
Q_3	$i_{Lr}(t_3) + i_{L2}(t_3) > 0$
Q_4	$i_{Lr}(t_0) + i_{L2}(t_0) < 0$
S_1	$i_d(t_2) > 0$
S_2	$i_d(t_5) < 0$
S_3	$i_d(t_1) + i_f(t_1) < 0$
S_4	$i_d(t_4) + i_f(t_4) > 0$

ZVS conditions for Q_2 and Q_3 can be expressed as

$$\begin{cases} i_{Lr}(t_3) - i_{L1}(t_3) > 0 & \text{for } Q_2 \\ i_{Lr}(t_3) + i_{L2}(t_3) > 0 & \text{for } Q_3 \end{cases}. \tag{6}$$

According to the analysis above and the symmetry, all switches can be summarized in Table I.

According to Fig. 3, t_0–t_3 can be expressed as

$$t_0 = 0, \quad t_1 = \varphi_1 T_s, \quad t_2 = (\varphi_1 + \varphi_2) T_s, \quad t_3 = 0.5\ T_s. \tag{7}$$

Based on the above analysis and the symmetry of the proposed converter, i_{Lr} under the balanced load condition can be expressed as

$$\begin{cases} i_{Lr}(t_0) = (4\varphi_2 V_o + V_o - 4\varphi_1 V_o - 2NV_c) T_s/(8NL_r) \\ i_{Lr}(t_1) = (4\varphi_2 V_o + V_o + 8N\varphi_1 V_c - 2NV_c) T_s/(8NL_r) \\ i_{Lr}(t_2) = \Big[(1 - 8\varphi_2) V_o + 8N\varphi_2 V_c \\ \qquad\qquad + 8N\varphi_1 V_c - 2NV_c\Big] T_s/(8NL_r) \end{cases}. \tag{8}$$

i_d and i_f under the balanced load condition can be expressed as

$$i_d = i_f = -i_{Lr}/N. \tag{9}$$

Moreover, i_{L1} and i_{L2} can be expressed as

$$\begin{cases} i_{L1}(t_0) = i_{L2}(t_3) = P_o/2\ V_{in} + V_{in} T_s/(4L_1) \\ i_{L1}(t_3) = i_{L2}(t_0) = P_o/2\ V_{in} - V_{in} T_s/(4L_1) \end{cases} \tag{10}$$

where P_o is the transferred power.

B. Principle of Voltage Balancing

The equivalent circuit of the auto-voltage-balancing function is shown in Fig. 7. S_3 and S_4 have the same duty cycle of 0.5. When S_3 is ON and S_4 is OFF, the secondary magnetic inductor L_m of T_{r2} is charged by V_{o1}. Similarly, L_m is discharged by V_{o2} when S_4 is ON. Applying the voltage–second balance theory on L_m during steady state, V_{o1} and V_{o2} should be the same, indicating the auto-voltage-sharing realized.

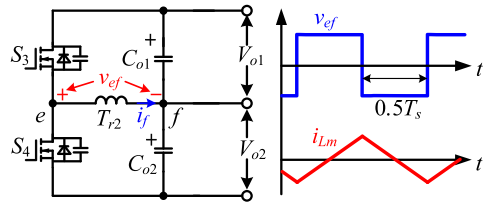

Fig. 7. Equivalent circuit of auto-voltage-balancing function.

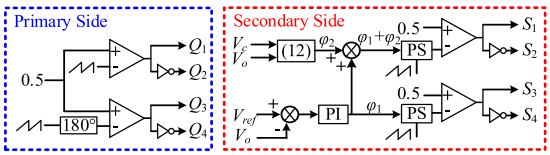

Fig. 8. Control diagram of the EVM mode.

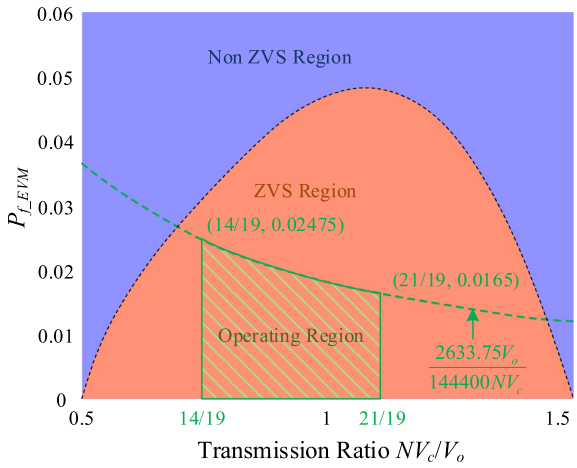

Fig. 9. ZVS region of EVM mode.

C. Principle of Input Current Ripple-Free

For the duty cycle of primary switches is 0.5, one can have $V_c = 2V_{in}$. Hence, when Q_1 and Q_4 are ON, the voltages across L_1 and L_2 are $V_{\text{in}} - V_c = -V_{in}$ and $V_c - V_{\text{in}} = V_{in}$, respectively. As a result, the variations of i_{L1} and i_{L2} just offset each other with the input current constant. The condition is the same when Q_1 and Q_4 are OFF. To conclude, the input current is ripple-free.

III. Design Consideration and Proposed Control

A. Principle of Equivalent-Voltage-Match

The waveforms of v_{ab} and v_{cb} $(v_{cb} = (v_{ef} - v_{de})/N)$ are shown in Fig. 5(a), where S_a and S_b are the voltage–second products of v_{ab} and v_{cb} in a half cycle, respectively. S_a and S_b can be expressed as

$$\begin{cases} S_a = 0.5\ V_c T_s \\ S_b = (\varphi_2 + 0.25) T_s V_o\ / N \end{cases}. \tag{11}$$

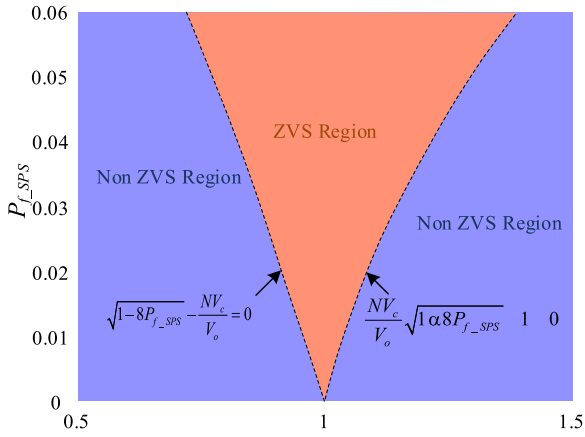

Fig. 10. ZVS region of SPS mode.

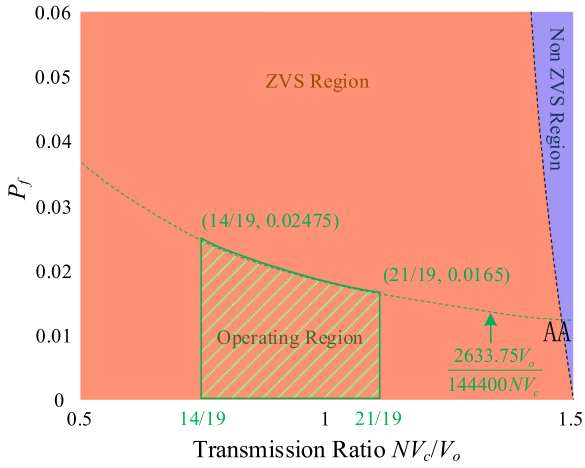

Fig. 11. ZVS region of S_3 and S_4 under extremely unbalanced load condition.

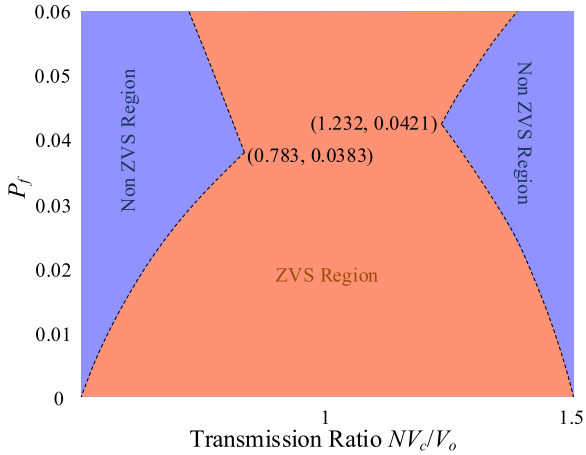

Fig. 12. ZVS region of EVM mode and SPS mode.

As is well known, the voltage match is preferred for DAB converters [30]. Hence, the EVM is adopted for the proposed converter, namely $S_a = S_b$, and one can obtain

$$\varphi_2 = \frac{NV_c}{2\ V_o} - \frac{1}{4}. \tag{12}$$

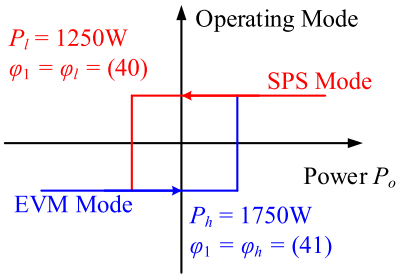

Fig. 13. Hysteresis comparator of the proposed converter.

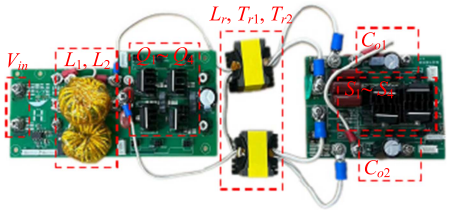

Fig. 14. Prototype of the proposed converter.

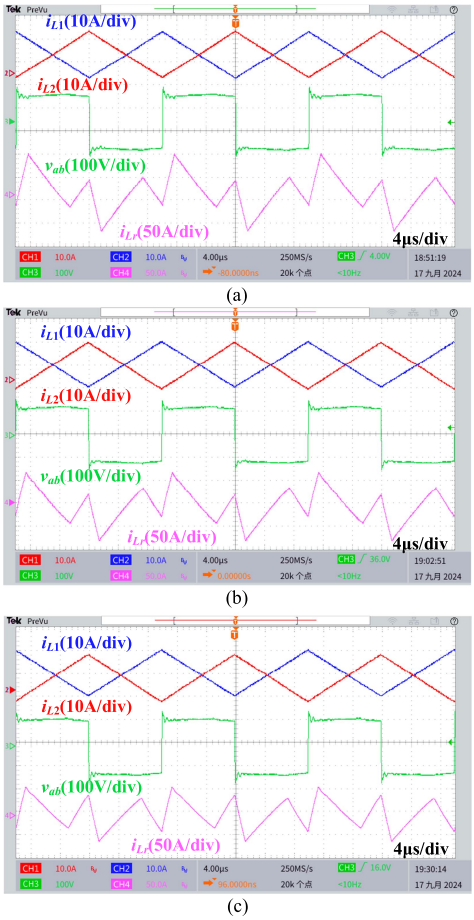

Fig. 15. Waveforms of voltage of v_{ab} and current of i_{L1}, i_{L2}, and i_{Lr}. (a) Condition A. (b) Condition B. (c) Condition C.

B. Power Expressions

Since v_{ab} equals V_c from t_0 to t_3, the power transferred by i_{Lr} in a half cycle can be expressed as

$$0.5P_o = 2f_s \int_{t_0}^{t_3} v_{ab}(t) i_{Lr}(t) dt = 2f_s V_c \int_{t_0}^{t_3} i_{Lr}(t) dt. \quad (13)$$

By substituting (1), (3), (5), and (7) into (13), one can obtain

$$P_o = \left(-\varphi_1^2 + 0.5\varphi_1 + 2\varphi_1\varphi_2 + \varphi_2^2 - 0.5\varphi_2\right) T_s V_c V_o / \left(N L_r\right). \quad (14)$$

Define P_f as $P_o N L_r/(T_s V_c V_o)$. To distinguish the P_f in two operating modes, P_f in the EVM mode is named P_{f_EVM}, and P_f in the SPS mode is named P_{f_SPS}, where

$$P_{f\_EVM} = -\varphi_1^2 + 0.5\varphi_1 + 2\varphi_1\varphi_2 + \varphi_2^2 - 0.5\varphi_2. \quad (15)$$

Similarly, the transfer power of the SPS mode can be obtained as

$$P_o = \frac{V_c V_o T_s P_{f\_SPS}}{N L_r} \quad (16)$$

where $P_{f\_SPS} = \varphi_1(1 - 2\varphi_1)$.

C. Control Strategy and Closed-Loop Parameter Design

Based on (12) and (15), the EVM-based control is shown in Fig. 8, where φ_1 can be obtained through a simple PI controller. To design the PI controller, the transfer function of the proposed converter should be derived first. In this part, the model in EVM mode is provided.

Substituting (12) into (14), the output power P_o of the proposed converter can be expressed as

$$P_o = \frac{\left(\varphi_1^2 - \varphi_1 + \varphi_1 \frac{NV_c}{V_o} + \frac{NV_c}{2V_o} - \frac{N^2V_c^2}{4V_o^2} - \frac{3}{16}\right) T_s V_c V_o}{N L_r}. \quad (17)$$

P_o is the sum of P_{o1} and P_{o2} and $P_{o1} = V_{o1} i_1$, $P_{o2} = V_{o2} i_2$, where i_1 and i_2 are the currents flowing into the bipolar output capacitor and load. Because of the self-balance of output voltage, $V_{o1} = V_{o2} = V_o/2$ and $P_o = V_o(i_1 + i_2)$. Thus, i_1+i_2 can be calculated as P_o/V_o. Introducing perturbation at phase shift $\varphi_1 = \Phi_1 + \hat{\varphi}_1$, $i_1 + i_2 = I_1 + I_2 + \hat{i}_1 + \hat{i}_2$, the transfer function from $\hat{\varphi}_1$ to $\hat{i}_1 + \hat{i}_2$ can be expressed as

$$\begin{aligned} G_{\varphi_1 i_o} &= \frac{\hat{i}_1 + \hat{i}_2}{\hat{\varphi}_1} = \frac{\partial(i_1 + i_2)}{\partial \varphi_1}\Big|_{\varphi_1 = \Phi_1} \\ &= \frac{\left(2\Phi_1 - 1 + \frac{NV_c}{V_o}\right) T_s V_c}{N L_r} \end{aligned} \quad (18)$$

where V_c, V_o, Φ_1, I_1, and I_2 are the quiescent values of v_c, v_o, φ_1, i_1, and i_2. Φ_1 and $I_1 + I_2$ can be expressed as

$$\Phi_1 = \frac{\frac{NVc}{V_o} - \sqrt{\frac{3}{4} + 2\left(\frac{NV_c}{V_o}\right)^2 - 2\left(\frac{NV_c}{V_o}\right) - \frac{4P_o N L_r}{T_s V_c V_o}}}{2}$$

$$I_1 + I_2 = \frac{2P_o}{V_o}. \quad (19)$$

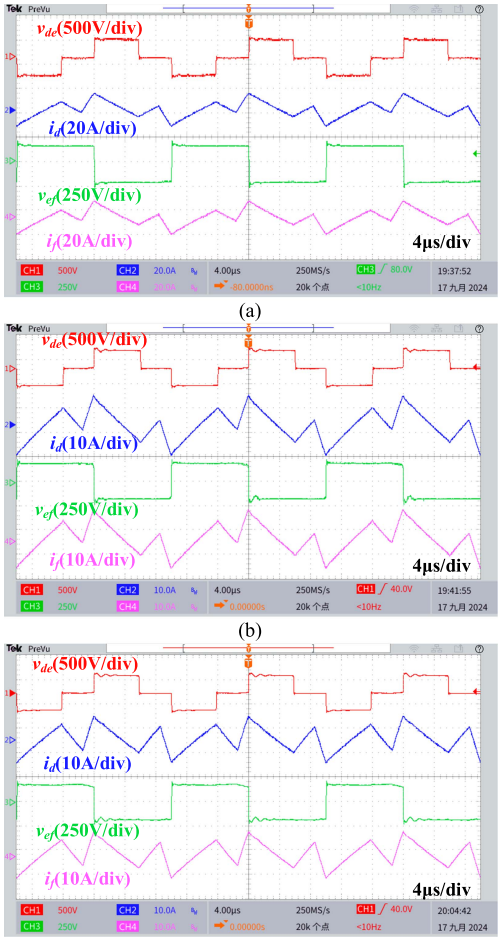

Fig. 16. Waveforms of voltage of v_{de} and v_{ef} and current of i_d and i_f. (a) Condition A. (b) Condition B. (c) Condition C.

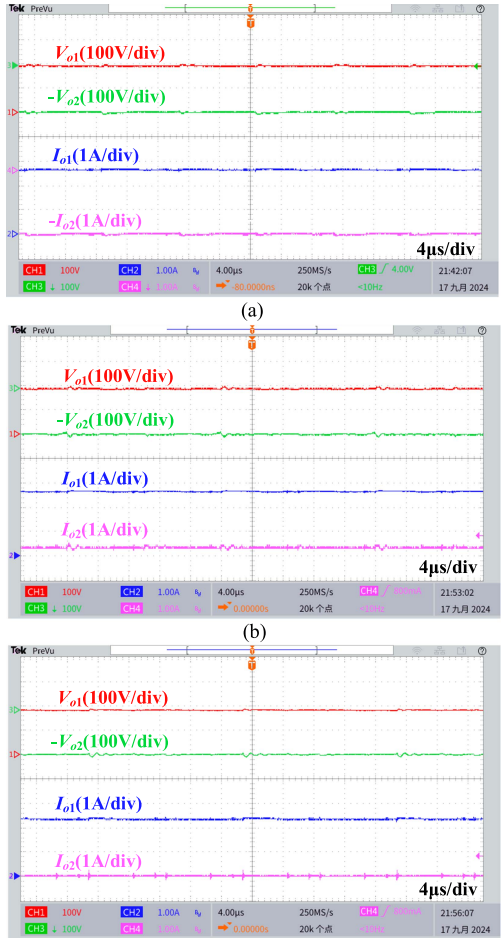

Fig. 17. Waveforms of V_{o1}, V_{o2}, I_{o1}, and I_{o2}. (a) Condition A. (b) Condition B. (c) Condition C.

Ignoring the dynamics of the voltage balancing inductor, the transfer function from $\hat{i}_1$ and $\hat{i}_2$ to $\hat{v}_o$ can be calculated as

$$\hat{v}_o = \hat{v}_1 + \hat{v}_2 = \hat{i}_1 \frac{R_{o1}}{R_{o1}C_{o1}s+1} + \hat{i}_2 \frac{R_{o2}}{R_{o2}C_{o2}s+1}. \tag{20}$$

Since the magnetizing inductor of T_{r2} is only involved in balancing V_{o1} and V_{o2}, which does not affect V_o, the transfer function from $\hat{i}_1 + \hat{i}_2$ to $\hat{v}_o$ can be designed by using a current source model [31], [32]. V_{o1} equals to $\frac{i_1 R_{o1}}{R_{o1}C_{o1}s+1}$, V_{o2} equals to $\frac{i_2 R_{o2}}{R_{o2}C_{o2}s+1}$, and $V_{o1} = V_{o2}$. Thus, two output ports can be treated as parallel, whereas the transfer function can be simplified as

$$\begin{aligned}\hat{v}_o &= \left(\hat{i}_1 + \hat{i}_2\right)\left(\frac{R_{o1}}{R_{o1}C_{o1}s+1} \| \frac{R_{o2}}{R_{o2}C_{o2}s+1}\right) \\ &= \left(\hat{i}_1 + \hat{i}_2\right)\left(\frac{R_{o1}R_{o2}}{R_{o1}R_{o2}(C_{o1}+C_{o2})s + R_{o1} + R_{o2}}\right).\end{aligned} \tag{21}$$

Thus, the transfer function from $\hat{\varphi}_1$ to $\hat{v}_o$ can be derived as

$$G_{v\varphi_1}(s) = \frac{2\frac{NV_c}{V_o} - \sqrt{\frac{3}{4} + 2\left(\frac{NV_c}{V_o}\right)^2 - 2\frac{NV_c}{V_o} - \frac{4P_oNL_r}{T_sV_cV_o}} - 1}{NL_r\left(\left(C_{o1}+C_{o2}\right)s + \frac{1}{R_{o1}} + \frac{1}{R_{o2}}\right)} T_sV_c. \tag{22}$$

Designing the compensator as a PI controller and can be expressed as

$$G_c(s) = k_p + \frac{k_i}{s}. \tag{23}$$

Then, according to (22) and (23), the transfer function of the closed-loop system can be derived as

$$G(s) = \frac{G_c(s)G_{v\varphi 1}(s)}{1 + G_c(s)G_{v\varphi 1}(s)} = \frac{1}{\frac{Bs^2+s}{Ak_ps+Ak_i} + 1} \tag{24}$$

where

$$A = \frac{2\frac{NV_c}{V_o} - \sqrt{\frac{3}{4} + 2\left(\frac{NV_c}{V_o}\right)^2 - 2\frac{NV_c}{V_o} - \frac{4P_oNL_r}{T_sV_cV_o}} - 1}{NL_r\left(\frac{1}{R_{o1}} + \frac{1}{R_{o2}}\right)} T_sV_c$$

$$B = \frac{R_{o1}R_{o2}}{R_{o1}+R_{o2}}(C_{o1}+C_{o2}). \tag{25}$$

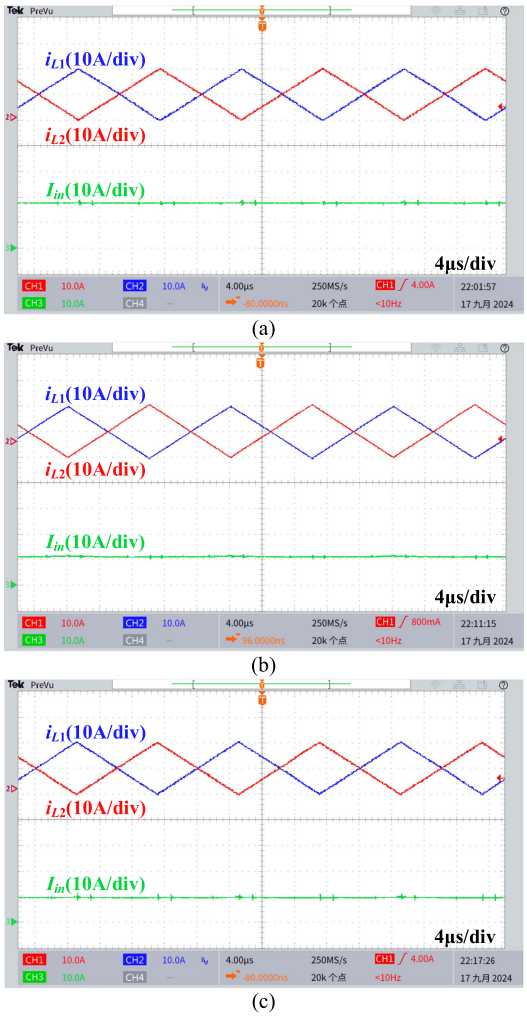

Fig. 18. Waveforms of I_{in}, i_{L1}, and i_{L2}. (a) Condition A. (b) Condition B. (c) Condition C.

While a simple way to design PI parameters is to set the closed-loop system as a first-order inertial link, and another rule is to set the cutoff frequency less the one-fifth of the switching frequency to avoid the influence of switching action, the relation between A, B, k_p, and k_i can be expressed as

$$\begin{cases} \dfrac{B}{Ak_p} = \dfrac{1}{Ak_i} \\ \dfrac{Ak_p}{B} < \dfrac{2\pi}{5\,T_s} \end{cases}. \tag{26}$$

To ensure the response speed, the cutoff frequency should be set as high as possible. Finally, the PI parameter can be derived as

$$\begin{cases} k_p = \dfrac{5BT_s}{\pi A} \\ k_i = \dfrac{5\,T_s}{\pi A} \end{cases}. \tag{27}$$

D. Soft-Switching Conditions

1) Under Balanced Load Condition: Based on the above analysis and the symmetry of the proposed converter, Q_1 and

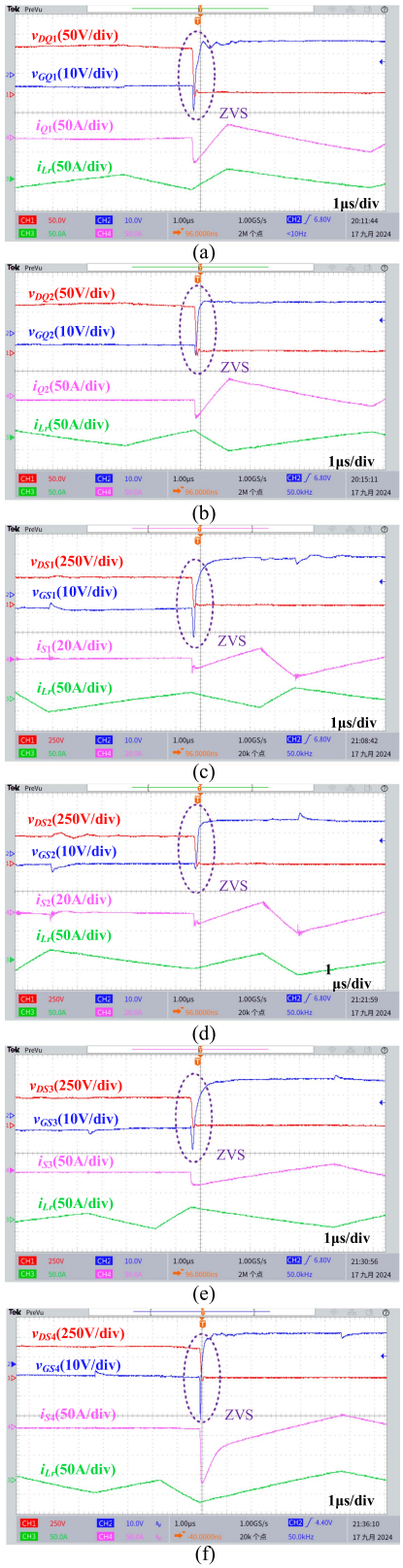

Fig. 19. ZVS waveforms of Condition C. (a) Q_1. (b) Q_2. (c) S_1. (d) S_2. (e) S_3. (f) S_4.

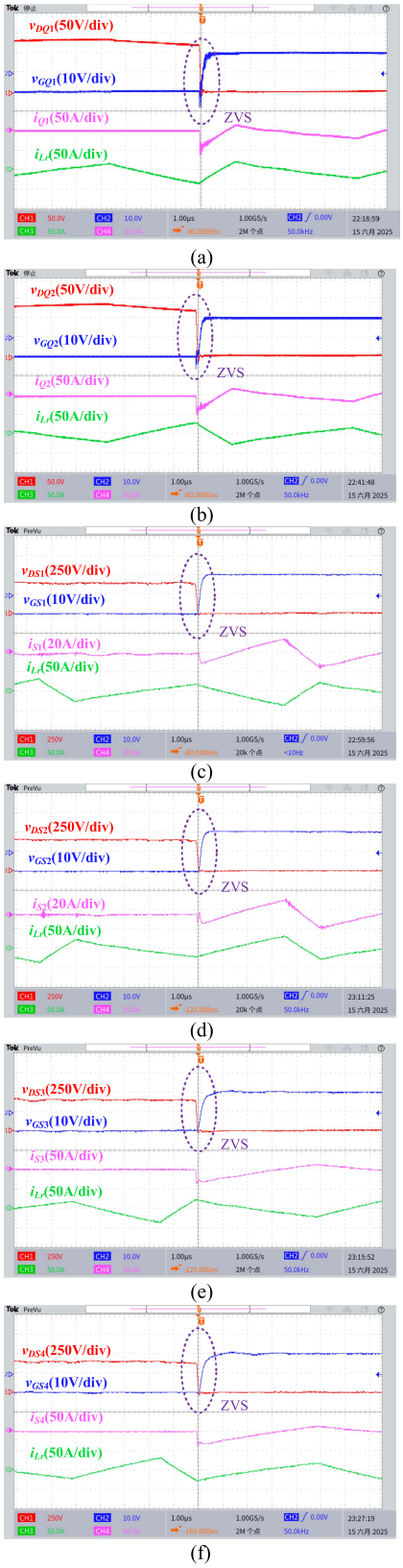

Fig. 20. ZVS waveforms under 14.44% load condition. (a) Q_1. (b) Q_2. (c) S_1. (d) S_2. (e) S_3. (f) S_4.

TABLE II
ZVS CONDITIONS FOR SWITCHES

Switches	Conditions
Q_1, Q_3	$-\varphi_1 V_o T_s/(2NL_r) - P_o/V_o - V_{in}T_s/(4L_1) < 0$
Q_2, Q_4	$-\varphi_1 V_o T_s/(2NL_r) + P_o/V_o - V_{in}T_s/(4L_1) < 0$
S_1, S_2	$-\varphi_2 + 2\varphi_2^2 + 2\varphi_1\varphi_2 + \varphi_1/2 < 0$
S_3, S_4	$-\varphi_1 < 0$

TABLE III
EXPERIMENTAL PARAMETERS

Parameters	Value
Input voltage (V_{in})	40–60 V
Output voltage(V_{o1}, V_{o2})	190 V
Rated output power (P_o)	1 kW
Leakage inductor (L_r)	4.3 μH
Boost inductor (L_1, L_2)	30 μH
Turns ratio (N)	3.5
Switching frequency (f_s)	50 kHz

Q_3 have the same ZVS condition, as well as Q_2 and Q_4, S_1 and S_2, and S_3 and S_4. The ZVS conditions of all switches can be obtained as Table II by substituting (8), (9), (10), and (12) into (2), (4), and (6).

Obviously, the ZVS of Q_1, Q_3, S_3 and S_4 can be always obtained, and the ZVS of Q_2 and Q_4 can be achieved by designing L_1 and L_2 as

$$L_1 = L_2 < 0.25 V_{in} T_s V_o / P_o. \tag{28}$$

Referring to (12) and (15), the ZVS condition of S_1 and S_2 can be expressed as

$$\frac{3}{8} - \frac{NV_c}{V_o} + \frac{N^2 V_o^2}{V_o^2} - \frac{NV_c}{2V_o}\sqrt{2\frac{N^2V_o^2}{V_o^2} - 2\frac{NV_c}{V_o} + \frac{3}{4} - 4P_{f\_EVM}} < 0. \tag{29}$$

Fig. 9 shows the ZVS region with P_{f_EVM} and V_c and V_o as variables, where the black dashed line is the critical form of the inequality (29). According to the experimental parameters in Table III, NV_c/V_o varies from 14/19 to 21/19. The green dashed line in Fig. 9 is the working point under the full load conditions, P_{f_EVM} varies from 0 to the green dashed line, and then the green box in Fig. 9 can be obtained. As a result, the ZVS of S_1 and S_2 can always be realized as well.

Similarly, the ZVS region of SPS mode under the balanced load condition can be shown in Fig. 10, where the black dashed line is the critical form of the ZVS conditions under SPS mode.

As can be seen, when the output power is small, a wide range of the ZVS region can be derived under the EVM mode.

When output power is high, a wide range of ZVS region can be derived under the SPS mode.

2) Under Unbalanced Load Condition: While under the unbalanced load condition, assuming that $P_{o1} > P_{o2}$, a dc bias $I_{\rm dc}$ will be added to i_f. The current i_f under the unbalanced load

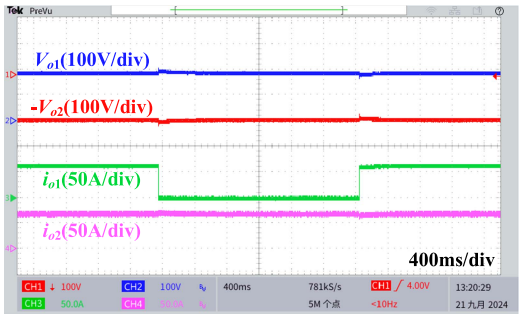

Fig. 21. Dynamic waveforms of i_{o1} and i_{o2} when the load changes.

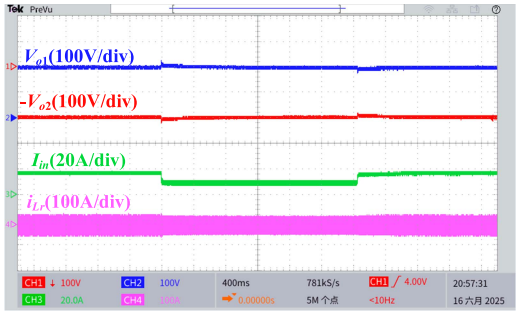

Fig. 22. Dynamic waveforms of I_{in} and i_{Lr} when the load changes.

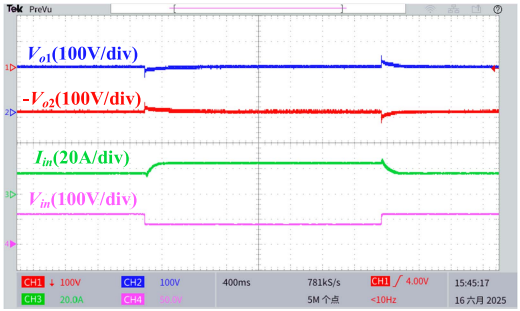

Fig. 23. Dynamic waveforms of V_{o1}, V_{o2}, and I_{in} when the input voltage changes.

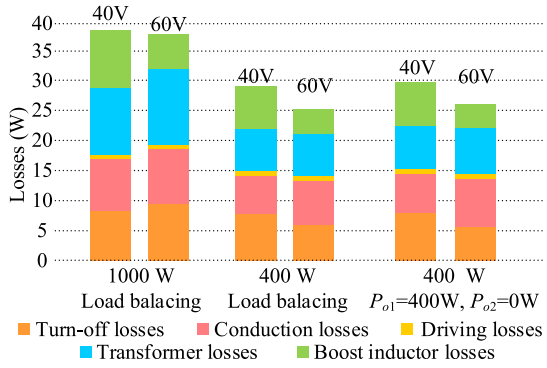

Fig. 24. Theoretical loss calculations under different V_{in}, P_o, and load conditions.

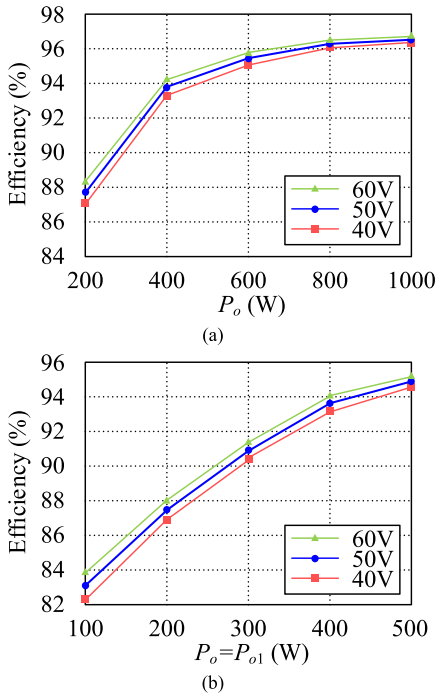

Fig. 25. Efficiency Curve. (a) Under balanced condition $P_{o1} = P_{o2}$. (b) Under extremely unbalanced condition $P_{o2} = 0$ and $P_{o1} = P_o$.

condition can be expressed as

$$i_f(t) = I_{\rm dc} - i_{Lr}(t)/N. \tag{30}$$

When S_3 is ON and S_4 is OFF, the energy transferred from T_{r2} to P_{o1} is

$$E_1 = \int_{t_1}^{t_4} -V_o i_f(t)/2\ dt. \tag{31}$$

When S_3 is OFF and S_4 is ON, the energy transferred from T_{r2} to P_{o2} is

$$E_2 = \int_{t_0}^{t_1} V_o i_f(t)/2\ dt + \int_{t_4}^{t_6} V_o i_f(t)/2\ dt. \tag{32}$$

The difference between P_{o1} and P_{o2} can be derived by

$$\Delta P_o = (E_1 - E_2)/T_s \tag{33}$$

where ΔP_o is the power difference between P_{o1} and P_{o2}. It is worth noting that ΔP_o can be totally balanced by T_{r2}, thus, no dc bias will be added to i_d and i_{Lr}. Hence, the ZVS conditions of Q_1–Q_4 and S_1 and S_2 can still be obtained under the unbalanced mode.

By (8), (31), (32), and (33), $I_{\rm dc}$ can be derived as

$$I_{\rm dc} = -2\Delta P_o/V_o. \tag{34}$$

According to Table I, (8), (12), (30), and (34), the ZVS conditions of S_3 and S_4 as

$$\begin{cases} -2\Delta P_o/V_o - \varphi_1(4\varphi_2+1)V_o T_s/(N^2 L_r) < 0 & \text{for } S_3 \\ -2\Delta P_o/V_o + \varphi_1(4\varphi_2+1)V_o T_s/(N^2 L_r) > 0 & \text{for } S_4 \end{cases}. \tag{35}$$

As can be seen, the ZVS of S_3 can always be obtained.

TABLE IV
COMPARISON WITH OTHER CURRENT-FED CONVERTER TOPOLOGIES

Topologies	[27]	[28]	[29]	Proposed converter
Number of magnetic components	4	9	4	4
Number of switches	4	6	10	8
Number of diodes	4	6	0	0
Soft switching	Primary: ZVS Secondary: ZCS Range: Partial	Primary: ZVS Secondary: ZCS Range: Partial	Primary: ZVS Secondary: ZVS Range: Full range	Primary: ZVS Secondary: ZVS Range: Full range
Auxiliary switch for ZVS	Not needed	Not needed	Needed	Not needed
Input voltage	28-43 V	26-39 V	24-36 V	40-60 V
Output voltage	380 V	370 V	400 V	380 V
Rated power	1.2 kW	1 kW	1 kW	1 kW
Peak efficiency	94 %	96 %	96%	96.5%
Ability of bipolar output	No	No	No	Yes

TABLE V
COMPARISON WITH OTHER BIPOLAR OUTPUT CONVERTER TOPOLOGIES

Topologies	[14]	[17]	[22]	Proposed converter
Number of magnetic components	4	2	3	4
Number of switches	8	12	6	8
Number of diodes	0	6	0	0
ZVS Range	Partial	Partial	Full range	Full range
Complexity of control	Low	High	Low	Low
Input voltage	380 V	600 V	32-53 V	40-60 V
Output voltage	380 V	600 V	400 V	380 V
Rated power	3 kW	3 kW	750 W	1 kW
Peak efficiency	97 %	95 %	97 %	96.5 %
Input current ripple-free	No	No	No	Yes

Substituting (12) and (15) into (35), the ZVS condition of S_4 can be expressed as

$$\frac{NV_c}{V_o}-\sqrt{2\left(\frac{NV_c}{V_o}\right)^2-2\left(\frac{NV_c}{V_o}\right)+\frac{3}{4}-4P_f-2\Delta P_f}>0 \tag{36}$$

where $\Delta P_f = N\Delta P_o L_r / (T_s V_c V_o)$.

When the load is extremely unbalanced, namely when $\Delta P_o = P_o$ and $\Delta P_f = P_f$, the ZVS region of S_4 with P_f and V_c and V_o as variables can be shown as Fig. 11, where the black dashed line is the critical form of the inequality (36). It can be seen that ZVS of S_3 can be obtained in this operating region.

3) Magnitude Criteria of ZVS by Considering the Parasitic Capacitance: Considering the parasitic capacitor of the switches, to achieve ZVS, the charge of the parasitic capacitor C_{oss} should be released before the switches turned ON. The charge Q_{oss} stored by C_{oss} can be expressed as

$$Q_{\text{oss}} = C_{\text{oss}} V_{\text{cmax}} \tag{37}$$

where V_{cmax} is the voltage across the switches. The charge released during the deadtime can be expressed as

$$Q_{\text{rel}} = I_{\text{off}} T_d \tag{38}$$

where T_d is the dead time of the switches. To discharge C_{oss}, the charge Q_{rel} released during the deadtime should be more than Q_{oss} as

$$I_{\text{off}} > \frac{C_{\text{oss}} V_{\text{cmax}}}{T_d}. \tag{39}$$

V_{cmax} of S_1 and S_2 are the largest ones among all of the switches, which means S_1 and S_2 are the most difficult to achieve the magnitude criteria of ZVS. In the prototype, IRFP340 is chosen as S_1 and S_2, whose C_{oss} is 400 pF. According to the parameters of the proposed converter shown in Table III, V_{cmax} of S_1 and S_2 is 380 V. T_d is set to 2×10^{-8}. Then, according to (39), i_{off} of S_1 and S_2 should be bigger than 0.304 A, which can be easily achieved by the proposed converter. In conclusion, all the switches can achieve ZVS even taking the parasitic capacitor into consideration and the ZVS condition can refer Table II for convenience.

E. Switching Process Between EVM Mode and SPS Mode

By combining the EVM mode and SPS mode, a wider ZVS range can be obtained, as shown in Fig. 12.

To switch the operating mode of the proposed converter, one can select the operating mode by a hysteresis comparator, as shown in Fig. 13, where φ_l and φ_h are φ_1 in the SPS mode and EVM mode, correspondingly, and can be expressed as

$$\varphi_l = \frac{1-\sqrt{1-8P_f}}{4} \tag{40}$$

$$\varphi_h = \frac{NV_c}{2V_o} - \sqrt{\frac{1}{2}\left(\frac{NV_c}{V_o}\right)^2 - \frac{NV_c}{2V_o} + \frac{3}{16} - P_f}. \quad (41)$$

There are two switching points P_l and P_h where the power transferred in SPS mode when $P_o = P_l$ is a bit lower than the power transferred in EVM mode when $P_o = P_h$. The operation mode will depend on the power transferred by the converter and the change direction of the power transferred by the converter. However, it is not convenient to measure the transferred power. According to (16) and (17), the transferred power can be reflected by the phase shift value φ_1, thus, two thresholds are preset as φ_l when $P_o = P_l$ in SPS mode and φ_h when $P_o = P_h$ in EVM mode. For example, assuming the converter is operating in EVM mode, the converter will switch from EVM mode to SPS mode when the load of the converter increases to a specific value while $\varphi_1 > \varphi_h$. Assuming the converter is operating in SPS mode, the converter will switch from SPS mode to EVM mode when the load of the converter increases to a specific value while $\varphi_1 < \varphi_l$.

IV. Experimental Verification

A 1-kW hardware prototype of the proposed converter is built and tested to verify its performance as shown in Fig. 14. Table III shows the experimental parameters.

To verify the performance of the proposed converter, three different load conditions were tested: Condition A of $P_{o1} = P_{o2} = 500$ W, Condition B of $P_{o1} = 500$ W and $P_{o2} = 72$ W, and Condition C of $P_{o1} = 500$ W and $P_{o2} = 0$ W. Fig. 15 shows the waveforms of primary i_{L1}, i_{L2}, v_{ab}, and i_{Lr} and Fig. 16 shows secondary v_{de}, v_{ef}, i_d, and i_f under three conditions. As can be seen, i_{L1} and i_{L2} are interleaved, and i_{Lr}, i_d, and i_f have the same or complementary shape. It has a good agreement with the theoretical analyses.

Fig. 17 shows the waveforms of V_{o1}, V_{o2}, I_{o1}, and I_{o2} and Fig. 18 shows I_{in} under Conditions A–C. As can be seen, regardless of the load condition, both of V_{o1} and V_{o2} can naturally maintain at 190 V, realizing the auto-voltage-sharing. Meanwhile, the input current ripple-free can be achieved.

Based on the theoretical analysis, the ZVS can always be realized. Hence, only the ZVS under Condition C is presented, as shown in Fig. 19. As can be seen, all switches achieve ZVS.

To validate the ZVS under light load condition, the ZVS performance under light load condition is also tested. Fig. 20 shows the ZVS turn-ON under 14.44% load (500 Ω) conditions. It can be seen that ZVS turn-ON can always be achieved for all switches.

Figs. 21 and 22 show the experimental results when P_{o1} changes from full load to no load and back to full load. Under the step load change, it can be observed that V_{o1} and V_{o2} are well-regulated to maintain voltage balancing rapidly.

Fig. 23 shows the experimental results when V_{in} changes from 60 to 40 V and back to 60 V. Under the step input voltage change, it can be observed that V_{o1} and V_{o2} are also well-regulated to maintain voltage balancing rapidly.

The histogram of the theoretical loss is shown in Fig. 24. As can be seen, the transformer losses and boost inductors losses account for the majority of the total losses. When the load is unbalanced, due to the C_{bp} and C_{bs}, the losses of primary side components remain unchanged. But the copper losses of T_{r2} and the conduction losses of S_3 and S_4 increased. Therefore, the total losses under the unbalanced load are greater than those under the balanced load.

Fig. 25(a) shows the measured efficiency curves of different P_o and V_{in} under balanced load conditions. The maximum efficiency is 96.4%. When V_{in} is 40 V, the efficiency is slightly lower than that at 60 V. Fig. 25(b) shows the efficiency curve when one output port is no load and the other port power changes. It can be seen that when P_o is same, under extremely unbalanced load conditions, the efficiency slightly decreases.

V. Comparison

To show the advantage compared to the prior art, the input current ripple cancellation methods proposed in [27], [28], and [29] are taken as examples, where the current-fed structure is used to reduce the input current ripple. In [27], to control the output power of the converter, the duty cycle of the primary side is not 0.5. Thus, the ripple of two boost inductors is not complementary. A small current ripple still exists in the input current. In [28], due to the three-phase structure, more switches and transformers are needed, and the duty cycle of the primary side is also not 0.5, so that the transfer power can be adjusted. In [29], the duty cycle of the primary side switches is 0.5. Thus, the ripple of the input current can be cancelled by the current-fed structure. However, to achieve a wider range of ZVS turn-ON, two auxiliary switches are added to achieve the extended voltage match, leading to a more complex control strategy. In the proposed converter, the ripple of the input current can also be cancelled, and with two different operating modes, full-range ZVS can be achieved with fewer switches and an easier control strategy. In Table IV, the comparison of the proposed converter with the other three solutions is provided.

A comparison between the proposed converter and those having an output bipolar voltage with self-balancing ability is provided. In [14], with the help of two voltage-balancing inductors, the bipolar voltage can be balanced with no auxiliary structures. However, as the number of inductors increases, the power density of the converter decreases. Furthermore, the full-range ZVS turn-ON cannot be achieved for [14]. In [17], to balance the bipolar output voltage, an extra control loop is added, which makes the control strategy of the converter more complex, and this converter increases the number of switches, which increases the cost. Moreover, the full range of ZVS cannot be achieved. In [22], to reduce the number of inductors, this topology uses the magnetizing inductor of the transformer to balance the bipolar output voltage. However, a dc bias exists in the transformer, which may cause magnetic saturation. And all three of these topologies cannot reduce the input current ripple. In the proposed converter, with a full-range ZVS region, the bipolar output voltage can be balanced, and the input current ripple can be cancelled. In Table V, the comparison

of the proposed converter with the other three solutions is provided.

VI. Conclusion

In this article, a novel DAB-based bipolar dc–dc converter is proposed, which can achieve current ripple-free on the input side and auto-voltage-balancing on the bipolar output side. By adjusting the phase shift angles between the primary and secondary switches, all of the switches can achieve ZVS in a wide range, as well as a wide range of power transmission. Finally, all the theoretical analysis results are well verified by the built 1-kW prototype.

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