Fixed-Frequency K+2D Modulation of Modular Multilevel Resonant DC/DC Converter for All Submodule ZVS Operation

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***Abstract*—Modular multilevel resonant dc–dc converters (MMRDCs) are increasingly recognized as competitive solutions for medium-voltage to low-voltage (MV-LV) conversion with wide input ranges. However, these systems often face challenges of low conversion efficiency due to the inability to achieve sufficient soft-switching or excessive conduction loss. This article proposes a novel fixed-frequency K+2D control strategy, which combines submodule (SM) number K and 2 SMs adjusting width D. This approach ensures zero-voltage switching (ZVS) on for all SMs, thereby reducing switching losses. It also effectively reduces the loop resonant current, leading to lower conduction losses. The fixed-frequency control method simplifies the magnetic components design. Simulations are conducted to demonstrate the performance under conditions of 9 to 18 kV input, 200 kW power, and 750 V output. Experimental results from a prototype further validate the feasibility and effectiveness.**

***Index Terms*—Fixed-frequency k+2D control, LLC converter, modular multilevel resonant dc–dc converters (MMRDCs), soft switching, wide input range.**

I. Introduction

MEDIUM-VOLTAGE direct current (MVdc) systems are increasingly adopted in various applications due to their high efficiency, cost-effectiveness, reliability, and flexibility. Typical applications include renewable energy generation, rail-based electric transportation, marine power systems, and data centers [1], [2], [3], [4]. A critical component in dc distribution systems is the medium-voltage to low-voltage (MV-LV) dc power electronic converter, which facilitates voltage conversion between different voltage levels [5], [6], [7], [8].

Since individual semiconductor devices are hard to withstand voltages out range of 10 kV, these converters require multiple modules connected in series to share the medium-voltage stress. The isolation conversion schemes for MV-LV applications can be classified into three types: the input-series output-parallel (ISOP) cascaded H-bridge, the series-connected-device dc/dc converter, and the modular multilevel resonant dc/dc converter (MMRDC).

The input-series output-parallel (ISOP) [9], [10] cascaded H-bridge configuration offers advantages such as modularity and ease of control. However, each module in this structure incorporates a high-frequency transformer, which must operate under high voltage stress (around 10 kV). This requirement significantly increases the size of the modules and limits the applicability of ISOP structures in high-voltage, high-power-density scenarios [7], [11], [12].

Series-connected-device topologies are also used as the MV side to withstand medium-voltage and achieve soft-switching operation, but the dynamic voltage balance of multiple devices in series is still complicated to achieve [13], [14], [15].

The combination of modular multilevel converters (MMC) and resonant converters has emerged as a highly competitive solution for MV-LV conversion systems. The MMC topology effectively manages MV voltage stresses, while the resonant topology facilitates soft switching and high-efficiency energy conversion. By adjusting the number of inserted submodules (SMs), operating frequency, and ramp-up slope, this approach accommodates a wide range of input voltage variations [16], [17], [18], [19], [20], [21], [22], [23].

Gray et al. [16] proposed the CS-MMC structure, which was further improved in 2022 with the addition of isolation transformers. Additionally, Shao et al. [17] proposed a double strings MMRDC for MV-LV conversion in subsea observation networks, with Sheng et al. [18] refining the topology. Cui et al. [24] further improved the bidirectional characteristics of this topology. Expanding the soft-switching operation range is used by MMRDC to improve conversion efficiency [19], [20]. The topology in work [25] used four switching devices on the secondary side, enabling bidirectional power flow of modular multilevel dc transformer (MM-DCT). The exploration of internal-phase-shifted control, trapezoidal current control,

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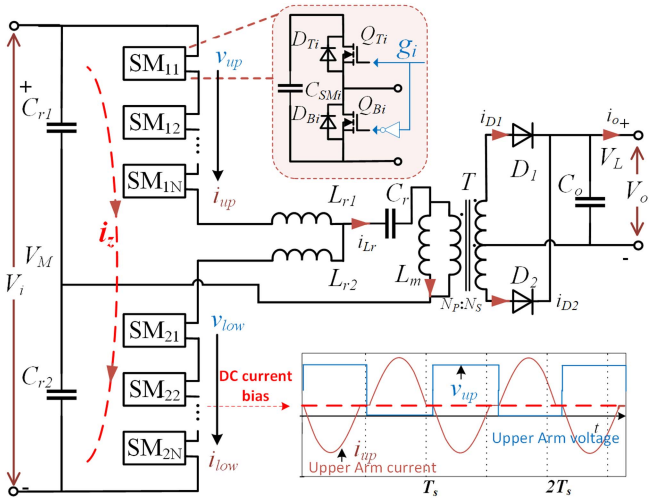

Fig. 1. Double strings MMRDC.

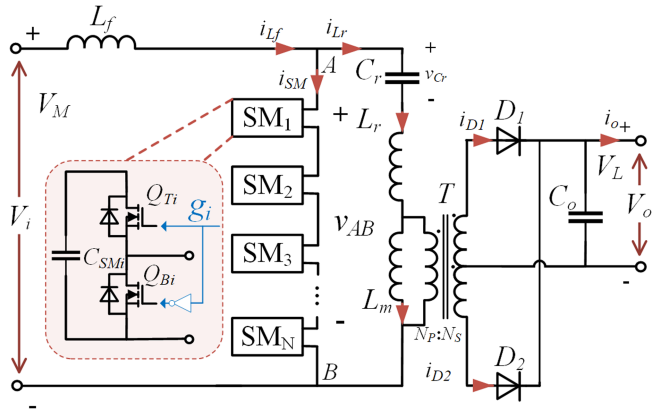

Fig. 2. Single string MMRDC.

TABLE I
SOFT SWITCHING STATES OF DOUBLE STRINGS MMRDC

Device	Q_{Ti}	D_{Ti}	Q_{Bi}	D_{Bi}
Switching status	ZVS ON	Hard OFF	Hard ON	No current

and dual-phase-shifted control aim to extend the range of soft switching operations are presented [21], [22], [23].

The MMRDC topology can be divided into types as double-strings and single-string.

The typical double-series topology is shown in Fig. 1. Similar to MMC, a dc component i_z exists between the two series of converter arm. This dc component prevents half of the SM switches from achieving soft switching, leading to higher switching losses. The specific conditions for soft switching are summarized in Table I. The switching status corresponds to the condition where the magnetizing inductance is sufficiently large and the magnetizing current can be neglected as depicted in [18]. Some dual-strings structure MMRDCs have 50% SM switches that are unable to achieve soft switching.

Duan et al. [26] proposed a single-series SM-based *LLC* converter structure, as illustrated in Fig. 2. The PFM+K control method requires a small $m = L_m/L_r$ value to ensure a wide input voltage range [10], [27], [28], [29], which results in the use of smaller magnetizing inductance L_m. A smaller L_m leads to higher resonant currents and conduction losses. Furthermore, variable-frequency control necessitates designing the magnetic core for the lower operating frequency, which reduces core utilization, increases the converter's volume, and raises costs.

Is it possible to both address the issue of 50% switches zero-voltage switching (ZVS) and conduction loss inherent in the PFM+K control method?

This article proposes a novel K+2D control scheme based on single string MMRDC as shown in Fig. 2. This control method operates at a fixed resonant frequency and adjusts the output voltage by changing the number of inserted SMs (denoted as K) and duty cycle D of 2 SMs. The proposed K+2D control scheme offers the following advantages.

1) *All switches ZVS* ON: By combining the control of K and 2 duty cycle D, the system can achieve soft switching for all switches across the full power range and full voltage gain, significantly reducing switching losses and improving conversion efficiency.
2) *Reduced loop current:* A larger magnetizing inductance L_m can be designed to minimize magnetizing current and reduce conduction losses. Unlike traditional *LLC* circuits, the ratio $m = L_m/L_r$ has minimal impact on system gain, thus enabling the use of larger L_m values to decrease conduction losses.
3) *Fixed-frequency modulation:* The operating frequency remains constant, which simplifies the design of resonant inductors and transformers.

The rest of this article is organized as follows. Section II introduces the MMRDC topology and the proposed K+2D modulation. In Section III, the converter's operating modes and performance are analyzed, followed by a simulation validation. Section IV presents experimental results from a prototype MMRDC. Finally, Section V concludes this article.

II. TOPOLOGY AND MODULATION

As illustrated in Fig. 2, the MMRDC topology comprises a filter inductor L_f, a single-string series-connected SM branch (SSB), a resonant capacitor C_r, and a resonant inductor L_r on the MV side. On the LV side, a half-rectifier bridge is employed, interconnected with the MV section through a high-frequency transformer T with magnetizing inductance L_m. The input voltage V_i is supplied from the MV dc source on the left, while the output voltage V_o is delivered to the LV dc load on the right.

The input dc voltage is converted into a square wave through the insertion and extraction of SMs. A filter inductor (L_f) is incorporated into the input arms to suppress circulating currents within the dc loop. The voltage V_{AB} represents the output of the SSB.

On the MV side, the gate signals for the top and bottom switches in each SM are complementary, with sufficient dead

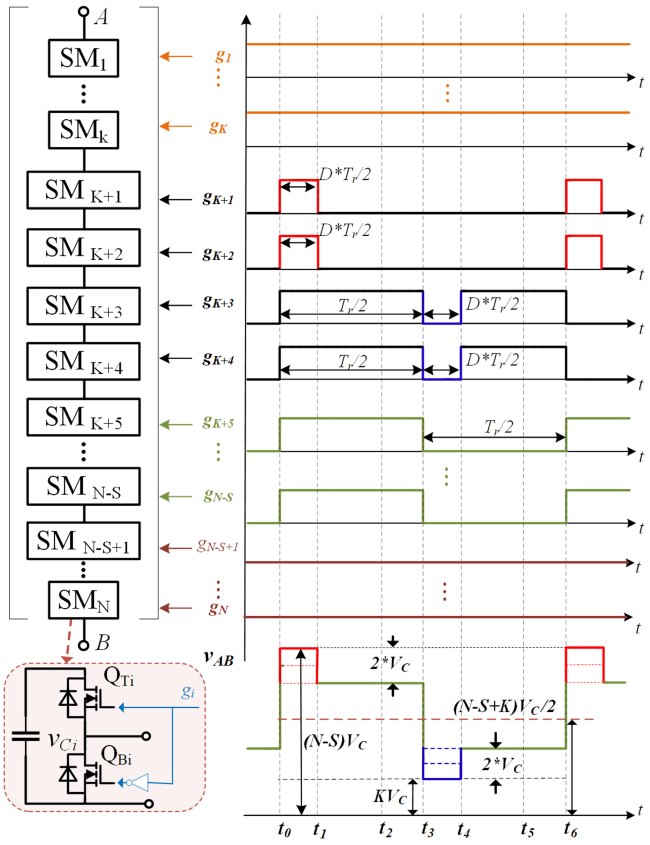

Fig. 3. Key waveforms of the proposed K+2D modulation.

time to prevent overlap. When capacitors from varying numbers of SMs are connected across points A and B, the voltage V_{AB} fluctuates similarly to the output of a full-bridge converter. The output voltage can be regulated by adjusting the number of inserted SMs and the width of the input pulses.

Applying Kirchhoff's current law (KCL) at point A in Fig. 2, the current through the SSB is by $i_{SM} = i_{Lf} - i_{Lr}$, where i_{Lf} denotes the MV terminal current, and i_{Lr} represents the resonant cavity current.

A. Modulation Strategy

As depicted in Fig. 3, N SMs are employed between points A and B within the MMRDC. The variables g_i and V_{Ci} represent the driving signal and the voltage across the capacitor of the ith SM, respectively, for i ranging from 1 to N. The switching frequency, denoted by f_r, is set to the resonant frequency and remains fixed.

In Fig. 3, the driving signals g_1 to g_K are sustained at a high level throughout the entire switching period, thereby ensuring the continuous insertion of capacitors in SMs SM_1 to SM_K.

For SMs SM_{K+1} and SM_{K+2}, the driving signals g_{K+1} and g_{K+2} are high from time t_0 to t_1. The duty cycle is D for the first half of the cycle, while the second half is at a low state. The high level part of g_{K+1} and g_{K+2} is highlighted in red, corresponding to the maximum segment of V_{AB}.

Conversely, the driving signals g_{K+3} and g_{K+4} are active during the first half of the cycle, with a duty cycle of 1-D for the second half. The inactive phase of g_{K+3} and g_{K+4} is indicated in blue, representing the segment of V_{AB} with the minimum voltage.

SMs SM_{K+5} to SM_{N-S} operate with a constant duty cycle of 50% for their driving signals g_{K+5} to g_{N-S}.

Finally, the driving signals g_{N-S+1} to g_N are maintained at a low level throughout the entire switching period, ensuring the continuous extraction of capacitors in SMs SM_{N-S+1} through SM_N. This continuous extraction is denoted by the variable S, and it is imperative that $K = S$ in the proposed modulation scheme.

As a result of the volt-second balance of L_f, (1) could be obtained, where T_r is the switching period and $T_r = 1/f_r$, V_C denotes average voltage of all SMs. D is the proportion of the adjustment ratio to half a period, ranging from [0,1]

$$(V_i - (N - S - 2D)V_C)\,T_r/2 + (V_i - (K + 2D)V_C)\,T_r/2 = 0. \tag{1}$$

Using (1), capacitor voltage of SM can be determined via: $V_C = 2V_i/(N - S + K)$. According to the waveform in Fig. 3, the amplitude of V_{AB} can be calculated by (2). V_{AB} is vertically translational symmetric about $(N - S + K)V_C/2$

$$V_{AB}(t) = \begin{cases} (N-S)V_C, & t_0 \le t < DT_r/2 \\ (N-S-2)V_C, & DT_r/2 \le t < T_r/2 \\ KV_C, & T_r/2 \le t < (1+D)T_r/2 \\ (K+2)V_C, & (1+D)T_r/2 \le t < T_r. \end{cases} \tag{2}$$

The voltage V_{AB} serves as the input voltage for the resonant cavity. When $K = S = 0$ and $D = 1$, the root mean square (rms) value of V_{AB} reaches its maximum. As the input voltage increases, the D-value gradually decreases, the value of S and K increases one by one.

As illustrated in Fig. 4, assuming K is increased by one when $D = 0$, at near-zero D values, modules SM_{K+1} and SM_{K+2} are extracted at time t_1, where $i_{SM} > 0$. At this point, t_1 falls within the ZVS-lost region (indicated in red). Thus soft switching cannot be achieved for modules SM_{K+1} to SM_{K+4}.

However, as shown in Fig. 4(b), setting the D switching time within the green region (e.g., switching K at $D = 1/3$) allows soft switching for modules SM_{K+1} to SM_{K+4}. When D approaches 1/3, modules SM_{K+1} and SM_{K+2} are extracted at time t_2, where $i_{SM} < 0$. Here, t_2 falls within the ZVS-on green region, thus enabling soft switching for modules SM_{K+1} to SM_{K+4}.

Therefore, the key of achieving ZVS for all switches in this $K + 2D$ control method is to ensure switching to $K + 1$ before the red ZVS-lost region appears as D decreases (e.g., setting this threshold at $D = 1/3$). This approach also should enable continuous dc voltage gain transformation.

B. Operating Principle

As shown in Fig. 5, the proposed modulation of MMRDC can be divided into two half-cycles: $t_0 - t_3$ and $t_3 - t_6$. Since two half-cycles are symmetric, only $[t_0 - t_3]$ is introduced.

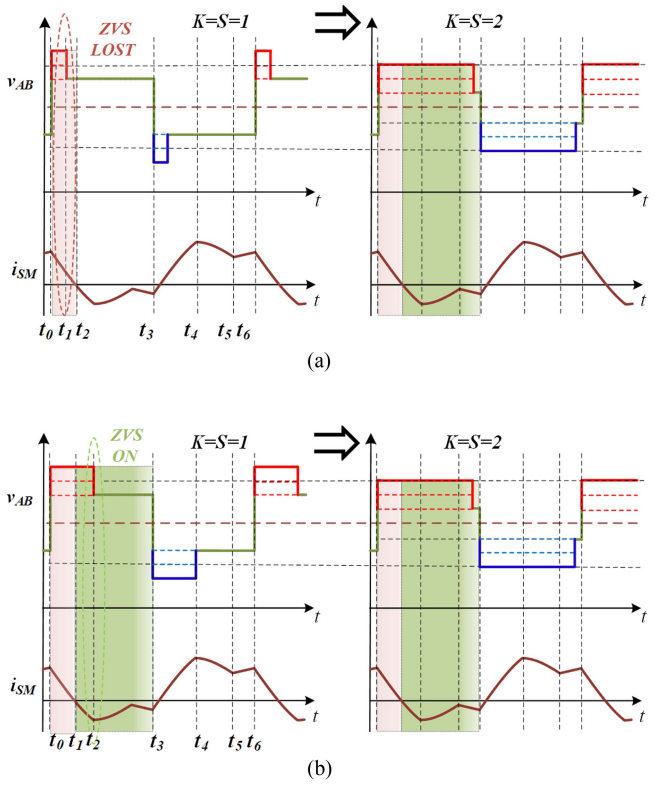

Fig. 4. Key waveforms of K switching with different D value. (a) $K \to K+1$ when $D \to 0$. (b) $K \to K+1$ when $D \to 1/3$.

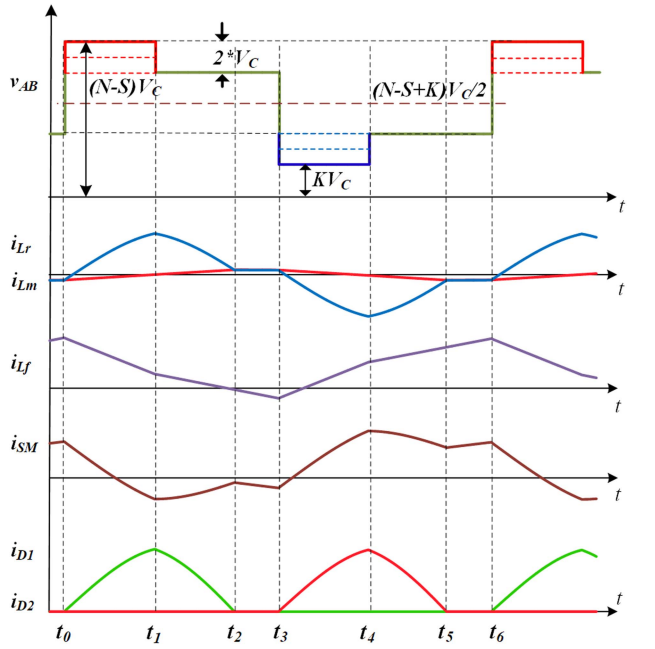

Fig. 5. Key waveforms of the MMRDC with the proposed K + 2D modulation.

Resonant frequency f_r and resonant impedance Z_r and Z_m of the resonant tank are defined as follows:

$\omega_r = 1/\sqrt{L_r \cdot C_r}$, $f_r = \omega_r/2\pi$, $Z_r = \sqrt{L_r/C_r}$, $\omega_m = 1/\sqrt{(L_r + L_m) \cdot C_r}$, $f_m = \omega_m/2\pi$, $Z_m = \sqrt{(L_r + L_m)/C_r}$.

There are three operating steps during half a switching cycle. Since V_{AB} between two half-cycles is symmetric about $(N - S + K)V_C/2$ and the direct current is isolated by the C_r, i_{Lr} and i_{Lm} are symmetrical about the time axis t.

N_{in} is employed to denote the number of SMs engaged in voltage distribution, calculated as $N_{in} = N - S$.

Mode 1 [$t_0 - t_1$]: At time t_0, all g_i are activated except for S SMs, and N_{in} SMs are inserted into the circuit. The string voltage V_{AB} is equal to $N_{in}V_C$. The resonant current i_{Lr} is negative, while the string current i_{SM} is positive. The resonance between L_r and C_r begins. During the interval $[t_0 - t_1]$, N_{in} SMs are inserted, causing V_{AB} to increase to $N_{in}V_C$ after t_0. Meanwhile, i_{D1} starts to rise from zero. The top switches Q_{Ti} of the SMs inserted during this interval can achieve ZVS ON as $i_{SM} > 0$. The state equation governing the circuit in this mode is as follows:

$$\begin{cases} L_r \frac{di_{Lr}(t)}{dt} = -v_{Cr}(t) + N_{in}V_C - nV_o \\ L_m \frac{di_{Lm}(t)}{dt} = nV_o \\ C_r \frac{dv_{Cr}(t)}{dt} = i_{Lr}(t). \end{cases} \tag{3}$$

Mode 2 [$t_1 - t_2$]: At time t_1, switches g_{K+1} and g_{K+2} are turned OFF, and $(N_{in} - 2)$ SMs remain connected to the circuit. The string voltage V_{AB} stabilizes at $(N_{in} - 2)V_C$. The resonant current i_{Lr} is positive and the string current i_{SM} negative, and the resonance between L_r and C_r continues until t_2. The lower switches Q_{BK+1} and Q_{BK+2} are turned ON, and SM_{K+1} and SM_{K+2} are removed. The state equation is expressed as

$$\begin{cases} L_r \frac{di_{Lr}(t)}{dt} = -v_{Cr}(t) + (N_{in} - 2)V_C - nV_o \\ L_m \frac{di_{Lm}(t)}{dt} = nV_o \\ C_r \frac{dv_{Cr}(t)}{dt} = i_{Lr}(t). \end{cases} \tag{4}$$

Mode 3 [$t_2 - t_3$]: At time t_2, the resonant current i_{Lr} equals the magnetizing inductor current i_{Lm}, initiating resonance between $L_r + L_m$ and C_r. During this period, the string voltage V_{AB} remains constant at $(N_{in} - 2)V_C$. The i_{Lr} is positive, while i_{SM} becomes negative. The resonance between $L_r + L_m$ and C_r persists until t_3. The state equation is as follows:

$$\begin{cases} (L_m + L_r)\frac{di_{Lr}(t)}{dt} = -v_{Cr}(t) + (N_{in} - 2)V_C \\ i_{Lm}(t) = i_{Lr}(t) \\ C_r \frac{dv_{Cr}(t)}{dt} = i_{Lr}(t). \end{cases} \tag{5}$$

Mode 4 [$t_3 - t_4$]: At time t_3, switches g_1 to g_K are turned ON, while the other SMs are turned OFF. As a result, K SMs are inserted into the circuit. Resonance begins between L_r and C_r. The i_{Lr} is positive, and i_{SM} is negative. The string voltage V_{AB} decreases from $(N_{in} - 2)V_C$ to KV_C after t_3, and i_{D2} rises from zero. The lower switches Q_{Bi} of the SMs can achieve ZVS ON, as $i_{SM} < 0$.

Mode 5 [$t_4 - t_5$]: At time t_4, the lower switches Q_{BK+3} and Q_{BK+4} are turned ON, inserting SM_{K+3} and SM_{K+4} into the circuit. $K + 2$ SMs are inserted. The $i_{Lr} < 0$, while $i_{SM} > 0$. Resonance between L_r and C_r continues until t_5.

Mode 6 [$t_5 - t_6$]: At time t_5, the resonant current i_{Lr} equals the magnetizing inductor current i_{Lm}, initiating resonance between $L_r + L_m$ and C_r. During this period, $(K + 2)$ SMs remain inserted, and the string voltage V_{AB} stabilizes at

$(K+2)V_C$. The string current i_{SM} remains positive, and the resonance between $L_r + L_m$ and C_r continues until t_6.

III. Converter Performance Analysis

A. Voltage Gain Analysis

The conventional approach to determining voltage gain is the fundamental harmonic approximation (FHA) method [30]. However, this method overlooks the influence of higher order harmonics in the voltage and current waveforms, resulting in reduced accuracy. To enhance precision in gain analysis, this study adopts a time-domain analysis technique [31].

By solving the differential equations for Mode 1 to Mode 3, (6) and (7) shown at the bottom of this page,–(8) can be obtained

$$i_{Lm}(t) = \begin{cases} i_{Lr}(t_0) + (nV_o/L_m)t & t_0 \le t < t_2 \\ i_{Lr}(t) & t_2 \le t < t_3. \end{cases} \tag{8}$$

Due to the waveforms of $v_{Cr}(t)$ and $i_{Lr}(t)$ are half-wave symmetric signals, the following relationships as shown in (9) can be established. At time t_2, both L_r and L_m are involved in resonance. These relationships are expressed as

$$\begin{cases} i_{Lr}(t_0) = -i_{Lr}(t_3) \\ v_{Cr}(t_0) = -v_{Cr}(t_3) \\ i_{Lr}(t_2) = i_{Lm}(t_2) \end{cases}. \tag{9}$$

Additionally, the average value of the difference between the resonant current i_{Lr} and the magnetizing current i_{Lm} over half a cycle is the output average current. Therefore, the output current can be expressed as

$$\frac{1}{T_r}\int_0^{T_r} \left(i_{L_r}(t) - i_{L_m}(t)\right) dt = I_o/n = \frac{V_o}{nR_o} = \frac{8nV_oQ}{Z_r\pi^2}, \tag{10}$$

$$Q = \pi^2 Z_r/(8n^2 R_o). \tag{11}$$

Since (6)–(10) form a transcendental equation, it is difficult to obtain an explicit analytical relationship for M in terms of K and D. Therefore, we employed a numerical analysis method to determine the relationship among K, D, and M.

By numerically solving (6)–(10) for various values of N, K, S, D, and V_i, the four parameters ($i_{Lr}(t_0)$, $v_{Cr}(t_0)$, t_2, and V_o) can be determined. This allows the derivation of the gain ratio $M = nV_o/V_i$ of the dc converter as a function of K and duty cycle D, under varying conditions of the quality factor Q and inductor ratio $m = i_{Lm}/i_{Lr}$, as shown in Fig. 6.

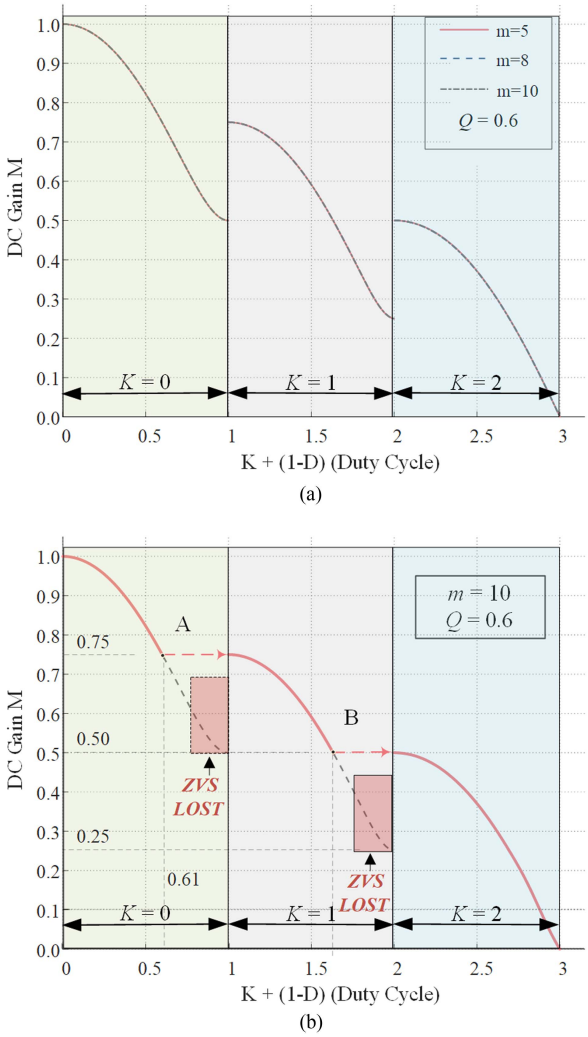

Fig. 6. Gain curves versus K+2D for MMRDC. (a) Q=0.6. (b) m=10.

The simulation parameters are configured as follows: the circuit input voltage is set to 300 V, and the transformer turns ratio is 3:1:1. The resonant tank is defined by $L_r = 338\,\mu$H and $C_r = 187$ nF, with the switching frequency f_s equaling the resonant frequency $f_r = 20$ kHz.

$$i_{Lr}(t) = \begin{cases} i_{Lr}(t_0)\cos(\omega_r(t-t_0)) - (v_{Cr}(t_0) - (N_{in}V_C - nV_o))\frac{1}{Z_r}\sin(\omega_r(t-t_0)), & t_0 \le t < t_1 \\ i_{Lr}(t_1)\cos(\omega_r(t-t_1)) - (v_{Cr}(t_1) - ((N_{in}-2)V_C - nV_o))\frac{1}{Z_r}\sin(\omega_r(t-t_1)), & t_1 \le t < t_2 \\ i_{Lr}(t_2)\cos(\omega_m(t-t_2)) - (v_{Cr}(t_2) - (N_{in}-2)V_C)\frac{1}{Z_m}\sin(\omega_m(t-t_2)), & t_2 \le t < t_3 \end{cases} \tag{6}$$

$$v_{Cr}(t) = \begin{cases} i_{Lr}(t_0) & Z_r\sin(\omega_r(t-t_0)) \\ & +(v_{Cr}(t_0) - (N_{in}V_C - nV_o))\cos(\omega_r(t-t_0)) + (N_{in}V_C - nV_o), & t_0 \le t < t_1 \\ i_{Lr}(t_1) & Z_r\sin(\omega_r(t-t_1)) \\ & +(v_{Cr}(t_1) - ((N_{in}-2)V_C - nV_o))\cos(\omega_r(t-t_1)) + ((N_{in}-2)V_C - nV_o), & t_1 \le t < t_2 \\ i_{Lr}(t_2) & Z_m\sin(\omega_m(t-t_2)) \\ & +(v_{Cr}(t_2) - (N_{in}-2)V_C)\cos(\omega_m(t-t_2)) + ((N_{in}-2)V_C), & t_2 \le t < t_3. \end{cases} \tag{7}$$

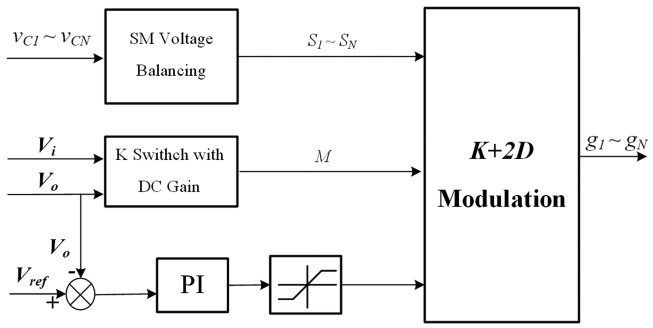

Fig. 7. Voltage balancing plus feedback control to regulate the MMRDC output voltage.

Fig. 6 illustrates the dc voltage gain for different values of K and D under the K+2D modulation method.

As shown in Fig. 6(a), for a fixed Q value, and with $m = L_m/L_r$ taking values of 5, 8, and 10, the gain curves of M for varying K and D inputs are nearly overlapped when using the proposed K+2D modulation method. In contrast, for conventional *LLC* resonant converters utilizing PFM+K control, the m value is closely related to the dc voltage gain M, and excessively large m values may fail to provide a sufficiently high dc gain. However, as illustrated in Fig. 6(a), with the K+2D control method, the m value has negligible impact on the gain achieved by the converter. Therefore, selecting a larger L_m value can reduce the effective value of i_{Lm}, thereby decreasing the conduction losses in the system.

Fig. 6(b) shows the system operation parameters with $m = 10$ and $Q = 0.6$. When $K = 0$, as D changes from 1 to 0, the output gain decreases from 1 to 0.5. Similarly, when $K = 1$ and D changes from 1 to 0, the output gain decreases from 0.75 to 0.25.

As depicted in Fig. 6(b), when $K = 0$ and $1 - D \approx 0.9$, SM_{K+1} and SM_{K+2} switch, operating in the red gain region. Since $i_{SM} > 0$, ZVS loss occurs for these two SMs.

To avoid this ZVS loss, the system switches the K value at point A, where the gain is approximately $M = 0.75$ (or slightly lower). At $M = 0.75$, $1 - D = 0.61$. At point A, since $i_{SM} < 0$, SM_{K+1} and SM_{K+2} can achieve ZVS turn-ON. The switching condition at point B, where $M = 0.5$, is similar to that at point A. For other SM modules during turn-ON and turn-OFF, i_{SM} always satisfies the ZVS turn-ON condition. Therefore, using the proposed K+2D control method, all switches can achieve ZVS turn-ON.

B. Output Voltage Control Scheme

Fig. 7 illustrates the block diagram of the MMRDC with the proposed output voltage control scheme. The scheme incorporates an SM voltage balancing that samples the SM capacitor voltage V_{C_i} to regulate the output voltage V_o by altering the value of K and modulating duty cycle D of g_{k+1} to g_{k+4}. Within the feedback loop, V_o is compared with its reference V_{ref}, and any discrepancy is conveyed to a PI compensator to fine-tune the switching K+2D.

As shown in the gain curves Fig. 6, the system's dc output gain is a piecewise monotonically increasing function of the input control parameters K+2D. This feature enables the adoption of a PI feedback control strategy to stabilize the output voltage at the desired target value. Specifically, by adjusting the values of K and D, the number of SMs connected to the resonant tank and the pulsewidth can be modified, thereby regulating the output voltage. The underlying implementation is achieved through the control signals (g_1 to g_N) of the SMs.

However, particular attention must be paid to the switching points of the K values and the voltage balance of the capacitors in each SM module.

As shown in Fig. 6(b), overlapping gain regions exist when D transitions from 1 to 0 under different K values. When the gain reaches $M = K/N$, such as at points A and B, the control parameter transitions from K to $K + 1$ for the SM modules. This ensures the continuity of both the control parameters and the output gain. Furthermore, at these points, as $i_{SM} < 0$, SMs SM_{K+1} and SM_{K+2} achieve ZVS on.

The SM voltage balancing strategy is adapted from the algorithm described in [17]. This approach involves sorting the SM capacitor voltages to establish their relative order. Simultaneously, the voltage variation for each SM is calculated as the difference between its current voltage and its previous value. Gate signals are then allocated such that SMs with lower voltages are paired with larger voltage variations, while those with higher voltages receive smaller variations. This method ensures effective balancing of SM capacitor voltages across varying voltage gain and load conditions.

C. Soft Switching Analysis

In the MMRDC topology, the voltage across the filter inductor L_f alternates between positive and negative values. The average voltage applied to L_f can be expressed as

$$|v_{Lf}| = \frac{(N - S - K - 2D)V_i}{(N - S + K)}. \tag{12}$$

Using this voltage, the current ripple of L_f is calculated as

$$\Delta i_{Lf} = \frac{|v_{Lf}|}{2L_f f_r} \tag{13}$$

where f_r is the switching frequency.

At steady state, the input power and output power are balanced. Therefore, the average input current is by

$$I_{Lf} = P_o/V_{in} \tag{14}$$

where P_o is the output power and V_{in} is the input voltage.

The instantaneous current of L_f can be further derived as

$$i_{Lf}(t) = \begin{cases} I_{Lf} + \frac{|v_{Lf}|}{L_f}\left(t - \frac{T_r}{4}\right), & 0 \le t \le \frac{T_r}{2} \\ I_{Lf} + \frac{|v_{Lf}|}{L_f}\left(\frac{3T_r}{4} - t\right), & \frac{T_r}{2} < t \le T_r. \end{cases} \tag{15}$$

The current flowing through the SM valve strings, $i_{SM}(t)$, can be determined by subtracting the resonant inductor current, $i_{Lr}(t)$, from $i_{Lf}(t)$

$$i_{SM}(t) = i_{Lf}(t) - i_{Lr}(t). \tag{16}$$

Expanding $i_{SM}(t)$, we get

$$i_{SM}(t) = \begin{cases} I_{Lf} + \frac{|v_{Lf}|}{L_f}\left(t - \frac{T_r}{4}\right) - i_{Lr}(t), & 0 \le t \le \frac{T_r}{2} \\ I_{Lf} + \frac{|v_{Lf}|}{L_f}\left(\frac{3T_r}{4} - t\right) - i_{Lr}(t), & \frac{T_r}{2} < t \le T_r. \end{cases} \tag{17}$$

At time t_0, i_{Lf} ensures $i_{Lf}(t_0) \gg 0$, thereby guaranteeing $i_{SM}(t_1) > 2C_{oss}V_C$. This condition enables ZVS for the upper switch during the insertion of the SM module. The situation at t_6 is similar to that at t_0.

At time t_3, the design can select i_{Lf} to ensure $i_{Lf}(t_3) < 0$, which results in $i_{SM}(t_3) < -2C_{oss}V_C$. This ensures ZVS for the lower switch during the removal of the SM module.

Time t_1 and t_4 are the PWM edge timing. To achieve ZVS for the SM module, the current $i_{SM}(t) > 0$ at the removal time t_1 and $i_{SM}(t) < 0$ at the insertion time t_4 must be satisfied. Additionally, the parasitic capacitance (C_{oss}) of the switching devices and the dead time (t_d) between the top and bottom switches must be considered. Therefore, the ZVS conditions for the top switch (Q_{Ti}) and the bottom switch (Q_{Bi}) can be expressed as follows:

$$\begin{cases} i_{SM}(t_d) \ge 0 \\ \left|\int_0^{t_d} i_{SM}(t)\,dt\right| > 2C_{oss}V_C \\ i_{SM}(t_1) \ge 0 \end{cases} \tag{18}$$

and for removal

$$\begin{cases} i_{SM}\left(\frac{T_r}{2} + t_d\right) \le 0 \\ \left|\int_{\frac{T_r}{2}}^{\frac{T_r}{2}+t_d} i_{SM}(t)\,dt\right| > 2C_{oss}V_C \\ i_{SM}\left(\frac{T_r}{2} + t_1\right) \le 0. \end{cases} \tag{19}$$

Thus, within a single cycle, the switching of SMs at positions t_0, t_3, and t_6 ensures ZVS for all switches.

However, at positions t_1 and t_4, the edge-switching timing must be sufficiently delayed to ensure that ZVS is achieved during edge transitions.

This indicates that, under the premise of maintaining continuous dc gain, switching the K value at sufficiently large D values allows all SM switches to achieve ZVS.

The value D = 1/3 in Fig. 6(b) is an approximate estimate to illustrate the control method. For specific designs, the method for determining this minimum D boundary during K-switching is as follows.

First, the current waveform $i_{SM}(t)$ in Fig. 5 of manuscript is derived through modeling and calculations presented in Sections II and III. By numerically solving (6)–(10) for various N, K, S, D, and V_i, the four parameters ($i_{Lr}(t_0)$, $v_{Cr}(t_0)$, t_2, and V_o) can be determined. This implies that the system's $i_{Lr}(t)$ waveform is analytically obtainable. Since the waveform $i_{Lf}(t)$ is also known, the expression $i_{SM}(t) = i_{Lf}(t) - i_{Lr}(t)$ can be computed.

Next, the critical point where $i_{SM}(t)$ transitions from positive to negative is identified in in Fig. 5 of the manuscript. The corresponding D value that satisfies the soft-switching conditions in (18)–(19) of Section III-C determines the minimum boundary of D. This boundary corresponds to the ZVS LOST region (red area) in Fig. 6(b).

TABLE II
CIRCUIT PARAMETERS OF THE SIMULATION

Parameters	Value
MV terminal voltage V_i	9∼18 kV
LV terminal voltage V_o	750 V
Transformer turns ratio n	12:1
Rated power P_w	200 kW
Number of SMs N	32
Filter inductance L_f	10 mH
SM capacitance C_{SM}	150 μF
Switching frequency f	10 kHz
Resonant capacitance C_r	81 nF
Resonant inductance L_r	3.12 mH
Magnetizing inductance L_m	31.2 mH
LV terminal capacitance C_o	3 mF
Primary switches	C3M0021120K 1200 V / 100 A from Wolfspeed
Diodes D1/D2	CAS300M17BM2 1700 V / 325 A from Wolfspeed

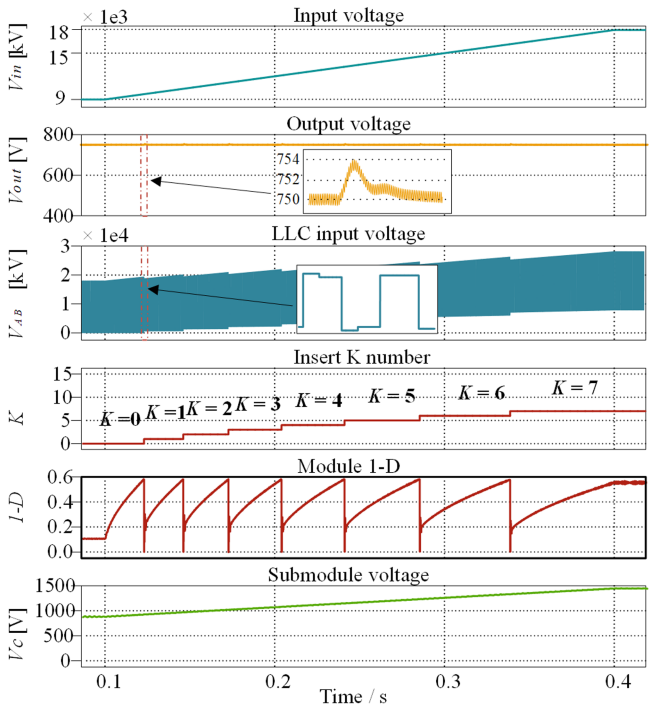

Fig. 8. Dynamic waveform of the proposed fixed frequency K+2D control.

D. Simulation Verifications

To validate the proposed K+2D control strategy, an MMRDC simulation system was constructed using the PLECS software. The simulation parameters are specified in Table II.

Fig. 8 illustrates the simulation results for an input voltage V_i varying from 9 to 18 kV over 0.4 seconds under a full-load output power condition of $P_o = 200$ kW. Despite the wide input voltage range, the output voltage v_o remains regulated at 750 V. Although there are minor voltage fluctuations during K-value

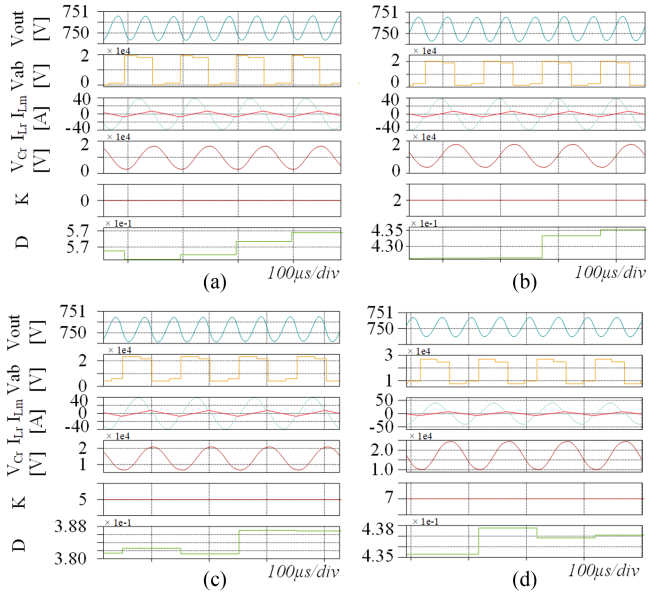

Fig. 9. Simulation steady-state voltage and current waveforms under full load with various K and D. (a) $K = 0$. (b) $K = 2$. (c) $K = 5$. (d) $K = 7$.

switching, these fluctuations are negligible, measuring approximately 4 V, or 0.53% of 750 V. Such a 0.5% variation has an insignificant impact on low-voltage stability.

The corresponding zoomed-out simulation results are presented in the Fig. 9, showing the detailed operating waveforms for (a) $K = 0$, (b) $K = 2$, (c) $K = 5$, and (d) $K = 7$. It can be observed that under different K values, the output remains stable around the target value of 750 V.

The feedforward control adjusts v_o by updating K as shown in Fig. 7, while the feedback control refines v_o by modulating double SM pulsewidth D-value to correct any deviations.

As the input voltage rises from 9 to 18 kV, the average value of the resonant cavity input voltage V_{AB} gradually increases. However, the amplitude of the ac component of V_{AB} remains largely unchanged.

To further evaluate the losses and conversion efficiency in the simulation environment, we established thermal models of the main components in the PLECS simulation software. The losses of the conversion system were analyzed. When the input power is 200 kW, the total losses of all MOSFETs are 2.16 kW, the losses of the output diodes are 1.02 kW, the losses of the filter inductor L_f are 0.92kW, the losses of the SM capacitor are 0.21 kW, and the losses of the high-frequency transformer are 0.95 kW. Finally, the calculated efficiency of the converter is 97.37% .

At an input voltage of 9 kV, $K = S = 0$, meaning that all SMs are fully engaged in modulation. As the voltage increases, the D-value, representing the double SM pulsewidth adjustment, progressively rises. When D reaches approximately 0.6, the K-value transitions to $K + 1$.

Although further increasing D could accommodate the rising input voltage, excessively high D-values lead to the loss of ZVS in certain SM modules. Thus, at $1 - D \approx 0.6$, the K-value switches to $K + 1$. As shown in the gain diagram, the K+2D control method ensures overlap in the dc gain of K and $K + 1$, enabling K-value switching before ZVS is lost while maintaining continuous output gain.

As depicted in Fig. 6(b), during K-value switching, the $1 - D$ transition point occurs near 0.6, allowing all SM modules to achieve ZVS ON. In contrast, as described in [17] and [20], the presence of dc circulating current in the SM string causes 50% of the modules to fail to achieve ZVS ON.

Compared to single-SM $D \to 0$ switching control methods, this approach employs double-SM $D \to 1/3$ switching control. This ensures that all modules achieve ZVS ON during insertion and removal, thereby reducing system switching losses. The voltage across the SM consistently remains below 1.5 kV over an input voltage range of 9–18 kV, demonstrating the practicality and effectiveness of the theoretical design.

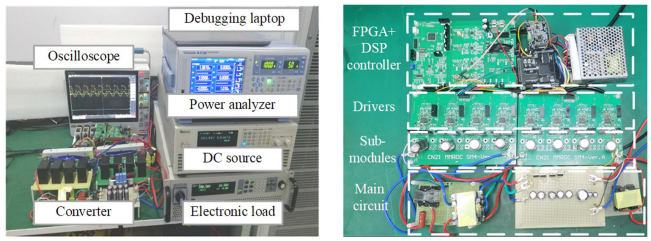

Fig. 10. Experimental prototype and platform.

TABLE III
CIRCUIT PARAMETERS OF THE PROTOTYPE

Parameters	Value
MV terminal voltage V_i	300∼600 V
LV terminal voltage V_o	100 V
Rated power P_w	1 kW
Number of SMs N	8
Filter inductance L_f	0.75 mH
SM capacitance C_{SM}	20 μF
Switching frequency f	20 kHz
Resonant inductance L_r	380 μH
Resonant capacitance C_r	166.5 nF
Transformer turns ratio n	43:16
Magnetizing inductance L_m	3.8 mH
LV terminal capacitance C_o	900 μF
Primary switches	IRFP90N20DPBF 200 V 94 A from Infineon
Diodes D1/D2	MBRF40250T 250 V 40 A from LGE

IV. EXPERIMENTAL RESULTS

This section presents the converter prototype and its corresponding experimental results. The prototype operates with an input voltage range of 300–600 V, an output voltage of 100 V, and a rated power of 1 kW. The experimental setup is shown in Fig. 10 and the converter control is implemented using an FPGA+DSP control board. The detailed circuit parameters are provided in Table III.

A. Steady-State Experimental Results

Fig. 11 presents steady-state waveforms under different input voltages with 1 kW output power. Fig. 11(a) shows the key

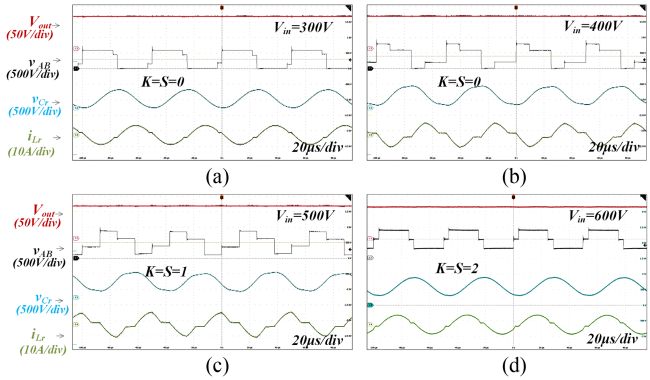

Fig. 11. Measured steady-state voltage and current waveforms under full load with various input voltages. (a) $V_{in} = 300$ V. (b) $V_{in} = 400$ V. (c) $V_{in} = 500$ V. (d) $V_{in} = 600$ V.

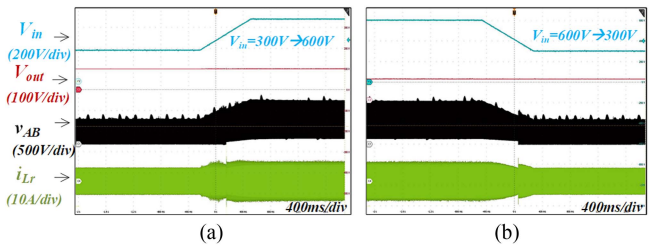

Fig. 12. Dynamic performance of the MMRDC in response to step changes in input voltage. (a) Step increase of input voltage from 300 to 600 V. (b) Step decrease of input voltage from 600 to 300 V.

waveforms at an input voltage of 300 V, where $K = S = 0$. At this operating point, the resonant input voltage V_{AB} works at a fixed frequency of 20 kHz with two SMs participating in D-value modulation. Since V_{AB} closely resembles a square wave, V_{Cr} and I_{Lr} exhibit sinusoidal-like waveforms. The output voltage remains stable at the predetermined value of 100 V. Fig. 11(b), (c), and (d) illustrates that as the input voltage increases, D gradually decreases, while K and S progressively increase, maintaining the output voltage at 100 V.

B. Transient Experimental Results

Fig. 12 demonstrates the key system waveforms under full-load conditions when the input voltage undergoes sudden changes. Fig. 12(a) shows that when the input voltage V_{in} abruptly rises from 300 to 600 V, the resonant input voltage V_{AB} increases due to the rise in K and S. The resonant current waveform adapts accordingly, but the output voltage remains stable at the target value. Conversely, Fig. 12(b) shows the waveforms when V_{in} decreases from 600 to 300 V under full-load conditions.

Fig. 13 illustrates the waveforms when the system is subjected to sudden changes in load at an input voltage of 300 V. Fig. 13(a) depicts the scenario where the load transitions from 10% to 100%, causing i_o and i_r to increase. The output voltage remains stable at the rated value. Fig. 13(b) presents the reverse case, where the load decreases from 100% to 10% .

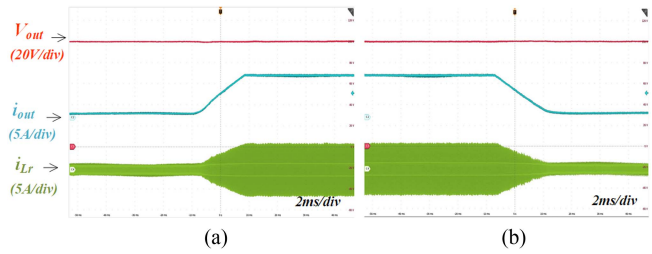

Fig. 13. Dynamic performance of the MMRDC in response to step changes in the load. (a) Step increase of load from 10% load to full load. (b) Step decrease of load from full load to 10% load.

Based on the switching positions of the SM within one cycle, two switching modes are defined: E-mode and W-mode. When the SM operates at the cycle edges, it is defined as E-mode switching, corresponding to g_{k+5} to g_{N-S} in Fig. 3, with the associated events highlighted by the green dashed area. When operating under pulsewidth modulation, it is defined as W-mode switching, corresponding to g_{k+1} to g_{k+4}, with related events marked by the brown dashed area in Fig. 14.

Fig. 14 illustrates the ZVS operation of SM under various input voltages and load conditions. Fig. 14(a) and (b) demonstrates that at an input voltage of 300 V and load levels of 10% and 100%, respectively, all SM switching events (2 W-mode and 6 E-mode) satisfy $I_{SM} > 0$, achieving ZVS ON. Fig. 14(c) and (d) shows similar results for an input voltage of 600 V and load levels of 10% and 100%, respectively, where $K = S = 2$. Here, only 2 W-mode and 2 E-mode switches occur, but they still satisfy $I_{SM} > 0$, achieving ZVS ON.

The proposed converter employs the fixed-frequency K+2D modulation and control method, which ensures gain continuity by switching K at higher D-values. This approach achieves ZVS across the entire input voltage and load range. Full ZVS operation of all SMs significantly reduces switching losses and enhances system efficiency.

The results of voltage balance in the experiment are shown in Fig. 17. It can be observed from the figure that the voltage of each SM is well balanced.

To verify the thermal effects of the SM switches, we conducted dedicated thermal experiments. The converter was operated at full load (1000 W) for 20 min, after which the temperatures of the SM switching devices and heat sink were measured. With a heat sink, the maximum temperature of the heat sink reached 34.7 °C. Without a heat sink, the maximum temperature of the switching device reached 84 °C. From the thermal imaging results, the temperature of the SM capacitor remained close to room temperature, around 20 °C.

As shown in the Fig. 18, even without a heat sink, the chip temperature did not exceed the 150 °C operating limit of the MOSFET, indicating that the converter experiences relatively low thermal stress.

The transformer's losses can be categorized into core losses and winding losses, denoted as P_{TC} and P_{TW}, respectively. The core loss of the transformer can be estimated using the following:

$$P_{TC} = K_0 \cdot f_m^{\alpha} \cdot B_p^{\beta} \cdot V_e$$

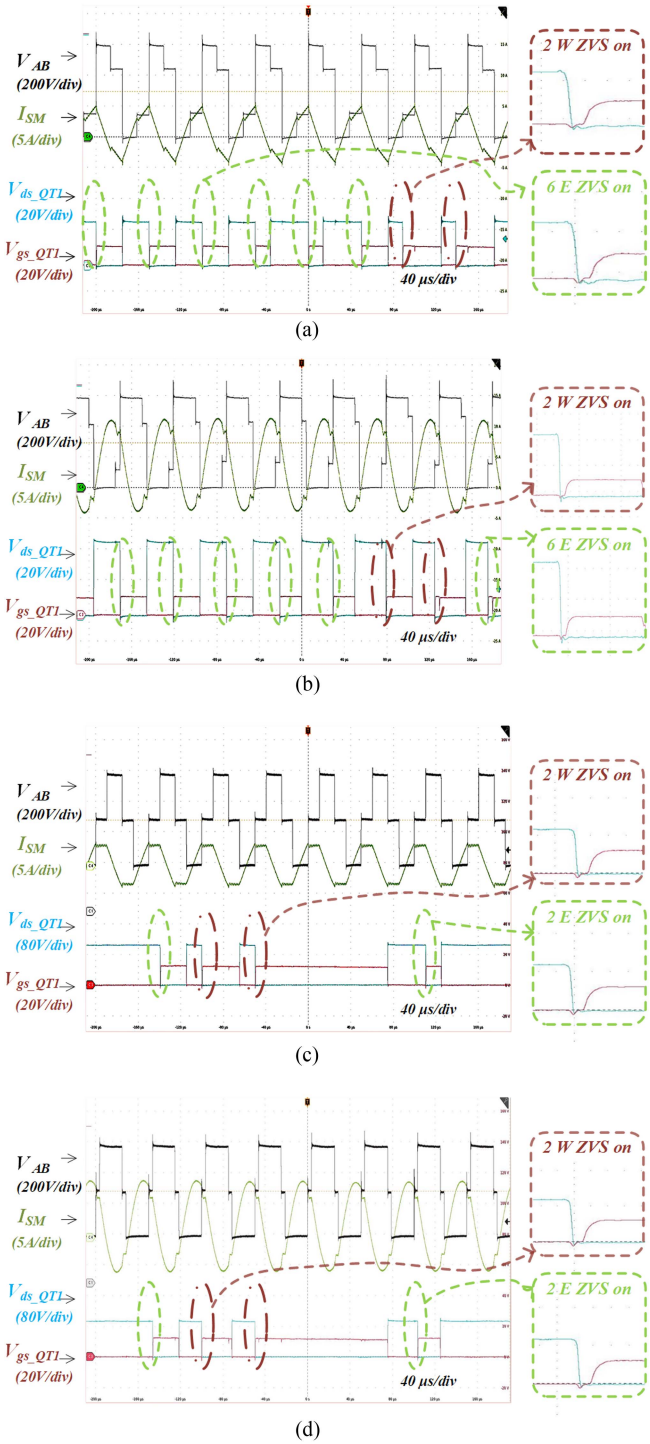

Fig. 14. Measured drive and drain-source voltages of the top SM switch. (a) $P_t = 100$ W and $V_{in} = 300$ V. (b) $P_t = 1000$ W and $V_{in} = 300$ V. (c) $P_t = 100$ W and $V_{in} = 600$ V. (d) $P_t = 1000$ W and $V_{in} = 580$ V.

where B_p is the maximum magnetic flux density, V_e is the core volume, f_m is the operating frequency, K_0, α and β are constants of magnetic core material.

In the PFM+K control mode, the maximum operating frequency is the resonant frequency f_r. Since the actual operating frequency is lower than f_r, the core volume V_e must be designed

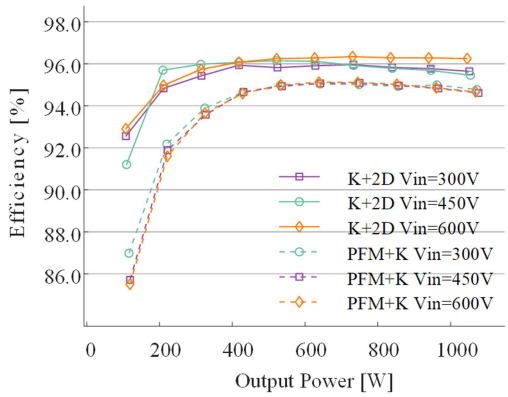

Fig. 15. Measured power stage efficiency of the K+2D and PFM+K controlled converter under different voltages.

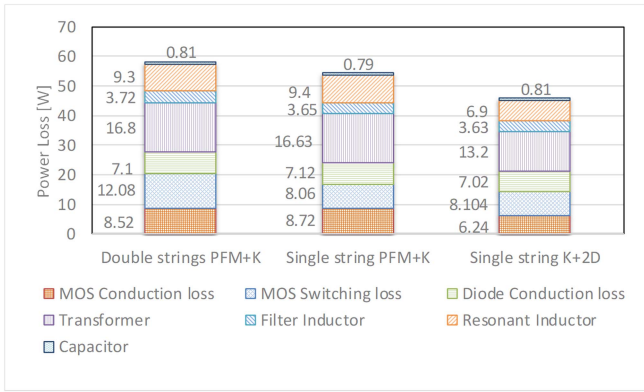

Fig. 16. Power loss breakdown of three dc/dc converter schemes.

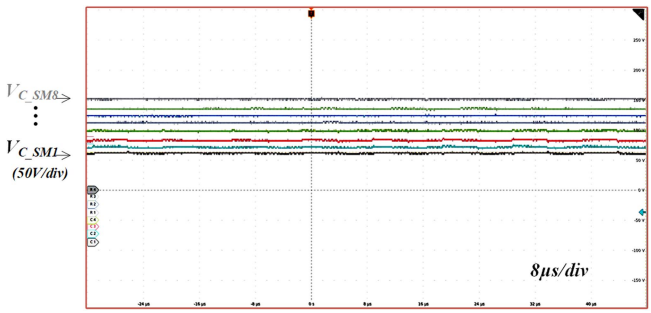

Fig. 17. Experiment test wave of SM capacitor voltage balancing.

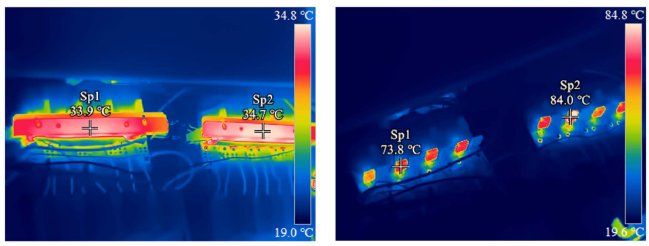

Fig. 18. Thermal test chart of SM MOSFET under full load operation for 20 minutes. (a) With heat sink. (b) Without heat sink.

TABLE IV
COMPARISON RESULTS OF FOUR DC/DC CONVERTER SCHEMES

Parameter	MMR [16]	MMRDC [17]	MMRDC [19]	MM-DCT [24]	Proposed
MV terminal voltage /kV	9–15	8–16	9–18	6–12	9–18
Rated power /kW	200	100	50	500	200
Output voltage /V	750	375	375	750	750
Number of string	2	2	2	1	1
Number of SM	32	32	36	9	32
Operating frequency /kHz	11.5-22	7-12	12	10	10
Blocking capacitor	no	no	no	yes	no
Bidirectional power transmission	no	no	no	yes	no
Modulation	PFM+K	Optimized PFM+K	Shift Angle + K	Quasi Square Wave	K+2D
Voltage overshoot /Output voltage /V	25/750	25/375	30/375	120/750	4/750
Larger magnetizing inductance L_m	no	yes	yes	not use L_m	yes
Percentage of ZVS ON switches	50%	50%	50%	full ZVS for partial gain and load	100%

larger compared to the K+2D control method. As a result, core losses are higher when operating at f_r in the PFM+K method.

The method of calculating transformer winding loss is further refined in this work by separating the dc and ac current components

$$P_{TW} = P_{cu\_p} + P_{cu\_s1} + P_{cu\_s2}$$

where P_{cu_p} represents the copper loss of the primary winding, and P_{cu_s1}, P_{cu_s2} represent the copper losses of the two secondary windings, respectively

$$P_{cu\_p} = I_{p\_dc}^2 \cdot R_{p\_dc} + I_{p\_ac}^2 \cdot AC\_{pri} \cdot R_{p\_dc}$$
$$P_{cu\_s1} = I_{s1\_dc}^2 \cdot R_{s1\_dc} + I_{s1\_ac}^2 \cdot AC\_{sec} \cdot R_{s1\_dc}$$
$$P_{cu\_s2} = I_{s2\_dc}^2 \cdot R_{s2\_dc} + I_{s2\_ac}^2 \cdot AC\_{sec} \cdot R_{s2\_dc}.$$

Here, I_{p_dc} and I_{p_ac} denote the dc and ac components of the primary current, respectively; R_{p_dc} is the primary dc resistance; and $AC_{\_\text{pri}}$ is the primary ac resistance coefficient. The subscripts $s1$ and $s2$ refer to the two secondary windings and their corresponding parameters.

As the resonant tank current decreases, the winding losses decrease accordingly due to the reduced equivalent primary-side current.

In summary, the PFM+K method results in higher transformer losses compared to the fixed-frequency K+2D method.

Fig. 15 compares the efficiency of the K+2D control method with the single-string PFM+K method. As shown, the K+2D method ensures all SM modules operate in ZVS ON mode during switching, leading to lower switching losses.

Additionally, this method not only achieves soft switching for all SM switches, but also allows for a larger magnetizing inductance L_m, resulting in smaller resonant currents and lower conduction losses. With the PFM+K method, the value of m is set to 5, and the L_m inductance is 2 mH. In contrast, using the K+2D control method, m can be increased to 10, with L_m set to 3.8 mH. As a result, the K+2D control method exhibits lower conduction current and conduction losses, leading to higher efficiency compared to the single-string PFM+K control method. The K+2D method achieves higher efficiency, with a peak efficiency of 96.3% .

To provide a more detailed analysis of the losses shown in Fig. 15, we utilized PLECS simulation data and followed the loss analysis approach.

Fig. 16 illustrates power loss breakdown of three dc/dc converter schemes.The analysis results show that, compared to the dual-strings PFM+K control method, the proposed K+2D method reduces switching losses by enabling ZVS for all switches. In comparison with the single-string PFM+K method, the K+2D method reduces conduction losses through the use of a larger magnetizing inductance. In addition, the copper losses of the resonant inductor and transformer are also reduced.

Table IV presents the characteristics of the proposed K+2D control strategy in comparison to previous works.

Regarding the blocking capacitor, [25] employs a blocking capacitor to isolate the dc component on the medium-voltage (MV) side, while still allowing voltage penetration. This design enables the use of control methods similar to those in the dual-active-bridge (DAB) converter, thus achieving bidirectional power transmission.

In terms of control strategies, [18] presents improvements on the PFM+K control method, while [20] adopts a shift-angle+K control strategy, which enhances the efficiency under light-load conditions.

Based on the review in Section I, several criteria have been established to compare the candidates for MMRDCs as follows.

1) 100% ZVS ON switch: Using traditional control methods, the arm current is no longer purely ac but contains a dc component, resulting in asymmetric currents that prevent half of the switches from achieving ZVS ON. In contrast, the proposed modulation scheme leverages L_f current oscillations to enable soft switching for all E-mode transitions. Additionally, the double-D pulsewidth modulation preemptively switches the K value, ensuring that the switches involved in double-D W-mode transitions also achieve soft switching. This approach guarantees ZVS ON for all switches.

2) Less output voltage overshoot: With other modulation methods, changes in K can cause frequency modulation or phase

shift jumps, leading to significant output voltage overshoot. In the proposed scheme, although gain experiences slight jumps during K-value transitions, switching at appropriate gain points minimizes voltage overshoot. As shown in Fig. 8, the output voltage overshoot is very small, only 4 for a 750 V output.

3) Larger magnetizing inductance: Since the inductance ratio $m = L_m/L_r$ has minimal impact on the overall output gain, the proposed scheme allows for the use of a larger magnetizing inductance. This reduces conduction losses, thereby improving system efficiency.

V. Conclusion

This article proposes a novel fixed-frequency K+2D control method to achieve ZVS for all SMs transitions. The modulation strategy, operating principles, and characteristics of the proposed approach are thoroughly investigated. By combining dual-SMs duty cycle (D) modulation, the system can transition K before D-value ZVS loss occurs, ensuring ZVS for all switches. This significantly reduces system switching losses, addressing the issue of conventional dual-string MMRDCs where only 50% of switches can achieve ZVS ON.

Compared to traditional PFM + K control-based MMRDCs, a larger inductance ratio can be adopted to reduce conduction losses. Additionally, fixed-frequency operation can simplify the design of resonant inductors and transformers.

The effectiveness of the proposed control strategy is validated through simulations of a 200 kW MMRDC. Experimental results from an MMRDC prototype further verify the feasibility. Under wide input voltage ranges and full-load conditions, all primary switches achieve ZVS on. Moreover, the converter demonstrates excellent dynamic performance in response to input and load variations under closed-loop control. Therefore, the K+2D controlled MMRDC is a competitive solution for MV-LV applications with wide input voltage ranges.

References

[1] L. Zheng, R. P. Kandula, and D. Divan, "Current-source solid-state DC transformer integrating LVDC microgrid, energy storage, and renewable energy into MVDC grid," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 1044–1058, Jan. 2022.

[2] Y. Chen, S. Zhao, Z. Li, X. Wei, and Y. Kang, "Modeling and control of the isolated DC–DC modular multilevel converter for electric ship medium voltage direct current power system," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 124–139, Mar. 2017.

[3] J. Zhang, J. Liu, J. Yang, N. Zhao, Y. Wang, and T. Q. Zheng, "A modified DC power electronic transformer based on series connection of full-bridge converters," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2119–2133, Mar. 2019.

[4] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% efficient 10 kV SiC-Based 7 kV/400 V DC transformer for future data centers," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 753–767, Jun. 2019.

[5] T. Guillod, D. Rothmund, and J. W. Kolar, "Active magnetizing current splitting ZVS modulation of a 7 kV/400 V DC transformer," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1293–1305, Feb. 2020.

[6] A. Q. Huang, "Medium-voltage solid-state transformer: Technology for a smarter and resilient grid," *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 29–42, Sep. 2016.

[7] J. Yao, W. Chen, C. Xue, Y. Yuan, and T. Wang, "An ISOP hybrid DC transformer combining multiple SRCs and DAB converters to interconnect MVDC and LVDC distribution networks," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11442–11452, Nov. 2020.

[8] J. Zhang et al., "A multiport DC power flow controller embedded in modular multilevel DC transformer," *IEEE Trans. Ind. Electron.*, vol. 70, no. 5, pp. 4831–4841, May 2023.

[9] D. Ma, W. Chen, and X. Ruan, "A review of voltage/current sharing techniques for series–parallel-connected modular power conversion systems," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12383–12400, Nov. 2020.

[10] M. Abbasi, R. Emamalipour, K. Kanathipan, M. A. M. Cheema, and J. Lam, "A step-up reconfigurable multimode LLC converter module with extended high-efficiency range for wide voltage gain application in medium voltage DC grid systems," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8118–8132, Jul. 2022.

[11] G. Ortiz, M. G. Leibl, J. E. Huber, and J. W. Kolar, "Design and experimental testing of a resonant DC–DC converter for solid-state transformers," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7534–7542, Oct. 2017.

[12] J. E. Huber and J. W. Kolar, "Analysis and design of fixed voltage transfer ratio DC/DC converter cells for phase-modular solid-state transformers," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 5021–5029.

[13] R. Chen et al., "Phase shift angle segmentation modulation for soft-switching medium-voltage DAB converter with series-connected SiC MOSFETs," *IEEE Trans. Transport. Electrific.*, vol. 10, no. 1, pp. 462–474, Mar. 2024.

[14] Z. Lu et al., "Medium voltage soft-switching DC/DC converter with series-connected SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1451–1462, Feb. 2021.

[15] G. Ulissi, U. R. Vemulapati, T. Stiasny, and D. Dujic, "High-frequency operation of series-connected IGCTs for resonant converters," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5664–5674, May 2022.

[16] P. A. Gray, Z. C. Ma, and P. W. Lehn, "A high-frequency MMC for DC–DC applications using a three-winding transformer with DC flux cancellation," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 3, no. 3, pp. 647–657, Jul. 2022.

[17] S. Shao et al., "A modular multilevel resonant DC–DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7921–7932, Aug. 2020.

[18] J. Sheng et al., "Control optimization of modular multilevel resonant DC converters for wide-input-range MVdc to LVdc applications," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5284–5298, May 2022.

[19] G. Zheng, Y. Chen, and Y. Kang, "Trapezoidal current modulation for a compact DC modular multilevel converter with ZVS of submodules and ZCS of voltage-balancing circuits," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 10986–10992, Oct. 2021.

[20] J. Sheng et al., "High-efficient operation for modular multilevel resonant DC–DC converters in medium voltage applications with wide input range and wide load condition," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12180–12194, Oct. 2023.

[21] H. Jin, W. Chen, Y. Xie, L. Shu, and Y. Xu, "Asymmetric trapezoidal wave (ATW) modulation of modular multilevel resonant DC/DC converter for current stress optimization," *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 8499–8512, Jul. 2023.

[22] C. Pineda, J. Pereda, F. Rojas, G. Droguett, C. Burgos-Mellado, and A. J. Watson, "Optimal ZCS modulation for bidirectional high-step-ratio modular multilevel DC–DC converter," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12540–12550, Nov. 2021.

[23] S. Bazyar, J.-H. Jung, H. Beiranvand, J. V. M. Farias, and M. Liserre, "Quasi two-level modulation for the MMC-based isolated DC/DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2023, pp. 2424–2430.

[24] W. Cui, S. Shao, T. Wu, W. Chen, and J. Zhang, "A bidirectional modular multilevel resonant DC–DC converter for wide voltage range medium-voltage power conversion," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12743–12756, Oct. 2023.

[25] H. Jin, W. Chen, K. Hou, S. Shao, L. Shu, and R. Li, "A sharing-branch modular multilevel DC transformer with wide voltage range regulation for DC distribution grids," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5714–5730, May. 2022.

[26] J. Duan, D. Zhang, X. Wang, and R. Gu, "Modular multilevel resonant DC transformer with inherent balancing capability," *IEEE Trans. Ind. Electron.*, vol. 70, no. 6, pp. 5717–5727, Jun. 2023.

[27] M. A. H. Rafi and J. Bauman, "Optimal control of semi-dual active bridge DC/DC converter with wide voltage gain in a fast-charging station with battery energy storage," *IEEE Trans. Transport. Electrific.*, vol. 8, no. 3, pp. 3164–3176, Sep. 2022.

[28] Q. Zhou et al., "A step-down resonant modular multilevel DC/DC converter with extendable ZVS range based on asymmetric triangular current," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11088–11099, Nov. 2022.

[29] K. Rajashekara, H. S. Krishnamoorthy, and B. S. Naik, "Electrification of subsea systems: Requirements and challenges in power distribution and conversion," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 4, pp. 259–266, Dec. 2017.
[30] T. Jiang, J. Zhang, X. Wu, K. Sheng, and Y. Wang, "A bidirectional three-level LLC resonant converter with PWAM control," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2213–2225, Mar. 2016.
[31] X. Fang, H. Hu, Z. J. Shen, and I. Batarseh, "Operation mode analysis and peak gain approximation of the LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1985–1995, Apr. 2012.

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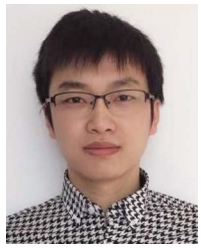

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