First Characterization of Si IGBT, SiC MOSFET, and GaN HEMT at Deep Cryogenic Temperatures Down to 10 Millikelvins

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***Abstract*—Electrical energy conversion at deep cryogenic temperatures ($T < 4.2$ K) is highly desirable for applications in space exploration, quantum computing, biomedical imaging, and emerging power delivery systems. However, the operational viability of power semiconductor devices in this temperature regime remains largely unexplored. Notably, no prior studies have reported high-voltage or dynamic switching characteristics of gallium nitride (GaN) and silicon carbide (SiC) power devices below 77 K. In this work, we present the first comprehensive characterization of the static and dynamic performance of silicon (Si) insulated-gate bipolar transistor (IGBT), SiC metal-oxide-semiconductor field-effect transistor (MOSFET), and GaN high-electron-mobility transistor (HEMT) devices down to 10 mK. A cryogen-free dilution refrigerator, originally designed for quantum physics experiments, is adapted for power device testing by integration with a custom circuit setup for double-pulse testing and dynamic ON-resistance (R_{ON}) test. At $T < 1$ K, all three devices are found to retain the normally-OFF operation, high breakdown voltage, and the capability of hard-switching under gate control. GaN HEMTs demonstrate the absence of dynamic R_{ON} degradation, with R_{ON} decreasing by four times compared to room temperature. This can be explained by the trap freeze-out and increased channel mobility. Differently, SiC MOSFET becomes non-Ohmic below ∼60 K. The knee voltages (V_K) of SiC MOSFET and Si IGBT both increase at lower temperatures, leading to elevated conduction loss. The sustained current conduction and high V_K in lowly doped SiC and Si drift layers, despite carrier freeze-out, can be explained by the shallow-level impact ionization with donor states. These findings lay the foundation for developing deep cryogenic power electronics at temperatures below the current operational boundaries.**

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***Index Terms*—Cryogenic measurement, dilution refrigerator, dynamic ON-resistance, GaN HEMT, power semiconductor, Si IGBT, SiC MOSFET , switching performances.**

I. Introduction

MANY applications in space exploration [1], [2], [3], biomedicine [4], [5], precision metrology [6], and quantum technologies [7], [8], [9], [10], [11] require electronics capable of operating at extremely low cryogenic temperatures, ranging from ∼4 K down to the millikelvin (mK) range – often referred to as the deep cryogenic temperature regime. Power electronics can play a crucial role in these application scenarios, enabling efficient electrical energy conversion. Deep cryogenic power electronics are also essential for supporting the future grids involving superconducting power delivery and energy storage. For example, by integrating the power converter inside the cryogenic system, the transmission loss on the power lines can be significantly reduced, because the high current/low voltage input for regular cryogenic load can be converted to low current/high voltage input instead [12]. However, the development of power electronics for these application scenarios is impeded by the limited understanding of power device behavior at ultralow temperatures.

For power semiconductor devices that incorporate a lightly doped drift region, such as power metal-oxide-semiconductor field-effect transistors (MOSFETS) and insulated-gate bipolar transistors (IGBTs), a major concern is the likelihood of carrier freeze-out at deep cryogenic temperatures [12]. In contrast, gallium nitride (GaN) power devices, which utilize a two-dimensional electron gas (2DEG) channel for current conduction, are known to be resilient to carrier freeze-out under cryogenic temperatures [13]. However, it remains unknown if the 2DEG can be dynamically supplied and extracted at high frequencies under ultralow temperatures.

Fig. 1 summarizes the lowest temperatures reported in cryogenic studies of GaN high-electron-mobility transistors (HEMTs) [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], silicon carbide (SiC) MOSFETS [15], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], and silicon (Si) IGBTs [33], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53]. These studies include various testing methods, including static low-voltage characterizations (e.g., output current-voltage (*I-V*) sweep), high-voltage

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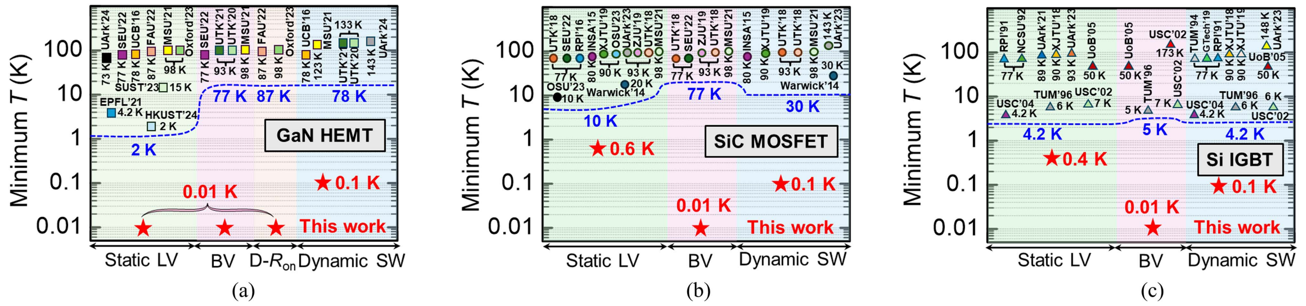


Fig. 1. Reported cryogenic studies of (a) GaN HEMT, (b) SiC MOSFET, and (c) Si IGBT, highlighting the unexplored range in the prior literature (below the dashed blue lines). The lowest temperature, research institute, and year of each report are marked. Studies are grouped into the static low-voltage (LV) test, breakdown voltage (BV) test, dynamic R_{ON} (D-R_{ON}) test, and dynamic switching (SW) test. The lowest temperature for device characterization in this work is marked with star symbols for different types of tests.

breakdown measurement, and inductive switching tests. To date, no reported studies have characterized power devices at temperatures below 4.2 K, likely due to the limitations of conventional cryogenic probe stations, which are incapable of achieving such extreme temperatures. Additionally, for SiC MOSFETS and GaN HEMTs, high-voltage and dynamic switching characterizations have only been conducted down to 77 K, leaving a significant gap in understanding their behaviors in the cryogenic regime.

To achieve cryogenic test conditions, various types of cryogenic refrigeration systems have been employed. The liquid nitrogen fridge is widely used in cryogenic power electronics testing due to its convenience and high cooling power. However, its base temperature is constrained to approximately 77 K, as determined by the boiling point of liquid nitrogen. The cryogen-free dilution refrigerator (i.e., dilution fridge), which integrates a pulse tube cryocooler with a helium-3/helium-4 dilution unit, represents the state-of-the-art in cryogenic measurement technology. This system offers a large experimental workspace, high cooling capacity, and an ultralow base temperature below 10 mK. While extensively used in many scientific disciplines, such as quantum computing with superconducting circuits [54], its application to power device testing remains unexplored. Adapting this system for power electronics, which operate at high voltage, high current, and fast switching speeds, poses great challenges such as increased measurement noise and potential thermal instability.

This study, for the first time, characterizes both static and dynamic characteristics of Si, SiC, and GaN power devices down to 10 mK using a dilution refrigerator. To conduct high-voltage (>1 kV) breakdown tests and hard-switching tests, we integrate custom protection and circuit setups with the fridge. A daughter board carrying the device under test (DUT) is mounted on the 10 mK plate in the fridge chamber and connected to external dynamic test circuits via coaxial cables from room temperature to 4 K and NbTi superconducting cables from 4 K to 10 mK, which can carry high currents with minimal resistance. The DPT waveforms are not only used for examining the hard-switching capability but also for reconstructing dynamic *I-V* characteristics, allowing for extracting key device parameters under actual switching conditions. This set of test hardware and methodologies enables a precise and comprehensive assessment of power device characteristics at record-low temperatures. The newly revealed device physics is also thoroughly discussed. Notably, as compared to our prior conference paper [55], this article elaborates on the test mechanism and setup, circuit-based test results, and the associated device physics.

The rest of this article is organized as follows. Section II details the deep-cryogenic power test system. Sections III–V present the cryogenic test results for GaN HEMT, SiC MOSFET, and Si IGBT, respectively. Key device physics for each device is also discussed in the respective sections. Finally, Section VI concludes this article.

II. Deep-Cryogenic Test System

Fig. 2(a) shows a photo of the cryogenic test system, which includes two main parts: the cooling system based on a cryogen-free dilution refrigerator and the measurement system, which includes the circuit setups and a curve tracer. The schematic of the test system is shown in Fig. 2(b).

The Bluefors LD250 dilution refrigerator has a multiplate structure that provides a range of temperatures from 70 K to 10 mK for measurement. The entire system is enclosed in four cans to ensure temperature isolation and to maintain a vacuum condition. A dilution unit with a turbo pump is used to maintain the cooling cycle during operation. The base temperature in the mixing chamber (located at the bottom of the fridge) can be stabilized to temperatures below 10 mK. A customized daughter board, mounted in the mixing chamber with thermal paste, carries the DUTs and connectors.

The connection of measurement signals follows the Kelvin connection (four-wire connection). From the daughter board to connectors inside the fridge, the coaxial cables (CCs) are used for high-current signals, while dupont wires (DWs) handle the control and sense signals. To reduce additional thermal load, the fridge provides several superconducting cables (SCs), which turn superconducting at cryogenic temperatures below 4 K. These SCs transmit signals from each plate to the top of the fridge via SMA and Micro-D25 (M-D25) connectors. Several SMA and Fisher connectors are located at the top exterior of the fridge for various measurements. The CCs are used from the SMA connectors to the motherboard or curve tracer for power and high-frequency signals, and DWs with Fisher-D25 connectors are applied for low-current and sense

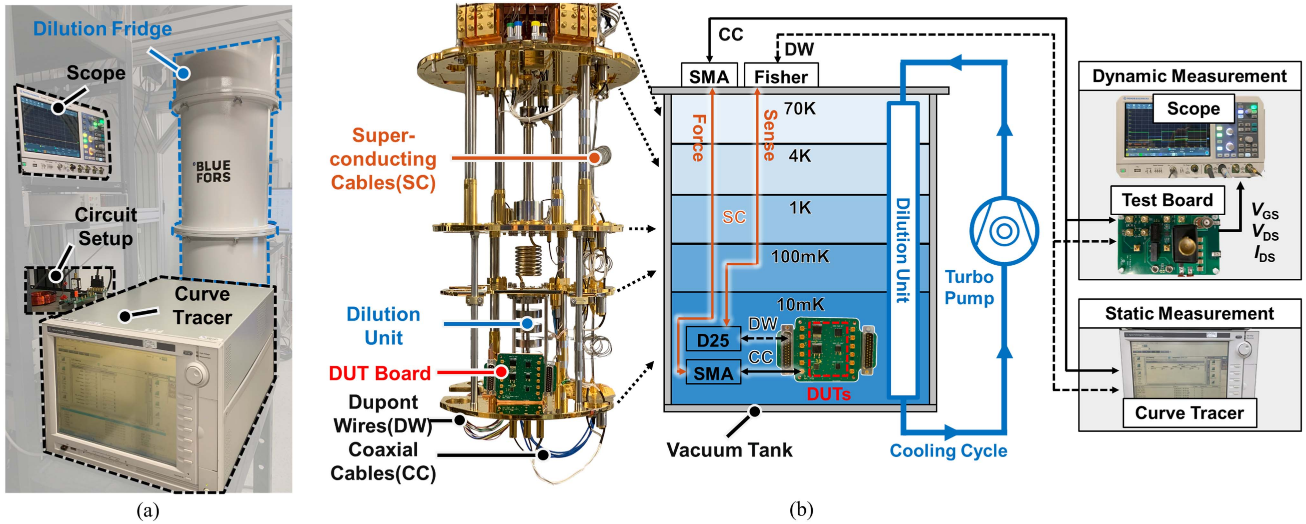


Fig. 2. (a) Photograph and (b) schematic of cryogenic test setup, which consists of a Bluefors dilution fridge, a Keysight B1505 curve tracer, and a customized circuit test setup. The daughter board with DUTs is mounted on the 10 mK plate, while other components and equipment are placed outside the fridge. Photos are taken by the authors.

TABLE I
MAJOR SPECIFICATIONS OF DILUTION FRIDGE

Parameters	Expected Values
Base temperature	< 10 mK
Cooling power at 20 mK	> 14 μW
Cooling power at 100 mK	> 300 μW
Cooling power at 4 K	~ 20 W
Cooldown time to base temperature	< 30 h

signals. The motherboard accommodates the DPT circuit with *in situ* dynamic ON-resistance (R_{ON}) extraction. The curve tracer, Keysight B1505A Power Device Analyzer, is used for static measurements with 100 ms pulse width to exclude the impact of measurement ringing.

A. Working Principles of Cryogen-Free Dilution Refrigerator

The cryogen-free dilution refrigerator achieves cooling by mixing helium-3 (He-3) and helium-4 (He-4) isotopes in the dilution unit, allowing it to reach temperatures below 10 mK. The major specifications of this dilution fridge are summarized in Table I [56].

Fig. 3(a) shows the phase diagram of the He-3 and He-4 mixture. Below 0.87 K, the mixture separates into two phases: a concentrated phase rich in He-3 and a dilute phase poor in He-3. The enthalpy of He-3 is lower in the concentrated phase than in the dilute phase, allowing heat absorption during the phase separation process. This cooling process occurs in the mixing chamber of the dilution unit, decreasing the system temperature.

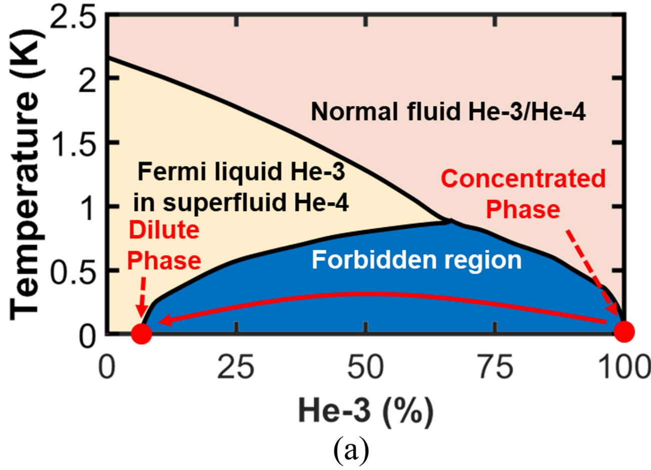
Fig. 3(b) illustrates the cycling process in the dilution unit. Before entering the dilution unit, He-3 is precooled to about 3 K by a pulse tube cryocooler system. It then passes through the still chamber and heat exchangers. In the mixing chamber, He-3 and He-4 are mixed, and He-3 is pumped across the phase boundary, where the cooling takes place. Subsequently, He-3 transitions to the dilute phase and flows back through the heat exchangers and still chamber. As the outgoing He-3 is cooler than the incoming He-3, it precools the incoming He-3 in heat exchangers. During this return process, the temperature and concentration of He-3 increase, and it transitions back to the concentrated phase when exiting the dilution unit.

B. Circuit Setups

To analyze DUT's switching performance, a DPT mother board and a DUT daughter board were carefully designed. Fig. 4(a) shows the circuit schematic of the DPT, with the mother board located outside the fridge. The power loop consists of a dc power supply (V_{dc}), dc input capacitors (C_{dc}), an inductor (L), and a free-wheeling diode (FWD). Fig. 4(b) shows the typical switching waveforms of DPT. The switching performance is characterized during the hard-switching transients at turn-OFF (end of the first pulse) and turn-ON (beginning of the second pulse). The dynamic R_{ON} is extracted during the second pulse, following the hard-switching turn-ON.

Fig. 4(c) shows the schematic of the cable connections. Following the Kelvin connection method, the force signals for the drain and source (D,F and S,F) are connected to SMP connectors on the daughter board, while the sense signals (D,S and S,S) are connected to D25 connectors. Since the gate loop typically carries less current than the power loop, both the force and sense signals for the gate (G,F and G,S) are connected to the D25 connector.

From the daughter board to the connectors carried by the fridge (located in the mixing chamber), coaxial cables connect the SMP and SMA for the D,F and S,F signals. A D25 to M-D25 cable with 25 dupont wires is used to conduct the sense and gate signals. $R_{\mathrm{CC},1}$ and $R_{\mathrm{DW},1}$ represent the equivalent cable resistances of a single coaxial cable and a dupont wire, respectively, while $L_{\mathrm{CC},1}$ and $L_{\mathrm{DW},1}$ represent their equivalent inductances.



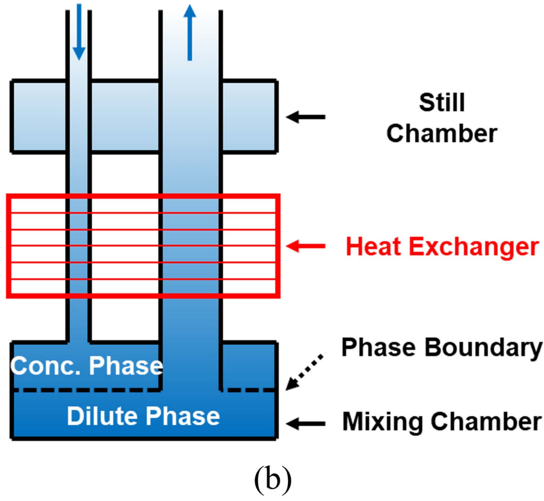


Fig. 3. (a) Phase diagram of helium-3/helium-4 mixture. (b) Schematic of the dilution unit.

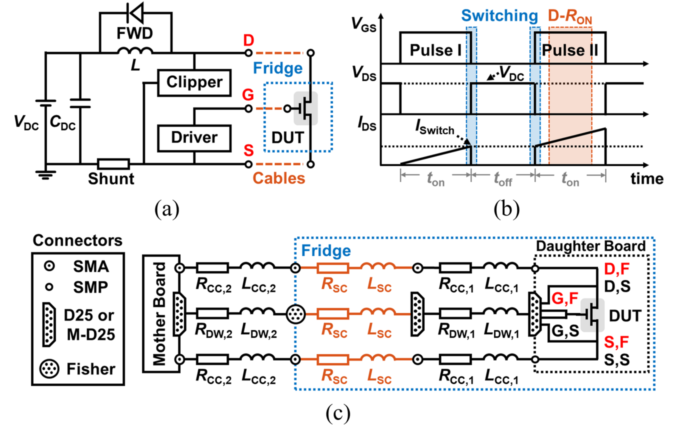


Fig. 4. (a) Circuit schematic. (b) typical switching waveforms of DPT. (c) Schematic of cable connections and equivalent *RL* network.

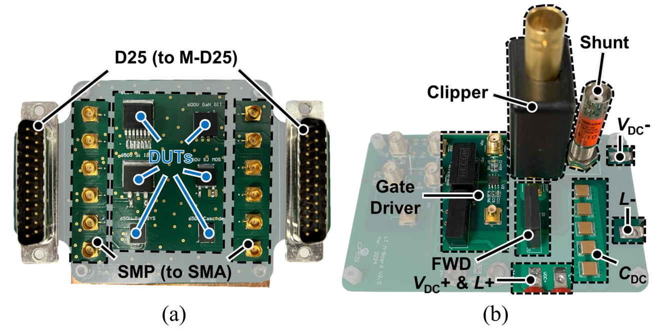


Fig. 5. Photographs of (a) daughter board (inside the fridge) and (b) mother board (outside the fridge).

TABLE II
SUMMARY OF MAJOR SPECIFICATIONS OF DUTS

Device	V_{RATED}	I_{RATED}	R_{ON} / V_F	Packaging
GaN HEMT	650 V	11 A	160 mΩ	DFN5x6
SiC MOSFET	650 V	21 A	120 mΩ	TO263-7
Si IGBT	650 V	50 A	1.35 V	TO263-3

From the mixing chamber to the top of the fridge, niobium-titanium (Nb-Ti) superconducting cables are used for signal conduction. R_{SC} and L_{SC} represent the equivalent resistance and inductance of a single superconducting cable. From the top connectors of the fridge (SMA and Fisher), longer coaxial cables are used for power signal conduction, and dupont wires with Fisher to D25 connectors connect the mother board to the Fisher connector. $R_{CC,2}$ and $L_{CC,2}$ represent the equivalent parameters for coaxial cables, while $R_{DW,2}$ and $L_{DW,2}$ represent those for dupont wires.

In this structure, the equivalent parameters outside the fridge ($R_{CC,2}$, $R_{DW,2}$, $L_{CC,2}$, and $L_{DW,2}$) remain constant, while the equivalent parameters of the cables inside the fridge change as the temperature decreases. For the superconducting cables, R_{SC} drops to zero below 4 K, while $R_{CC,1}$ and $R_{DW,1}$ decrease significantly at cryogenic temperatures. These temperature-dependent changes will influence measurement results, which will be discussed in the following sections.

Fig. 5(a) shows the photo of the daughter board, which consists of six different types of packaging to support various DUTs. The bottom of the daughter board is stripped of paste and covered with a large ground layer for direct contact with the mixing plate. A cryogenic thermal paste is applied to the bottom side to enhance thermal conduction. The daughter board features 12 SMP and 2 D25 connectors on its left and right sides.

The DUTs used in this study include a GaN HEMT (GS065011L), SiC MOSFET (C3M0120065J), and Si IGBT (IGB50N65S5). All DUTs have the same voltage rating (650 V) but different device structures and conduction physics (e.g., bipolar and unipolar), allowing for the study of cryogenic performance across different device technologies. The DUT parameters are summarized in Table II. It is worth noting that the GaN HEMT has a Schottky-type p-GaN gate, the SiC MOSFET has a planar gate design, and the Si IGBT has a trench gate and punch-through drift region designs; all three DUTs are enhancement-mode devices.

As shown in Fig. 5(b), the driver circuit, based on an external driver IC (Si8271), is located on the mother board. Both turn-ON and turn-OFF gate resistances ($R_{G,ON}$ and $R_{G,OFF}$) are set to 5 Ω. The positive drive voltage (V_{G+}) is +5 V for the GaN HEMT

TABLE III
DPT TEST PARAMETERS

Parameters	Values	Parameters	Values
V_{dc}	0–50 V	$R_{G,ON}$	5 Ω
C_{dc}	10 μF	$R_{G,OFF}$	5 Ω
L	5.5 mH	t_{off}	100 μs
V_{G+}	+5/+19 V	V_{G-}	-2 V

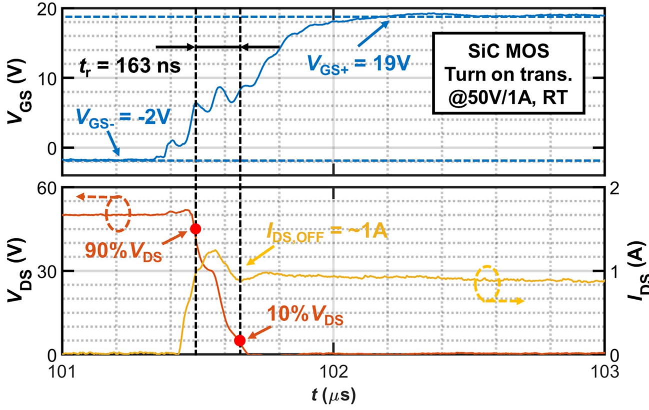


Fig. 6. SiC MOSFET turn-ON waveforms under 50 V/1 A DPT at room temperature. The extraction of the rise time is also illustrated.

and +19 V for the SiC MOSFET and Si IGBT, based on their different driving requirements. The negative drive voltage (V_{G-}) is −2 V for all DUTs. A 1.2 kV SiC Schottky diode (C4D10120) is used as the FWD, and a 10 μF capacitor is selected for C_{dc}. Due to the relatively long test loop, as shown in Fig. 4(c), the turn-ON and turn-OFF times (t_{ON} and t_{OFF}) are set to the hundred-microsecond level, and a 5.5 mH inductor is used to limit the peak current.

For hard-switching tests, V_{dc} is fixed at 20 V under all test conditions. For dynamic R_{ON} tests, V_{dc} varies from 0 V to 50 V to assess the dynamic R_{ON} performance of the GaN HEMT. The gate-source voltage (V_{GS}), drain-source voltage (V_{DS}), and collector-emitter voltage (V_{CE}) are measured using a passive probe (RT-ZP10). In the dynamic R_{ON} test, a 0.1 Ω current shunt and a voltage clipper (CLP1500V15A1) are used to measure the device's current (I_{DS}) and ON-state voltage drop ($V_{DS,ON}$), similar to our prior setups reported in [57], [58], and [59]. The clipper blocks high voltage when the DUT is OFF and measures $V_{DS,ON}$ when the device is ON. The DPT test conditions are summarized in Table III. The hundreds of μs turn-ON time is used to exclude the impact of switching ringing and to extract the results in a steady state. It should be noted that the maximum voltage for DPT is set to 50 V due to the voltage limitation of the dilution fridge, specifically because of the use of M-D25 connectors, which have a lower pin-to-pin voltage limitation compared to coaxial cables. In addition, the current level is limited to <2 A to prevent self-heating on DUTs.

C. Measurement and Extraction Methods

The rise time (t_r) and fall time (t_f) are extracted from the turn-OFF and turn-ON waveforms, respectively, as the times between 10% and 90% V_{DS}. Fig. 6 shows the exemplary turn-ON transient

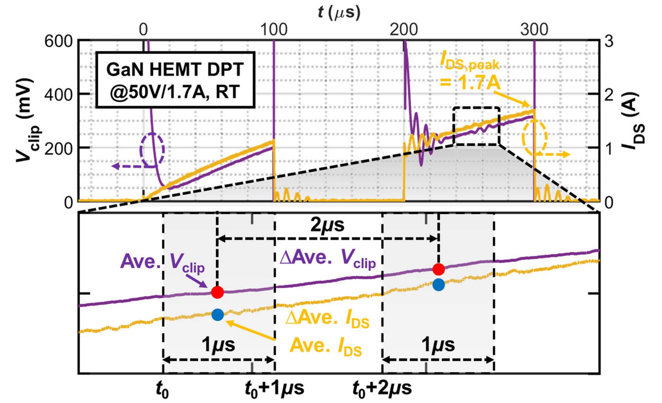


Fig. 7. 50 V/1.7 A DPT waveforms of GaN HEMT at room temperature and the illustration of the dynamic R_{ON} extraction based on the measured clip voltage (V_{clip}) and device I_{DS}.

waveforms of a SiC MOSFET under a 50 V/1 A DPT at room temperature, revealing t_r of 163 ns under this test condition.

The dynamic R_{ON} of GaN HEMT is characterized under various temperatures and V_{dc} levels. Fig. 7 shows the output waveforms of the clipper and shunt during a 50 V/1.7 A DPT at room temperature. The long test loop introduces undesired noise and ringing during device switching transients. To reduce noise impact, dynamic R_{ON} is calculated using the incremental values of the average ON-state voltage (ΔAve. V_{clip}) and current (ΔAve. I_{DS}) over a fixed period. The R_{ON} at time t_0 can then be calculated using the following equation:

$$R_{ON}(t_0) = \frac{\sum_{t_0+2\mu s}^{t_0+3\mu s} V_{clip} - \sum_{t_0}^{t_0+1\mu s} V_{clip}}{\sum_{t_0+2\mu s}^{t_0+3\mu s} I_{DS} - \sum_{t_0}^{t_0+1\mu s} I_{DS}}. \quad (1)$$

In this method, averaging the measured parameters is used to minimize the adverse effects of noise, while the deployment of incremental voltages and currents can cancel out the impact from stray inductances, which have been detailed in [58] and [59].

For static measurements, the output, transfer, third-quadrant, and OFF-state *I-V* characteristics of all DUTs are measured at various temperatures. To minimize the effect of self-heating, a very small duty cycle is used in *I-V* sweep with the maximum current kept below 1 A.

To compare the device characteristics in static measurements and dynamic switching, dynamic *I-V* characteristics are also constructed from the voltage and current waveforms in the DPT. As shown in Fig. 8, this method reconstructs the dynamic output *I-V* characteristics by mapping voltage and current values at the same moment onto the *I-V* coordinates. Benefitted from the shorter conduction time compared to static measurement, this dynamic *I-V* reconstruction can also achieve higher currents without inducing significant heating that impacts measurement.

D. Temperature Measurement Strategies

Fig. 9 shows the schematic of the temperature measurement system. The heat exchangers, where the cooling process happens inside, are connected to the thermal conduction plates. These plates are made of copper with a thin gold plating to achieve

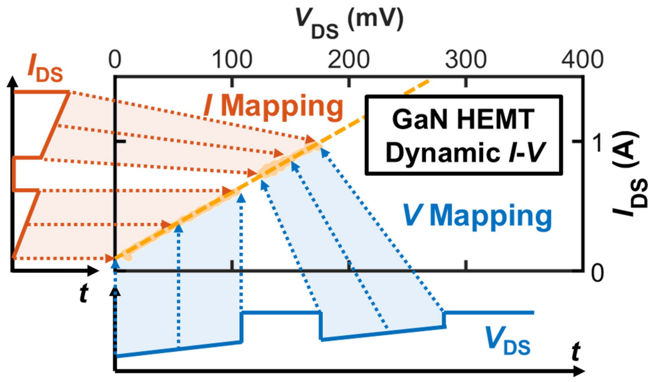


Fig. 8. Illustration of dynamic I-V construction based on DPT waveforms.

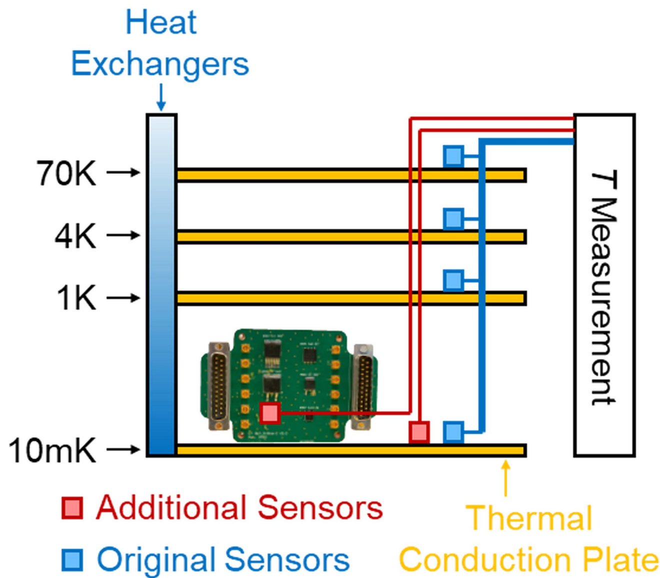


Fig. 9. Schematic of temperature measurement system.

good thermal conduction. Cooled by the heat exchangers, the DUT mounted on the daughter board is also cooled down to the target temperature with the help of tight connections between the daughter board and the thermal paste. Four original temperature sensors are mounted on each plate and connected to the temperature cycling measurement system. To obtain the real case temperature on the DUT, two additional temperature sensors (CX-1010-SD-HT-P) are located next to the original sensor at the 10 mK plate and on top of the DUT, respectively. By calibrating the outputs from additional and original sensors, the DUT's real case temperature can be extracted.

It should be noted that the temperature measurement cycle is around 2 s, which is set to prevent self-heating due to the injected current to the sensors. Hence, the measured temperature reflects a steady-state value, not a transient one. As a result, the measured electrical characteristics indicate device performance within a mK temperature range, which is widely accepted in cryogenic and quantum studies [60], [61], [62], [63]. In this work, all tests were conducted in the ~10 mK environment, and the temperatures marked in the figures were recorded right after testing, accounting for the thermal influences caused by

TABLE IV
SUMMARY OF DEVICE SELF-HEATING LEVEL UNDER VARIOUS TESTS

DUTs	Output	Transfer	Third-quadrant	Breakdown	DPT
GaN	★★	★	★★	★	★
SiC	★★★	★★★	★★★	★	★★★
Si	★★★	★★★	★★★	★	★★★

Note: The number of stars represents the self-heating level from low (★) to high (★★★).

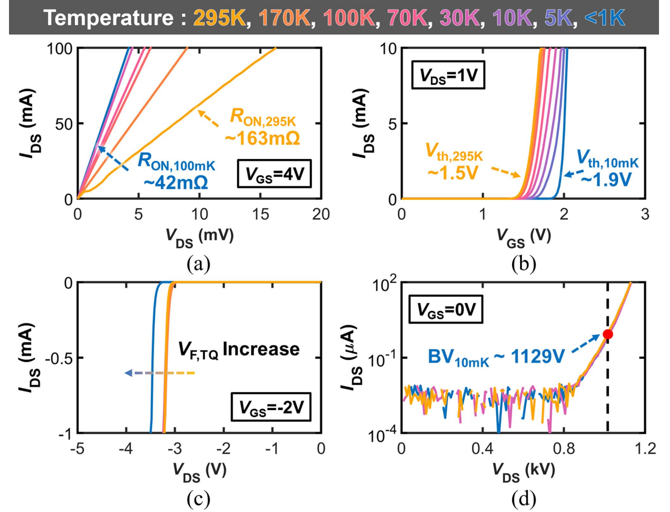


Fig. 10. (a) Output. (b) Transfer. (c) Third-quadrant. (d) OFF-state I_{DS}-V_{DS} characteristics of GaN HEMT at various temperatures.

measurements. Table IV summarizes the device self-heating level under various tests, explaining the variation of recorded temperatures in the following sections.

III. CRYOGENIC CHARACTERISTICS OF GAN HEMT

A. Test Results

The static characteristics of the GaN HEMT were first characterized at various temperatures, ranging from 295 K to below 1 K. Fig. 10(a) shows the output characteristics at a 4 V V_{GS}. The R_{ON} decreases from 163 mΩ at 295 K to 42 mΩ at 100 mK, demonstrating an Ohmic behavior and a 4x reduction in R_{ON} at cryogenic temperatures. Fig. 10(b) shows the transfer characteristics at 1 V V_{DS}, revealing a ~0.4 V increase in threshold voltage (V_{TH}) as the temperature drops to 10 mK. The third-quadrant characteristics under V_{GS} at −2 V are shown in Fig. 10(c), revealing an increase in third-quadrant forward voltage ($V_{F,TQ}$) as temperature decreases. Fig. 10(d) shows the OFF-state I_{DS}-V_{DS} characteristics at 0 V V_{GS}, indicating a nearly temperature-independent breakdown voltage (BV) of approximately 1129 V, extracted at $I_{DS} = 1\ \mu$A.

Fig. 11 shows zoomed-in switching waveforms of the GaN HEMT under a 20 V/0.5 A DPT at 100 mK and 295 K. The t_f/t_r is 283.2/303 ns at 100 mK and 403.2/576 ns at 295 K, respectively. Theoretically, the reduced switching times may be due to the increased transconductance of devices [12], [64] and the reduced loop parasitic parameters. In this test system, the latter factor is believed to be dominant, particularly considering the reduced

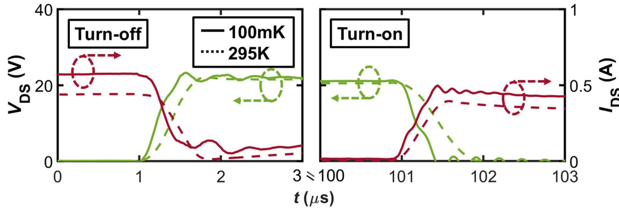


Fig. 11. Zoomed turn-OFF and turn-ON waveforms of GaN HEMT under 20 V/0.5 A DPT at 100 mK (solid lines) and 295 K (dashed lines).

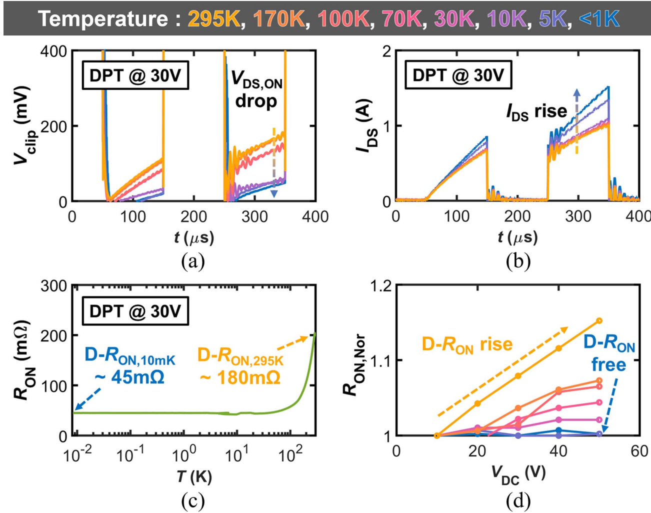


Fig. 12. (a) Voltage and (b) current waveforms of GaN HEMT under 30 V/0.7 A DPT at selected temperatures. (c) Extracted dynamic R_{ON} as a function of temperature down to 10 mK. (d) Extracted normalized R_{ON} as a function of V_{DS} at various temperatures.

R_{SC} with temperature in the gate driving loop. Therefore, the turn-ON and turn-OFF waveforms at 100 mK mainly demonstrate the viability of hard switching under gate control, but do not sufficiently prove the improvement of device switching speed at lower temperatures.

Fig. 12(a) and (b) shows the ON-state voltage and current waveforms during a 30 V/0.7 A DPT, revealing a lower ON-state voltage drop, higher current, and reduced R_{ON} at low temperatures. Switching ringing is observed on V_{clip} and I_{DS} during each turn-ON transient, which can be attributed to the changing of parasitic parameters. The extracted dynamic R_{ON} values from the DPT results are plotted as a function of temperature in Fig. 12(c). The dynamic R_{ON} decreases with temperature, reaching a saturation value of approximately 45 mΩ when the temperature drops below ~10 K. Note that, in this temperature regime, the dynamic R_{ON} is identical to the static value, suggesting the absence of dynamic R_{ON} degradation.

To further confirm this phenomenon, the dynamic R_{ON} is measured under various V_{dc}, as shown in Fig. 12(d). At 295 K, the dynamic R_{ON} increases with V_{dc}, rising to 15% higher than the static value at V_{dc} of 50 V. In contrast, at 100 mK, the dynamic R_{ON} remains the same as the static value under all V_{dc}, confirming the dynamic R_{ON}-free performance at cryogenic temperatures.

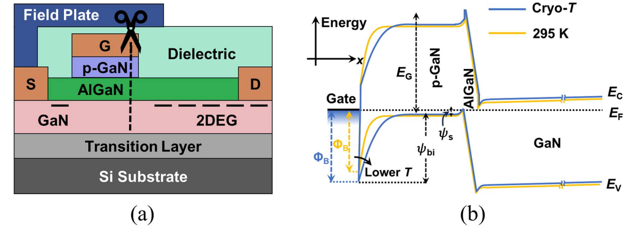


Fig. 13. (a) Schematic of a Schottky p-GaN-gated power HEMT. (b) Comparison of band diagram along the gate/p-GaN/AlGaN/GaN structure at 295 K and cryo-*T*, with higher barrier height at cryo-*T*.

B. Physical Mechanisms

As 2DEG originates from the net polarization charge at AlGaN/GaN heterostructures rather than impurity doping, the free electrons in the 2DEG channel are known to be immune to carrier freeze-out [65], [66]. The static *I-V* characteristics and dynamic switching characterization in this work confirm that this immunity holds down to 0.1 K.

The four-fold reduction in dynamic R_{ON} at $T < 1$ K can be explained by increased 2DEG mobility due to the reduced electron-phonon interactions compared to room temperature [67], [68]. The high BV at $V_{\mathrm{GS}} = 0$ V suggests the functionality of the p-n junction under the gate; otherwise, punch-through would occur. The dynamic R_{ON} degradation typically originates from charge trapping effects at different locations in GaN HEMTs [69]. Its elimination is attributed to the trap freeze-out [17], suggesting the stability issue of GaN HEMTs could be largely resolved at cryogenic temperatures. Additionally, the fast switching speed can be attributed to high transconductance as a result of higher electron mobility at cryogenic temperatures.

The positive V_{TH} shift, although inducing a R_{ON} increase, can derisk the false turn-ON at cryogenic temperatures. The electrostatic V_{TH} model for Schottky-type p-GaN-gated GaN HEMTs [see Fig. 13(a)] is given by [70]

$$V_{TH} \approx \phi_B - E_G/q + \psi_{bi} + \psi_s - \Delta V_b \quad (2)$$

where ϕ_B, ψ_{bi}, ψ_s, E_{G}, and ΔV_b denote the Schottky barrier height relative to the valence band edge, the built-in potential of the p-GaN Schottky contact, surface potential at the p-GaN/AlGaN barrier interface, and voltage drop across the AlGaN barrier.

In practical operational temperatures, the effective p-GaN Schottky barrier height is usually lowered due to the interfacial trap-assisted carrier tunneling, which is temperature-sensitive and can potentially lead to V_{TH} instability [71], [72]. However, at cryo-*T*, the trap freezes out [73], suppressing the trap-assisted tunneling and resulting in an increased Schottky barrier height, as illustrated in Fig. 13(b). According to (2), this causes a more positive V_{TH} in GaN HEMTs due to the widened depletion region across the metal/p-GaN junction [74], [75].

The rise in V_{TH} at cryo-*T* also impacts the third-quadrant *I-V* characteristics of the GaN HEMT, as seen in Fig. 10(c). At $V_{\mathrm{GS}} < V_{\mathrm{TH}}$, the device operates in the third-quadrant when the gate-to-drain bias (V_{GD}) exceeds the threshold voltage, which we denote as $V_{\mathrm{TH,GD}}$ to reflect the third-quadrant turn-ON

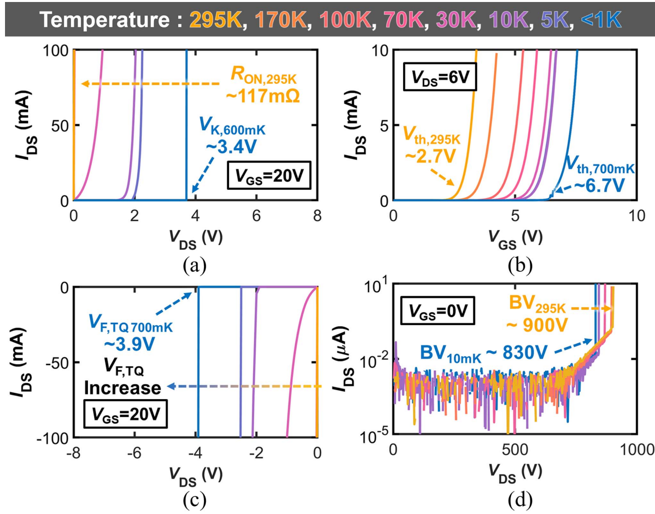


Fig. 14. (a) Output. (b) Transfer. (c) Third-quadrant. (d) OFF-state I_{DS}-V_{DS} characteristics of SiC MOSFET at various temperatures.

physics. The value for $V_{TH,GD}$ represents the fundamental device V_{TH}, which is experimentally determined as the gate-source V_{TH} from the first-quadrant *I-V* characteristics [76]. This turn-ON condition, $V_{GD} = V_{GS} + V_{SD} > V_{TH,GD}$, leads to an approximate relation for the third-quadrant forward voltage ($V_{F,TQ} = V_{SD}$), since the voltage drop across R_{ON} can be neglected due to the steep *I-V* characteristics and relatively low current

$$V_{F,\,TQ} \approx V_{TH,GD} - V_{GS}. \tag{3}$$

This equation suggests that the temperature-dependence of $V_{F,TQ}$ is directly tied to that of V_{TH}, which increases at lower *T*.

IV. Cryogenic Characteristics of SiC MOSFET

A. Test Results

Fig. 14(a) shows the output characteristics of SiC MOSFET at various temperatures under V_{GS} of 20 V. Unlike GaN HEMT, SiC MOSFET exhibits non-Ohmic behavior at temperatures below 70 K, indicating the presence of a knee voltage (V_K). At 295 K, the R_{ON} is 117 mΩ, and V_K is 0 V, but as the temperature drops to 600 mK, V_K increases to 3.4 V. Fig. 14(b) shows the transfer characteristics at a V_{DS} of 6 V, revealing a 4.0 V increase in V_{TH}, from 2.7 V at 295 K to 6.7 V at 700 mK. To further investigate the non-Ohmic behavior, third-quadrant performances were measured with the device in the ON-state at a V_{GS} of 20 V, allowing current to flow through the channel. Fig. 14(c) shows the third-quadrant characteristics under a V_{GS} of 20 V to keep the gated channel on, which almost mirrors those in Fig. 14(a). The $V_{F,TQ}$ is extracted 3.9 V at 700 mK.

The OFF-state I_{DS}-V_{DS} characteristics in Fig. 14(d) show a reduction in BV from approximately 900 V at 295 K to around 830 V at 600 mK. This suggests the avalanche breakdown holds down to cryogenic temperatures, which is known to show a positive temperature coefficient.

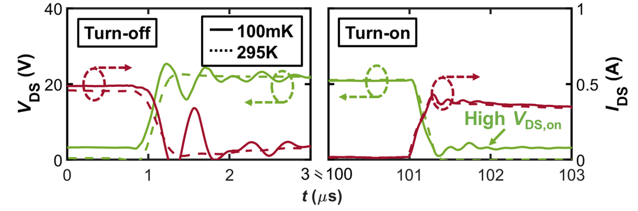


Fig. 15. Zoomed turn-OFF and turn-ON waveforms of SiC MOSFET under 20 V/0.5 A DPT at 100 mK (solid lines) and 295 K (dashed lines).

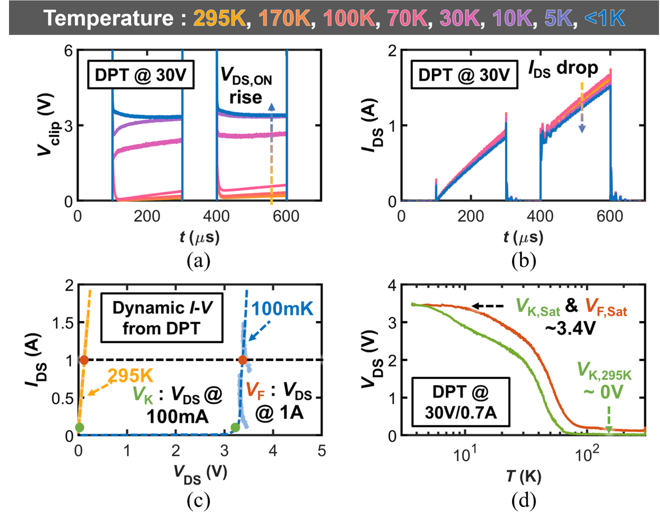


Fig. 16. (a) Voltage and (b) current waveforms of SiC MOSFET under 30 V/0.7 A DPT at selected temperatures. (c) Dynamic *I-V* characteristics extracted from DPT waveforms tested at 295 K and 100 mK. (d) Extracted V_K and V_F as a function of temperature down to 3 K.

Fig. 15 shows the zoomed switching waveforms in the 20 V/0.5 A DPT of SiC MOSFET, revealing a t_f of 197.2 ns and 230.4 ns at 100 mK and 295 K, respectively. The t_r remains relatively unchanged at around 225.0 ns for both temperatures. This result validates the SiC MOSFET's viability for hard-switching under gate control at cryogenic temperatures. A higher V_{DS} in the device's ON-state (VDS, $_{ON}$) can also be directly observed from the DPT waveform.

Fig. 16(a) and (b) shows the temperature-dependent on-state voltage and current waveforms in the DPT, revealing a substantial increase in $V_{DS,ON}$ and decrease in I_{DS} at lower temperatures. The reconstructed dynamic *I-V* characteristics are shown in Fig. 16(c), confirming a dynamic V_K exceeding 3 V at 100 mK. To quantify the non-Ohmic behavior, dynamic V_K is defined as the voltage drop when I_{DS} reaches 100 mA, while the V_F is measured at 1 A, both based on DPT waveforms. Fig. 16(d) shows the extracted dynamic V_K and V_F as a function of temperature, revealing the non-Ohmic behavior starts to appear when temperatures are below ∼60 K. The V_F saturates at ∼3.4 V when temperatures are below ∼10 K.

B. Physical Mechanisms

According to the classic carrier statistics, the lightly doped drift region in SiC power MOSFET is expected to suffer from carrier freeze-out at deep cryogenic temperatures, turning into

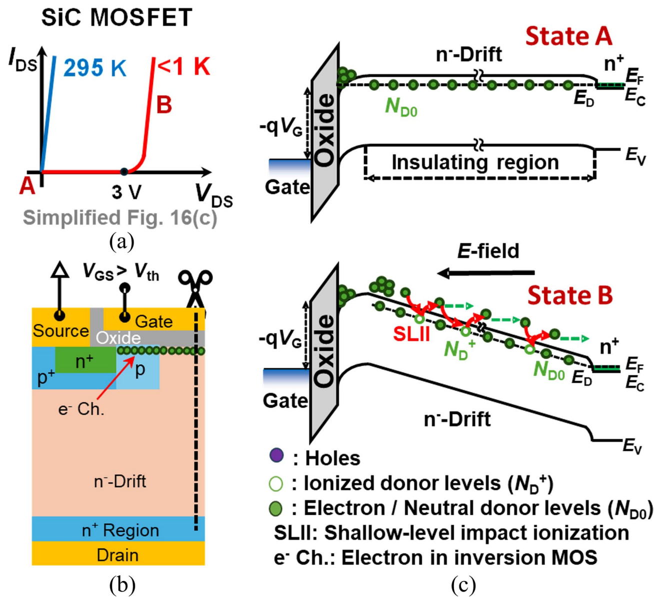


Fig. 17. (a) Illustration of dynamic I_{DS}-V_{DS} curves of SiC MOSFET under room temperature and cryogenic temperatures. (b) SiC MOSFET unit-cell showing electrons in the inversion and accumulation MOS channels. (c) Band diagrams along the cutline during states A and B, highlighting the electron tunneling and SLII processes in State B.

a semi-insulating state. The heavily doped n^+ and p^+ regions, however, can remain conductive at cryogenic temperatures due to Mott transition [77], ensuring the operational Ohmic contacts. In SiC MOSFET, the functionality of these heavily doped regions and the p^+-n^- junction at deep cryogenic temperatures is supported by the observed avalanche breakdown down to 10 mK, which suggests the absence of p^+-base punch-through.

A surprising yet significant finding is the viability of current conduction in the n^--SiC drift layer with a non-Ohmic behavior, despite carrier freeze-out [see Fig. 17(a)]. Here, we provide a physics-based model based on the shallow-level impact ionization (SLII) theory to explain this phenomenon at deep cryogenic temperatures.

At $V_{GS} > V_{TH}$, electrons from n^+-SiC transport via the inversion-MOS channels in the p-SiC region and possibly also the accumulation-MOS channel in the JFET region, as shown in Fig. 17(b). The formation of such inversion-MOS channels down to 15 mK has been reported in Si recently [78]. At zero or relatively low V_{DS}, i.e., State A in Fig. 17(a), the shallow donor level (E_D), which overlaps with the Fermi level (E_F), is fully occupied due to the energy minimization requirement – the Fermi level pinning effect. The band structure and carrier dynamics are illustrated in Fig. 17(c).

As V_{DS} increases, i.e., State B in Fig. 17(a), electrons injected via the MOS channels can then induce current conduction via the SLII in the drift region, in which the kinetic energy of electrons gained from the electric field reaches the ionization threshold and in turn ionizes the neutral donor (N_{D0}) through electron-donor collisions [79], [80], [81]. This SLII process is illustrated in Fig. 17(c). Notably, it differs from the conventional impact ionization in that it involves donors instead of holes.

The experimentally observed high V_K can be explained by the electric field required to initiate the SLII. After device turn-ON, carrier multiplication in the SLII can explain the sharp current increase and steep I-V. As the V_K appears when the temperature drops below ∼60 K, carrier freeze-out is believed to start appearing at this critical temperature. At $T \sim 3$ K, V_K starts to saturate [see Fig. 16(d)], indicating a full carrier freeze-out in the drift region and the dominance of current conduction by the above SLII mechanism.

Finally, as shown in Fig. 14(b), at high V_{DS}, V_{TH} shows a significant positive shift as T decreases, increasing from 2.7 V at 295 K to 6.7 V at 700 mK. This behavior, which has also been reported in other cryogenic studies of SiC MOSFET at higher temperatures [82], can be understood using the analytical V_{TH} model in a SiC MOSFET

$$V_{TH} = ln\left(\frac{N_A}{n_i}\right) + \frac{\sqrt{4\epsilon kT N_A \ln\left(\frac{N_A}{n_i}\right)}}{C_{ox}} - \frac{q\left[Q_F + Q_{IT}(T)\right]}{C_{ox}} \tag{4}$$

where N_A, n_i, k, C_{ox}, Q_F, and Q_{IT} denote the p-SiC doping concentration, intrinsic carrier concentration, Boltzmann constant, unit-area gate oxide capacitance, fixed oxide charge, and oxide/SiC interface traps, respectively.

This positive V_{TH} shift could be explained by two main physical mechanisms. First, as T decreases, n_i is reduced exponentially ($n_i \sim \exp(-E_G/kT)$) [83], which causes an increase in the first two terms in (4). Second, since the SiO_2/SiC interface contains a large density of Q_{IT}, continuously decreasing T could lead to the trap freeze out, leading to a further increase in V_{TH} [82], [84], [85].

V. Cryogenic Characteristics of Si IGBT

A. Test Results

Fig. 18(a)–(d) shows the static characteristics of Si IGBT at various temperatures. Similar to SiC MOSFET, V_K measured at 20 V gate-emitter voltage (V_{GE}) increases from 0.6 V at 295 K to 3.6 V at 400 mK. Additionally, a 0.8 V shift in V_{TH} is observed under 6 V collector-emitter voltage (V_{CE}) as temperature drops to 500 mK. Unlike SiC MOSFET and GaN HEMT, Si IGBT cannot operate in the third-quadrant due to its PNP structure. Instead, many commercial devices co-package a PN diode in parallel with IGBT for reverse conduction. Fig. 18(c) shows the third-quadrant characteristics of Si IGBT at 20 V V_{GE}, which reflect the diode's behavior, revealing an increase in forward voltage drop as temperature decreases. Similar to SiC MOSFET, the breakdown voltage of Si IGBT also decreases at lower temperatures, from 735 V at 295 K to 619 V at 10 mK, suggesting consistent avalanche breakdown.

Fig. 19 shows the zoomed switching waveforms of Si IGBT under a 20 V/0.5 A DPT. During the turn-OFF and turn-ON transients, the t_f/t_r is 326.4/202 ns at 295 K and 158.4/144 ns at 100 mK, respectively. This validates the hard-switching viability of Si IGBT under gate control at deep cryogenic temperatures.

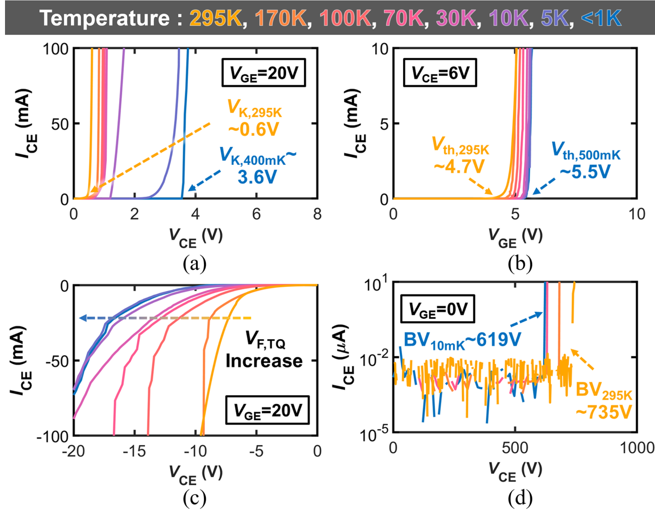


Fig. 18. (a) Output. (b) Transfer. (c) Third-quadrant. (d) OFF-state I_{CE}-V_{CE} characteristics of Si IGBT at various temperatures.

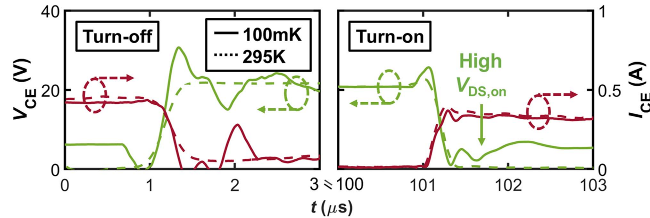


Fig. 19. Zoomed turn-OFF and turn-ON waveforms of Si IGBT under 20 V/0.5 A DPT at 100 mK (solid lines) and 295 K (dashed lines).

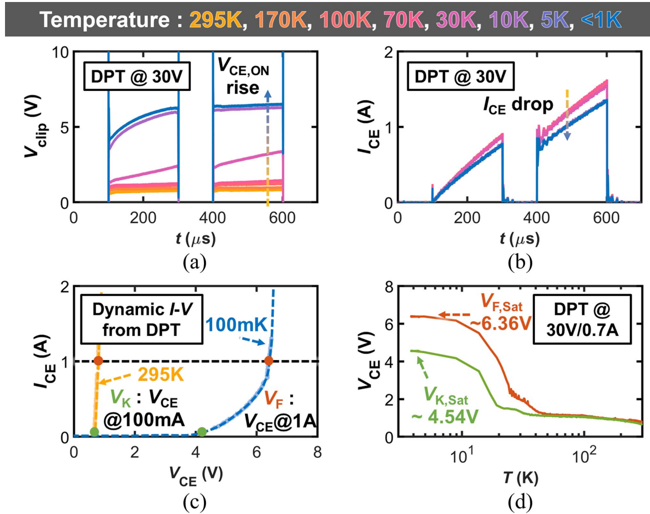


Fig. 20. (a) Voltage and (b) current waveforms of Si IGBT under 30 V/0.7 A DPT at selected temperatures. (c) Dynamic *I-V* characteristics extracted from DPT waveforms tested at 295 K and 100 mK. (d) Extracted V_{K} and V_{F} as a function of temperature down to 3 K.

Fig. 20(a) and (b) shows the ON-state voltage and current waveforms of Si IGBT in a 30 V/0.7 A DPT. Similar to SiC MOSFET, the increase in V_{CE} and decrease in collector-emitter current (I_{CE}) are observed as temperature decreases. The dynamic *I-V* curves in Fig. 20(c) reveal an increase in dynamic V_{K} and V_{F} at cryogenic temperatures. Fig. 20(d) provides a clearer view of the temperature dependence of the dynamic V_{K} and V_{F}, showing that both V_{K} and V_{F} start increasing at temperatures below 40 K and saturate at temperatures below 10 K. The saturated V_{K} and V_{F} reach 4.54 V and 6.36 V, respectively.

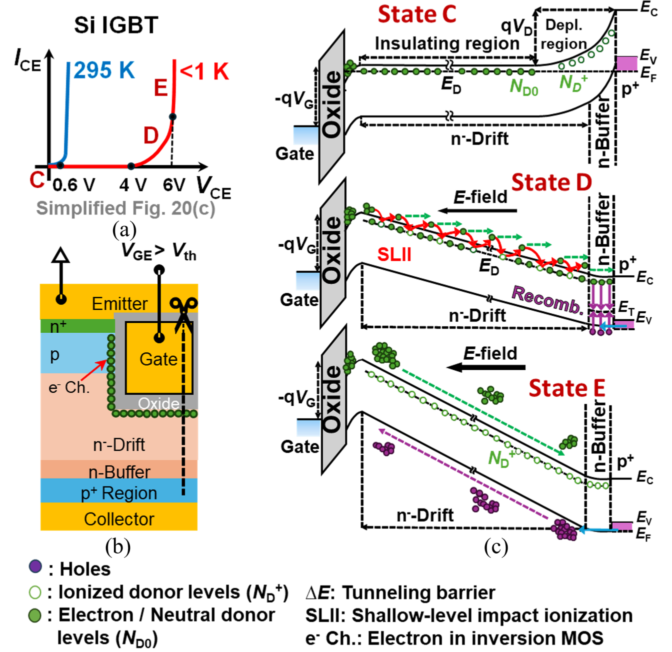


Fig. 21. (a) Illustration of dynamic I_{CE}-V_{CE} curves of Si IGBT under room temperature and cryogenic temperatures; three operation states are marked. (b) Si IGBT unit-cell showing electrons in the inversion and accumulation MOS channels. (c) Band diagrams along the cutline during states C, D, and E, highlighting the SLII-based unipolar conduction in State D and the bipolar conduction in State E.

B. Physical Mechanisms

Fig. 21(a) shows a simplified illustration of the forward characteristics of Si IGBT at room temperature and deep cryogenic temperatures. Compared to the behavior of SiC MOSFET, Si IGBT shows a similar increase in V_{K} at lower temperatures (i.e., State C); however, after turn-ON, Si IGBT exhibits a two-step conduction process at $V_{\mathrm{CE}} > 4$ V – unipolar conduction occurs at V_{CE} between 4 V and 6 V (State D), and it transitions into bipolar conduction at $V_{\mathrm{CE}} > 6$ V (State E).

The delayed turn-ON in Si IGBT can be explained similarly to SiC MOSFET. When $V_{\mathrm{GE}} > V_{\mathrm{TH}}$, electrons from n^{+}-Si transport via the inversion-mode MOS channels near the oxide/p-Si interface and possibly also the accumulation-mode MOS channels near the oxide/n^{-}-Si interface into the JFET region and drift region [see Fig. 21(b)]. Under zero and low V_{CE} bias (i.e., State C), carriers freeze out in the n^{-}-Si drift region, and E_{D} is fully occupied by electrons. Additionally, a diffusion barrier (qV_{D}) is formed across the depletion region near the p^{+}-Si substrate. The energy band diagram and carrier dynamics are shown in Fig. 21(c).

Similar to SiC MOSFET, the first turn-ON (i.e., State D) in Si IGBT can be explained by the electron transport through SLII in the n^{-}-Si drift layer, where unipolar conduction prevails [see

Fig. 21(c)]. At room temperature, bipolar conduction is established nearly instantaneously after Si IGBT turns ON. However, at deep cryogenic temperatures, an additional 2 V in V_{CE} is required to initiate bipolar conduction (i.e., State E).

This prolonged transition into bipolar states can be attributed to two factors. First, at low T, the hole recombination in the n-Si buffer layer is significantly enhanced due to the reduced hole lifetime under the combined Shockley–Read–Hall and Auger recombination [86]. This enhances the hole recombination rate, further requiring additional V_{CE} to sustain bipolar conduction. Moreover, the defect trap level (E_{T}) can act as a hole recombination barrier, rapidly annihilating the injected holes. Second, the holes injected into the drift region from the p^+-substrate further increase the electric field slope, enlarging the voltage drop in the drift region. As a result, a higher V_{CE} is required to reverse-bias the emitter/base junction to allow for hole extraction. This mechanism, in conjunction with the enhanced hole recombination, explains the delayed entry into the bipolar conduction under cryogenic temperatures.

Finally, as shown in Fig. 18(b), a positive V_{TH} shift is observed as T decreases, with V_{TH} increasing from 4.7 V at 295 K to 5.5 V at 500 mK. This 0.8 V shift is significantly smaller than the 4.0 V shift observed in SiC MOSFET, indicating an improved V_{TH} stability in Si IGBT at deep cryo-T. The physical origin can be understood using the same analytical model presented in (4), as the turn-ON of an IGBT is also governed by the formation of an inversion MOS channel. The key difference lies in the quality of the gate oxide interface. Unlike the SiC/SiO_2 interface, which is known to have a high density of interface traps, the thermally grown Si/SiO_2 interface in the Si IGBT is of exceptionally high quality. Thus, the contribution of the T-dependent Q_{IT} (T) to the V_{TH} shift is minimal in the Si IGBT, and the observed positive V_{TH} shift appears to be dominated by the more fundamental and predictable effect of n_{i} decreasing with lower T.

VI. Conclusion

We present the first static and dynamic characterizations of Si IGBT, SiC MOSFET, and GaN HEMT down to 10 mK using a dilution refrigerator integrated with a custom circuit setup to perform hard-switching DPT and *in situ* dynamic R_{ON} extraction during the steady-state switching. All three devices are found to be able to maintain high breakdown voltage and normally-OFF operation, and perform hard switching under the gate control.

As temperature dips into the cryogenic regime, GaN HEMT shows reduced conduction loss and fast switching speed, with a complete elimination of the dynamic R_{ON} degradation. The R_{ON} at cryogenic temperatures is 4.5 times lower than that at room temperature. This improved performance can be explained by the absence of carrier freeze-out in the 2DEG channel, the enhanced 2DEG mobility, and the deactivation of trap states at cryogenic temperatures. The positive shift in V_{TH} can be mainly attributed to the elevated Schottky barrier height on p-GaN.

When the temperature drops below 60 K, SiC MOSFET starts to become non-Ohmic with a V_{K} increase to over 3 V at cryogenic temperatures. This leads to an increase in conduction loss in both the first-quadrant and third-quadrant. At ultralow temperatures, the viability of current conduction despite carrier freeze-out can be explained by electron tunneling from the channel into the drift region, followed by the shallow-level impact ionization modulated by the donor states in the drift region. The nonzero V_{K} originates from the electric field required to initiate these tunneling and impact ionization processes.

Similar to SiC MOSFET, Si IGBT also exhibits a V_{K} increase down to cryogenic temperatures. In addition, Si IGBT shows a two-step conduction process after turn-ON, transitioning from a unipolar conduction to bipolar conduction. While the V_{K} increase can be explained by the SLII mechanism, the delayed onset of bipolar conduction is probably due to the enhanced hole recombination at cryogenic temperatures. Overall, the conduction loss of Si IGBT also increases with the decreased temperature.

From the application viewpoint, GaN HEMT can open the door for developing deep cryogenic power electronics. From the physics viewpoint, SiC MOSFET and Si IGBT provide platforms to study the unipolar and bipolar carrier transport in a nearly-intrinsic drift layer at cryogenic temperatures.

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