Complete Stability Region of the Double-Loop AC-Voltage Control in LC-Filtered VSIs and Its Improvement by Means of Voltage Decoupling

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***Abstract*—Voltage-controlled voltage-source inverters with an output LC filter are used in a wide variety of power supply applications. Common control structures include single-loop and double-loop voltage control, typically employing a proportional-resonant voltage controller. This article focuses on the double-loop voltage control, where a proportional controller is employed in the inner current control loop. The stability region is defined as the frequency ratios between the sampling frequency (f_s) and the natural frequency of the LC filter (f_n) with which the system can be stable. In previous publications, it has been proposed to place the current controller in the feedback path of the inner control loop, rather than in the forward path, with the aim of increasing the stability region. This article demonstrates that both control structures are equivalent, with the same stability region, although they require different controller tuning. This article presents, for the first time, the complete stability region of the double-loop voltage control, and demonstrates that it can be stable for any frequency ratio f_n/f_s. The stability region presented in previous publications, where $f_n = f_s/6$ is a critical frequency, is the stability region that allows obtaining a minimum-phase system, which should not be confused with the complete stability region. Finally, it is demonstrated that the unitary decoupling of the capacitor voltage allows obtaining a minimum-phase system across the complete stability region. Experimental results confirm the theoretical analysis conducted.**

***Index Terms*—Decoupling, double-loop voltage control, proportional-resonant controller, resonant frequency, sampling frequency, stability.**

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NOMENCLATURE

Acronyms

DG	Distributed generation.
DLVADC	Double-loop voltage-active damping control.
DLVCC	Double-loop voltage-current control.
ESR	Equivalent series resistance.
GPU	Ground power unit.
LHP	Left-half plane.
P	Proportional.
PI	Proportional integral.
PR	Proportional resonant.
PWM	Pulsewidth modulation.
RHP	Right-half plane.
SRF	Synchronous reference frame.
UPS	Uninterruptible power supply.
VSI	Voltage-source inverter.
ZOH	Zero-order hold.

Parameters

C_f	Filter capacitor.
f_n	Natural or resonant frequency of the LC filter.
f_o	Fundamental frequency.
f_s	Sampling frequency.
f_{sw}	Switching frequency.
K_{PI}	Proportional gain of the current controller or active damping coefficient.
K_{PV}	Proportional gain of the voltage controller.
K_{RV}	Resonant gain of the voltage controller.
L	Load inductor.
L_f	Filter inductor.
R	Load resistor.
R_f	Filter inductor ESR and converter equivalent loss resistance.
T_s	Sampling period.
ω_n	Natural or resonant angular frequency of the LC filter.
ω_o	Fundamental angular frequency.

Variables

i_C	Capacitor current.

i_L Inductor current.
i_O Output current.
s Continuous-time domain or Laplace variable.
v_C Capacitor voltage.
v_C^* Reference voltage.
v_{dc} DC-bus voltage.
v_i Voltage at the output of the converter.
w Continuous-time domain variable resulting from applying the inverse Tustin transform.
z Discrete-time domain variable.

I. Introduction

VOLTAGE-CONTROLLED VSIs with an output LC filter have been widely used in power supply applications, such as 50/60-Hz UPS systems [1], [2], [3], 400-Hz GPUs for airplanes [4], [5], and DG systems [6]. The main issue with LC filters is resonance, which may introduce stability problems that make the system unstable [7].

The voltage must be followed with zero steady-state error. In this context, numerous control alternatives have been studied, which can mainly be divided into linear [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26] and nonlinear control techniques [27], [28], [29], [30], [31]. Linear control techniques using transfer functions are usually employed [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], although there are also publications where state-space methods are applied [24], [25], [26].

Focusing on linear control, the use of PI controllers involves working with continuous signals, so it would be necessary to work in the SRF [32]. The use of PR controllers allows working within the stationary reference frame, avoiding transformations to the SRF and the associated cross-coupling between d and q axes [33], [34]. Furthermore, PR controllers will control the positive and negative sequences at the frequency to which they are tuned, the fundamental frequency (f_o), which is equivalent to two PI controllers in two SRFs, one of positive sequence and another of negative sequence [35]. This article focuses on the use of PR controllers in the stationary reference frame. However, the conclusions obtained can be extended to the use of PI controllers in the SRF. The comparison with other control methods is beyond the scope of this article.

In this context, the use of digital controllers has become the standard practice. When working with a digital control system, the inevitable presence of the computational delay, combined with the effect of the PWM, will significantly impact the stability of the system [36], [37].

Numerous previous publications have demonstrated that, when using a linear control strategy with a PR (or PI) controller in VSIs with an output resonant filter, the stability of the system primarily depends on the frequency ratio between the sampling frequency (f_s) and the natural (or resonant) frequency of the filter (f_n) [8], [9], [10], [11], [12], [21], [22], [23], [38], [39], [40], [41], [42]. Therefore, the stability region of these systems can be defined as the region created by the frequency ratios between f_s and f_n with which the system can be stable, taking the Nyquist frequency ($f_n = f_s/2$) as the maximum upper bound of this stability region. In [39], it is demonstrated that this stability region depends on the value of the computational delay considered. In this article, it will always be assumed that the computational delay is one sampling period (T_s), as this is the most common situation. Therefore, the frequency ratios presented in this article are valid for a computational delay of one sampling period.

In [43], a broader review of the different linear voltage and current control methods in VSIs with an output resonant filter is presented, where it is shown that voltage control structures with linear controllers in VSIs with an output LC filter can be classified into two main groups: single-loop voltage control with PR (or PI) controller [8], [9], [10], [11], [12] and double-loop voltage control with PR (or PI) controller [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23]. Hereafter, for the sake of brevity, they will be referred to as the single-loop voltage control and the double-loop voltage control.

The single-loop voltage control directly controls the capacitor voltage, while the double-loop voltage control includes an inner current control loop to add damping to the system. Including an inner control loop is a widely used active damping method, which has the advantage over passive damping [44], [45], [46] in that it does not require additional physical components, so it does not introduce additional power losses. In the double-loop voltage control, either the capacitor current or the inductor current can be controlled. The results obtained with both current control loops are similar in terms of setpoint tracking. However, controlling the capacitor current provides better results in terms of load harmonic rejection [47], [48], while controlling the inductor current allows easier implementation of overcurrent protection, making it the most widely used method [13], [14], [15], [16], [17], [18], [19], [20] and, therefore, the double-loop voltage control studied in this article.

The stability region of the single-loop voltage control has been derived in numerous previous publications [8], [9], [10]. In [8], it is stated that the single-loop voltage control can only be stable if $f_s/3 < f_n < f_s/2$. However, in [9], it is demonstrated that the results presented in [8] apply to the case of using a PR controller with positive P gain, and the stability region of the single-loop voltage control is defined as $f_s/3 < f_n < f_s/2$ when a positive P gain is used, whereas it is defined as $f_n < f_s/3$ when a negative P gain is used.

System stability requires that none of its poles lie in the RHP of Laplace. Therefore, for the single-loop voltage control to be stable, the resonant gain of the PR controller must be positive, regardless of the sign of the P gain, as the poles introduced by the PR controller must be located in the LHP of Laplace [10]. Nevertheless, the system may still be stable even if some of its zeros are located in the RHP of Laplace. A minimum-phase system has all its zeros located in the LHP of Laplace (i.e., with negative real parts), whereas a nonminimum-phase system has at least one zero located in the RHP of Laplace (i.e., with positive real part), which significantly worsens its transient response [49]. The single-loop voltage control with a PR controller with positive P gain results in a minimum-phase system, as the zeros of the PR controller will be located in the LHP of

Laplace, whereas if the P gain is negative, a nonminimum-phase system will be obtained, as the zeros of the PR controller will be located in the RHP of Laplace [9]. Therefore, for the single-loop voltage control to be stable: if $f_n < f_s/3$, a negative P gain must be used, resulting in a nonminimum phase system; whereas if $f_s/3 < f_n < f_s/2$, a positive P gain must be used, resulting in a minimum-phase system.

In [10], it is demonstrated that the single-loop voltage control with capacitor voltage unitary decoupling allows working with positive P gains when f_n is either above or below $f_s/3$, always resulting in a minimum-phase system. Hence, unitary decoupling of the capacitor voltage leads to a significant enhancement of the stability region in the single-loop voltage control. If f_n is exactly equal to $f_s/3$, the single-loop voltage control, with or without decoupling, will always be unstable. Therefore, in the single-loop voltage control, with or without decoupling, $f_n = f_s/3$ is a critical frequency [10].

The stability studies of the single-loop voltage control highlight the importance of determining the complete stability region of a system, which will be defined as the stability region encompassing all conditions under which the system can be stable, considering both minimum-phase and nonminimum-phase behavior. Once the complete stability region of the system has been determined, the effect of unitary decoupling of the capacitor voltage on this region can be analyzed, in order to assess whether the same advantages observed in the single-loop voltage control can also be achieved in other systems.

In the double-loop voltage control, there are a PR voltage controller and a P current controller. The placement of the PR voltage controller is fixed. However, the P current controller can be placed in the forward path [13], [14], [15], [16], [17], [18], [19], [20] or in the feedback path [21], [22], [23], where it ceases to be a controller and becomes an active damping coefficient. From this moment on, the double-loop voltage control with the P current controller in the forward path will be referred to as the DLVCC, while the double-loop voltage control with the active damping coefficient in the feedback path will be referred to as the DLVADC.

The determination of the complete stability region of the double-loop voltage control is more complex, as it must take into account the possibility that the system may be stable with either a stable or unstable inner current control loop. Furthermore, it must account for the possibility of operating with positive and negative gains in both controllers. Table I summarizes the state of the art of the double-loop voltage control and the main contributions of this article in terms of the stability region. To date, in both the DLVCC and the DLVADC, only the use of a PR voltage controller with positive P and resonant gains has been considered [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23]. Furthermore, on the one hand, in the DLVCC, only the possibility of using positive gains in the P current controller has been explored [13], [14], [15], [16], [17], [18], [19], [20]. On the other hand, in the DLVADC, the use of both positive and negative active damping coefficients has indeed been studied [21], [22], [23].

To date, there is no publication that calculates the stability region of the DLVCC (see Table I). However, in all previous works where this control method is used, the condition $f_n < f_s/6$ is satisfied [13], [14], [15], [16], [17], [18], [19], [20]. There are also publications in which unitary decoupling of the capacitor voltage has been applied to the DLVCC [16], [17], [18], [19], [20] (see Table I). However, in all these articles, a specific system with fixed parameters is studied, and the controllers are tuned using a trial-and-error method, without considering that the stability of the system depends on the parameters used.

There are publications that attempt to determine the complete stability region of the DLVADC, proposing the use of both positive and negative active damping coefficients [21], [22], [23] (see Table I). The physical interpretation of using negative active damping coefficients requires a brief explanation. The inner current control loop can be modeled as a virtual impedance in series with the filter inductor [21]. Due to control delays, this virtual impedance becomes frequency-dependent and, therefore, cannot behave as a pure resistor. Its real part (i.e., the resistive component), which is directly related to the damping, also varies with frequency, and can take on both positive and negative values. To ensure system stability, the overall damping must be positive. Consequently, when the real part of the virtual impedance becomes negative, the use of negative active damping coefficients is justified to maintain a positive damping.

The authors in [21] and [22] determined the stability region of the DLVADC considering only the case where the system is stable with a stable inner active damping control loop (see Table I). In [23], the possibility of the DLVADC being stable with an unstable inner active damping control loop is also considered (see Table I). The stability region of the DLVADC presented in [23] can be summarized as: if $f_n < f_s/6$, the active damping coefficient must be positive; if $f_s/6 < f_n < f_s/3$, the active damping coefficient must be negative; if $f_s/3 < f_n < f_s/2$, the active damping coefficient can be both positive and negative; and if $f_n = f_s/6$, the DLVADC cannot be stable. Therefore, it is concluded that $f_n = f_s/6$ is a critical frequency in the DLVADC. However, in all these papers [21], [22], [23], the

TABLE I
STABILITY REGION OF THE DOUBLE-LOOP VOLTAGE CONTROL: EXISTING LITERATURE VERSUS THIS ARTICLE

Control Structure	Ref.	Dec.[1]	SR[2]	K_{PI}[3]	K_{PV}[5]
DLVCC	[13]–[15]	✗	✗	NA[4]	NA
	[16]–[20]	✓	✗	NA	NA
	This article	✓	✓✓	+ –	+ –
DLVADC	[21], [22]	✗	✓	+ –	+
	[23]	✗	✓✓	+ –	+
	This article	✓	✓✓	+ –	+ –

[1] Effect of voltage decoupling considered.
[2] Stability region: "✗" not calculated, "✓" calculated only for stable inner loop, "✓✓" calculated for stable and unstable inner loop.
[3] Stability region calculated considering the possibility of using positive and negative proportional gains in the inner control loop.
[4] Not applicable since the stability region is not calculated.
[5] Stability region calculated considering the possibility of using positive and negative P gains in the outer control loop.

stability region of the DLVADC is calculated under the assumption that the P gain of the PR voltage controller is positive (see Table I), when the possibility of it being negative should also be considered to calculate the complete stability region of the DLVADC. This article demonstrates that the stability region presented in [23] corresponds to the stability region that guarantees a minimum-phase system; however, it does not represent the complete stability region. The effects of capacitor voltage unitary decoupling on the stability region of the DLVADC have not been investigated in any publication to date (see Table I).

There are numerous articles demonstrating that, in current-controlled VSIs with an output LCL filter, $f_n = f_s/6$ is a critical frequency [40], [41], [42]. As previously explained, this article focuses on voltage-controlled VSIs with an output LC filter. Therefore, although the same critical frequency appears in the double-loop voltage control [20], [21], [22], [23], the two systems should not be confused.

The main contributions of this article are as follows.

1) The demonstration that the DLVCC and the DLVADC are equivalent control structures. Therefore, one stability region for the double-loop voltage control can be defined and applied for both control structures. However, to achieve the same system with the DLVCC as with the DLVADC, the tuning of the controllers must be different. One key difference is that, in the DLVCC, the use of negative P gains in the current controller requires the use of negative resonant gains in the PR voltage controller. To the best of the authors' knowledge, no previous publication has proposed the use of negative resonant gains in a PR controller. This explains the absence of prior publications working with the DLVCC for $f_n > f_s/6$.
2) The determination, for the first time, of the complete stability region of the double-loop voltage control. This article demonstrates that the double-loop voltage control can be stable for any frequency ratio f_n/f_s, unlike the single-loop voltage control, where $f_n = f_s/3$ is a critical frequency. This article also demonstrates that the stability region of the double-loop voltage control presented in previous publications, where $f_n = f_s/6$ is a critical frequency, is the stability region that allows obtaining a minimum-phase system, which should not be confused with the complete stability region. The frequency ratio $f_n = f_s/6$ is the only case for which the double-loop voltage control cannot be a minimum-phase system.
3) The demonstration that the unitary decoupling of the capacitor voltage allows obtaining a minimum-phase system across the complete stability region of the double-loop voltage control, demonstrating the benefits of having determined it. It is concluded that the double-loop voltage control with unitary decoupling of the capacitor voltage is a highly interesting control method to be used in voltage-controlled VSIs with an output LC filter.
4) The proposal of a tuning method that ensures the stability of the double-loop voltage control, both with and without unitary decoupling of the capacitor voltage. It is experimentally demonstrated that the same controller tuning can be used in a situation where $f_n < f_s/6$, in another where $f_n = f_s/6$, and in another where $f_n > f_s/6$, something that was previously unthinkable.

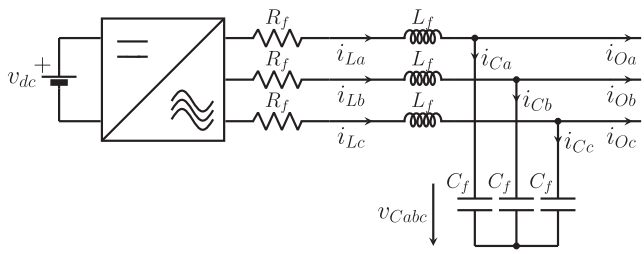


Fig. 1. Three-phase VSI with an output LC filter.

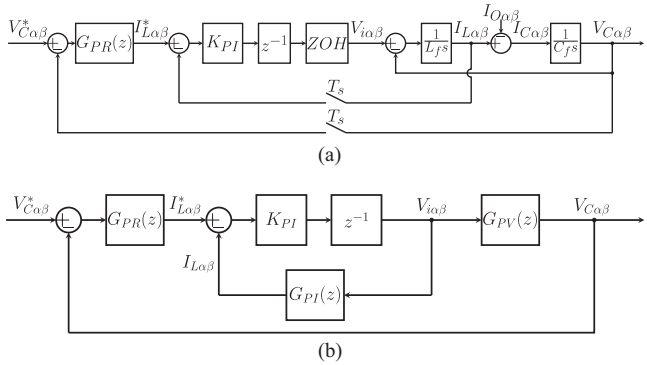


Fig. 2. DLVCC. (a) Block diagram. (b) Simplified block diagram in the discrete-time domain.

II. System Description

The system studied, a three-phase VSI with an output LC filter, is shown in Fig. 1. L_f and C_f are the filter inductor and the filter capacitor, respectively. R_f represents the inductor ESR and the VSI equivalent loss resistance, which is important to take into account when operating far from its nominal conditions [50]. Stability studies will be carried out considering that the filter and converter ESR is zero ($R_f = 0$), with the aim of working in the most unfavorable conditions, since this resistor will introduce a damping that increases the stability region. A constant dc-link voltage v_{dc} is assumed. The voltage at the output of the converter is v_i. The stability analysis will be carried out with no load connected to the system, so the output current, i_O, will be zero, and the inductor current, i_L, will be the same as the capacitor current, i_C. If working with a load that has a resistive component, which is the most common situation, damping would be added to the system, and the stability regions would be increased. Therefore, the calculated stability regions correspond to the most unfavorable case.

This article focuses on voltage-controlled VSIs, so the capacitor voltage, v_C, is the controlled variable, which must be controlled with zero steady-state error. As previously explained, the control structure studied is the double-loop voltage control. The block diagram of the DLVCC is shown in Fig. 2(a), and the block diagram of the DLVADC is shown in Fig. 3(a). The simplified block diagrams in the discrete-time domain are shown in Figs. 2(b) and 3(b). The controllers will work in the stationary

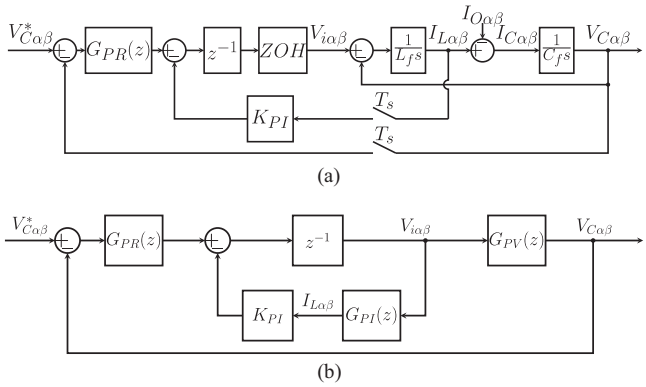


Fig. 3. DLVADC. (a) Block diagram. (b) Simplified block diagram in the discrete-time domain.

reference frame, so PR controllers tuned at the fundamental angular frequency (ω_o) are used in the voltage control loop. The P gain of the P current controller (DLVCC) and the active damping coefficient (DLVADC) are represented as K_{PI}. The inductor current is used in the inner current control loop, but the conclusions would be the same if the capacitor current were used, since no load is connected to the system in the stability analysis. The voltages and currents are denoted with the subscript $\alpha\beta$ to represent the stationary reference frame. The voltage and current references are denoted with the superscript*. The inverter introduces a gain of $v_{\mathrm{dc}}/2$ [51], so the modulating signals must be multiplied by $2/v_{\mathrm{dc}}$ to cancel that gain. These gains are not included in the block diagrams for simplicity. A computational delay of one sampling period (T_s) is considered, and it is represented by z^{-1}. The effect of the PWM is modeled as a ZOH [36], [37].

The continuous-time domain transfer functions that relate the voltage at the output of the converter with the capacitor voltage, $G_{\mathrm{PV}}(s)$, and with the inductor current, $G_{\mathrm{PI}}(s)$, considering the current through the load to be zero (open circuit), can be easily obtained by applying Mason's rule [49]

$$G_{\mathrm{PV}}(s) = \left.\frac{V_{c\alpha\beta}}{V_{i\alpha\beta}}\right|_{I_{O\alpha\beta}=0} = \frac{1}{L_f C_f s^2 + 1} = \frac{\omega_n^2}{s^2+\omega_n^2} \tag{1}$$

$$G_{\mathrm{PI}}(s) = \left.\frac{I_{L\alpha\beta}}{V_{i\alpha\beta}}\right|_{I_{O\alpha\beta}=0} = \frac{C_f s}{L_f C_f s^2 + 1} = \frac{\frac{1}{L_f}s}{s^2+\omega_n^2} \tag{2}$$

where ω_n is the natural (or resonant) angular frequency of the LC filter

$$\omega_n = \frac{1}{\sqrt{L_f C_f}} = 2\pi f_n. \tag{3}$$

For the discrete-time domain analysis, the effect of the PWM is included by discretizing (1) and (2) with a ZOH. The discrete-time domain transfer function that relates the voltage at the output of the converter with the capacitor voltage is

$$G_{\mathrm{PV}}(z) = \frac{(z+1)(1-\cos(\omega_n T_s))}{(z^2 - 2z\cos(\omega_n T_s)+1)} \tag{4}$$

while the discrete-time domain transfer function that relates the voltage at the output of the converter with the inductor current is

$$G_{\mathrm{PI}}(z) = \frac{(z-1)\sin(\omega_n T_s)}{\omega_n L_f (z^2 - 2z\cos(\omega_n T_s)+1)}. \tag{5}$$

The continuous-time domain transfer function of the PR controller is

$$G_{\mathrm{PR}}(s) = K_{\mathrm{PV}} + K_{\mathrm{RV}}\frac{s}{s^2+\omega_o^2} \tag{6}$$

where K_{PV} and K_{RV} are the P gain and the resonant gain, respectively. The discretization of the PR controllers is performed using the Tustin method with prewarping at the fundamental frequency [52], giving rise to the following transfer function in the discrete-time domain

$$G_{\mathrm{PR}}(z) = K_{\mathrm{PV}} + K_{\mathrm{RV}}\frac{\sin(\omega_o T_s)(z^2-1)}{2\omega_o(z^2 - 2z\cos(\omega_o T_s)+1)}. \tag{7}$$

For the stability analysis, the PR voltage controller can be considered as a P controller with gain K_{PV}, since the fundamental frequency is always much lower than the resonant frequency of the filter, and the resonant action only affects frequencies close to the fundamental frequency [9], [10]. The results presented in this article are also applicable to a quasi-PR controller, which can similarly be approximated as a P controller [21], [22], [23].

As explained in [10], the most suitable way to determine the stability region is in the discrete-time domain, where no approximations are used. Moreover, the discrete-time domain transfer function of the delay is rational, allowing the stability region to be determined by analyzing the characteristic polynomial of the system. The Jury stability criterion may lead to expressions that are complex to analyze. Therefore, in this article, the characteristic polynomial of the system will be transformed into the w-plane by applying the inverse Tustin transform, which maps the unit circle in the z-plane exactly to the LHP of Laplace [37], so that the stability region is preserved and the Routh stability criterion can be applied [22], [23]. The transformation to the w-plane will be used solely to apply the Routh stability criterion, but the system will always be analyzed in the z-domain. The transformation to the w-plane is given by

$$z = \frac{1+w}{1-w}. \tag{8}$$

Based on Fig. 2(b), the closed-loop transfer function of the DLVCC is obtained

$$G_{\mathrm{CL_{VC}}}(z) = \frac{K_{\mathrm{PV}}K_{\mathrm{PI}}(z+1)(1-\cos(\omega_n T_s))}{\mathrm{Den_{VC}}(z)} \tag{9}$$

where the characteristic polynomial of the DLVCC is

$$\begin{aligned}\mathrm{Den_{VC}}(z) &= z^3 - 2\cos(\omega_n T_s)z^2 \\ &+ \left(1 + \frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} + K_{\mathrm{PV}}K_{\mathrm{PI}}(1-\cos(\omega_n T_s))\right)z \\ &+ \left(-\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} + K_{\mathrm{PV}}K_{\mathrm{PI}}(1-\cos(\omega_n T_s))\right).\end{aligned} \tag{10}$$

Based on Fig. 3(b), the closed-loop transfer function of the DLVADC is obtained

$$G_{\mathrm{CL_{VAD}}}(z) = \frac{K_{\mathrm{PV}}(z+1)(1-\cos(\omega_n T_s))}{\mathrm{Den_{VAD}}(z)} \tag{11}$$

where the characteristic polynomial of the DLVADC is

$$\begin{aligned}\mathrm{Den_{VAD}}(z) &= z^3 - 2\cos(\omega_n T_s)z^2 \\ &+ \left(1 + \frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} + K_{\mathrm{PV}}(1-\cos(\omega_n T_s))\right) z \\ &+ \left(-\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} + K_{\mathrm{PV}}(1-\cos(\omega_n T_s))\right).\end{aligned} \tag{12}$$

From (9) and (10), it is concluded that, in the DLVCC, there is coupling between the PR voltage controller and the P current controller, as indicated by the term $K_{\mathrm{PV}}K_{\mathrm{PI}}$. This coupling between the controllers complicates the stability analysis of the system, and it is precisely the reason why, to date, there are no prior publications proposing the use of negative gains in the P current controller. This article demonstrates that, due to this coupling, using negative gains in the P current controller necessarily requires the use of negative resonant gains in the PR voltage controller. To the best of the authors' knowledge, no previous work has proposed the use of negative resonant gains in a PR controller.

From (11) and (12), it is concluded that, in the DLVADC, there is not coupling between the controllers. Therefore, the stability analysis of this system, presented in [21], [22], and [23], becomes simpler, since positive resonant gains must always be used in the PR voltage controller, regardless of the sign of the active damping coefficient used in the inner control loop. However, the stability region presented in those papers is not the complete stability region of the DLVADC.

In this article, the complete stability region of both the DLVCC and the DLVADC will be determined, and it will be demonstrated that they are equivalent control structures. Therefore, it will be possible to refer solely to the stability region of the double-loop voltage control. However, the tuning of the controllers will differ depending on whether the DLVCC or the DLVADC is used, so the stability analysis of both systems will be presented separately.

III. Stability of the DLVCC

In this section, the complete stability region of the DLVCC will be determined, and it will be demonstrated that it is possible to achieve a stable DLVCC for any frequency ratio f_n/f_s. Furthermore, it will be shown that it is not always possible to achieve a minimum-phase system. However, the complete stability region should not be confused with the stability region that allows for the achievement of a minimum-phase system.

A. Complete Stability Region

The characteristic polynomial of the DLVCC (10) in the w-plane is

$$Q_{\mathrm{VC}}(w) = a_3 w^3 + a_2 w^2 + a_1 w + a_0 \tag{13}$$

where

$$\begin{cases} a_3 = 2 + 2\cos(\omega_n T_s) + 2\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} \\ a_2 = 2 + 2\cos(\omega_n T_s) - 4\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} \\ \quad + 2K_{\mathrm{PV}}K_{\mathrm{PI}}(1-\cos(\omega_n T_s)) \\ a_1 = 2 - 2\cos(\omega_n T_s) + 2\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} \\ \quad - 4K_{\mathrm{PV}}K_{\mathrm{PI}}(1-\cos(\omega_n T_s)) \\ a_0 = 2 - 2\cos(\omega_n T_s) + 2K_{\mathrm{PV}}K_{\mathrm{PI}}(1-\cos(\omega_n T_s)). \end{cases} \tag{14}$$

It can be observed that the coefficients of the characteristic polynomial (14) depend on the ratio between the resonant frequency of the filter and the sampling frequency $(\omega_n T_s)$, on the parameters of the filter used $(\omega_n L_f)$, on the P gain of the current controller (K_{PI}), and on the product of the P gains of the controllers $(K_{\mathrm{PV}}K_{\mathrm{PI}})$. The Routh stability criterion states that all the coefficients of the characteristic polynomial must be of the same sign and nonzero. That is, for the DLVCC to be stable, all the coefficients in (14) could be either positive or negative. First, the case where all the coefficients are positive is considered, for which it is necessary to fulfill

$$\begin{cases} a_3 > 0 \;\rightarrow\; K_{\mathrm{PI}} > \frac{(-1-\cos(\omega_n T_s))\omega_n L_f}{\sin(\omega_n T_s)} \\ a_2 > 0 \;\rightarrow\; K_{\mathrm{PV}}K_{\mathrm{PI}} > \frac{2\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} - 1 - \cos(\omega_n T_s)}{(1-\cos(\omega_n T_s))} \\ a_1 > 0 \;\rightarrow\; K_{\mathrm{PV}}K_{\mathrm{PI}} < \frac{\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} + 1 - \cos(\omega_n T_s)}{2(1-\cos(\omega_n T_s))} \\ a_0 > 0 \;\rightarrow\; K_{\mathrm{PV}}K_{\mathrm{PI}} > -1. \end{cases} \tag{15}$$

For the DLVCC to be stable, the upper bound for $K_{\mathrm{PV}}K_{\mathrm{PI}}$, which arises from the condition $a_1 > 0$, must be larger than the lower bounds for $K_{\mathrm{PV}}K_{\mathrm{PI}}$, which arise from the conditions $a_2 > 0$ and $a_0 > 0$. From the comparison of the upper bound with the lower bounds, new constraints for K_{PI} emerge. Therefore, K_{PI} must satisfy these new conditions and also the condition given by $a_3 > 0$

$$\begin{cases} K_{\mathrm{PI}} > \frac{(-1-\cos(\omega_n T_s))\omega_n L_f}{\sin(\omega_n T_s)} \\ K_{\mathrm{PI}} < \frac{(3+\cos(\omega_n T_s))\omega_n L_f}{3\sin(\omega_n T_s)} \\ K_{\mathrm{PI}} > \frac{(-3+3\cos(\omega_n T_s))\omega_n L_f}{\sin(\omega_n T_s)}. \end{cases} \tag{16}$$

For the DLVCC to be stable, the upper bound for K_{PI} must be larger than the lower bounds for K_{PI}, defined in (16). From the comparison of the upper bound with the lower bounds, it is concluded that these conditions are always satisfied. If the necessary conditions for all the coefficients of the characteristic polynomial to be negative were studied, the conditions in (16) would be reversed, resulting in conditions that are never satisfied. Therefore, all the coefficients of the characteristic polynomial must be positive. Furthermore, all the coefficients in the first column of the table of Routh must also be positive. As the DLVCC is a third-order system (13), only the coefficient b_1, defined as $(a_2a_1 - a_3a_0)/a_2$, must be studied. The denominator of b_1 must be positive, therefore, the condition $b_1 > 0$ can be simplified to

$$a_2a_1 - a_3a_0 = 8\left[a_{b1}K_{\mathrm{PV}}^2K_{\mathrm{PI}}^2 + b_{b1}K_{\mathrm{PV}}K_{\mathrm{PI}} + c_{b1}\right] > 0 \tag{17}$$

where

$$\begin{cases} a_{b1} & = -1 + 2\cos(\omega_n T_s) - \cos^2(\omega_n T_s) \\ b_{b1} & = -1 - \cos(\omega_n T_s) + 2\cos^2(\omega_n T_s) \\ & \quad + 2\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f}(1 - \cos(\omega_n T_s)) \\ c_{b1} & = \frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f}\left(-1 + 2\cos(\omega_n T_s)\right) \\ & \quad - \frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f}\Big). \end{cases} \tag{18}$$

From (17), it is concluded that the condition $b_1 > 0$ gives rise to a quadratic function of $K_{\mathrm{PV}}K_{\mathrm{PI}}$. The coefficient a_{b1}, defined in (18), is always negative; therefore, it is a downward-facing parabola, and for the condition $b_1 > 0$ to be met, the discriminant must be positive, and the value of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ must lie within the interval defined by the two solutions of the quadratic equation

$$\begin{cases} b_{1.1} = \frac{-b_{b1} + \sqrt{b_{b1}^2 - 4a_{b1}c_{b1}}}{2a_{b1}} \\ b_{1.2} = \frac{-b_{b1} - \sqrt{b_{b1}^2 - 4a_{b1}c_{b1}}}{2a_{b1}} \end{cases} \tag{19}$$

where $b_{1.2}$ is always greater than $b_{1.1}$, as a_{b1} is always negative. From the condition that the discriminant must be positive, the following condition for K_{PI} is obtained.

$$b_{b1}^2 - 4a_{b1}c_{b1} > 0 \rightarrow K_{\mathrm{PI}} < \frac{(2\cos(\omega_n T_s) + 1)^2 \omega_n L_f}{8\sin(\omega_n T_s)}. \tag{20}$$

For the DLVCC to be stable, the three conditions for $K_{\mathrm{PV}}K_{\mathrm{PI}}$ described in (15) must be met, along with the conditions $K_{\mathrm{PV}}K_{\mathrm{PI}} > b_{1.1}$ and $K_{\mathrm{PV}}K_{\mathrm{PI}} < b_{1.2}$. That is, there are three lower bounds and two upper bounds for $K_{\mathrm{PV}}K_{\mathrm{PI}}$. Firstly, it is concluded that the upper bound $b_{1.2}$ is always more restrictive, allowing the condition $a_1 > 0$ to be eliminated. Secondly, it is also concluded that, for the upper bound $b_{1.2}$ to be greater than the lower bounds given by $a_2 > 0$ and $a_0 > 0$, it is necessary to fulfill

$$0 < f_n < \frac{f_s}{6} \rightarrow$$
$$\frac{(-3 + 3\cos(\omega_n T_s))\omega_n L_f}{\sin(\omega_n T_s)} < K_{\mathrm{PI}} < \frac{\cos(\omega_n T_s)\omega_n L_f}{\sin(\omega_n T_s)} \tag{21}$$

At this point, there are no more upper bounds to compare with lower bounds; therefore, there will be no further restrictions for K_{PI}. By combining (16), (20), and (21), and determining the intervals in which each condition is the most restrictive one, the stability region for K_{PI} in the DLVCC is obtained (22), shown at the bottom of this page. From (22), it is concluded that the permissible values for K_{PI} in the DLVCC depend on the frequency ratio f_n/f_s ($\omega_n T_s$) and on the filter used ($\omega_n L_f$). The filter used only modifies the limit values for K_{PI}, but it does not alter the intervals, which depend solely on the frequency ratio f_n/f_s. Observing (22), it can be seen that the value $K_{\mathrm{PI}} = 0$ is not included in the stability region of the DLVCC, as it would nullify the voltage controller (see Fig. 2).

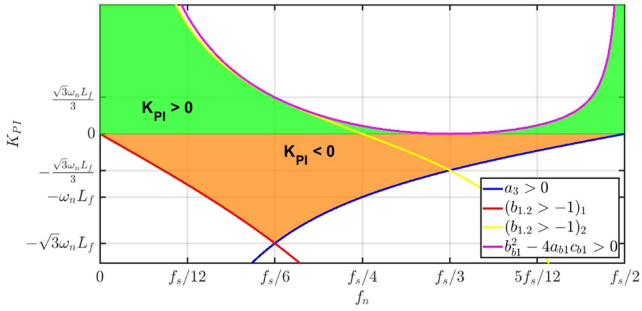


Fig. 4. Complete stability region for K_{PI} in the double-loop voltage control.

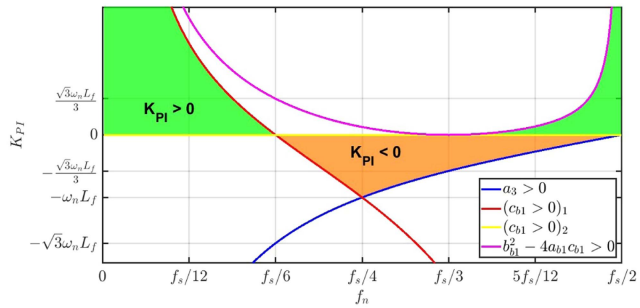


Fig. 5. Stability region for K_{PI} in the double-loop voltage control that allows obtaining a minimum-phase system.

The stability region for K_{PI} in the DLVCC (22) is represented in Fig. 4. The term "double-loop voltage control" is chosen for the figure caption to indicate that it encompasses both the DLVCC and the DLVADC, as it will be demonstrated later. The solid lines represent the conditions for K_{PI} resulting from the application of the Routh stability criterion (16), (20), and (21). The stability region is given by the most restrictive condition for each frequency ratio f_n/f_s. Therefore, not all the conditions resulting from the application of the Routh stability criterion are represented in Fig. 4, only those that define the complete stability region are shown. The X-axis shows the most relevant frequency ratios, f_n/f_s, at which transitions in the complete

$$\begin{cases} 0 < f_n < \frac{f_s}{6} & \rightarrow \left(\frac{(-3+3\cos(\omega_n T_s))\omega_n L_f}{\sin(\omega_n T_s)} < K_{\mathrm{PI}} < 0\right) \bigcup \left(0 < K_{\mathrm{PI}} < \frac{\cos(\omega_n T_s)\omega_n L_f}{\sin(\omega_n T_s)}\right) \\ \frac{f_s}{6} < f_n < \frac{f_s}{2} & \rightarrow \left(\frac{(-1-\cos(\omega_n T_s))\omega_n L_f}{\sin(\omega_n T_s)} < K_{\mathrm{PI}} < 0\right) \bigcup \left(0 < K_{\mathrm{PI}} < \frac{(2\cos(\omega_n T_s)+1)^2\omega_n L_f}{8\sin(\omega_n T_s)}\right) \end{cases} \tag{22}$$

$$\begin{cases} 0 < f_n < \frac{f_s}{6} & \rightarrow -1 < K_{\mathrm{PV}}K_{\mathrm{PI}} < b_{1.2} \\ \frac{f_s}{6} < f_n < \frac{f_s}{3} \;\&\; K_{\mathrm{PI}} < \frac{\cos(\omega_n T_s)\omega_n L_f}{\sin(\omega_n T_s)} & \rightarrow -1 < K_{\mathrm{PV}}K_{\mathrm{PI}} < b_{1.2} \\ \frac{f_s}{6} < f_n < \frac{f_s}{3} \;\&\; K_{\mathrm{PI}} > \frac{\cos(\omega_n T_s)\omega_n L_f}{\sin(\omega_n T_s)} & \rightarrow b_{1.1} < K_{\mathrm{PV}}K_{\mathrm{PI}} < b_{1.2} \\ \frac{f_s}{3} < f_n < \frac{f_s}{2} & \rightarrow b_{1.1} < K_{\mathrm{PV}}K_{\mathrm{PI}} < b_{1.2}. \end{cases} \tag{23}$$

stability region occur. The Y-axis shows the limit values of the gain K_{PI} at each of these transitions, which can be easily obtained by substituting the corresponding frequency ratio into (22).

Observing Fig. 4, it can be seen that there is an interval of values of K_{PI} for which the DLVCC can be stable for any frequency ratio f_n/f_s, so it is concluded that the DLVCC can be stable for any frequency ratio f_n/f_s, meaning there is no critical frequency in the DLVCC; that is, $f_n = f_s/6$ is not a critical frequency in the DLVCC, as previously thought. The DLVCC surpasses the performance of the single-loop voltage control, where $f_n = f_s/3$ is a critical frequency [10]. Furthermore, observing Fig. 4, it can be seen that, in the DLVCC, positive and negative values of K_{PI} can be used for any frequency ratio f_n/f_s, except for $f_n = f_s/3$, where the upper limit of K_{PI} becomes zero, and only negative values of K_{PI} can be used.

For the DLVCC to be stable, K_{PI} must satisfy (22). However, the admissible values of K_{PV} must also be determined. The two conditions for $K_{\mathrm{PV}}K_{\mathrm{PI}}$ given by $a_2 > 0$ and $a_0 > 0$ must be met, along with the conditions $K_{\mathrm{PV}}K_{\mathrm{PI}} > b_{1.1}$ and $K_{\mathrm{PV}}K_{\mathrm{PI}} < b_{1.2}$. There is only one upper limit for $K_{\mathrm{PV}}K_{\mathrm{PI}}$, so the upper limit will always be $b_{1.2}$. First, it is concluded that, for the DLVCC to be stable, the conditions given by $a_0 > 0$ and $K_{\mathrm{PV}}K_{\mathrm{PI}} > b_{1.1}$ are always more restrictive than the condition given by $a_2 > 0$. Therefore, the condition $a_2 > 0$ can be eliminated. Second, it is concluded that, on the one hand, if $f_n < f_s/6$, the condition given by $a_0 > 0$ is always more restrictive than the condition given by $K_{\mathrm{PV}}K_{\mathrm{PI}} > b_{1.1}$. On the other hand, if $f_s/3 < f_n < f_s/2$, the condition given by $K_{\mathrm{PV}}K_{\mathrm{PI}} > b_{1.1}$ is always more restrictive than the condition given by $a_0 > 0$. However, if $f_s/6 < f_n < f_s/3$, the lower limit for $K_{\mathrm{PV}}K_{\mathrm{PI}}$ depends on the value of K_{PI} selected. Taking all of this into account, the stability region for $K_{\mathrm{PV}}K_{\mathrm{PI}}$ is obtained (23), shown at the bottom of the previous page. Based on the stability region for $K_{\mathrm{PV}}K_{\mathrm{PI}}$ (23), and on the value of K_{PI} selected [which must satisfy (22)], the stability region for K_{PV} can be obtained.

From Fig. 2 and based on the transfer function of the PR controller (6), it is concluded that, on the one hand, if a positive value of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ is used, the DLVCC will be minimum-phase, as the zeros of the PR voltage controller will be located in the LHP of laplace. On the other hand, if a negative value of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ is used, the DLVCC will be nonminimum-phase, as the zeros of the PR voltage controller will be located in the RHP of Laplace. It is very important to indicate that, since K_{PI} multiplies the entire PR voltage controller, and as the poles introduced by the PR voltage controller must be located in the LHP of Laplace for the system to be stable, if a positive K_{PI} is used, the resonant gain K_{RV} must be positive, whereas if a negative K_{PI} is used, K_{RV} must be negative. The use of negative resonant gains in a PR controller has not been addressed in any publication to date.

The tuning process of the controllers in the DLVCC can be divided into the following steps, avoiding the use of a trial-and-error method.

1) Select the filter and the sampling frequency. Calculate the ratio f_n/f_s.
2) Calculate the admissible values of K_{PI} using (22). Select K_{PI}.
3) Calculate the admissible values of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ using (23).
4) If a positive K_{PI} is selected, a positive resonant gain K_{RV} must be used, and the admissible values of K_{PV} can be obtained directly from the admissible values of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ and the value of K_{PI} selected. If a positive K_{PV} is selected, a minimum-phase system is obtained, while if a negative K_{PV} is selected, a nonminimum-phase system is obtained.
5) If a negative K_{PI} is selected, a negative resonant gain K_{RV} must be used, and the admissible values of K_{PV} can also be obtained from the admissible values of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ and the value of K_{PI} selected, but taking into account that lower limits for $K_{\mathrm{PV}}K_{\mathrm{PI}}$ become upper limits for K_{PV} and upper limits for $K_{\mathrm{PV}}K_{\mathrm{PI}}$ become lower limits for K_{PV}. If a positive K_{PV} is selected, a nonminimum-phase system is obtained, while if a negative K_{PV} is selected, a minimum-phase system is obtained.

The DLVCC is a control structure in which another PR controller could be used in the inner current control loop, ensuring that it operates with zero steady-state error (see Fig. 2). The DLVCC with a PR current controller has been used in previous publications [53], [54], [55], [56]. However, in all these articles, the PR controllers are tuned using a trial-and-error method and the condition $f_n < f_s/6$ is satisfied. The analysis of the DLVCC with a PR current controller is beyond the scope of this article. However, based on the analysis presented in this article, it is concluded that the DLVCC with a PR current controller could be used for any frequency ratio f_n/f_s, and the PR controllers could be tuned using the method described in this section, taking into account the resonant component of the PR current controller.

B. Stability Region for Minimum-Phase System

As previously explained, if a positive value of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ is used, the DLVCC will be minimum-phase, whereas if a negative value of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ is used, the DLVCC will be nonminimum-phase. Therefore, it is preferred to use a positive value of $K_{\mathrm{PV}}K_{\mathrm{PI}}$. However, it will not always be possible to use a positive value for $K_{\mathrm{PV}}K_{\mathrm{PI}}$. For $K_{\mathrm{PV}}K_{\mathrm{PI}}$ to be positive, the upper limit defined in (23), $b_{1.2}$, must be positive. By calculating the necessary conditions for the upper limit of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ to be positive, it is found that K_{PI} must lie within the interval defined in (24), shown at the bottom of this page. Obviously, this interval for K_{PI} is

$$\begin{cases} 0 < f_n < \frac{f_s}{6} \rightarrow & 0 & < K_{\mathrm{PI}} < \frac{(2\cos(\omega_n T_s)-1)\omega_n L_f}{\sin(\omega_n T_s)} \\ \frac{f_s}{6} < f_n < \frac{f_s}{4} \rightarrow & \frac{(2\cos(\omega_n T_s)-1)\omega_n L_f}{\sin(\omega_n T_s)} & < K_{\mathrm{PI}} < 0 \\ \frac{f_s}{4} < f_n < \frac{f_s}{3} \rightarrow & \frac{(-1-\cos(\omega_n T_s))\omega_n L_f}{\sin(\omega_n T_s)} & < K_{\mathrm{PI}} < 0 \\ \frac{f_s}{3} < f_n < \frac{f_s}{2} \rightarrow & \left(\frac{(-1-\cos(\omega_n T_s))\omega_n L_f}{\sin(\omega_n T_s)} < K_{\mathrm{PI}} < 0\right) & \bigcup \quad \left(0 < K_{\mathrm{PI}} < \frac{(2\cos(\omega_n T_s)+1)^2\omega_n L_f}{8\sin(\omega_n T_s)}\right). \end{cases} \tag{24}$$

smaller than the interval for K_{PI} with which the DLVCC can be stable (22), where a positive or a negative $K_{\mathrm{PV}}K_{\mathrm{PI}}$ can be used.

Fig. 5 shows the stability region for K_{PI} in the DLVCC that allows obtaining a minimum-phase system (24). The term "double-loop voltage control" is chosen for the figure caption in Fig. 5 to indicate that it encompasses both the DLVCC and the DLVADC, as it will be demonstrated later. The X-axis shows the most relevant frequency ratios, f_n/f_s, at which transitions in the stability region for minimum-phase system occur. The Y-axis shows the limit values of the gain K_{PI} at each of these transitions, which can be easily obtained by substituting the corresponding frequency ratio into (24).

From Fig. 5, it is concluded that, for the DLVCC to be a minimum-phase system, K_{PI} must be positive if $f_n < f_s/6$, K_{PI} must be negative if $f_s/6 < f_n < f_s/3$, and K_{PI} can be both positive and negative if $f_s/3 < f_n < f_s/2$. In addition, it is concluded that $f_n = f_s/6$ is the only frequency ratio for which a minimum-phase system cannot be achieved. Therefore, from (24) and Fig. 5, it is concluded that the stability region for K_{PI} in the DLVCC that allows obtaining a minimum-phase system coincides with the stability region of the DLVADC presented in [23] and explained in the Introduction of this article. Therefore, it makes sense to question whether the stability region presented in [23] is not the complete stability region of the DLVADC and, even more, whether the stability region of the DLVADC is the same as the stability region of the DLVCC (22).

Comparing Fig. 5 with Fig. 4, it is verified how the range of K_{PI} values that can be used in order to obtain a minimum-phase system (24) is smaller than the range of K_{PI} values that allow obtaining a stable system (22), which can be a minimum-phase system or a nonminimum-phase system. On the one hand, if $f_n < f_s/3$, the range of K_{PI} values that can be used to obtain a minimum-phase system is smaller than the range of K_{PI} values that can be used to obtain a stable system. On the other hand, if $f_s/3 < f_n < f_s/2$, the range of K_{PI} values that can be used to obtain a minimum-phase system matches the range of K_{PI} values for which the system can be stable. Therefore, if $f_s/3 < f_n < f_s/2$, any K_{PI} value with which the system is stable can be used to obtain a minimum-phase system.

IV. Stability of the DLVADC

In this section, the same procedure as in the previous section will be followed, and it will be demonstrated that the complete stability region of the DLVADC is the same as the one obtained in the previous section for the DLVCC. Therefore, both control structures are equivalent. However, it will also be shown that the tuning of the controllers is different.

A. Complete Stability Region

The characteristic polynomial of the DLVADC (12) in the w-plane is

$$Q_{\mathrm{AD}}(w) = a_3 w^3 + a_2 w^2 + a_1 w + a_0 \tag{25}$$

where

$$\begin{cases} a_3 = 2 + 2\cos(\omega_n T_s) + 2\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} \\ a_2 = 2 + 2\cos(\omega_n T_s) - 4\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} \\ \quad + 2K_{\mathrm{PV}}(1 - \cos(\omega_n T_s)) \\ a_1 = 2 - 2\cos(\omega_n T_s) + 2\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} \\ \quad - 4K_{\mathrm{PV}}(1 - \cos(\omega_n T_s)) \\ a_0 = 2 - 2\cos(\omega_n T_s) + 2K_{\mathrm{PV}}(1 - \cos(\omega_n T_s)) \end{cases} \tag{26}$$

Comparing (26) with (14), it can be seen that that the only change is that the term $K_{\mathrm{PV}}K_{\mathrm{PI}}$ of the DLVCC is reduced to K_{PV} in the DLVADC. In other words, the DLVADC eliminates the coupling between the controllers, as previously mentioned.

After applying the Routh stability criterion to (25) following the same steps as in the previous section, the stability region for K_{PI} in the DLVADC is obtained (27), shown at the bottom of the next page. It can be seen how the stability region for K_{PI} in the DLVADC (27) is the same as the stability region for K_{PI} in the DLVCC (22), except that in the DLVADC it is possible to work with a null K_{PI}, as it was expected, since it is equivalent to working with the single-loop voltage-control (see Fig. 3). However, in that case, one would no longer be working with a double-loop control system. Therefore, Fig. 4 also shows the complete stability region for K_{PI} in the DLVADC (27), as previously mentioned, and the conclusions obtained are the same as in the previous section. Therefore, it is concluded that the DLVCC and the DLVADC are equivalent control structures.

For the DLVADC to be stable, K_{PI} must satisfy (27). However, the admissible values of K_{PV} must also be determined. The stability region for K_{PV} in the DLVADC is defined by (28), shown at the bottom of the next page. Comparing (28) with (23), it can be observed how the upper and lower limits are the same. However, in the DLVADC, the limits are directly defined for K_{PV}, rather than being defined for $K_{\mathrm{PV}}K_{\mathrm{PI}}$. Based on (28), it is concluded that K_{PV} could be either positive or negative depending on the value of $b_{1.2}$.

From Fig. 3 and based on the transfer-function of the PR controller (6), it is concluded that, on the one hand, if a positive value of K_{PV} is used, the DLVADC will be minimum-phase, as the zeros of the PR voltage controller will be located in the LHP of Laplace. On the other hand, if a negative value of K_{PV} is used, the DLVADC will be nonminimum-phase, as the zeros of the PR voltage controller will be located in the RHP of Laplace. It is very important to indicate that, with this control structure, as the coupling between the controllers is eliminated, a positive resonant gain in the PR voltage controller must be used for the system to be stable, as the poles introduced by the PR voltage controller must be located in the LHP of Laplace. The tuning process of the controllers in the DLVADC can be divided into the following steps, avoiding the use of a trial-and-error method.

1) Select the filter and the sampling frequency. Calculate the ratio f_n/f_s.
2) Calculate the admissible values of K_{PI} using (27). Select K_{PI}.
3) Calculate the admissible values of K_{PV} using (28). Select K_{PV}. If a positive K_{PV} is used, a minimum-phase system is

obtained, while if a negative K_{PV} is used, a nonminimum-phase system is obtained. A positive resonant gain K_{RV} must be used.

The DLVADC is a control structure in which a PR controller cannot be used in the feedback path to serve as the active damping coefficient.

B. Stability Region for Minimum-Phase System

As previously explained, if a positive value of K_{PV} is used, the DLVADC will be minimum-phase, whereas if a negative value of K_{PV} is used, the DLVADC will be nonminimum-phase. Therefore, it is preferred to use a positive value of K_{PV}. However, it will not always be possible to use a positive value of K_{PV}. For K_{PV} to be positive, the upper limit defined in (28), $b_{1.2}$, must be positive. By calculating the necessary conditions for the upper limit of K_{PV} to be positive, it is found that K_{PI} must lie within the interval defined in (29), shown at the bottom of this page. It can be seen how the stability region for K_{PI} in the DLVADC in order to obtain a minimum-phase system is the same as the one calculated in the previous section for the DLVCC (24), except that in the DLVADC it is possible to work with a null K_{PI} if $f_s/3 < f_n < f_s/2$. This was expected, as in the single-loop voltage control K_{PV} can be positive if $f_s/3 < f_n < f_s/2$ [10]. However, in that case, one would no longer be working with a double-loop control system, as previously explained. Therefore, Fig. 5 also shows the stability region for K_{PI} in the DLVADC that allows obtaining a minimum-phase system (29), as previously mentioned, and the conclusions obtained are the same as in the previous section.

Therefore, it is concluded that the stability region for K_{PI} in the DLVADC that allows obtaining a minimum-phase system, defined by (29), coincides with the stability region of the DLVADC presented in [23] and explained in the Introduction of this article. The suspicions introduced at the end of the previous section are confirmed. However, (29) is only part of the stability region for K_{PI} in the DLVADC. The complete stability region for K_{PI} in the DLVADC is defined by (27). The usefulness of obtaining the complete stability region will be shown in the next section, where the effects of unitary decoupling of the capacitor voltage in the complete stability region of the double-loop voltage control are analyzed.

V. Capacitor Voltage Unitary Decoupling

The DLVCC with capacitor voltage unitary decoupling and the DLVADC with capacitor voltage unitary decoupling are analyzed in this section. In the previous sections, it was demonstrated that the DLVCC and the DLVADC are equivalent control structures, but it is decided to analyze them separately to explain the tuning of the controllers in both systems, as it is different.

As it was demonstrated in the previous sections, the double-loop voltage control can be stable for any frequency ratio f_n/f_s. However, it is not possible to obtain a minimum-phase system for all the values of K_{PI} with which the double-loop voltage control is stable. As it is demonstrated in this section, the unitary decoupling of the capacitor voltage allows obtaining a minimum-phase system for all the values of K_{PI} with which the double-loop voltage control is stable.

A. DLVCC With Capacitor Voltage Unitary Decoupling

Fig. 6 shows the block diagram of the DLVCC with unitary decoupling of the capacitor voltage. Taking into account that a P voltage controller is considered for the stability analysis and applying Mason's rule to the system in Fig. 6, the closed-loop transfer function of the DLVCC with unitary decoupling of the capacitor voltage is obtained

$$G_{\mathrm{CL}_{\mathrm{VC}_D}}(z) = \frac{K_{\mathrm{PV}}K_{\mathrm{PI}}(z+1)(1-\cos(\omega_n T_s))}{\mathrm{Den}_{\mathrm{VC}_D}(z)} \tag{30}$$

where the characteristic polynomial of the system is

$$\mathrm{Den}_{\mathrm{VC}_D}(z) = z^3 - 2\cos(\omega_n T_s)z^2 + \left(\cos(\omega_n T_s) + \frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} + K_{\mathrm{PV}}K_{\mathrm{PI}}(1-\cos(\omega_n T_s))\right)z + \left(-1 + \cos(\omega_n T_s) - \frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} + K_{\mathrm{PV}}K_{\mathrm{PI}}(1-\cos(\omega_n T_s))\right). \tag{31}$$

Comparing (10) with (31), it is concluded that the only difference is that, with the decoupling, the value $(-1+\cos(\omega_n T_s))$ is added to the coefficient of degree one and to the constant term.

$$\begin{cases} 0 < f_n < \frac{f_s}{6} & \rightarrow \quad \frac{(-3+3\cos(\omega_n T_s))\omega_n L_f}{\sin(\omega_n T_s)} < K_{\mathrm{PI}} < \frac{\cos(\omega_n T_s)\omega_n L_f}{\sin(\omega_n T_s)} \\ \frac{f_s}{6} < f_n < \frac{f_s}{2} & \rightarrow \quad \frac{(-1-\cos(\omega_n T_s))\omega_n L_f}{\sin(\omega_n T_s)} < K_{\mathrm{PI}} < \frac{(2\cos(\omega_n T_s)+1)^2\omega_n L_f}{8\sin(\omega_n T_s)}. \end{cases} \tag{27}$$

$$\begin{cases} 0 < f_n < \frac{f_s}{6} & \rightarrow -1 < K_{\mathrm{PV}} < b_{1.2} \\ \frac{f_s}{6} < f_n < \frac{f_s}{3} & \& K_{\mathrm{PI}} < \frac{\cos(\omega_n T_s)\omega_n L_f}{\sin(\omega_n T_s)} \rightarrow -1 < K_{\mathrm{PV}} < b_{1.2} \\ \frac{f_s}{6} < f_n < \frac{f_s}{3} & \& K_{\mathrm{PI}} > \frac{\cos(\omega_n T_s)\omega_n L_f}{\sin(\omega_n T_s)} \rightarrow b_{1.1} < K_{\mathrm{PV}} < b_{1.2} \\ \frac{f_s}{3} < f_n < \frac{f_s}{2} & \rightarrow b_{1.1} < K_{\mathrm{PV}} < b_{1.2}. \end{cases} \tag{28}$$

$$\begin{cases} 0 < f_n < \frac{f_s}{6} & \rightarrow \quad 0 < K_{\mathrm{PI}} < \frac{(2\cos(\omega_n T_s)-1)\omega_n L_f}{\sin(\omega_n T_s)} \\ \frac{f_s}{6} < f_n < \frac{f_s}{4} & \rightarrow \quad \frac{(2\cos(\omega_n T_s)-1)\omega_n L_f}{\sin(\omega_n T_s)} < K_{\mathrm{PI}} < 0 \\ \frac{f_s}{4} < f_n < \frac{f_s}{3} & \rightarrow \quad \frac{(-1-\cos(\omega_n T_s))\omega_n L_f}{\sin(\omega_n T_s)} < K_{\mathrm{PI}} < 0 \\ \frac{f_s}{3} < f_n < \frac{f_s}{2} & \rightarrow \quad \frac{(-1-\cos(\omega_n T_s))\omega_n L_f}{\sin(\omega_n T_s)} < K_{\mathrm{PI}} < \frac{(2\cos(\omega_n T_s)+1)^2\omega_n L_f}{8\sin(\omega_n T_s)}. \end{cases} \tag{29}$$

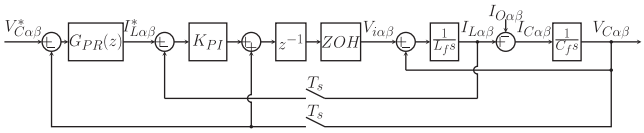


Fig. 6. Block diagram of the DLVCC with unitary decoupling of the capacitor voltage.

The characteristic polynomial of the system (31) in the w-plane is

$$Q_{\mathrm{VC}_D}(w) = a_3 w^3 + a_2 w^2 + a_1 w + a_0 \tag{32}$$

where

$$\begin{cases} a_3 = 2 + 2\cos(\omega_n T_s) + 2\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} \\ a_2 = 4\cos(\omega_n T_s) - 4\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} \\ \quad + 2K_{\mathrm{PV}}K_{\mathrm{PI}}(1-\cos(\omega_n T_s)) \\ a_1 = 6 - 6\cos(\omega_n T_s) + 2\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} \\ \quad - 4K_{\mathrm{PV}}K_{\mathrm{PI}}(1-\cos(\omega_n T_s)) \\ a_0 = 2K_{\mathrm{PV}}K_{\mathrm{PI}}(1-\cos(\omega_n T_s)) \end{cases}. \tag{33}$$

After applying the Routh stability criterion to (32) following the same steps as in the previous sections, the same stability region for K_{PI} as in the DLVCC without decoupling is obtained (22). Therefore, Fig. 4 also shows the stability region for K_{PI} in the DLVCC with capacitor voltage unitary decoupling (22), and the conclusions obtained are the same as in the previous sections. As the DLVCC and the DLVADC are equivalent control structures, the same is expected in the DLVADC with unitary decoupling of the capacitor voltage.

The stability region for $K_{\mathrm{PV}}K_{\mathrm{PI}}$ in the DLVCC with capacitor voltage unitary decoupling is defined by (34), shown at the bottom of this page. Comparing (34) with (23), it is concluded that, with the unitary decoupling of the capacitor voltage, the stability region for $K_{\mathrm{PV}}K_{\mathrm{PI}}$ is shifted one unit upwards. Since the same quantity is added to both the upper and lower bounds of $K_{\mathrm{PV}}K_{\mathrm{PI}}$, it makes sense that the stability region for K_{PI} (22), which is determined by comparing the upper and lower bounds of $K_{\mathrm{PV}}K_{\mathrm{PI}}$, remains unchanged when the decoupling is applied.

Based on (34), it is concluded that $K_{\mathrm{PV}}K_{\mathrm{PI}}$ must be positive. Therefore, K_{PI} and K_{PV} must have the same sign. From Fig. 6 and based on the transfer-function of the PR controller (6), it is concluded that, if a positive value of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ is used, the system will be minimum-phase. Therefore, a minimum-phase system is always obtained. It is very important to indicate that, with this control structure, as there is coupling between the controllers, the resonant gain in the PR voltage controller must have the same sign as K_{PI}. Therefore, for the system to be stable, either K_{PV}, K_{PI}, and K_{RV} are all positive, or they are all negative. The tuning process of the controllers in the DLVCC with unitary decoupling

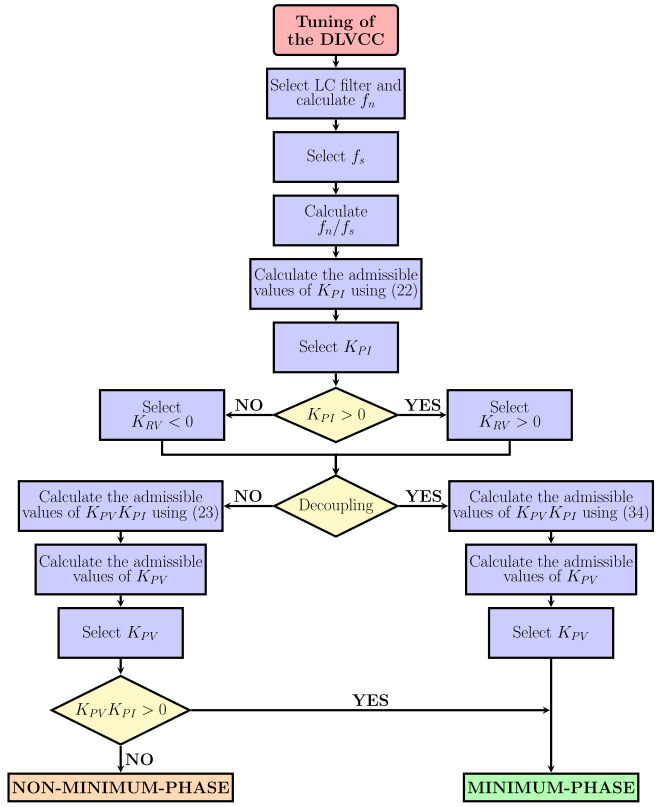


Fig. 7. Proposed tuning process for the DLVCC to ensure stability, both with and without unitary decoupling of the capacitor voltage.

of the capacitor voltage can be divided into the following steps, avoiding the use of a trial-and-error method.

1) Select the filter and the sampling frequency. Calculate the ratio f_n/f_s.
2) Calculate the admissible values of K_{PI} using (22). Select K_{PI}.
3) Calculate the admissible values of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ using (34).
4) If a positive K_{PI} is selected, K_{PV} must be positive and the admissible values of K_{PV} can be obtained directly from the admissible values of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ and the value of K_{PI} selected. A minimum-phase system is obtained. A positive resonant gain K_{RV} must be used.
5) If a negative K_{PI} is selected, K_{PV} must be negative and the admissible values of K_{PV} can also be obtained from the admissible values of $K_{\mathrm{PV}}K_{\mathrm{PI}}$ and the value of K_{PI} selected, but taking into account that lower limits for $K_{\mathrm{PV}}K_{\mathrm{PI}}$ become upper limits for K_{PV} and upper limits for $K_{\mathrm{PV}}K_{\mathrm{PI}}$ become lower limits for K_{PV}. A minimum-phase system is obtained. A negative resonant gain K_{RV} must be used.

Fig. 7 summarizes the proposed tuning process for the DLVCC to ensure stability. On the one hand, the DLVCC

$$\begin{cases} 0 < f_n < \frac{f_s}{6} & \rightarrow \quad 0 \quad < K_{\mathrm{PV}}K_{\mathrm{PI}} < b_{1.2}+1 \\ \frac{f_s}{6} < f_n < \frac{f_s}{3} \,\&\, K_{\mathrm{PI}} < \frac{\cos(\omega_n T_s)\omega_n L_f}{\sin(\omega_n T_s)} & \rightarrow \quad 0 \quad < K_{\mathrm{PV}}K_{\mathrm{PI}} < b_{1.2}+1 \\ \frac{f_s}{6} < f_n < \frac{f_s}{3} \,\&\, K_{\mathrm{PI}} > \frac{\cos(\omega_n T_s)\omega_n L_f}{\sin(\omega_n T_s)} & \rightarrow \quad b_{1.1}+1 \quad < K_{\mathrm{PV}}K_{\mathrm{PI}} < b_{1.2}+1 \\ \frac{f_s}{3} < f_n < \frac{f_s}{2} & \rightarrow \quad b_{1.1}+1 \quad < K_{\mathrm{PV}}K_{\mathrm{PI}} < b_{1.2}+1. \end{cases} \tag{34}$$

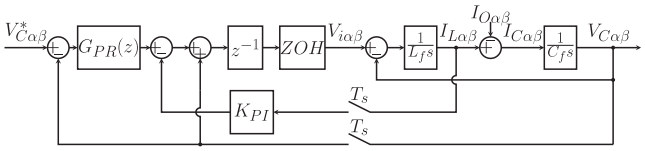


Fig. 8. Block diagram of the DLVADC with unitary decoupling of the capacitor voltage.

without decoupling, if stable, can be either a minimum-phase or a nonminimum-phase system. On the other hand, the DLVCC with decoupling, if stable, is always a minimum-phase system.

B. DLVADC With Capacitor Voltage Unitary Decoupling

Fig. 8 shows the block diagram of the DLVADC with unitary decoupling of the capacitor voltage. Taking into account that a P voltage controller is considered for the stability analysis and applying Mason's rule to the system in Fig. 8, the closed-loop transfer function of the DLVADC with unitary decoupling of the capacitor voltage is obtained

$$G_{\mathrm{CL}_{\mathrm{VAD}_D}}(z) = \frac{K_{\mathrm{PV}}(z+1)(1-\cos(\omega_n T_s))}{\mathrm{Den}_{\mathrm{VAD}_D}(z)} \tag{35}$$

where the characteristic polynomial of the system is

$$\begin{aligned}\mathrm{Den}_{\mathrm{VAD}_D}(z) = {} & z^3 - 2\cos(\omega_n T_s)z^2 + \left(\cos(\omega_n T_s)\right. \\ & \left. + \frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} + K_{\mathrm{PV}}(1-\cos(\omega_n T_s))\right) z + \left(-1\right. \\ & \left. + \cos(\omega_n T_s) - \frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} + K_{\mathrm{PV}}(1-\cos(\omega_n T_s))\right).\end{aligned} \tag{36}$$

Comparing (12) with (36), it is concluded that the only difference is that, with the decoupling, the value $(-1+\cos(\omega_n T_s))$ is added to the coefficient of degree one and to the constant term. The characteristic polynomial of the system (36) in the w-plane is

$$Q_{\mathrm{VAD}_D}(w) = a_3 w^3 + a_2 w^2 + a_1 w + a_0 \tag{37}$$

where

$$\begin{cases} a_3 = & 2 + 2\cos(\omega_n T_s) + 2\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} \\ a_2 = & 4\cos(\omega_n T_s) - 4\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} \\ & + 2K_{\mathrm{PV}}(1-\cos(\omega_n T_s)) \\ a_1 = & 6 - 6\cos(\omega_n T_s) + 2\frac{K_{\mathrm{PI}}\sin(\omega_n T_s)}{\omega_n L_f} \\ & - 4K_{\mathrm{PV}}(1-\cos(\omega_n T_s)) \\ a_0 = & 2K_{\mathrm{PV}}(1-\cos(\omega_n T_s)) \end{cases} \tag{38}$$

After applying the Routh stability criterion to (37) following the same steps as in the previous sections, the same stability region for K_{PI} as in the DLVADC without decoupling is obtained (27), as expected. Therefore, Fig. 4 also shows the stability region for K_{PI} in the DLVADC with capacitor voltage unitary decoupling (27), and the conclusions obtained are the same as in the previous sections.

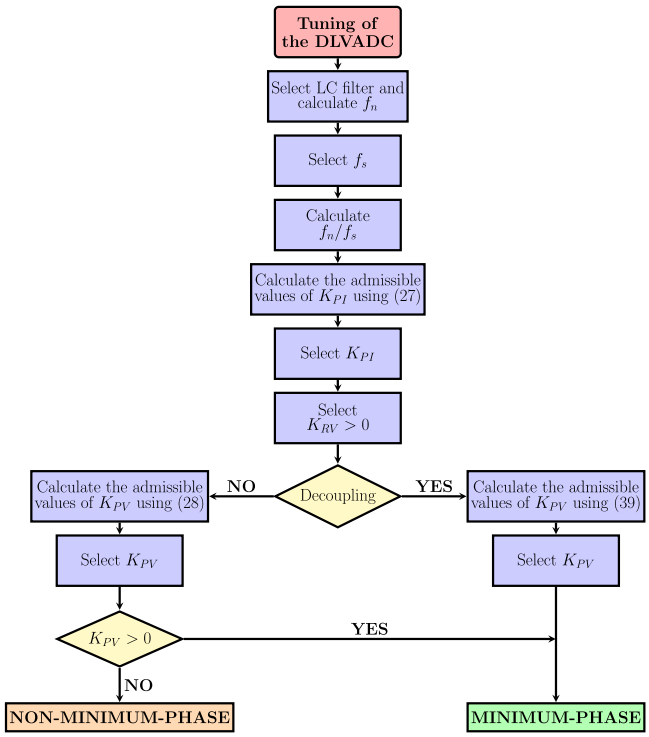


Fig. 9. Proposed tuning process for the DLVADC to ensure stability, both with and without unitary decoupling of the capacitor voltage.

The stability region for K_{PV} in the DLVADC with capacitor voltage unitary decoupling is defined by (39), shown at the bottom of the next page. Comparing (39) with (28), it is concluded that, with the unitary decoupling of the capacitor voltage, the stability region for K_{PV} is shifted one unit of P gain upwards. Since the same quantity is added to both the upper and lower bounds of K_{PV}, it makes sense that the stability region for K_{PI}, which is determined by comparing the upper and lower bounds of K_{PV}, remains unchanged even when the decoupling is applied (27).

Based on (39), it is concluded that K_{PV} must be positive. From Fig. 8 and based on the transfer-function of the PR controller (6), it is concluded that, if a positive value of K_{PV} is used, the system will be minimum-phase. Therefore, a minimum-phase system is always obtained. It is very important to indicate that, with this control structure, as the coupling between the controllers is eliminated, a positive resonant gain in the PR voltage controller must be used. The tuning process of the controllers can be divided into the following steps.

1) Select the filter and the sampling frequency. Calculate the ratio f_n/f_s.
2) Calculate the admissible values of K_{PI} using (27). Select K_{PI}.
3) Calculate the admissible values of K_{PV} using (39). Select K_{PV}. Since a positive K_{PV} must be used, a minimum-phase system is obtained. A positive resonant gain K_{RV} must be used.

Fig. 9 summarizes the proposed tuning process for the DLVADC to ensure stability. On the one hand, the DLVADC

TABLE II
EXPERIMENTAL SETUP PARAMETERS

Parameter	Symbol	Value
Filter inductor	L_f	2.5 mH
Filter capacitor	C_f	10 μF
Resonant frequency of the LC filter	f_n	1 kHz
Sampling frequency	f_s	8 / 6 / 4 kHz
Switching frequency	f_{sw}	8 / 6 / 4 kHz
DC-bus voltage	v_{dc}	750 V
Reference line-to-line voltage (RMS)	V_C^*	400 V
Fundamental frequency	f_o	50 Hz
Load resistor	R	100 Ω
Load inductor	L	125 mH

without decoupling, if stable, can be either a minimum-phase or a nonminimum-phase system. On the other hand, the DLVADC with decoupling, if stable, is always a minimum-phase system.

VI. EXPERIMENTAL RESULTS

The experimental tests are conducted with a 5-kW three-phase two-level VSI. The proposed controllers are implemented in a dSPACE DS1006 processor board. The analog signals are acquired using synchronous sampling. An LC filter with a 2.5 mH inductor and a 10 μF capacitor is used ($f_n = 1$ kHz). The fundamental frequency is set to 50 Hz, the switching frequency (f_{sw}) is equal to the sampling frequency, and the dead time is set to 3 μs in all tests. The dc-bus voltage, provided by a dc-voltage source, is 750 V.

On the one hand, the reference tracking capability is analyzed under no load, by applying a step in the capacitor voltage reference. The results obtained show how decoupling allows achieving a minimum-phase system, which translates to a much faster transient response. On the other hand, the disturbance rejection capability is analyzed by connecting an RL load. Therefore, in this test, only the results obtained with decoupling are shown, as this load introduces a disturbance at the fundamental frequency, where the sensitivity function of both systems is zero, which results in a very similar response. To demonstrate the good performance of the proposed controller, despite operating without harmonic control, the results obtained when connecting a nonlinear load are also presented. The nonlinear load is an uncontrolled three-phase full-wave rectifier, to which a 320 Ω resistive load is connected. The system parameters are summarized in Table II. Fig. 10 includes a photograph of the experimental setup.

First, it is demonstrated that the DLVCC and DLVADC are equivalent control structures (see Figs. 11–15). These tests are conducted with $f_n < f_s/6$, and it is decided to work with a negative K_{PI}, conditions that have not been explored in any

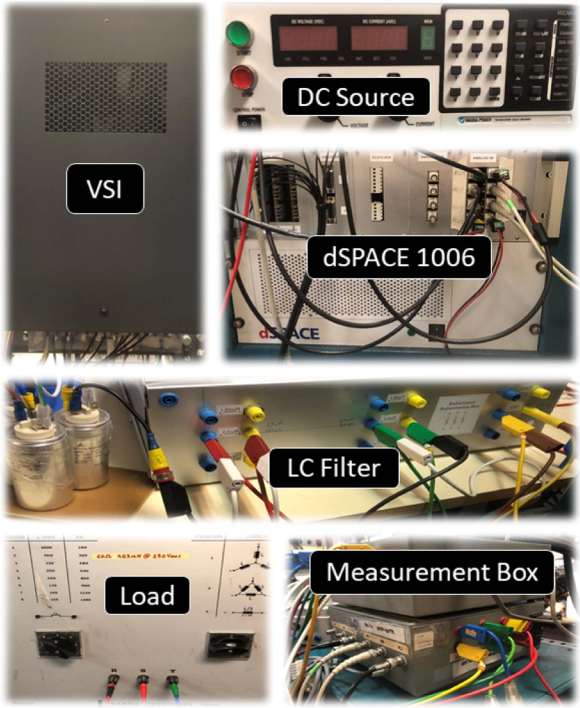


Fig. 10. Experimental setup.

previous publication. That is, the study is conducted within the complete stability region (see Fig. 4) but outside the stability region that allows obtaining a minimum-phase system (see Fig. 5).

Second, it is shown, for the first time, that the double-loop voltage control can be stable for $f_n = f_s/6$ (see Figs. 16 and 17); that is, it is demonstrated that $f_n = f_s/6$ is not a critical frequency in the double-loop voltage control.

Finally, the proposed stability regions are also verified for $f_n > f_s/6$ (see Figs. 18 and 19).

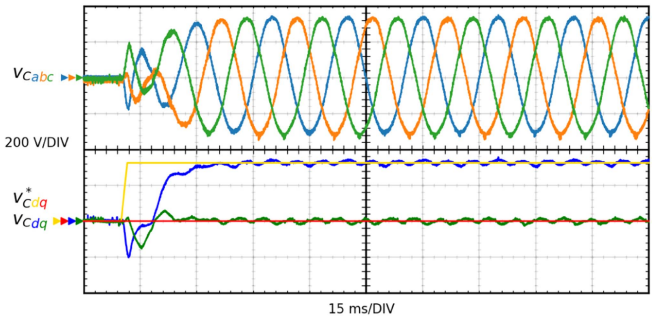
The tuning of the controllers is the same in all experiments, demonstrating that the same controller can be used for both $f_n < f_s/6$ and $f_n > f_s/6$. This was previously considered unfeasible (see Fig. 5). The complete stability region presented in this article explains why it is indeed possible (see Fig. 4).

A. Experimental Results for $f_n < f_s/6$

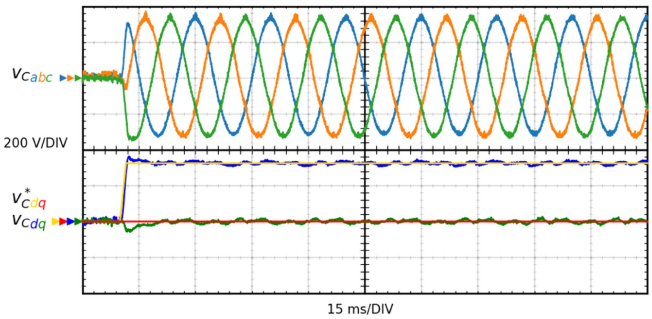
First, it is demonstrated that the DLVCC and DLVADC are equivalent control structures. These tests are conducted with a sampling frequency of 8 kHz ($f_n = f_s/8$), that is, $f_n < f_s/6$.

On the one hand, applying (22), it is concluded that K_{PI} must be within the interval $(-19.65, 0) \cup (0, 15.81)$ for the DLVCC to be stable, while applying (24) it is concluded that K_{PI} must be

$$\begin{cases} 0 < f_n < \frac{f_s}{6} & \to \quad 0 \quad < K_{\text{PV}} < b_{1.2} + 1 \\ \frac{f_s}{6} < f_n < \frac{f_s}{3} \;\&\; K_{\text{PI}} < \frac{\cos(\omega_n T_s)\omega_n L_f}{\sin(\omega_n T_s)} & \to \quad 0 \quad < K_{\text{PV}} < b_{1.2} + 1 \\ \frac{f_s}{6} < f_n < \frac{f_s}{3} \;\&\; K_{\text{PI}} > \frac{\cos(\omega_n T_s)\omega_n L_f}{\sin(\omega_n T_s)} & \to \quad b_{1.1} + 1 \quad < K_{\text{PV}} < b_{1.2} + 1 \\ \frac{f_s}{3} < f_n < \frac{f_s}{2} & \to \quad b_{1.1} + 1 \quad < K_{\text{PV}} < b_{1.2} + 1. \end{cases} \tag{39}$$

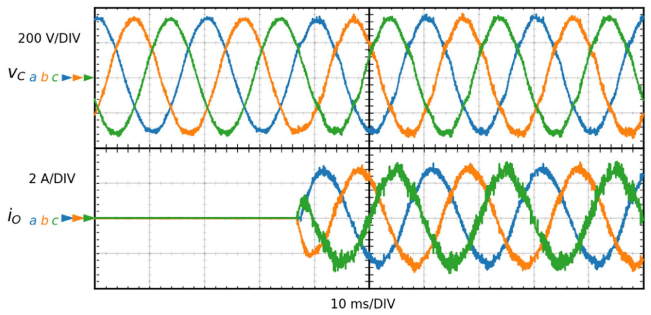


(a)

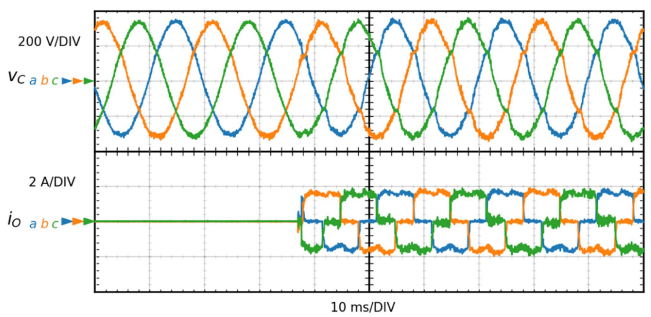


(b)

Fig. 11. Reference tracking capability of the DLVCC for $f_n < f_s/6$. $K_{\mathrm{PI}} = -5$ and $K_{\mathrm{RV}} = -30$. Capacitor phase voltage in the abc reference frame and in the dq reference frame rotating at the fundamental frequency for a reference step under no load. (a) Without decoupling ($K_{\mathrm{PV}} = 0.1$). (b) With decoupling ($K_{\mathrm{PV}} = -0.1$).

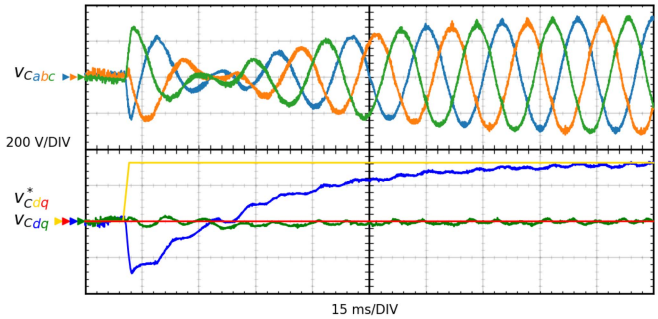


(a)

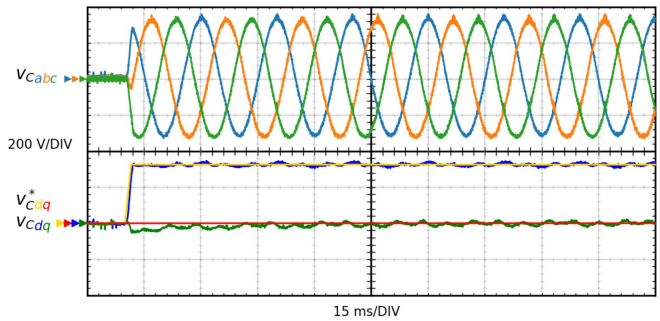


(b)

Fig. 12. Transient response of the DLVCC with capacitor voltage unitary decoupling to a load connection step for $f_n < f_s/6$. $K_{\mathrm{PI}} = -5$, $K_{\mathrm{RV}} = -30$, and $K_{\mathrm{PV}} = -0.1$. Capacitor phase voltage and output phase current in the abc reference frame. (a) Linear load. (b) Nonlinear load.

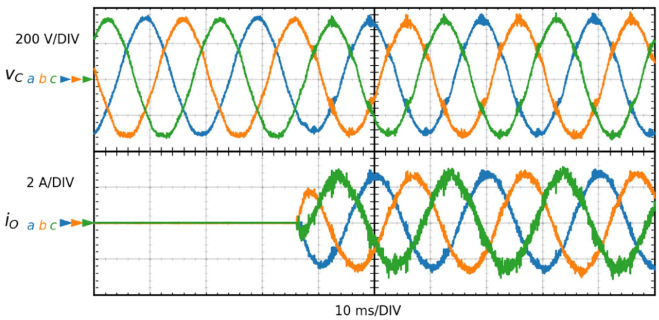


(a)

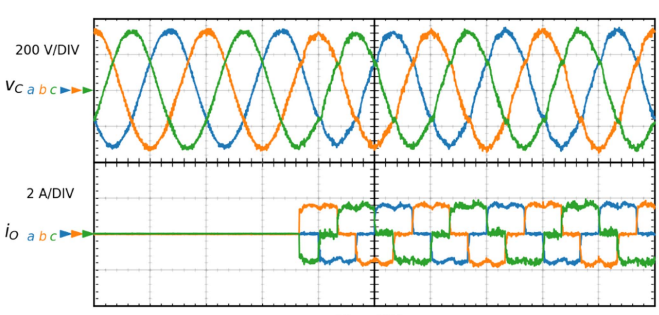


(b)

Fig. 13. Reference tracking capability of the DLVADC for $f_n < f_s/6$. $K_{\mathrm{PI}} = -5$ and $K_{\mathrm{RV}} = 30$. Capacitor phase voltage in the abc reference frame and in the dq reference frame rotating at the fundamental frequency for a reference step under no load. (a) Without decoupling ($K_{\mathrm{PV}} = -0.5$). (b) With decoupling ($K_{\mathrm{PV}} = 0.5$).



(a)



(b)

Fig. 14. Transient response of the DLVADC with capacitor voltage unitary decoupling to a load connection step for $f_n < f_s/6$. $K_{\mathrm{PI}} = -5$, $K_{\mathrm{RV}} = 30$, and $K_{\mathrm{PV}} = 0.5$. Capacitor phase voltage and output phase current in the abc reference frame. (a) Linear load. (b) Nonlinear load.

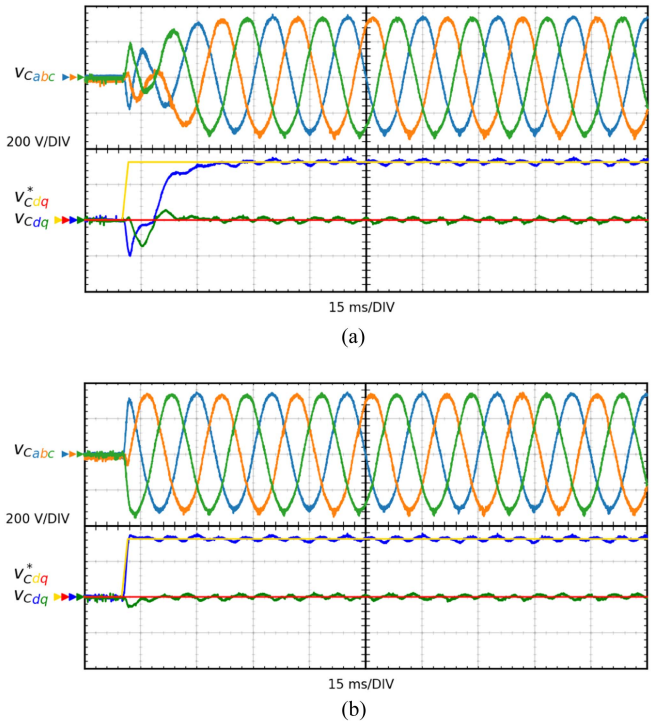


Fig. 15. Reference tracking capability of the DLVADC for $f_n < f_s/6$. $K_{\mathrm{PI}} = -5$ and $K_{\mathrm{RV}} = 150$. Capacitor phase voltage in the abc reference frame and in the dq reference frame rotating at the fundamental frequency for a reference step under no load. (a) Without decoupling ($K_{\mathrm{PV}} = -0.5$). (b) With decoupling ($K_{\mathrm{PV}} = 0.5$).

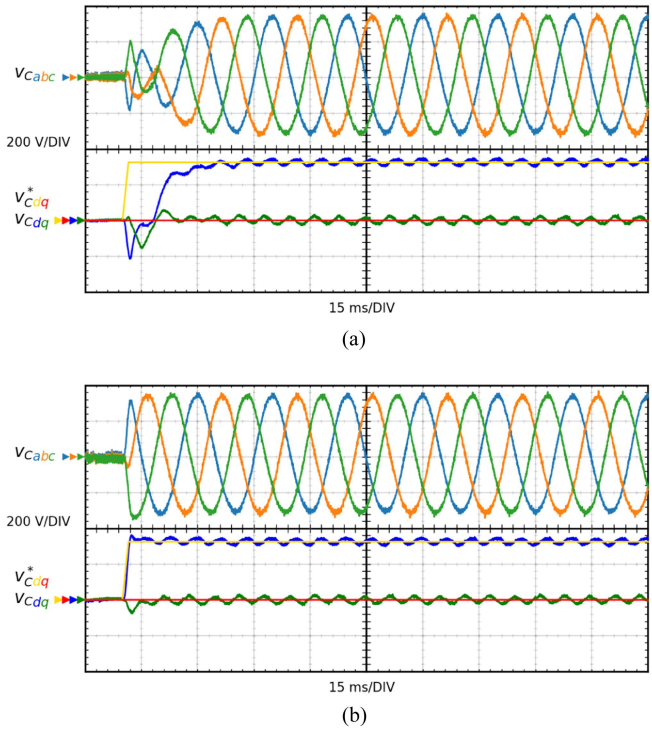


Fig. 16. Reference tracking capability of the DLVCC for $f_n = f_s/6$. $K_{\mathrm{PI}} = -5$ and $K_{\mathrm{RV}} = -30$. Capacitor phase voltage in the abc reference frame and in the dq reference frame rotating at the fundamental frequency for a reference step under no load. (a) Without decoupling ($K_{\mathrm{PV}} = 0.1$). (b) With decoupling ($K_{\mathrm{PV}} = -0.1$).

within the interval $(0, 9.26)$ for the DLVCC to be a minimum-phase system. On the other hand, applying (27), it is concluded that K_{PI} must be within the interval $(-19.65, 15.81)$ for the DLVADC to be stable, while applying (29) it is concluded that K_{PI} must be within the interval $(0, 9.26)$ for the DLVADC to be a minimum-phase system. As explained in the previous sections, the stability region for K_{PI} is the same for both control structures, with the only difference being that, in the DLVCC, a null K_{PI} cannot be used.

It is decided to work within the complete stability region (see Fig. 4) but outside the stability region that allows obtaining a minimum-phase system (see Fig. 5), so that it can be demonstrated how unitary decoupling of the capacitor voltage allows achieving a minimum-phase system with both control structures. Therefore, a negative K_{PI} is used, and $K_{\mathrm{PI}} = -5$ is selected, a value for which both control structures give rise to stable systems [$K_{\mathrm{PI}} \in$ (22) and $K_{\mathrm{PI}} \in$ (27)], but which are nonminimum-phase systems [$K_{\mathrm{PI}} \notin$ (24) and $K_{\mathrm{PI}} \notin$ (29)].

Firstly, the DLVCC is used. The tuning of the controllers is carried out according to the method shown in Fig. 7. As explained before, K_{PI} is set to -5. Since K_{PI} is negative, the resonant gain must also be negative (see Fig. 7), and it is decided to work with $K_{RV} = -30$. On the one hand, applying (23), it is concluded that $K_{\mathrm{PV}}K_{\mathrm{PI}}$ must be within the interval $(-1, -0.17)$ for the DLVCC without decoupling to be stable, so it is also concluded that K_{PV} must be within the interval $(0.034, 0.20)$ for

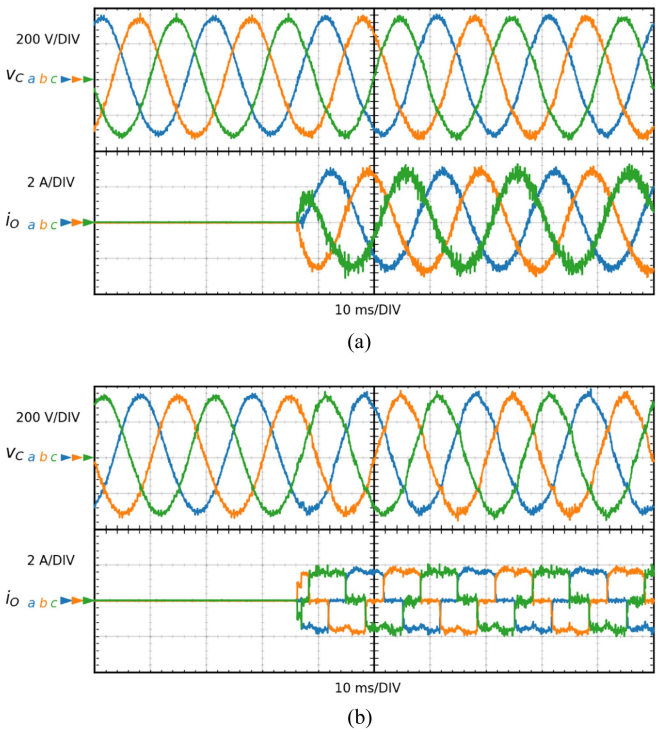
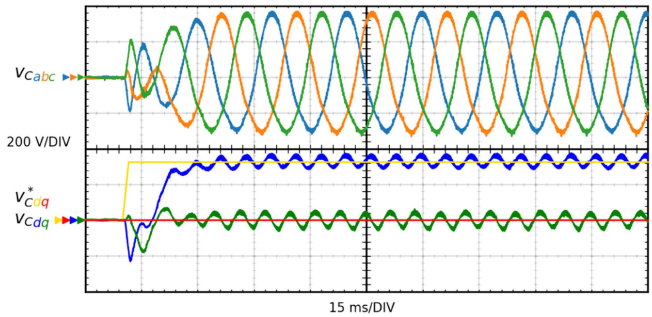
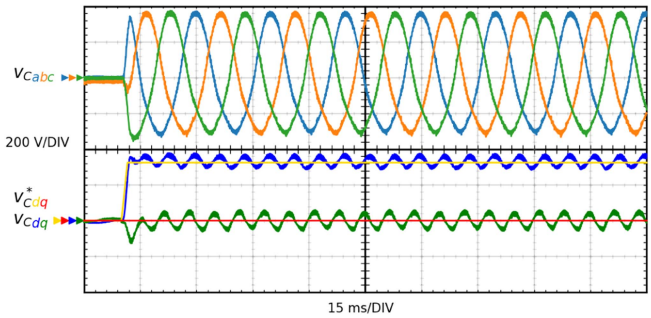


Fig. 17. Transient response of the DLVCC with capacitor voltage unitary decoupling to a load connection step for $f_n = f_s/6$. $K_{\mathrm{PI}} = -5$, $K_{\mathrm{RV}} = -30$, and $K_{\mathrm{PV}} = -0.1$. Capacitor phase voltage and output phase current in the abc reference frame. (a) Linear load. (b) Nonlinear load.

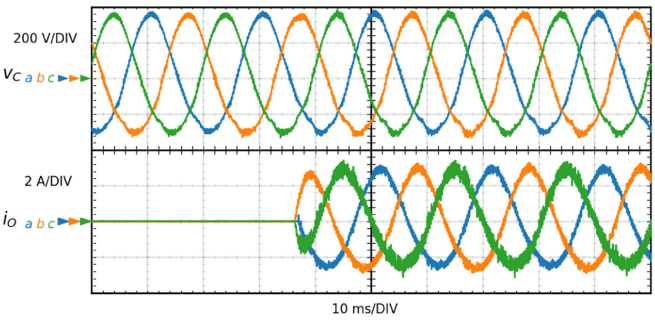


(a)

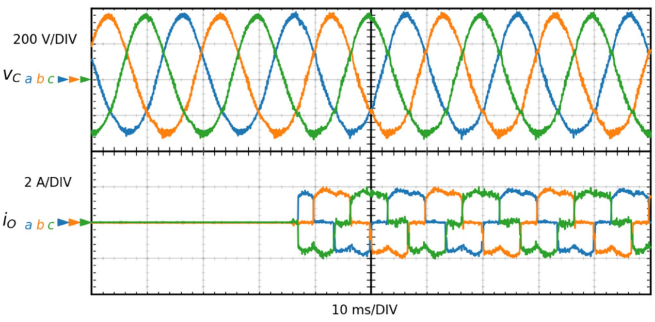


(b)

Fig. 18. Reference tracking capability of the DLVCC for $f_n > f_s/6$. $K_{\mathrm{PI}} = -5$ and $K_{\mathrm{RV}} = -30$. Capacitor phase voltage in the abc reference frame and in the dq reference frame rotating at the fundamental frequency for a reference step under no load. (a) Without decoupling ($K_{\mathrm{PV}} = 0.1$). (b) With decoupling ($K_{\mathrm{PV}} = -0.1$).



(a)



(b)

Fig. 19. Transient response of the DLVCC with capacitor voltage unitary decoupling to a load connection step for $f_n > f_s/6$. $K_{\mathrm{PI}} = -5$, $K_{\mathrm{RV}} = -30$, and $K_{\mathrm{PV}} = -0.1$. Capacitor phase voltage and output phase current in the abc reference frame. (a) Linear load. (b) Nonlinear load.

the DLVCC without decoupling to be stable, and it is decided to work with $K_{\mathrm{PV}} = 0.1$. Since $K_{\mathrm{PV}}K_{\mathrm{PI}}$ must be negative, a nonminimum-phase system will be obtained (see Fig. 7). On the other hand, applying (34), it is concluded that $K_{\mathrm{PV}}K_{\mathrm{PI}}$ must be within the interval $(0, 0.83)$ for the DLVCC with decoupling to be stable, so it is also concluded that K_{PV} must be within the interval $(-0.166, 0)$ for the DLVCC with decoupling to be stable, and it is decided to work with $K_{\mathrm{PV}} = -0.1$. It can be seen how the decoupling has shifted the admissible interval for $K_{\mathrm{PV}}K_{\mathrm{PI}}$ one unit upwards and, since $K_{\mathrm{PV}}K_{\mathrm{PI}}$ must be positive, a minimum-phase system will be obtained (see Fig. 7). It is decided to work with the same K_{PV} in absolute value with and without decoupling, with the aim of highlighting the advantages of decoupling.

Fig. 11 shows the response of the DLVCC under no load to a step in the voltage reference. Fig. 11(a) shows the capacitor voltage when operating without decoupling, while Fig. 11(b) shows the capacitor voltage when working with decoupling. It can be seen how, without decoupling, a nonminimum-phase system is obtained, as the response starts in the opposite direction to the reference (see Fig. 11(a)). Decoupling allows achieving a minimum-phase system, resulting in a fast transient response (see Fig. 11(b)).

The disturbance rejection capability is only analyzed with decoupling, as explained before. Fig. 12 shows the response of the DLVCC to the connection of the loads. Fig. 12(a) shows the capacitor voltage and the output current when the linear load is connected. Fig. 12(b) shows the capacitor voltage and the output current when the nonlinear load is connected. It can be observed how, when the loads are connected, the voltage continues to be precisely controlled.

Second, the DLVADC is used. The tuning of the controllers is carried out according to the method shown in Fig. 9. As explained before, K_{PI} is set to -5. The resonant gain must be positive (see Fig. 9), and it is decided to work with $K_{\mathrm{RV}} = 30$. On the one hand, applying (28), it is concluded that K_{PV} must be within the interval $(-1, -0.17)$ for the DLVADC without decoupling to be stable, and it is decided to work with $K_{\mathrm{PV}} = -0.5$. Since K_{PV} must be negative, a nonminimum-phase system will be obtained (see Fig. 9). On the other hand, applying (39), it is concluded that K_{PV} must be within the interval $(0, 0.83)$ for the DLVADC with decoupling to be stable, and it is decided to work with $K_{\mathrm{PV}} = 0.5$. Since K_{PV} must be positive, a minimum-phase system will be obtained (see Fig. 9). It is decided to work again with the same K_{PV} in absolute value with and without decoupling, with the aim of highlighting the advantages of decoupling.

Fig. 13 shows the response of the DLVADC under no load to a step in the voltage reference. Fig. 13(a) shows the capacitor voltage when operating without decoupling, while Fig. 13(b) shows the capacitor voltage when working with decoupling. It can be seen how, without decoupling, a nonminimum-phase system is obtained, as the response starts in the opposite direction to the reference (see Fig. 13(a)). Decoupling allows achieving a minimum-phase system, resulting in a fast transient response (see Fig. 13(b)).

The disturbance rejection capability is only analyzed with decoupling, as explained before. Fig. 14 shows the response of the DLVADC to the connection of the loads. Fig. 14(a) shows the capacitor voltage and the output current when the linear load is connected. Fig. 14(b) shows the capacitor voltage and the output current when the nonlinear load is connected. It can be observed how, when the loads are connected, the voltage continues to be precisely controlled.

Comparing Fig. 13(a) with Fig. 11(a), it is observed that the response of the DLVADC without decoupling is slower than the response of the DLVCC without decoupling. This is because, in the DLVCC, a ratio $K_{\text{RV}}/K_{\text{PV}} = -300$ is used, whereas in the DLVADC a ratio $K_{\text{RV}}/K_{\text{PV}} = -60$ is used. If $K_{\text{RV}} = -6$ had been chosen for the DLVCC, or if $K_{\text{RV}} = 150$ had been chosen for the DLVADC, both systems would be equivalent, and the response would be the same. Comparing Fig. 13(b) with Fig. 11(b), it is observed that the response of the DLVADC with decoupling is very similar to the response of the DLVCC with decoupling, so it is concluded that the decoupling significantly reduces the influence of the value of K_{RV} selected. It is decided to show the results obtained with the DLVADC for $K_{\text{RV}} = 150$, with the aim of demonstrating that the DLVCC and DLVADC are equivalent control structures, but that the tuning of the controllers to obtain the same system is different. Fig. 15 shows the response of the DLVADC under no load to a step in the voltage reference when $K_{\text{RV}} = 150$, where it can be seen that the same results are obtained as with the DLVCC (see Fig. 11). This demonstrates that the DLVCC and the DLVADC are equivalent control structures and that the stability analysis holds when varying K_{RV}.

Once it has been demonstrated that the DLVCC and DLVADC are equivalent control structures, the following experiments present only the results obtained with the DLVCC, as the same results could be achieved with the DLVADC. It is decided to use the DLVCC because it has not been used in any previous publication for $f_n > f_s\ /6$.

B. Experimental Results for $f_n = f_s/6$

These tests are conducted with a sampling frequency of 6 kHz ($f_n = f_s/6$). Applying (22), it is concluded that K_{PI} must be within the interval $(-27.38, 0) \cup (0, 9.12)$ for the DLVCC to be stable, while applying (24) it is concluded that there is not a value of K_{PI} that allows obtaining a minimum-phase system. It is decided to continue using the same value of K_{PI}, and $K_{\text{PI}} = -5$ is selected, a value for which the DLVCC gives rise to a stable system [$K_{\text{PI}} \in$ (22)], but which is a nonminimum-phase system [$K_{\text{PI}} \notin$ (24)].

The tuning of the controllers is carried out according to the method shown in Fig. 7. Since K_{PI} is negative, the resonant gain must also be negative (see Fig. 7), and it is decided to work again with $K_{RV} = -30$. On the one hand, applying (23), it is concluded that $K_{\text{PV}}K_{\text{PI}}$ must be within the interval $(-1, -0.06)$ for the DLVCC without decoupling to be stable, so it is also concluded that K_{PV} must be within the interval $(0.012, 0.20)$ for the DLVCC without decoupling to be stable, and it is decided to work with $K_{\text{PV}} = 0.1$ again. Since $K_{\text{PV}}K_{\text{PI}}$ must be negative, a nonminimum-phase system will be obtained (see Fig. 7). On the other hand, applying (34), it is concluded that $K_{\text{PV}}K_{\text{PI}}$ must be within the interval $(0, 0.94)$ for the DLVCC with decoupling to be stable, so it is also concluded that K_{PV} must be within the interval $(-0.188, 0)$ for the DLVCC with decoupling to be stable, and it is decided to work with $K_{\text{PV}} = -0.1$ again. It can be seen how the decoupling has shifted the admissible interval for $K_{\text{PV}}K_{\text{PI}}$ one unit upwards and, since $K_{\text{PV}}K_{\text{PI}}$ must be positive, a minimum-phase system will be obtained (see Fig. 7). The same controller tuning is used as the one used for $f_n < f_s/6$, with the aim of demonstrating that the system is stable in both situations.

Fig. 16 shows the response of the DLVCC under no load to a step in the voltage reference. Fig. 16(a) shows the capacitor voltage when operating without decoupling, while Fig. 16(b) shows the capacitor voltage when working with decoupling. Fig. 17 shows the response to the connection of the loads. It is demonstrated, for the first time, that the double-loop voltage control can be stable at $f_n = f_s/6$.

C. Experimental Results for $f_n > f_s/6$

These tests are conducted with a sampling frequency of 4 kHz ($f_n = f_s/4$), that is, $f_n > f_s/6$. Applying (22), it is concluded that K_{PI} must be within the interval $(-15.81, 0) \cup (0, 1.97)$ for the DLVCC to be stable, while applying (24) it is concluded that K_{PI} must be within the interval $(-15.81, 0)$ for the DLVCC to be a minimum-phase system. It is decided to continue using the same value of K_{PI}, and $K_{\text{PI}} = -5$ is selected, a value for which the DLVCC gives rise to a stable system [$K_{\text{PI}} \in$ (22)], which can be a minimum-phase system [$K_{\text{PI}} \in$ (24)].

The tuning of the controllers is carried out according to the method shown in Fig. 7. Since K_{PI} is negative, the resonant gain must also be negative (see Fig. 7), and it is decided to work again with $K_{\text{RV}} = -30$. On the one hand, applying (23), it is concluded that $K_{\text{PV}}K_{\text{PI}}$ must be within the interval $(-1, 0.12)$ for the DLVCC without decoupling to be stable, so it is also concluded that K_{PV} must be within the interval $(-0.024, 0.20)$ for the DLVCC without decoupling to be stable, and it is decided to work with $K_{\text{PV}} = 0.1$ again, so a nonminimum-phase system will be obtained. In this case, $K_{\text{PV}}K_{\text{PI}}$ does not need to be negative, so a minimum-phase system could have been obtained (see Fig. 7). On the other hand, applying (34), it is concluded that $K_{\text{PV}}K_{\text{PI}}$ must be within the interval $(0, 1.12)$ for the DLVCC with decoupling to be stable, so it is also concluded that K_{PV} must be within the interval $(-0.22, 0)$ for the DLVCC with decoupling to be stable, and it is decided to work with $K_{\text{PV}} = -0.1$ again. It can be seen how the decoupling has shifted the admissible interval for $K_{\text{PV}}K_{\text{PI}}$ one unit upwards and, since $K_{\text{PV}}K_{\text{PI}}$ must be positive, a minimum-phase system will be obtained (see Fig. 7). The same controller tuning is used as the one used for $f_n < f_s/6$ and $f_n = f_s/6$, with the aim of demonstrating that the system is stable in all situations.

Fig. 18 shows the response of the DLVCC under no load to a step in the voltage reference. Fig. 18(a) shows the capacitor voltage when operating without decoupling, while Fig. 18(b) shows the capacitor voltage when working with decoupling. Fig. 19 shows the response to the connection of the loads.

It is demonstrated that the same controller can be used for $f_n < f_s/6$, $f_n = f_s/6$, and $f_n > f_s/6$. The results obtained are very similar, with the only difference being that the switching harmonics become more significant as f_s decreases, since the LC filter is not able to attenuate them correctly.

VII. Conclusion

This article presents a detailed stability analysis of the double-loop voltage control with PR voltage controller in VSIs with an output LC filter. In this control structure, a P controller is usually employed in the inner current control loop. The stability region is defined as the frequency ratios between the sampling frequency (f_s) and the natural frequency of the LC filter (f_n) with which the system can be stable. In previous publications, it has been proposed to place the P current controller in the feedback path of the inner control loop (DLVADC), rather than in the forward path (DLVCC), with the aim of increasing the stability region. This article demonstrates that the DLVCC and the DLVADC are equivalent control structures, with the same stability region, but that the tuning of the controllers is different. This article presents, for the first time, the complete stability region of the double-loop voltage control, and demonstrates that it can be stable for any frequency ratio f_n/f_s, and that the stability region presented in previous publications, where $f_n = f_s/6$ is a critical frequency, is the stability region that allows obtaining a minimum-phase system, which should not be confused with the complete stability region. Furthermore, it is demonstrated that the unitary decoupling of the capacitor voltage results in a minimum-phase system across the complete stability region of the double-loop voltage control, demonstrating the benefits of having determined it. To conclude, a tuning method is proposed that ensures the stability of the double-loop voltage control. Experimental results confirm the theoretical analysis conducted.

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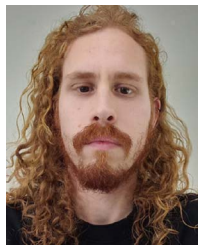

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