Compact Interleaved PCB Rogowski Coil Array for Chip Current Measuring in SiC MOSFET Power Modules

Yongfan Zhan, Xuebao Li, *Member, IEEE*, Xiaofeng Yang, *Graduate Student Member, IEEE*, Hao Li, Lei Wang, Rui Jin, *Member, IEEE*, Zhibin Zhao, *Member, IEEE*, and Xiang Cui, *Senior Member, IEEE*

***Abstract*—The use of printed circuit board (PCB) Rogowski coils to measure chip currents in power modules may significantly help address current imbalance problems that lead to derating or overcurrent failure. Compared to silicon-based power devices, silicon carbide (SiC) power modules feature smaller chips and more compact chip arrangements. This necessitates more compact current measuring probes. This paper proposes a novel design method for PCB Rogowski coil arrays that utilizes the interturn spacing to achieve an interleaved arrangement of Rogowski coils, thereby solving manufacturability problems while increasing the mutual inductance of the Rogowski coils. For a prototype SiC MOSFET power module, given the same spatial constraints, the coil array with the interleaved arrangement exhibits an average mutual inductance that is 98% higher than that of a coil array with the conventional arrangement. The circuit of the Rogowski transducer, consisting of the Rogowski coil and an integrator, is presented. The packaging processes for integrating the interleaved PCB Rogowski coil array into the power module are also described. The sensitivity of the Rogowski transducer is evaluated, and the impact of capacitive coupling interference is assessed. The switching currents of the 12 SiC MOSFET chips are measured using the interleaved PCB Rogowski coil array in a double-pulse test, which reveals the detailed commutation behavior within the power module. The interleaved PCB Rogowski coil array proves to be an effective current measurement tool for densely arranged branches, providing a foundation for measuring the internal chip current distribution of power modules.**

***Index Terms*—Current distribution, mutual inductance, power module, Rogowski coil, silicon carbide (SiC).**

I. Introduction

SILICON carbide (SiC) devices have emerged as transformative technologies in power electronics, distinguished by remarkable performance metrics including high blocking voltage, high operating temperature, high switching frequencies, low power loss, and high thermal conductivity [1], [2], [3]. These characteristics render SiC devices particularly attractive for power converters [4], energy transmission systems [5], and traction inverters [6], [7].

The inherent challenges associated with SiC substrate and epitaxial defects, coupled with subsequent processing issues, necessitate smaller chip sizes compared to silicon-based devices to maintain acceptable yield rates [8], [9], [10]. To meet current-carrying requirements, high-power SiC MOSFET modules typically employ multiple chips connected in parallel [11]. Ideally, the rated current of such power modules is determined by the number of parallel-connected chips and their individual rated currents. However, the current distribution among parallel-connected SiC chips is nonuniform, influenced by chip parameters [12], packaging parasitics [13], [14], and junction temperature distributions [15]. Excessive current through localized chips may lead to chip failure and subsequently module failure [16]. An approach to mitigate current imbalance involves measuring current across parallel-connected chips, investigating influencing factors, and developing industrially viable current balancing methods [17], [18], [19]. The critical initial step in this approach is the development of instrumentation capable of accurately measuring chip currents within SiC MOSFET power modules.

Rogowski coils have emerged as a prominent current measurement instrumentation in power electronics [20], [21], leveraging their advantageous characteristics, including wide bandwidth, galvanic isolation, compact form factor, and thermal stability [22], [23], [24]. A micro-PCB Rogowski coil has been developed for current measurement and overcurrent protection of power modules [25]. Low-Temperature Co-fired Ceramic (LTCC) Rogowski coils, distinguished by exceptional high-temperature stability, could be directly integrated into SiC MOSFET modules for current measuring [26]. Compact planar Rogowski coils achieve remarkable volume miniaturization while maintaining measurement fidelity [27]. This characteristic has propelled their popularity in power electronics applications [28], [29].

The need to measure currents in multiple branches has been a catalytic force in the continuing evolution of Rogowski coil technologies. As early as 1997, wound current sensing coils

Received 15 April 2025; revised 3 July 2025 and 23 August 2025; accepted 23 September 2025. Date of publication 26 September 2025; date of current version 13 November 2025. This work was supported by the Program of Beijing Huairou Laboratory under Grant ZD2022004A. Recommended for publication by Associate Editor W. Huang. *(Corresponding author: Xuebao Li.)*

Yongfan Zhan, Xuebao Li, Xiaofeng Yang, Zhibin Zhao, and Xiang Cui are with the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Beijing 102206, China, and also with the Beijing Institute of Smart Energy, Beijing Huairou Laboratory, Beijing 102209, China (e-mail: zhanyongfan@ncepu.edu.cn; lxb08357x@ncepu.edu.cn; 120232101071@ncepu.edu.cn; zhibinzhao@ncepu.edu.cn; x.cui@ncepu.edu.cn).

Hao Li, Lei Wang, and Rui Jin are with the Beijing Institute of Smart Energy, Beijing Huairou Laboratory, Beijing 102209, China (e-mail: lihao@bise.hrl.ac.cn; wanglei@bise.hrl.ac.cn; jinrui@bise.hrl.ac.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3615168.

Digital Object Identifier 10.1109/TPEL.2025.3615168

were embedded in IGBT power modules to study current redistribution phenomena across two parallel-connected chips [30]. A special variant of the Rogowski coil uses a pair of spiral traces implemented on a thin-film substrate to capture magnetic field variations. Such sensor arrays enable comprehensive current distribution measurements across eight parallel bonding wires, revealing intricate current redistribution [31]. PCB Rogowski coils may be seamlessly incorporated into gate drivers. Two adjacent PCB Rogowski coils were seamlessly incorporated into a gate driver to measure the terminal currents of a SiC MOSFET module and provide short-circuit protection [32]. The arm currents of three-phase bridge SiC MOSFET modules may also be measured using miniaturized PCB Rogowski coils integrated within their driver circuits [33]. For chip configurations with more distributed layouts, circular Rogowski coils can be embedded in IGBT devices to measure the chip currents [34]. For press-pack devices with more compact chip layouts, a denser, rectangular coil array is required [35], [36]. An ingenious approach uses two vertically stacked PCB Rogowski coil arrays, allowing overlapping placement of Rogowski coils without mutual interference, enabling more compact and multibranch current measurements [37].

The above studies have significantly advanced the state-of-the-art for Rogowski coil applications in power electronics. Most of the research has focused on improving the performance of individual Rogowski coils and measuring currents in branches outside the power modules. Existing multibranch current measurement methods are also somewhat overstretched by the compact chip layout in SiC MOSFET power modules. This article proposes a compact arrangement for PCB Rogowski coil arrays. By exploiting the interturn spacing of PCB Rogowski coils, the proposed method enables manufacturability and larger mutual inductance without requiring more space. Accordingly, coil arrays designed by using this method can effectively address the current measurement requirements for densely packed chips in SiC MOSFET power modules.

The rest of this article is organized as follows. In Section II, a SiC MOSFET power module is presented. The dimensions of the PCB Rogowski coil array for chip current measurement in the module are derived. The manufacturability problem in the design of a PCB Rogowski coil array using the conventional method is described. The mutual inductances of the coils are compared between the conventional and the proposed coil arrangement method. In Section III, the stages of the packaging processes for integrating the compact interleaved coil arrays into the power modules are presented. The chip currents in the SiC MOSFET power modules are measured and discussed for different module configurations. Finally, Section IV concludes this article.

II. Compact Interleaved PCB Rogowski Coil Array

A. Manufacturability of the Conventional Coil Array

Consider a prototype 1200 V/600 A SiC MOSFET power module in a 62 mm package, shown in Fig. 1, which features a half-bridge topology. Each bridge arm may accommodate up to six parallel-connected SiC MOSFET chips. The SiC MOSFET chips used in the module have a size of 5 mm × 5 mm. Within a bridge arm, the six parallel chips are uniformly aligned in a single row, with a spacing of 3.2 mm between adjacent chips.

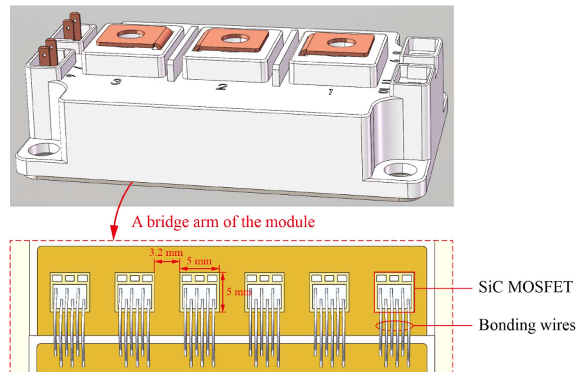


Fig. 1. Internal view and chip layout of the prototype power module.

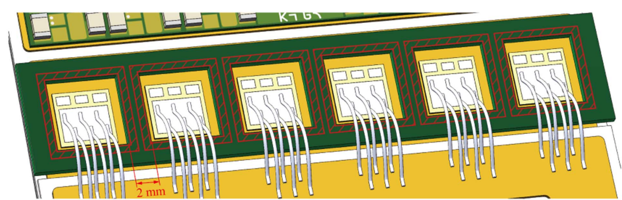


Fig. 2. Prototype coil array corresponding to a bridge arm. Each red frame is supposed to be a Rogowski coil.

Fig. 2 illustrates a prototype coil array used to measure the current of the chips in one bridge arm. The coil array would be implemented on a single PCB, featuring six rectangular cutouts, each may be encircled by a rectangular PCB Rogowski coil. The array is positioned directly above the chips, with each cutout aligned to a corresponding chip. Bond wires connected to the source pads of the SiC MOSFET chips pass through these cutouts, enabling the PCB Rogowski coils to measure the chip currents by sensing the current in the bond wires.

Considering the clearance between the soldering fixture and the chips, the actual positions of the chips may vary randomly during the packaging processes of the power module. Consequently, the coil array cannot fully utilize the designed spacing between adjacent chips, leaving only 2 mm of available PCB width between two coils. This width is shared by two adjacent Rogowski coils.

In the conventional PCB Rogowski coil array arrangement, the turns of adjacent coils are aligned uniformly [36]. When attempting to arrange six PCB Rogowski coils on the aforementioned PCB using this conventional method, the turns arrangement and adjacent details of two of the coils are illustrated in Fig. 3. Each turn of the PCB Rogowski coil consists of two vias and traces. In the middle layer of the PCB, there is also a perpendicular return wire between the two vias [38]. In Fig. 3(a), the red dashed box outlines the area between two adjacent coils, and Fig. 3(b) provides a detailed view of this region. Fig. 3(b) additionally lists some typical PCB manufacturing constraints.

With the conventional arrangement method, even when employing the most compact parameters, the vias of two Rogowski coils inevitably come into contact, leading to short-circuits.

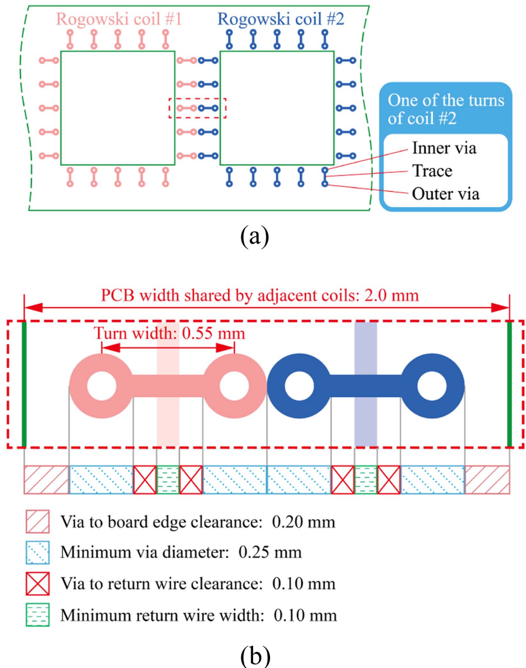


Fig. 3. Conventional arrangement, taking two of the coils. (a) Basic patterns. (b) Details of adjacent turns.

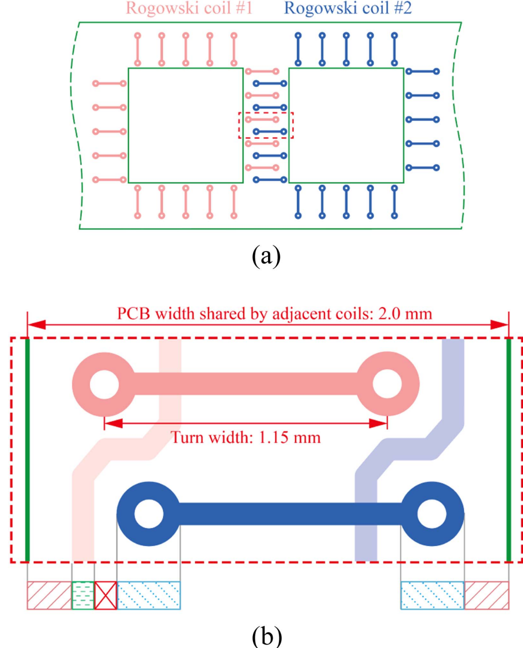


Fig. 4. Interleaved arrangement, taking two of the coils. (a) Basic patterns. (b) Details of adjacent turns.

Therefore, the coil array using the conventional arrangement method is nearly impractical to implement with standard manufacturing parameters. Even if fabricated through advanced process, the resulting coil array would have low mutual inductance, making it inadequate for measuring the current of SiC MOSFET chips.

B. The Concept of the Interleaved Arrangement

To address the manufacturing challenges as well as the insufficiency of mutual inductance for densely arranged Rogowski coil arrays, this article proposes an interleaved arrangement method for Rogowski coil arrays. The fundamental concept of the proposed method is to maximize the utilization of the PCB area for placing the turns of the Rogowski coils.

As observed in Fig. 3, the regions between the turns are free of traces or vias. Where two coils are adjacent to each other, by lifting the turns of one coil upwards and moving the turns of the other coil downward, it is possible to have adjacent turns occupying different rows. The vertical space is thus utilized more efficiently. This configuration also reduces the design complexity and fabrication difficulty of the coil array.

The turns arrangement and adjacent details of two coils in the interleaved coil array are depicted in Fig. 4. Compared to the conventional method, the proposed method requires only two vias to be placed in a row space, thus ensuring the manufacturability of the coil arrays under the existing process constraints. The turns of adjacent coils are interleaved like the pages of two books, enabling high integration density and manufacturability within a limited space. In addition, more relaxed spatial constraints allow for larger vias and wider traces, enabling the use of economical PCB manufacturing process. This offers considerable cost advantages for coil arrays containing hundreds of vias.

Each turn of the coil with the interleaved arrangement has a width of 1.15 mm compared to the 0.55 mm turn width (via spacing) of the conventional arrangement. Theoretically, since the coils have larger dimensions, their mutual inductance would also be larger. Therefore, the interleaved arrangement provides a feasible solution for high-sensitivity current measurement in SiC power modules with densely packed chips.

C. Comparison of the Conventional and Interleaved Arrangements

With the fabrication challenges resolved, the current measurement performance of the interleaved coil array should also be evaluated. A primary concern is how the mutual inductance of the proposed arrangement compares to that of the conventional arrangement, as the mutual inductance directly affects the sensitivity of the current measurement.

Ignoring the manufacturing constraints for the moment, it is assumed that either conventional coils or interleaved coils could be ideally arranged within the PCB. For a coil, target region Ω_1 and interference region Ω_2 are defined in Fig. 5, where O is the origin. The definition of the regions is the same for both conventional and interleaved arrangements.

The target region is located at the center of the coil and has the same size as the SiC MOSFET chip. This region represents the area through which the bonding wires of the target chip, or equivalently, the chip current, will traverse. Therefore, it may be used to calculate the mutual inductance of the coil to the measured target chip.

The definition of the interference region comes from concern about the effect of the neighboring chip currents on this coil.

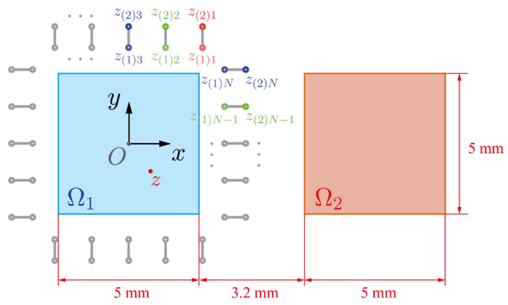


Fig. 5. Target region Ω_1 and interference region Ω_2 for a Rogowski coil, taking the conventional arrangement as an example.

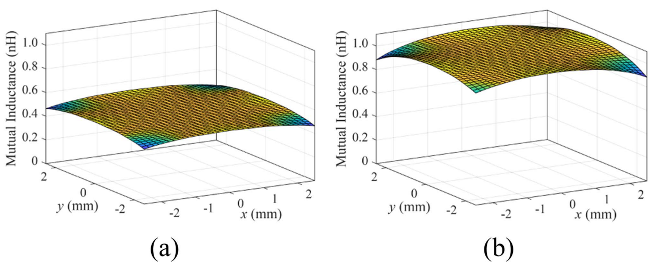


Fig. 6. Mutual inductance surfaces in the target region for different Rogowski coils. (a) Conventional arrangement. (b) Interleaved arrangement.

Although the current of the neighbouring chip should be measured by the neighbouring coil, the distance of just a few millimetres means that the current of the neighbouring chip may still cause some interference to this coil.

It should be noted that the mutual inductance between a bonding wire and a Rogowski coil varies depending on the position of the wire and the arrangement of the coil vias. When the bonding wire is located at a specific position in the target region or in the interference region, the exact mutual inductance between the wire and the coil may be expressed as follows [39]:

$$M = \frac{\mu_0 a}{2\pi} \sum_{n=1}^{N} \left(\ln |z - z_{(2)n}| - \ln |z - z_{(1)n}| \right) \tag{1}$$

where $\mu_0 = 4\pi \times 10^{-7}$ H/m is the permeability of free space, a is the is the thickness of the Rogowski coil PCB, N is the number of turns of the Rogowski coil, z is the position of the bonding wire, $z_{(1)n}$ and $z_{(2)n}$ is the positions of the inner vias and outer vias, respectively.

In a 3-D space defined by x, y, and mutual inductance M, the points representing the mutual inductance at different positions form a surface, enabling the visualization of the mutual inductance characteristics. For the two coils with conventional and interleaved arrangements, respectively, their mutual inductance surfaces in the target region are shown in Fig. 6. It is evident that the coil with the interleaved arrangement exhibits a higher mutual inductance surface compared to the coil with the conventional arrangement.

In addition to graphical representations, a numerical metric is introduced to evaluate and compare the mutual inductance characteristics of the Rogowski coils. Based on the mutual inductance (1), the average mutual inductance over the entire target region is given by

$$M_{\mathrm{m}} = \frac{1}{\int_{\Omega_1} \mathrm{d}s} \int_{\Omega_1} M(x,y) \mathrm{d}s. \tag{2}$$

This value is commonly referred to as the "mutual inductance" of a Rogowski coil in datasheets.

For the coil with the conventional arrangement, the average mutual inductance in the target region is 0.51 nH. At the four corners of the target region, the mutual inductance reaches its minimum value of 0.46 nH. At the midpoints on each side of the target region, the mutual inductance reaches its maximum value of 0.52 nH.

For the coil with the interleaved arrangement, the average mutual inductance in the target region is 1.01 nH. At the two corners where the turns are sparser due to the shift, the mutual inductance reaches its minimum value of 1.88 nH, as exemplified by the point $(-2.5, 2.5)$ in the target region. At a point on a side of the target region, the mutual inductance reaches its maximum value of 1.03 nH.

In addition to the characteristics of individual coils, the influence of adjacent currents on the coil is also significant. Given uniform current distribution across parallel-connected chips, the current through each chip is identical. The effect of the current in the interference region on the Rogowski coil may be evaluated by the interference ratio

$$R_{\mathrm{I}} = \frac{100\%}{\int_{\Omega_2} \mathrm{d}s} \int_{\Omega_2} \frac{M(x,y)}{M_{\mathrm{m}}} \mathrm{d}s \tag{3}$$

where $M(x,y)$ is the exact mutual inductance while bonding wire $z(x,y)$ is in the interference region Ω_2, and M_{m} is the average mutual inductance of the target region Ω_1. The calculation shows that the coil with the conventional arrangement exhibits an interference ratio of -2.03%. In comparison, the coil with the interleaved arrangement shows a slightly worse interference ratio of -3.18%. This may be readily explained by the fact that the larger Rogowski coils have turns closer to the interference region. The interference is attributed to the mutual cancellation of magnetic fields between parallel current-carrying conductors, which accounts for the typically negative interference ratios.

TABLE I
COMPARISON OF THE TWO ARRANGEMENTS

	Conventional Arrangement	Interleaved Arrangement
Average Mutual Inductance M_{m}	0.51 nH	1.01 nH
Interference Ratio R_{I}	-2.03%	-3.18%

Table I presents a comparison of the evaluation metrics for the two arrangements. In summary, the interleaved arrangement not only resolves the manufacturing challenges of Rogowski coil arrays in compact spaces but also delivers almost double the

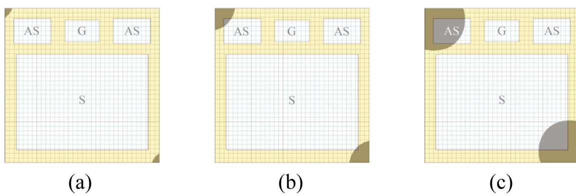


Fig. 7. Mutual inductance tolerance regions for different maximum acceptable deviations. (a) 5% tolerance. (b) 3% tolerance. (c) 1% tolerance.

mutual inductance, which is particularly valuable for current measurement in SiC MOSFET chips.

III. Integration and Experiments of the Interleaved Rogowski Coil Array

A. Mutual Inductance Tolerance Regions for Bonding Wire Placement

The previous section indicated that the mutual inductance deviates from the average mutual inductance when the bonding wires are positioned at the corners of the target region. These deviations may need to be controlled depending on the precision requirements of the measurement. In the case of soldered power modules, the deviation control could be effectively achieved by restricting the bonding wires within specific regions of the Rogowski coils. These regions are referred to as "mutual inductance tolerance regions" in this article.

Taking the 5% measurement accuracy tolerance, commonly encountered in engineering practice, as the maximum acceptable deviation. The points with mutual inductance deviations less than the tolerance are filtered from the mutual inductance surface shown in Fig. 6(b). This yields the unshaded mutual inductance tolerance region in Fig. 7(a).

By employing the SiC MOSFET chip as a background reference, Fig. 7(a) provides a more visual guidance for wire bonding placement. Positioning the bonding wires within the mutual inductance tolerance region ensures that the deviation does not exceed the specified tolerance. Supplementary visualizations in Fig. 7(b) and (c) demonstrates the mutual inductance tolerance regions for 3% and 1% maximum acceptable deviations. For 5% and 3% tolerance levels, the pads of the SiC MOSFET chip are almost entirely contained within the mutual inductance tolerance region, thus enabling unrestricted wire bonding placement. However, for the more restrictive 1% tolerance, it is recommended to avoid placing bonding wires on the left auxiliary source pad (AS) and the small area at the bottom right of the source pad (S).

This analysis concentrates on measurement accuracy when the total measured current flows through a single bonding wire. For a more common configuration involving multiple bonding wires on a chip, each wire carries a portion of the total chip current. When one of the bonding wires lies outside the mutual inductance tolerance region, only a small fraction of the total current is measured with excessive deviation, which does not imply such a compromise in the overall current measurement. Nevertheless, constraining all bonding wires within the mutual inductance tolerance region remains a more conservative practice.

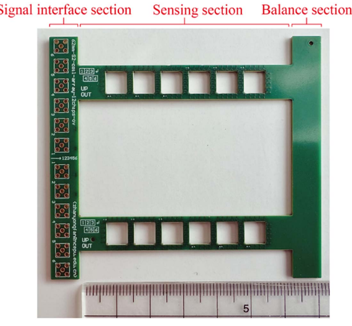


Fig. 8. Photo of the coil array with the interleaved arrangement.

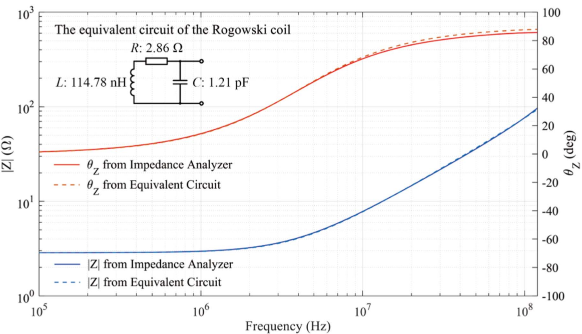


Fig. 9. Impedance–frequency characteristics of a coil in the coil array.

B. Rogowski Coil Array and Integrator

The PCB Rogowski coil array designed for the SiC power module is presented in Fig. 8, which employs the interleaved arrangement. Structurally, the coil array consists of three functional sections: the signal interface section, the sensing section, and the balance section. The sensing section consists of 12 Rogowski coils, which enable simultaneous current measurement for all chips in both bridge arms. The signal interface section provides mounting positions for 12 MMCX coaxial connectors, which channel the measured signals from the Rogowski coils to subsequent processing circuits. The balance section serves to maintain positional stability of the coil array throughout the packaging processes. The sensing section, with a width of 63 mm, is to be housed within the module, while the signal interface section and balance section are positioned externally. The coil array employs a PCB material with a decomposition temperature of 355 °C to ensure stable performance within the typical junction temperature range (<175 °C) of industrial SiC power modules.

The impedance–frequency characteristic of a single Rogowski coil in the array is measured using an impedance analyzer (E4990 A from Keysight with a bandwidth of 20 Hz to 120 MHz). The equivalent circuit of the coil obtained by the analyzer is shown in Fig. 9, which includes a 114.78 nH inductor, a 2.86 Ω resistor, and a 1.21 pF capacitor.

The Rogowski coil operates on the principle of electromagnetic induction, where its output voltage is directly proportional to the time derivative of the measured current. To obtain a signal proportional to the actual current amplitude, this derivative signal should be processed through an integrator circuit,

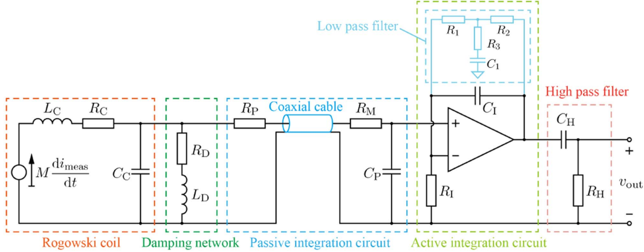


Fig. 10. Circuit schematic of the Rogowski transducer.

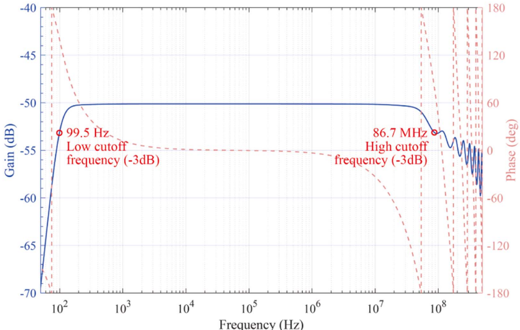


Fig. 11. Frequency response characteristic of the Rogowski transducer.

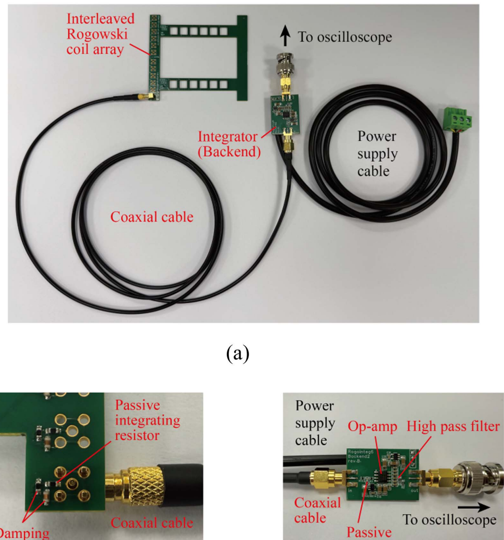


Fig. 12. Physical implementation of the Rogowski transducer. (a) Overall view of the Rogowski transducer. (b) Detailed view of the coil array output port. (c) Detailed view of the integrator backend.

which reconstructs the original current waveform. Together, the Rogowski coil and the integrator form the complete Rogowski transducer.

The integrator designed for the interleaved Rogowski coil array utilizes a classic noninverting configuration that incorporates both passive and active integration stages [40], [41]. The complete circuit schematic of the Rogowski transducer is presented in Fig. 10.

The passive integration circuit consists of a passive integrating resistor R_{P}, a coaxial cable, a matching resistor R_{M}, and a passive integrating capacitor C_{P}. The active integration circuit comprises an operational amplifier, an integrating resistor R_{I}, an integrating capacitor C_{I}, and a low-pass filtering network [42]. A high-pass filter is connected in series at the output to suppress the flicker noise and zero-drift of the operational amplifier [43]. In addition, a damping network comprising a resistor R_{D} and an inductor L_{D} in series is connected to the Rogowski coil. This damping network draws inspiration from the design of a Rogowski coil characteristic shaper [44], with parameters optimized to achieve higher bandwidth for the proposed interleaved Rogowski coil array.

Small-signal analysis of the Rogowski transducer is performed using SPICE software. The frequency response characteristic of the output voltage v_{out} as a function of the measured current i_{meas} is presented in Fig. 11. The analysis demonstrates that this Rogowski transducer exhibits a bandwidth extending from 99.5 Hz to 86.7 MHz. This frequency response adequately satisfies the current measurement requirements for SiC applications.

Fig. 12 illustrates a physical implementation of the Rogowski transducer based on the interleaved Rogowski coil array. The interleaved Rogowski coil array would be integrated into the SiC power module, while the integrator backend could be directly connected to oscilloscopes. A coaxial cable establishes the connection between the coil array and the integrator backend. The compact form factor of the integrator backend enables attachment to measurement instruments without occupying additional space. The operational amplifier is powered through a dedicated cable connected to a specialized power supply unit. The damping components and passive integrating resistors are soldered onto the corresponding pads of the interleaved Rogowski coil array.

C. Integration of the Rogowski Coil Array

The packaging processes for the SiC power module incorporating the PCB Rogowski coil array are partially illustrated in Fig. 13. First of all, the SiC MOSFET chips are soldered onto the designated positions of the active metal brazing (AMB) substrates, and the AMB substrates are soldered onto the copper baseplate. Neither of these soldering steps is related to the coil array.

Once the chips are firmly in place, the coil array could be positioned above the chips. Since the coil array features cutouts corresponding to the chip positions, the chips remain unobstructed, allowing subsequent packaging processes to proceed without interference. In the bonding process, the source pads of the SiC MOSFET chips are connected to the source AMB substrates using bonding wires, while the gate pads and auxiliary source pads are bonded to the driver connectors. By slightly increasing the loop parameters of the wire bonder, sufficient insulation clearance is provided for the coil array. The bonding wires are intentionally placed within the previously defined 3%-deviation mutual inductance tolerance region. After bonding, the bonding wires pass through the cutouts of the coil array, enabling the current of the SiC MOSFET chips to be measured by the Rogowski coils enclosing the cutouts. Each coil measures the sum of the currents

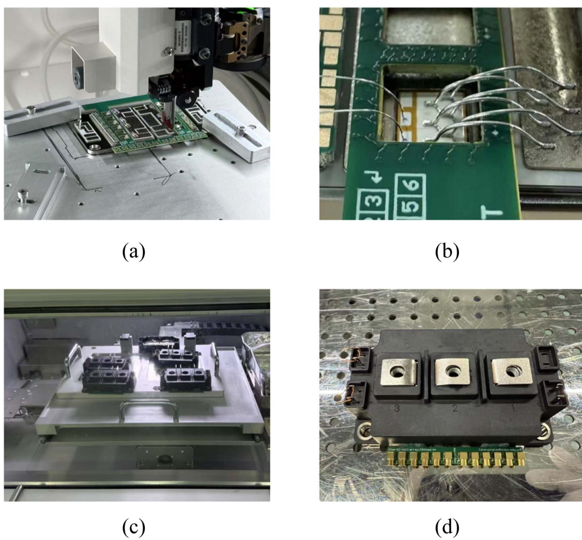


Fig. 13. Photos of the key packaging processes. (a) Wire bonding. (b) Details of the bonding wires for a chip. (c) Silicone rubber potting. (d) Appearance of the finished module.

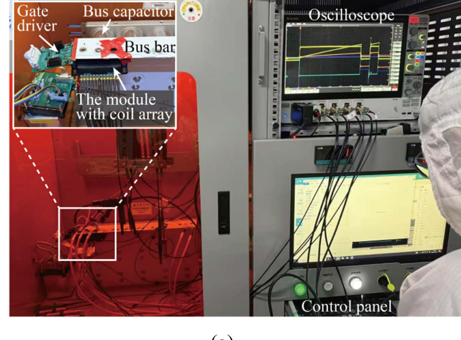
in the corresponding source bonding wires, gate bonding wire, and auxiliary source bonding wire. According to Kirchhoff's current law, this is equivalent to measuring the drain current of the corresponding chip, thereby avoiding measurement errors caused by the auxiliary source current loop [45], [46].

The subsequent processes are the terminal soldering and framing. The terminal soldering involves attaching metal terminals to the AMB substrates. The framing process involves the adhesion of a plastic case to the copper baseplate, thereby forming the enclosure of the power module. To allow the signal interface section of the coil array to protrude from the enclosure, slots are created in the plastic case, a task readily accomplished by using an electric drill. During the framing process, introducing spacers between the coil array and the copper baseplate elevates the coil array, establishing an insulation gap of 1 mm between the coil array and the AMB substrates. Subsequently, silicone rubber with a dielectric breakdown strength of 30 kV/mm is potted into the module, filling the 1 mm gap. This configuration provides sufficient insulation for the PCB Rogowski coil array to operate reliably with the 1200 V module.

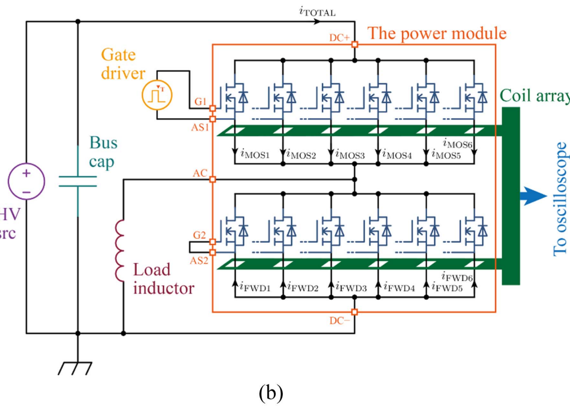
After the silicone rubber potting and curing, the packaging processes conclude with integrity testing. Finally, coaxial connectors are soldered to the signal interface section of the coil array. The balance section could optionally be trimmed off. Apart from the additional coaxial connectors, the power module with the coil array is visually identical to a standard 62 mm power module.

D. Experiment Platform and Conditions

The experiments on the SiC power module with the interleaved Rogowski coil array are conducted on a double-pulse test platform, as shown in Fig. 14. The double-pulse test platform consists of a bus capacitor, a gate driver, a bus bar, a load inductor, and an oscilloscope. The packaged SiC power module



(a)



(b)

Fig. 14. Double-pulse test platform for the current measurement experiment. (a) Photo of the platform. (b) Equivalent circuit diagram.

is mounted into the test circuit through the bus bar. The coil array is connected to the oscilloscope with coaxial cables.

A high voltage source provides a voltage of 600 V for the double-pulse test. The lower arm's gate terminal (G2) and auxiliary source terminal (AS2) are shorted, thereby enabling the six lower arm chips to function as freewheeling diodes. The upper arm is driven by the gate driver, which generates two sequential positive pulses.

To capture all waveforms during double-pulse testing, including gate-source voltage v_{GS}, drain-source voltage v_{DS}, total module current i_{TOTAL}, and individual chip currents from 12 chips measured by the interleaved Rogowski coil array, a time-division measurement approach is employed. Multiple double-pulse tests are conducted under identical conditions, with each test capturing a subset of waveforms. The gate-source voltage v_{GS} is measured in every test, and all waveforms are synchronized using the rising edge of the second v_{GS} pulse as a temporal reference to ensure proper alignment of the composite waveform plots. Sufficient cooling intervals are maintained between successive tests to allow adequate heat dissipation from the power module, thereby preventing thermally induced variations in current distribution among the parallel-connected chips.

E. Determination of Sensitivity

The sensitivity of a Rogowski transducer is defined as the ratio between the output voltage signal v_{out} and the measured

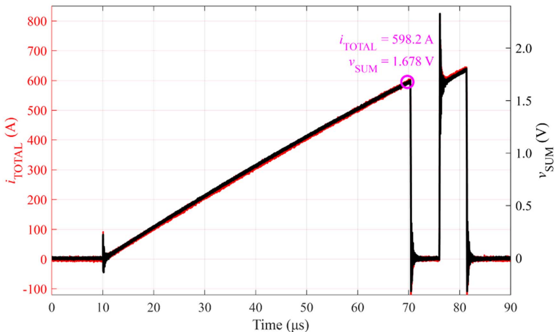


Fig. 15. Waveforms of the sensitivity experiment.

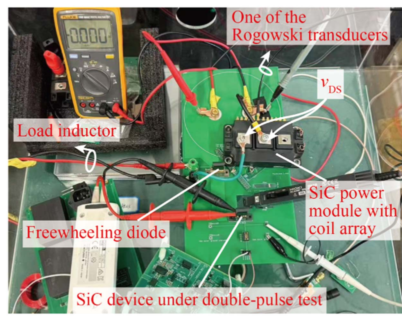


Fig. 16. Configuration of the capacitive coupling interference test.

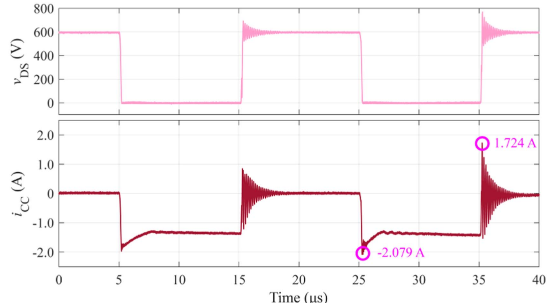


Fig. 17. Measurements of the capacitive coupling interference test.

current i_{meas}. This sensitivity is jointly determined by the mutual inductance of the Rogowski coil and the integration time constant of the integrator [22], [34]. Due to variations in PCB manufacturing parameters and the spatial positioning of bonding wires, the mutual inductance between bonding wires and the Rogowski coil may deviate from the design value. Therefore, it is good practice to conduct a comparison experiment with a commercial current probe to determine the actual sensitivity of the Rogowski transducer.

During a double-pulse test, the proposed interleaved Rogowski coil array combined with the integrator is employed to measure the currents of the six parallel MOSFET chips in the SiC power module, yielding output voltage waveforms $v_{\text{out}k}$, where $k = 1, 2, \ldots, 6$. These waveforms were summed to obtain the total voltage waveform v_{SUM}. For validation, v_{SUM} is plotted alongside the total device current i_{TOTAL} measured by a commercial current probe CWTUM 6B (30 MHz bandwidth, 1.2 kA range) on the same coordinate system, as illustrated in Fig. 15. The sensitivity of the PCB Rogowski transducers is derived from the plot as 2.8 mV/A.

Furthermore, the operational amplifier utilized in the integrator exhibits an output swing of $\pm$3.7 V under $\pm$5 V supply conditions. Considering the aforementioned sensitivity, the maximum measurement range of the proposed Rogowski transducer could be calculated as $\pm$1321.4 A.

F. Evaluation of Capacitive Coupling Interference

The Rogowski coil array is positioned adjacent to the AMB substrate. During switching operations of the SiC power module, the conductor potential of the AMB substrate varies from zero to several hundred volts, potentially introducing capacitive coupling interference to the coil array. The displacement current injected through the coupling capacitance generates an interference voltage at the Rogowski coil's output node. This interference voltage is subsequently integrated by the following circuitry, resulting in a spurious output from the entire transducer. The spurious output can be estimated as

$$i_{\text{CC}} = \frac{1}{R_{\text{sh}}T_{\text{i}}}\int_{t_1}^{t_2} R_{\text{eq}}C_{\text{eq}}\frac{\mathrm{d}v_{\text{DS}}}{\mathrm{d}t}\mathrm{d}t = \pm\frac{R_{\text{eq}}C_{\text{eq}}}{R_{\text{sh}}T_{\text{i}}}v_{\text{bus}} \qquad (4)$$

where R_{sh} is the sensitivity of the Rogowski transducer, T_{i} is the time constant of the integration circuitry, C_{eq} is the equivalent lumped coupling capacitance between the AMB substrate and the Rogowski coil's output node, R_{eq} is the equivalent node resistance which maps the injected current to the voltage at the Rogowski coil's output node, v_{bus} is the configured bus voltage, t_1 denotes the start time of the transient, and t_2 corresponds to the end time of the transient, satisfying $\frac{\mathrm{d}v_{\text{DS}}}{\mathrm{d}t} = \pm\frac{v_{\text{bus}}}{t_2 - t_1}$. The equation yields a negative value during turn-ON transients and a positive value during turn-OFF transients. This indicates the spurious output reverts to zero after each switching pulse. Furthermore, (4) demonstrates that the interference amplitude is predominantly determined by the configured bus voltage.

To evaluate the impact of capacitive coupling interference, a dedicated test circuit is constructed. Initially, a double-pulse test circuit is established for a discrete SiC MOSFET device, with a bus voltage of 600 V set. Subsequently, one bridge arm of the SiC power module, which contains the Rogowski coil array, is connected in parallel with this discrete device, as illustrated in Fig. 16. The switching voltage v_{DS} generated by the discrete device during double-pulse testing is applied via terminals to the AMB substrate conductor below the Rogowski coil array. The gate and auxiliary source terminals of the SiC power module are short-circuited to ensure no switching current flows through the chips. Consequently, the signals measured by the Rogowski transducers could be attributed solely to capacitive coupling interference induced by the switching voltage.

Fig. 17 presents the waveforms from the capacitive coupling interference test. When the AMB substrate switches at 600 V, the spurious current i_{CC} measured by the Rogowski transducer ranges from -2.079 to 1.724 A. Given the transducer's measurement range of $\pm$1321.4 A, the ratio of error to range is less than 1%. When referenced against the 100 A

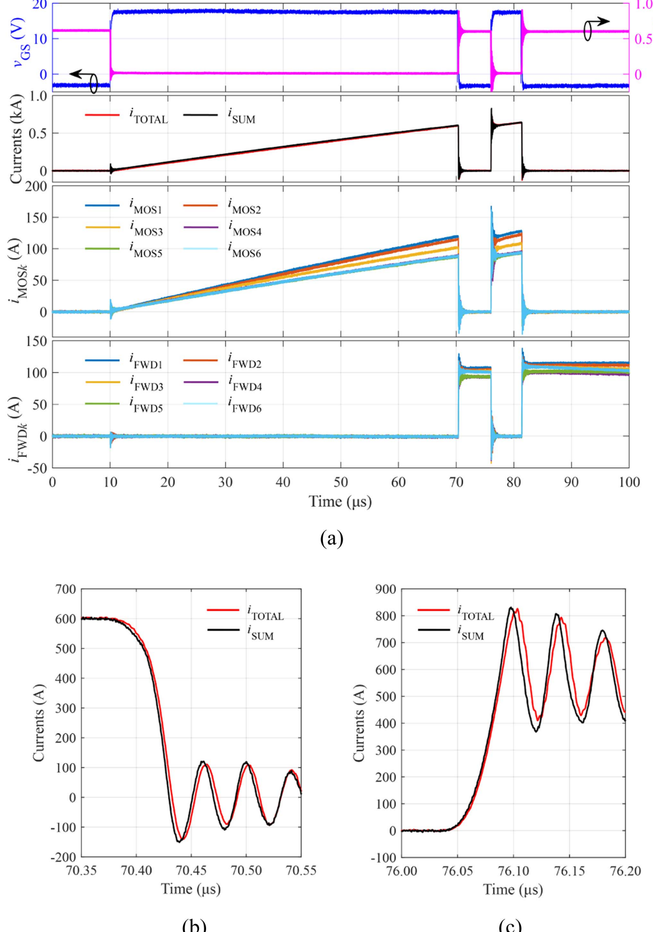


Fig. 18. Measurements of the double-pulse test. (a) Overall waveforms. (b) Turn-OFF transient current comparison. (c) Turn-ON transient current comparison.

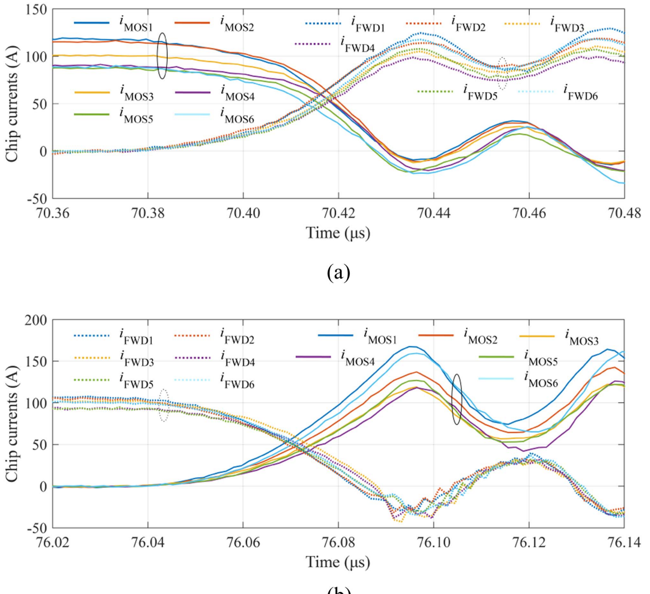


Fig. 19. Transient current waveforms of the 12 SiC MOSFET chips within the power module. (a) Turn-OFF transient. (b) Turn-on transient.

rated current of the chips used in the SiC power module, the measurement error induced by capacitive coupling interference remains below 3%. These error levels are well within acceptable limits for the current measurement applications presented in this work.

G. Current Measurement Experiment

Fig. 18 shows the measurements of the double-pulse test, which include the upper arm's gate-to-source voltage v_{GS}, the upper arm's drain-to-source voltage v_{DS}, the upper arm's chip currents i_{MOSk}, and the lower arm's chip currents i_{FWDk}, where $k = 1, 2, \ldots, 6$. In addition, Fig. 18(a) provides a comparison between i_{SUM}, the sum of the six currents i_{MOSk} measured by the PCB Rogowski coil array, and the total current i_{TOTAL} measured by CWTUM 6B. Fig. 18(b) and (c) illustrates the detailed comparison of i_{SUM} and i_{TOTAL} during the first turn-OFF transient and second turn-ON transient, respectively. Both steady-state and transient comparisons demonstrate the accuracy of the PCB Rogowski coil array measurements.

During the double-pulse test, when the gate driver applies a positive drive voltage, the upper arm of the power module turns on. The current entering the dc+ terminal, flowing through the six parallel-connected chips in the upper arm, and exiting through the ac terminal into the load inductor. Conversely, when a negative drive voltage is applied, the upper arm turns OFF. Because of the load inductor's inherent property to maintain current, the load current is forced to commutate, entering the dc-terminal, flowing through the six parallel-connected chips in the lower arm, and exiting from the ac terminal.

Fig. 19 presents the current waveforms of the 12 chips within the power module during the first turn-OFF transient and the second turn-ON transient in the double-pulse test. The measurements reveal that parallel-connected SiC MOSFET chips operating as freewheeling diodes exhibit better transient current balancing compared to those in forward conduction mode. During the turn-ON transient, i_{MOS1} and i_{MOS6} exhibit large overshoot peaks, whereas i_{MOS3} and i_{MOS4} exhibit lower overshoot peaks. This current distribution is consistent with the eddy current effect observed in linearly aligned branches. In the steady-state conduction phase, where i_{MOS6} has the minimal current value, the current distribution is predominantly influenced by the chip parameters. The turn-OFF transient, following the steady-state conduction phase, partially inherits its current distribution from the preceding phase.

It should be noted that the above conclusions are derived from the prototype power module discussed in this article. The current distribution across chips in other power modules may differ depending on factors such as chip characteristics, the number of chips, package design, and thermal distribution. Nevertheless, the interleaved PCB Rogowski coil array arrangement method proposed in this article enables current measurement of compactly arranged chips in SiC power modules, thereby facilitating strategies to mitigate current imbalance among parallel-connected chips and enhanced condition monitoring for power modules.

IV. Conclusion

This article proposes an interleaved PCB Rogowski coil array arrangement method for current measurement of compactly arranged chips within SiC power modules. For a prototype power module, the manufacturability problem of the conventional coil array arrangement in a confined space is analyzed. In addition to solving the manufacturability problem, the interleaved coil array exhibits an average mutual inductance of 1.01 nH, which is significantly higher than the 0.51 nH average mutual inductance of the conventional coil array. The proposed mutual inductance tolerance region involving the bonding wire placement provides an effective approach to further improve the current measurement accuracy of Rogowski coils. The packaging processes for integrating the interleaved PCB Rogowski coil array into the SiC power module are described in detail. The switching currents of the 12 chips in the SiC power module are measured, with comprehensive visualization of the commutation process across the upper and lower arms of the half-bridge module. The proposed interleaved PCB Rogowski coil array provides an effective solution for current measurement in space-constrained applications, such as chip current measurement within SiC power modules. This work advances the repertoire of current sensor design methodologies and establishes a valuable approach for condition monitoring and design optimization of power modules.

References

[1] M. Ostling, R. Ghandi, and C.-M. Zetterling, "SiC power devices–present status, applications and future perspective," in *Proc. IEEE 23rd Int. Symp. Power Semicond. Devices ICs*, San Diego, CA, USA: IEEE, May 2011, pp. 10–15.

[2] J. Rabkowski, D. Peftitsis, and H.-P. Nee, "Silicon carbide power transistors: A new era in power electronics is initiated," *IEEE Ind. Electron. Mag.*, vol. 6, no. 2, pp. 17–26, Jun. 2012.

[3] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[4] S. Zhao, A. Kempitiya, V. Palija, and C. Bonfiglio, "Variable DC-link voltage LLC resonant DC/DC converter with wide bandgap power devices," *IEEE Trans. Ind. Appl.*, vol. 58, no. 3, pp. 2965–2977, May/Jun. 2022.

[5] X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.

[6] H. Zhang, L. M. Tolbert, and B. Ozpineci, "Impact of SiC devices on hybrid electric and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 912–921, Mar./Apr. 2011.

[7] J. Feng, W. Q. Chu, Z. Zhang, and Z. Q. Zhu, "Power electronic transformer-based railway traction systems: Challenges and opportunities," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 3, pp. 1237–1253, Sep. 2017.

[8] P. Neudeck and J. Powell, "Performance limiting micropipe defects in silicon carbide wafers," *IEEE Electron Device Lett.*, vol. 15, no. 2, pp. 63–65, Feb. 1994.

[9] T. Kimoto, N. Miyamoto, and H. Matsunami, "Performance limiting surface defects in SiC epitaxial p-n junction diodes," *IEEE Trans. Electron Devices*, vol. 46, no. 3, pp. 471–477, Mar. 1999.

[10] M. Spencer, J. Palmour, and C. Carter, "Substrate and epitaxial issues for SiC power devices," *IEEE Trans. Electron Devices*, vol. 49, no. 5, pp. 940–945, May 2002.

[11] H. Li, S. Zhao, X. Wang, L. Ding, and H. A. Mantooth, "Parallel connection of silicon carbide MOSFETs–Challenges, mechanism, and solutions," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9731–9749, Aug. 2023.

[12] J. Ke, Z. Zhao, P. Sun, H. Huang, J. Abuogo, and X. Cui, "Influence of device parameters spread on current distribution of paralleled silicon carbide MOSFETs," *J. Power Electron.*, vol. 19, no. 4, pp. 1054–1067, 2019.

[13] H. Li et al., "Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, Jan. 2016.

[14] Z. Zeng, X. Zhang, and X. Li, "Layout-dominated dynamic current imbalance in multichip power module: Mechanism modeling and comparative evaluation," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11199–11214, Nov. 2019.

[15] C. Zhao, L. Wang, and F. Zhang, "Effect of asymmetric layout and unequal junction temperature on current sharing of paralleled SiC MOSFETs with kelvin-source connection," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7392–7404, Jul. 2020.

[16] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. D. Doncker, *Semiconductor Power Devices: Physics, Characteristics, Reliability*. New York, NY, USA: Springer, 2018.

[17] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active current balancing for parallel-connected silicon carbide MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA: IEEE, Sep. 2013, pp. 1563–1569.

[18] Z. Zeng, X. Zhang, and Z. Zhang, "Imbalance current analysis and its suppression methodology for parallel SiC MOSFETs with aid of a differential mode choke," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1508–1519, Feb. 2020.

[19] L. Wang et al., "Cu clip-bonding method with optimized source inductance for current balancing in multichip SiC MOSFET power module," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7952–7964, Jul. 2022.

[20] Z. Xin, H. Li, Q. Liu, and P. C. Loh, "A review of megahertz current sensors for megahertz power converters," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6720–6738, Jun. 2022.

[21] A. Rafiq, S. K. Pramanick, and R. Maheshwari, "Design of PCB coil based high bandwidth current sensor with power-loop stray inductance characterization," *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 12791–12801, Dec. 2021.

[22] W. Ray and R. Davis, "Wide bandwidth rogowski current transducers," *EPE J.*, vol. 3, no. 1, pp. 51–59, Mar. 1993.

[23] M. H. Samimi, A. Mahari, M. A. Farahnakian, and H. Mohseni, "The Rogowski coil principles and applications: A review," *IEEE Sensors J.*, vol. 15, no. 2, pp. 651–658, Feb. 2015.

[24] C. Hewson and J. Aberdeen, "An improved Rogowski coil configuration for a high speed, compact current sensor with high immunity to voltage transients," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2018, pp. 571–578.

[25] M. Tsukuda, M. Koga, K. Nakashima, and I. Omura, "Micro PCB rogowski coil for current monitoring and protection of high voltage power modules," *Microelectronics Rel.*, vol. 64, pp. 479–483, Sep. 2016.

[26] P. Sun, Z. Zhao, and Z. Chen, "LTCC based current sensor for silicon carbide power module integration," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1605–1614, Feb. 2022.

[27] L. Zhao, J. Van Wyk, and W. Odendaal, "Planar embedded pick-up coil sensor for integrated power electronic modules," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Anaheim, CA, USA: IEEE, 2004, pp. 945–951.

[28] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "A compact planar Rogowski coil current sensor for active current balancing of parallel-connected silicon carbide MOSFETs," in *Proc. 2014 IEEE Energy Convers. Congr. Expo. (ECCE)*, Pittsburgh, PA, USA: IEEE, Sep. 2014, pp. 4685–4690.

[29] K. Wang, X. Yang, H. Li, L. Wang, and P. Jain, "A high-bandwidth integrated current measurement for detecting switching current of fast GAN devices," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6199–6210, Jul. 2018.

[30] P. Palmer, B. Stark, and J. Joyce, "Noninvasive measurement of chip currents in IGBT modules," in *Proc. Rec. 28th Annu. IEEE Power Electron. Specialists Conf.. Formerly Power Conditioning Specialists Conf. Power Process. Electron. Specialists Conf.*, Jun. 1997, pp. 166–171.

[31] H. Hirai, Y. Kasho, M. Tsukuda, and I. Omura, "Bonding wire current measurement with tiny film current sensors," in *Proc. 24th Int. Symp. Power Semicond. Devices ICs*, Bruges, Belgium, Jun. 2012, pp. 287–290.

[32] J. Wang, Z. Shen, R. Burgos, and D. Boroyevich, "Integrated switch current sensor for shortcircuit protection and current control of 1.7-kV SiC MOSFET modules," in *Proc. IEEE Energy Convers. Congr. Expo.*, Milwaukee, WI, USA: IEEE, Sep. 2016, pp. 1–7.

[33] W. Zhang, S. B. Sohid, F. Wang, H. Cui, and B. Holzinger, "High-bandwidth combinational rogowski coil for SiC MOSFET power module," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4397–4405, Apr. 2022.

[34] Y. Zhan et al., “PCB Rogowski coil array with discrete electrostatic shielding for current measurement of paralleled chips in power devices,” *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 10276–10286, Aug. 2024.
[35] S. Fu, E. Deng, C. Peng, G. Zhang, Z. Zhao, and X. Cui, “Method of turns arrangement of noncircular Rogowski coil with rectangular section,” *IEEE Trans. Instrum. Meas.*, vol. 70, 2021, Art. no. 9000310.
[36] S. Fu et al., “Current measurement method of multiple chips using rectangular PCB rogowski coils integrated in press pack IGBT device,” *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 96–100, Jan. 2023.
[37] E. Deng, S. Fu, Y. Zhang, B. Ren, Z. Zhao, and X. Cui, “Crimp IGBT device chip current online measuring system,” Chinese Patent CN109856441B, May 2024.
[38] Y. Shi, Z. Xin, P. C. Loh, and F. Blaabjerg, “A review of traditional helical to recent miniaturized printed circuit board Rogowski coils for power-electronic applications,” *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12207–12222, Nov. 2020.
[39] Y. Zhan, X. Li, P. Sun, Z. Zhao, and X. Cui, “Method of turns arrangement with minimized mutual inductance deviation for discontinuous Rogowski coils,” *IEEE Trans. Instrum. Meas.*, vol. 74, 2025, Art. no. 9506209.
[40] W. Ray and C. Hewson, “High performance Rogowski current transducers,” in *Proc. Conf. Rec. IEEE Ind. Appl. Conf.. 35th IAS Annu. Meeting World Conf. Ind. Appl. Elect. Energy*, 2000, pp. 3083–3090.
[41] C. Hewson, W. Ray, and R. Davis, “Verification of Rogowski current transducer’s ability to measure fast switching transients,” in *Proc. 21st Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2006, pp. 573–579.
[42] L. Ming, Z. Xin, W. Liu, and P. Chiang Loh, “Structure and modelling of four-layer screen-returned PCB Rogowski coil with very few turns for high-bandwidth SiC current measurement,” *IET Power Electron.*, vol. 13, no. 4, pp. 765–775, Mar. 2020.
[43] C. Hewson, W. Ray, and J. Metcalfe, “Optimising high frequency integrator operation of Rogowski current transducers,” in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2007, pp. 1–9.
[44] H. Li, Z. Xin, X. Li, J. Chen, P. C. Loh, and F. Blaabjerg, “Extended wide-bandwidth Rogowski current sensor with PCB coil and electronic characteristic shaper,” *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 29–33, Jan. 2021.
[45] N. Baker, F. Iannuzzo, and H. Li, “Impact of kelvin-source resistors on current sharing and failure detection in multichip power modules,” in *Proc. 20th Eur. Conf. Power Electron. Appl.*, Sep. 2018, pp. 1–7.
[46] H. Li, S. Munk-Nielsen, X. Wang, S. Bęczkowski, S. R. Jones, and X. Dai, “Effects of auxiliary-source connections in multichip power module,” *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7816–7823, Oct. 2017.

Yongfan Zhan was born in Hunan, China, in 1999. He received the B.Sc. degree in electrical engineering from North China Electric Power University, Baoding, China, in 2020. He is currently working toward the Ph.D. degree in electrical engineering with North China Electric Power University and Beijing Huairou Laboratory, Beijing, China.

His research interests include the Rogowski current sensors and the packaging of high-power electronic devices.

Xuebao Li (Member, IEEE) was born in Tianjin, China, in 1988. He received the B.Sc. and Ph.D. degrees in electrical engineering from North China Electric Power University, Beijing, China, in 2011 and 2016, respectively.

He is currently an Associate Professor with the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Beijing, China, and a Scientist with Beijing Huairou Laboratory, Beijing, China. His research interests include the electromagnetic environment and electromagnetic compatibility in power systems, and insulation problems in high-voltage apparatus.

Xiaofeng Yang (Graduate Student Member, IEEE) was born in Shandong, China, in 1998. He received the M.Sc. degree in electrical engineering from China Three Gorges University, Yichang, China, in 2023. He is currently working toward the Ph.D. degree in electrical engineering with North China Electric Power University and Beijing Huairou Laboratory, Beijing, China.

His research interests include parasitic parameter modeling and analysis of current balancing for SiC power modules.

Hao Li was born in Shijiazhuang, China, in 1989. He received the M.Sc. degree in physics from Tianjin University, Tianjin, China, in 2015.

He is currently a Scientist with Beijing Huairou Laboratory, Beijing, China. His research interests include the development of SiC power modules, advanced packaging process integration, and nano silver sintering technology with high thermal conductivity.

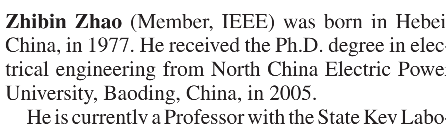
Lei Wang was born in Henan, China, in 1990. He received the Ph.D degree in electrical engineering from University of Chinese Academy of Sciences, Beijing, China, in 2021.

He is currently a Scientist with Beijing Huairou Laboratory, Beijing, China. His research interests include thermal design, advanced thermal management, and multiphysics simulation of power modules.

Rui Jin (Member, IEEE) was born in Liaoning, China, in 1982. She received the Ph.D. degree in physics from Imperial College London, London, U.K., in 2009.

She is currently the Director of the Power Semiconductor Research Institute, Beijing Institute of Smart Energy, Beijing, China, and a Scientist with Beijing Huairou Laboratory, Beijing. Her research interests include the design and fabrication of high-power electronic devices.

Prof. Jin is a Fellow of the IEEE PES Technical Committee on Transmission and the Deputy Secretary-General of China IGBT Technology Innovation and Industry Alliance.



Zhibin Zhao (Member, IEEE) was born in Hebei, China, in 1977. He received the Ph.D. degree in electrical engineering from North China Electric Power University, Baoding, China, in 2005.

He is currently a Professor with the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Beijing, China, and a Scientist with Beijing Huairou Laboratory, Beijing, China. His research interests include computational electromagnetics and electromagnetic compatibility in high-power electronic devices.

Xiang Cui (Senior Member, IEEE) was born in Baoding, Hebei, China, in 1960. He received the B.Sc. and M.Sc. degrees in electrical engineering from North China Electric Power University, Baoding, China, in 1982 and 1984, respectively, and the Ph.D. degree in accelerator physics from the China Institute of Atomic Energy, Beijing, China, in 1988.

He is currently a Professor with the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Beijing, China, and a Scientist with Beijing Huairou Laboratory. His research interests include electromagnetics, high-voltage apparatus, and high-power electronic devices.

Dr. Cui is a Fellow of the Chinese Society for Electrical Engineering and the China Electrotechnical Society.